

Pulse Input Bipolar Stepper Motor Driver

■ GENERAL DESCRIPTION

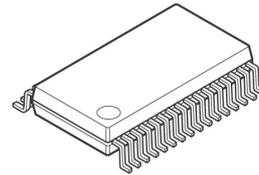
NJU7384 is a bipolar drive stepping motor driver.

The control method used is a simple pulse train input control (STEP & DIR) method of programming. Also, low power consumption was realized as a result of the adoption of a highly efficient CMOS.

As the control functions, the external input RESET and ENABLE functions are used, and as the protective function, a thermal shutdown (TSD) is incorporated.

The package uses the low thermal resistance SSOP32 which can withstand a high output current.

■ PACKAGE OUTLINE

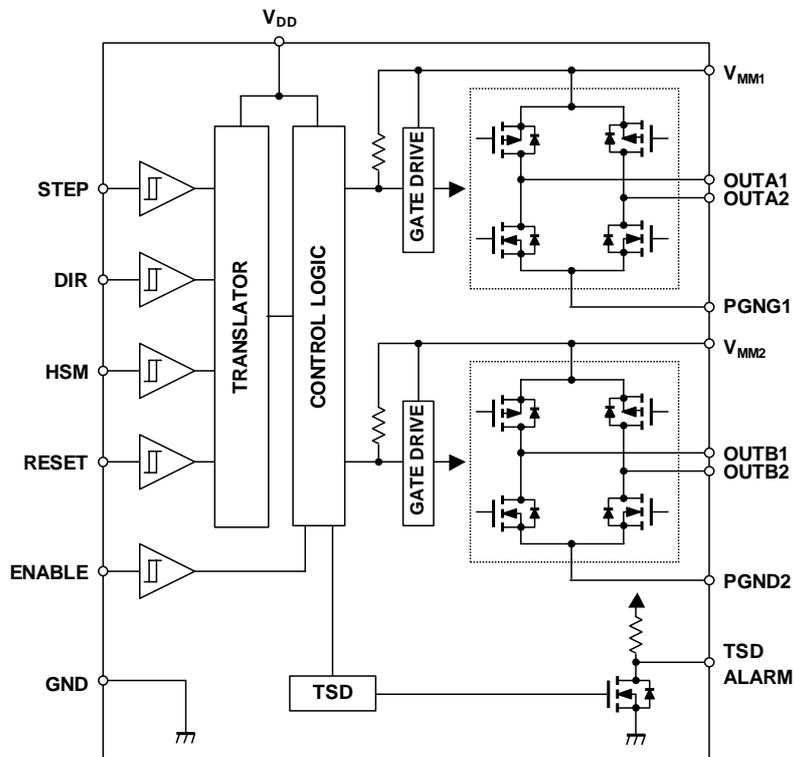


NJU7384V

■ FEATURES

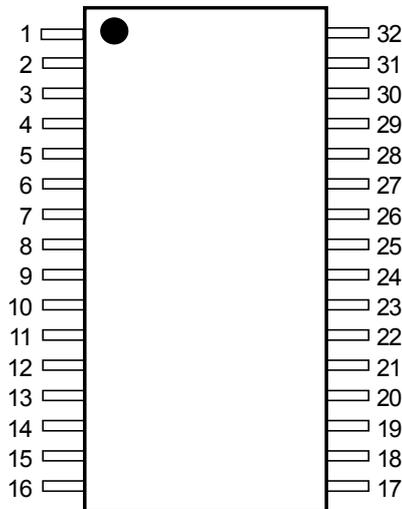
- Operating Voltage 3.0 to 5.5V (Logic : V_{DD})
 4.0 to 8.0V (H bridge : V_{MM})
- Maximum Output Current 700mA/ch
- Pulse Input (STEP & DIR) Control
- Half / Full Step Change Function
- Thermal Shutdown Circuit
- Thermal Shutdown Alarm Output
- RESET Function
- ENABLE Function
- CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



NJU7384

■ PIN FUNCTION



| | |
|---------------|---------------|
| 1. NC | 32. V_{MM1} |
| 2. NC | 31. V_{MM1} |
| 3. NC | 30. OUTA1 |
| 4. V_{DD} | 29. OUTA1 |
| 5. NC | 28. OUTA2 |
| 6. STEP | 27. OUTA2 |
| 7. DIR | 26. PGND1 |
| 8. HSM | 25. PGND1 |
| 9. RESET | 24. PGND2 |
| 10. ENABLE | 23. PGND2 |
| 11. TSD ALARM | 22. OUTB2 |
| 12. NC | 21. OUTB2 |
| 13. GND | 20. OUTB1 |
| 14. NC | 19. OUTB1 |
| 15. NC | 18. V_{MM2} |
| 16. NC | 17. V_{MM2} |

■ PIN DESCRIPTION

| PIN No. | SYMBOL | FUNCTION | NOTE |
|----------|-----------|---|---|
| 1,2,3 | NC | Non connection pins | - |
| 4 | V_{DD} | Logic Power-Supply input pin | - |
| 5 | NC | Non connection pin | - |
| 6 | STEP | Pulse signal input pin for motor rotation control pin | 1 pulse input \Rightarrow 1 clock motion |
| 7 | DIR | Forward / Reverse rotation control | "H"= Forward (CW), "L"= Reverse (CCW) |
| 8 | HSM | Full / Half step mode control pin | "H"= Full step, "L"= Half step |
| 9 | RESET | Phase initialize signal input pin | "H"= Normal operation, "L"= Phase initialize |
| 10 | ENABLE | Output signal all off control signal input pin | "H"= Normal operation, "L"= Output all off |
| 11 | TSD ALARM | TSD alarm output pin | TSD operating ="L" signal output |
| 12 | NC | Non connection pins | - |
| 13 | GND | Logic ground (GND) pin | - |
| 14,15,16 | NC | Non connection pins | - |
| 17,18 | V_{MM2} | H bridge power-supply pins | Connect to motor power-supply |
| 19,20 | OUTB1 | Output pin B1 | - |
| 21,22 | OUTB2 | Output pin B2 | - |
| 23,24 | PGND2 | H bridge ground (GND) pin | - |
| 25,26 | PGND1 | H bridge ground (GND) pin | - |
| 27,28 | OUTA2 | Output pin A2 | - |
| 29,30 | OUTA1 | Output pin A1 | - |
| 31,32 | V_{MM1} | H bridge power-supply pins | Connect to motor power-supply |

* Short all logic ground terminals and the H bridge ground terminal externally.

* Short all H bridge power supply voltage terminals externally.

* Fix the potential of unused logic input terminals externally.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | RATINGS | SYMBOL(unit) | NOTE |
|--------------------------------------|------------------------|----------------------------|------|
| Logic Power Supply Voltage | +7.0 | V _{DD} (V) | *1) |
| H Bridge Power Supply Voltage | +9.0 | V _{MM} (V) | - |
| Logic Input Voltage | -0.3 ~ V _{DD} | V _{ID} (V) | - |
| Motor Output Current (Max) | 700 | I _{OPEAK} (mA/ch) | - |
| Logic Input Current | 10 | I _{IPEAK} (mA) | - |
| Operating Temperature Range | -40 ~ +85 | T _{opr} (°C) | - |
| Operating Junction Temperature Range | -40 ~ +150 | T _j (°C) | - |
| Storage Temperature Range | -50 ~ +150 | T _{stg} (°C) | - |
| Power Dissipation | 1175 | P _D (mW) | *2) |

*1) : V_{DD} ≤ V_{MM}

*2) : EIAJ/JEDEC STD 2 Layer substrate

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

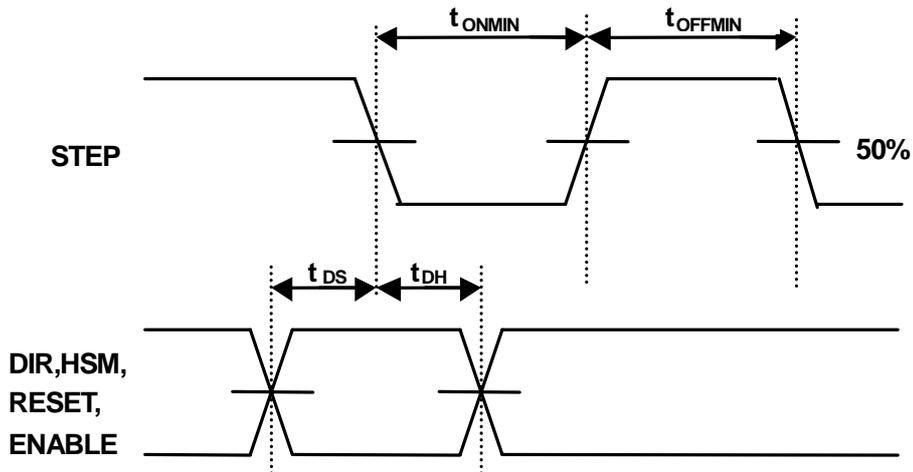
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|-------------------------------------|---------------------|------|------|-----------------|------|-----------------------------------|
| Logic Power Supply Voltage Range | V _{DD} | 3.0 | 5.0 | 5.5 | V | V _{DD} ≤ V _{MM} |
| H Bridge Power Supply Voltage Range | V _{MM} | 4.0 | 6.0 | 8.0 | V | - |
| Logic H Input Voltage | V _{IH} | 3.5 | - | V _{DD} | V | V _{DD} =5.0V, No load |
| Logic L Input Voltage | V _{IL} | 0 | - | 1.2 | V | |
| STEP-ON Time | t _{ONMIN} | 10 | - | - | μs | |
| STEP-OFF Time | t _{OFFMIN} | 10 | - | - | μs | |
| Data Setup Time | t _{DS} | 1 | - | - | μs | |
| Hold Time | t _{DH} | 1 | - | - | μs | |
| Input Clock Frequency | f _{CLK} | - | - | 50 | kHz | |

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=5V, V_{MM}=6V)

| PARAMETER | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|---------------------|--|------|------|------|------|
| ■ General | | | | | | |
| Operating Current | I _{DD} | STEP, DIR, HSM, RESET, ENABLE="5V", No Load, V _{DD} Meas. | - | 0.3 | 0.6 | mA |
| | I _{MM} | STEP, DIR, HSM, RESET, ENABLE="5V", No load, V _{MM} Meas. | - | 0.3 | 0.6 | mA |
| Thermal Shutdown Operating Temperature | T _{TSD} | - | - | 180 | - | °C |
| Thermal Shutdown Hysteresis | T _{HYS} | - | - | 30 | - | °C |
| ■ Input (STEP, DIR, HSM, ENABLE, RESET Terminals) | | | | | | |
| Logic Input Current | I _{IH} | STEP, DIR, HSM, ENABLE, RESET ="5V" | - | - | 1 | μA |
| | I _{IL} | STEP, DIR, HSM, ENABLE, RESET ="0V" | -1 | - | - | μA |
| ■ H Bridge (Output) | | | | | | |
| H Output Voltage | V _{OH} | I _o =+400mA | 5.5 | 5.7 | - | V |
| L Output Voltage | V _{OL} | I _o = -400mA | - | 0.2 | 0.4 | V |
| Upper Side Output ON Resistance | R _{OH} | I _o =400mA | - | 0.75 | 1.25 | Ω |
| Under Side Output ON Resistance | R _{OL} | I _o =400mA | - | 0.50 | 1.00 | Ω |
| Output Leak Current | I _{O LEAK} | - | - | 1.0 | - | μA |
| ■ Signal Output | | | | | | |
| TSD Alarm L Output Voltage | V _{TSD} | No external pull-up resistance | - | - | 0.3 | V |
| TSD Pull-up Resistance | R _{TSD} | - | - | 10 | - | kΩ |

■ TIMING CONDITION



■ TRUTH TABLE

| LOGIC IN | | MODE |
|----------|---|-----------|
| V_{DD} | H | OPERATE |
| | L | Hi Z |
| DIR | H | CW |
| | L | CCW |
| HSM | H | FULL STEP |
| | L | HALF STEP |
| RESET | H | OPERATE |
| | L | RESET |
| ENABLE | H | OPERATE |
| | L | Hi Z |

* V_{MM} : Motor voltage supply

*OPERATE : Follow the input logic

*Hi Z : Output all off (A1, A2, B1,B2)

■ EXCITATION SEQUENCE

Condition: FULL STEP, HSM=ENABLE=RESET

| Pulse | 0 | 1 | 2 | 3 |
|----------|---|---|---|---|
| OUTA1 | L | H | H | L |
| OUTA2 | H | L | L | H |
| OUTB1 | L | L | H | H |
| OUTB2 | H | H | L | L |
| IA | - | + | + | - |
| IB | - | - | + | + |
| DIR=HIGH | → | | | |
| DIR=LOW | ← | | | |

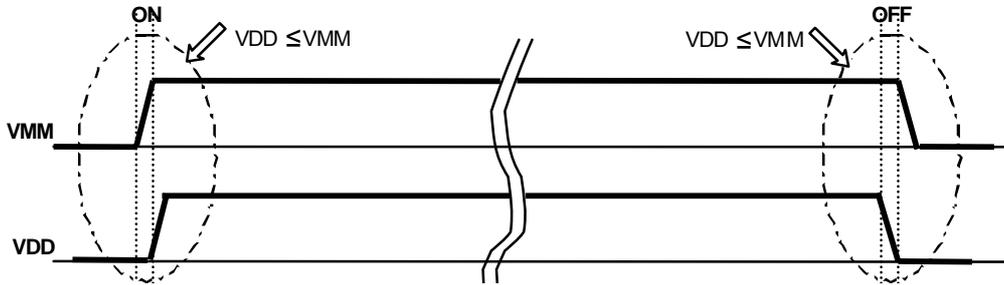
Condition: HALF STEP, HSM=LOW, ENABLE=RESET=HIGH

| Pulse | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|---|------|---|------|---|------|---|------|
| OUTA1 | L | Hi Z | H | H | H | Hi Z | L | L |
| OUTA2 | H | Hi Z | L | L | L | Hi Z | H | H |
| OUTB1 | L | L | L | Hi Z | H | H | H | Hi Z |
| OUTB2 | H | H | H | Hi Z | L | L | L | Hi Z |
| IA | - | 0 | + | + | + | 0 | - | - |
| IB | - | - | - | 0 | + | + | + | 0 |
| DIR=HIGH | → | | | | | | | |
| DIR=LOW | ← | | | | | | | |

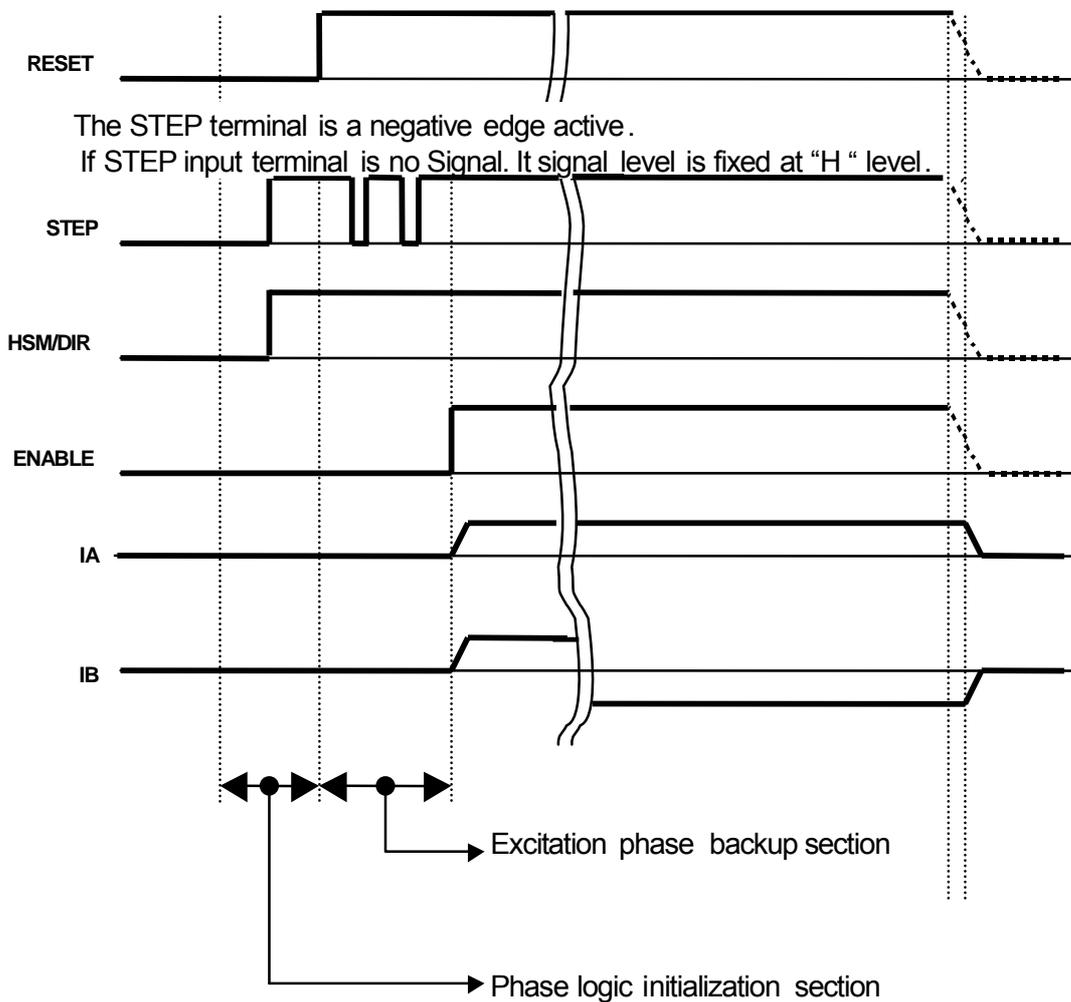
* Regarding the current flow direction, the direction A1→A2 and B1→B2 is indicated as +, and the direction A2→A1 and B2→B1 is indicated as -.

POWER SUPPLY ON/OFF TIMING

Regarding the switch-on sequence of the logic power supply V_{DD} and the motor power supply V_{MM} , input V_{DD} after V_{MM} has risen. The recommended sequence is shown below.



The RESET signal is "L" level in the range of turning ON. And Phase logic is initialized.



The STEP terminal is a negative edge active.

If STEP input terminal is no Signal. Its signal level is fixed at "H" level.

RECOMMENDED STEP MODE CHANGEOVER (HSM)

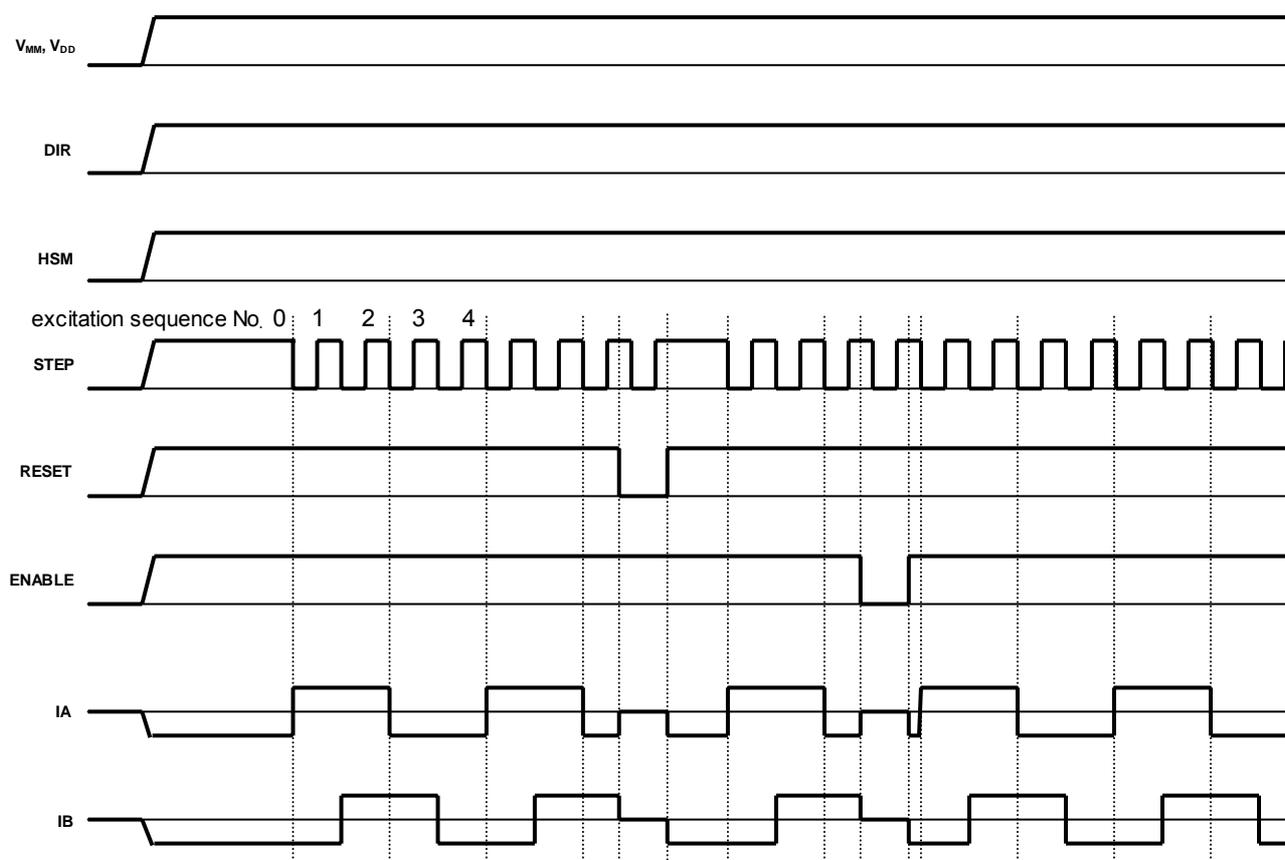
The current flowing through the stepping motor must be controlled continuously so that a mis-step does not occur. Also, the following precautions must be observed concerning changing of the setting of the HSM input.

- (1) A mis-step does not occur during changeover from a full step to a half step
- (2) Regarding changeover from a half step to a full step,
 - (a) A mis-step does not occur during changeover from a half step (excitation sequence 0, 2, 4, 6) to a full step.
 - (b) A mis-step occurs during changeover from a half step (excitation sequence 1, 3, 5, 7) to a full step.

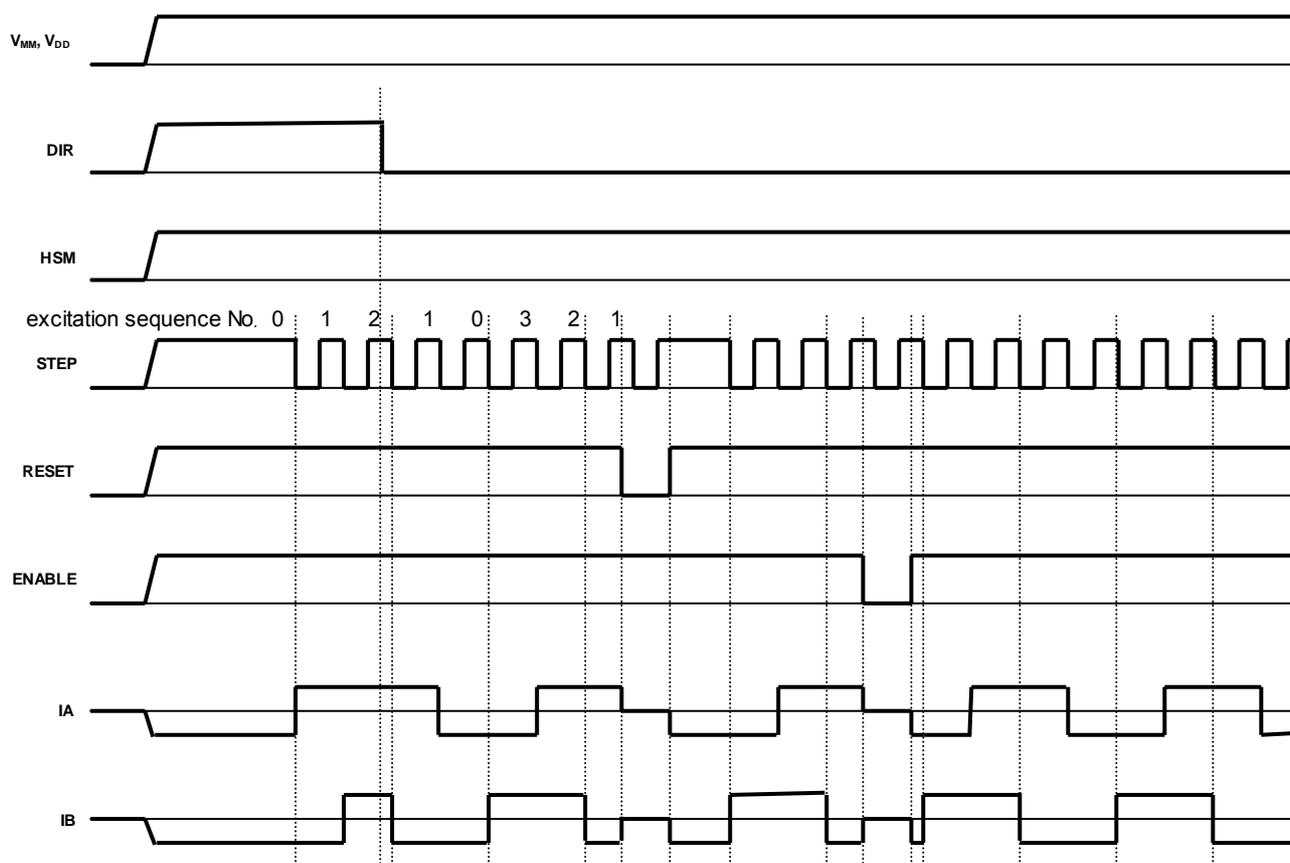
For the above reason, it is recommended that mode changeover from a half step to a full step be carried out during the period when the RESET input is "L" logic.

■ TIMING CHART

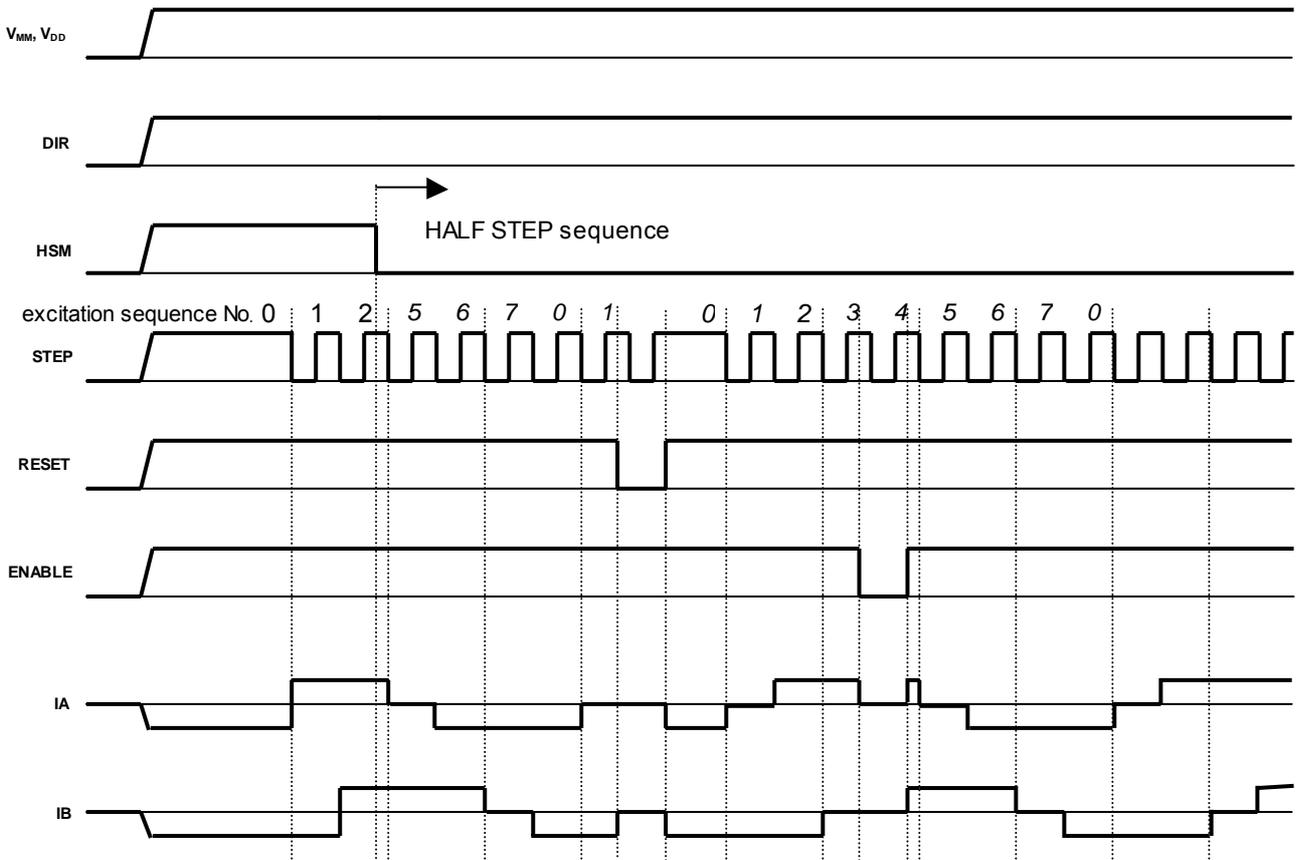
- Fixed mode (Full step / Forward direction)
Condition : DIR="H", HSM="H"



- Direction change (Full step / Forward direction \Rightarrow Reverse direction)
 Condition : DIR="H" \Rightarrow "L", HSM="H"

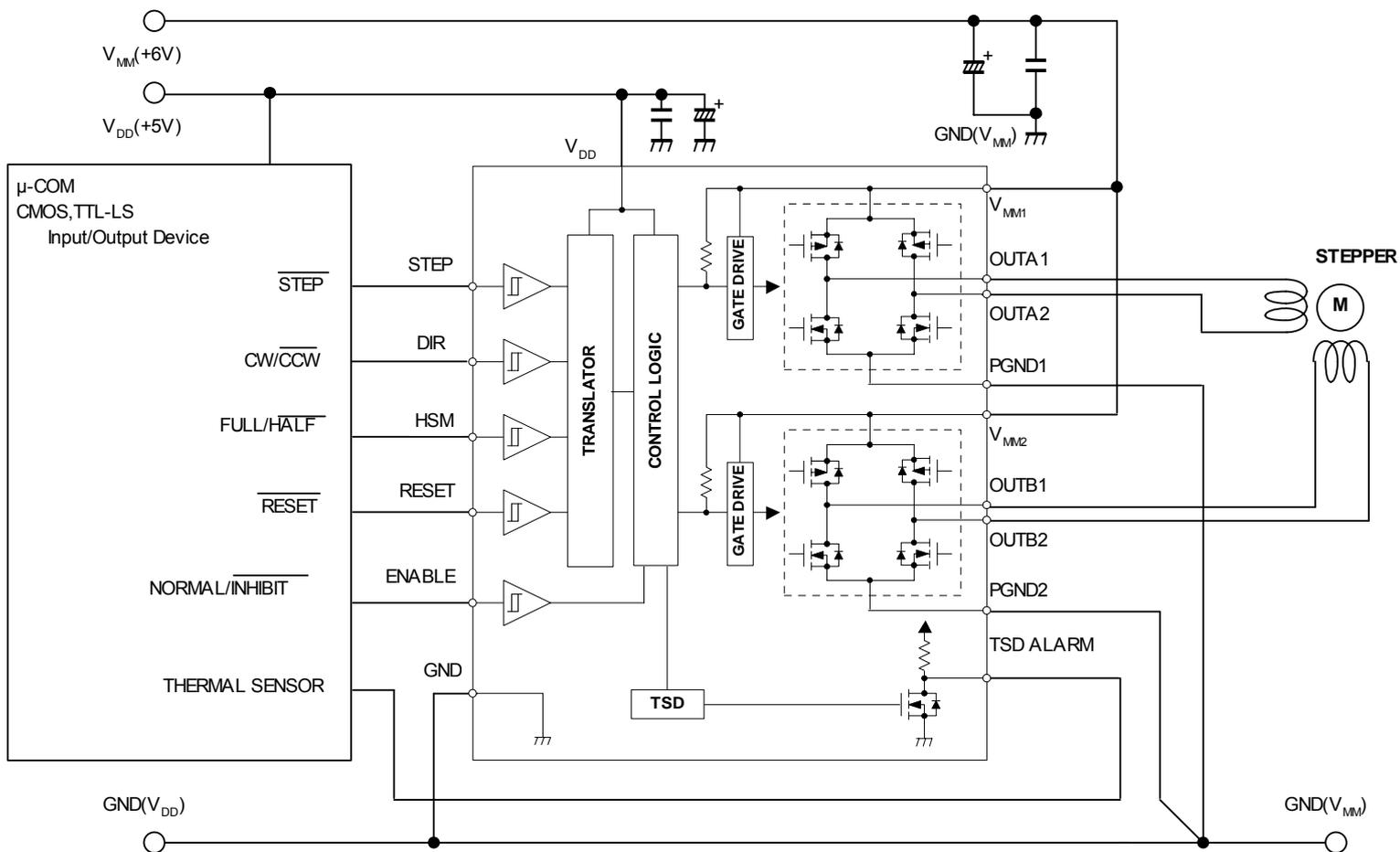


- Step mode change (Full step ⇒ Half step)
 Condition : DIR="H", HSM="H" ⇒ "L"



NJU7384

APPLICATION CIRCUIT



[CAUTION]

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