## SMBus Multi-Output Power-Supply Controller

## DESCRIPTION

The Si9135 is a current-mode PWM and PSM converter controller, with two synchronous buck converters (3.3 V and 5 V ) and a flyback (non-isolated buck-boost) converter ( 12 V ). Designed for portable devices, it offers a total five power outputs (three tightly regulated dc/dc converter outputs, a precision 3.3 V reference and a 5 V LDO output). It requires minimum external components and is capable of achieving conversion efficiencies approaching $95 \%$.
Along with the SMBUS interface, the Si9135 provides programmable output selection capability.
The Si9135 is available in both standard and lead (Pb)-free 28-pin SSOP packages and specified to operate over the extended commercial $\left(0^{\circ} \mathrm{C}\right.$ to $\left.90^{\circ} \mathrm{C}\right)$ temperature range.

## FEATURES

- Up to 95 \% Efficiency
- $3 \%$ Total Regulation (Each Controller)
- 5.5 V to 30 V Input Voltage Range
- $3.3 \mathrm{~V}, 5 \mathrm{~V}$, and 12 V Outputs
- $200 \mathrm{kHz} / 300 \mathrm{kHz}$ Low-Noise Frequency Operation
- Precision 3.3 V Reference Output
- 30 mA Linear Regulator Output
- SMBUS Interface
- High Efficiency Pulse Skipping Mode Operation at Light Load
- Only Three Inductors Required - No Transformer
- LITTLE FOOT ${ }^{\circledR}$ Optimized Output Drivers
- Internal Soft-Start
- Synchronizable
- Minimal External Control Components
- 28-Pin SSOP Package


## FUNCTIONAL BLOCK DIAGRAM



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Notes：
a．Device Mounted with all leads soldered or welded to PC board．
b．Derate $9.52 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $90^{\circ} \mathrm{C}$ ．
Stresses beyond those listed under＂Absolute Maximum Ratings＂may cause permanent damage to the device．These are stress ratings only，and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied．Exposure to absolute maximum rating conditions for extended periods may affect device reliability．

## SPECIFICATIONS

| Parameter | $\begin{gathered} \text { Specific Test Conditions } \\ V_{I N}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{VL}}=I_{\mathrm{REF}}=0 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 90^{\circ} \mathrm{C} \text {, All Converters } \mathrm{ON} \end{gathered}$ | Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min．${ }^{\text {a }}$ | Typ．${ }^{\text {b }}$ | Max．${ }^{\text {a }}$ |  |
| 3．3 V Buck Controller |  |  |  |  |  |
| Total Regulation（Line，Load，and Temperature） | $\mathrm{V}_{\mathrm{IN}}=6$ to $30,0<\mathrm{V}_{\text {CS3 }}-\mathrm{V}_{\text {FB3 }}<90 \mathrm{mV}$ | 3.23 | 3.33 | 3.43 | V |
| Line Regulation | $\mathrm{V}_{\text {IN }}=6$ to 30 V |  |  | $\pm 0.5$ | \％ |
| Load Regulation | $0<\mathrm{V}_{\text {CS3 }}-\mathrm{V}_{\text {FB3 }}<90 \mathrm{mV}$ |  |  | $\pm 0.5$ | \％ |
| Current Limit | $\mathrm{V}_{\text {CS3 }}-\mathrm{V}_{\text {FB3 }}$ | 90 | 125 | 160 | mV |
| Bandwidth | $\mathrm{L}=10 \mu \mathrm{H}, \mathrm{C}=330 \mu \mathrm{~F}$ |  | 50 |  | kHz |
| Phase Margin | $\mathrm{R}_{\text {SENSE }}=20 \mathrm{~m} \Omega$ |  | 65 |  | 。 |
| 5 V Buck Controller |  |  |  |  |  |
| Total Regulation（Line，Load，and Temperature） | $\mathrm{V}_{\text {IN }}=6$ to $30,0<\mathrm{V}_{\text {CS5 }}-\mathrm{V}_{\text {FB5 }}<90 \mathrm{mV}$ | 4.88 | 5.03 | 5.18 | V |
| Line Regulation | $\mathrm{V}_{\text {IN }}=6$ to 30 V |  |  | $\pm 0.5$ |  |
| Load Regulation | $0<\mathrm{V}_{\mathrm{CS5} 5}-\mathrm{V}_{\mathrm{FB5}}<90 \mathrm{mV}$ |  |  | $\pm 0.5$ |  |
| Current Limit | $\mathrm{V}_{\text {CS5 }}-\mathrm{V}_{\text {FB5 }}$ | 90 | 125 | 160 | mV |
| Bandwidth | $\mathrm{L}=10 \mu \mathrm{H}, \mathrm{C}=330 \mu \mathrm{~F}$ |  | 50 |  | kHz |
| Phase Margin | $\mathrm{R}_{\text {SENSE }}=20 \mathrm{~m} \Omega$ |  | 60 |  | 。 |
| 12 V Flyback Controller |  |  |  |  |  |
| Total Regulation（Line，Load，and Temperature） | $\mathrm{V}_{\text {IN }}=6$ to $30,0<\mathrm{V}_{\text {CSP }}-\mathrm{V}_{\text {CSN }}<300 \mathrm{mV}$ | 11.4 | 12.0 | 12.6 | V |
| Line Regulation | $\mathrm{V}_{\text {IN }}=6$ to 30 V |  |  | $\pm 0.5$ | \％ |
| Load Regulation | $0<\mathrm{V}_{\text {CSP }}-\mathrm{V}_{\text {FBN }}<300 \mathrm{mV}$ |  |  | $\pm 0.5$ | \％ |
| Current Limit | $\mathrm{V}_{\text {CSP }}-\mathrm{V}_{\text {CSN }}$ | 330 | 410 | 510 | mV |
| Bandwidth | $\mathrm{L}=10 \mu \mathrm{H}, \mathrm{C}=100 \mu \mathrm{~F}$ |  | 10 |  | kHz |
| Phase Margin | $\mathrm{R}_{\text {SENSE }}=100 \mathrm{~m} \Omega, \mathrm{C}_{\text {comp }}=120 \mathrm{pF}$ |  | 65 |  | 。 |


| SPECIFICATIONS |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | $\begin{gathered} \text { Specific Test Conditions } \\ V_{I N}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{VL}}=\mathrm{I}_{\mathrm{REF}}=0 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 90^{\circ} \mathrm{C} \text {, All Converters ON } \end{gathered}$ | Limits |  |  | Unit |
|  |  | Min. ${ }^{\text {a }}$ | Typ. ${ }^{\text {b }}$ | Max. ${ }^{\text {a }}$ |  |
| Internal Regulator |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{L}}$ Output | All Converters OFF, $\mathrm{V}_{\mathrm{IN}}>5.5 \mathrm{~V}, 0<\mathrm{I}_{\mathrm{L}}<30 \mathrm{~mA}$ | 4.7 |  | 5.5 | V |
| $\mathrm{V}_{\mathrm{L}}$ Fault Lockout Voltage |  | 3.6 |  | 4.2 |  |
| $\mathrm{V}_{\mathrm{L}}$ Fault Lockout Hysteresis |  |  | 75 |  | mV |
| V /FB5 Switchover Voltage |  | 4.2 |  | 4.7 | V |
| V /FB5 Switchover Hysteresis |  |  | 75 |  | mV |
| Reference |  |  |  |  |  |
| REF Output | No External Load | 3.24 | 3.30 | 3.36 | V |
| REF Load Regulation | 0 to 1 mA |  | 30 | 75 | mV |
| Supply Current |  |  |  |  |  |
| Supply Current - Shutdown | All Converters OFF, No Load |  | 35 | 60 | $\mu \mathrm{A}$ |
| Supply Current - Operation | All Converters ON, No Load, Focs $=200 \mathrm{kHz}$ |  | 1100 | 1800 |  |
| Oscillator |  |  |  |  |  |
| Oscillator Frequency | SYNC tied to REF | 270 | 300 | 330 | kHz |
|  | SYNC tied to GND or $\mathrm{V}_{\mathrm{L}}$ | 180 | 200 | 220 |  |
| SYNC High-Pulse Width |  | 200 |  |  | nsec |
| SYNC Low-Pulse Width |  | 200 |  |  |  |
| SYNC Rise/Fall Range |  |  |  | 200 |  |
| SYNC V ${ }_{\text {IL }}$ |  |  |  | 0.8 |  |
| SYNC $\mathrm{V}_{\mathrm{IH}}$ |  | $\mathrm{V}_{\mathrm{L}}-0.5$ |  |  |  |
| Oscillator SYNC Range |  | 250 |  | 400 | kHz |
| Maximum Duty Cycle | SYNC tied to GND or $\mathrm{V}_{\mathrm{L}}$ | 92 | 95 |  | \% |
|  | SYNC tied to REF | 89 | 92 |  |  |
| Outputs |  |  |  |  |  |
| Gate Driver Sink/Source Current (Buck) | DL3, DH3, DL5, DH5 Forced to 2 V |  | 1 |  | A |
| Gate Driver On-Resistance (Buck) | High or Low |  | 2 | 7 | $\Omega$ |
| Gate Driver Sink/Source Current (Flyback) | DHFY, DLFY Forced to 2 V |  | 0.2 |  | A |
| Gate Driver On-Resistance (Flyback) | High or Low |  |  | 15 | $\Omega$ |
| SCL, SDA |  |  |  |  |  |
| $\mathrm{V}_{\text {IL }}$ |  |  |  | 0.6 | V |
| $\mathrm{V}_{\mathrm{IH}}$ |  | 1.4 |  |  |  |

## Notes:

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

## PIN CONFIGURATION

|  |  | SSOP-28 |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{CS}_{3}$ | 1 |  | 28 | $\mathrm{FB}_{3}$ |
| FBFY | 2 |  | 27 | $\mathrm{DH}_{3}$ |
| BSTFY | 3 |  | 26 | $\mathrm{LX}_{3}$ |
| DHFY | 4 |  | 25 | $\mathrm{BST}_{3}$ |
| LXFY | 5 |  | 24 | $\mathrm{DL}_{3}$ |
| DLFY | 6 |  | 23 | $\mathrm{V}_{\text {IN }}$ |
| CSP | 7 |  | 22 | $V_{L}$ |
| CSN | 8 |  | 21 | $\mathrm{FB}_{5}$ |
| GND | 9 |  | 20 | PGND |
| COMP | 10 |  | 19 | $\mathrm{DL}_{5}$ |
| REF | 11 |  | 18 | $\mathrm{BST}_{5}$ |
| SYNC | 12 |  | 17 | $L^{1} 5$ |
| SCL | 12 |  | 16 | $\mathrm{DH}_{5}$ |
| SDA | 14 |  | 15 | $\mathrm{CS}_{5}$ |
|  |  | Top View |  |  |


| ORDERING INFORMATION |  |  |  |
| :--- | :---: | :---: | :---: |
| Part Number | Lead (Pb)-free <br> Part Number | Temperature <br> Range | V $_{\text {OUT }}$ |
| Si9135LG |  | 0 to $90^{\circ} \mathrm{C}$ | $3.3 \mathrm{~V}, 5 \mathrm{~V}, 12 \mathrm{~V}$ |
| Si9135LG-T1 | Si9135LG-T1-E3 |  |  |

Top View

| PIN DESCRIPTION |  |  |
| :---: | :---: | :---: |
| Pin Number | Symbol | Description |
| 1 | $\mathrm{CS}_{3}$ | Current sense input for 3.3 V buck. |
| 2 | FBFY | Feedback for flyback. |
| 3 | BSTFY | Boost capacitor connection for flyback converter. |
| 4 | DHFY | Gate-drive output for flyback high-side MOSFET. |
| 5 | LXFY | Inductor connection for flyback converter. |
| 6 | DLFY | Gate-drive output for flyback low-side MOSFET. |
| 7 | CSP | Current sense positive input for flyback converter. |
| 8 | CSN | Current sense negative input for flyback converter. |
| 9 | GND | Analog ground. |
| 10 | COMP | Flyback compensation connection, if required. |
| 11 | REF | 3.3 V internal reference. |
| 12 | SYNC | Oscillator synchronization inputs. |
| 13 | SCL | SMBUS clock line. |
| 14 | SDA | SMBUS data line. |
| 15 | $\mathrm{CS}_{5}$ | Current sense input for 5 V buck controller. |
| 16 | DH5 | Inductor connection for buck 5 V . |
| 17 | $\mathrm{LX}_{5}$ | Gate-drive output for 5 V buck high-side MOSFET. |
| 18 | $\mathrm{BST}_{5}$ | Boost capacitor connection for 5 V buck converter. |
| 19 | $\mathrm{DL}_{5}$ | Gate-drive output for 5 V buck low-side MOSFET. |
| 20 | PGND | Power ground. |
| 21 | $\mathrm{FB}_{5}$ | Feedback for 5 V buck. |
| 22 | $\mathrm{V}_{\mathrm{L}}$ | 5 V logic supply voltage for internal circuitry. |
| 23 | $\mathrm{V}_{\text {IN }}$ | Input voltage |
| 24 | $\mathrm{DL}_{3}$ | Gate-drive output for 3.3 V buck low-side MOSFET. |
| 25 | $\mathrm{BST}_{3}$ | Boost capacitor connection for 3.3 V buck converter. |
| 26 | $\mathrm{LX}_{3}$ | Inductor connection for 3.3 V buck low-side MOSFET. |
| 27 | $\mathrm{DH}_{3}$ | Gate-drive output for 3.3 V buck high-side MOSFET. |
| 28 | $\mathrm{FB}_{3}$ | Feedback for 3.3 V buck. |

TYPICAL CHARACTERISTICS ( $25^{\circ} \mathrm{C}$ unless otherwise noted)


Efficiency vs. 3.3 V Output Current


Efficiency vs. 5.0 V Output Current


Efficiency vs. 12 V Output Current

## TYPICAL WAVEFORMS




## TYPICAL WAVEFORMS



## STANDARD APPLICATION CIRCUIT



Figure 1.

## SMBUS Specification

SMBus: The System Management Bus is a two-wire interface through which simple power related chips can communicate with the rest of the system. It uses $I^{2} \mathrm{C}$ as its backbone. Both SDA and SCL are bidirectional lines, connected to a positive voltage via a pull-up resistor. When
the bus is free, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector in order to perform the wired AND function. Data on the SMBus can be transferred at a clock rate up to 100 kHz . Si9135 is a slave with SMBus address of 0110000.

## SMBUS TRUTH TABLE

| State | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Shutdown | 0 | 0 | 0 | X | X | X | X | X |
| Buck3 On | 1 | 0 | 0 | X | X | X | X | X |
| Buck5 On | 0 | 1 | 0 | X | X | X | X | X |
| Flyback On | 0 | 0 | 1 | X | X | X | X | X |
| Buck3, Buck5 On | 1 | 1 | 0 | X | X | X | X | X |
| Buck3, Flyback On | 1 | 0 | 1 | X | X | X | X | X |
| Buck5, Flyback on | 0 | 1 | 1 | X | X | X | X | X |
| All On | 1 | 1 | 1 | X | X | X | X | X |

Notes:

1. Positive logic level is used.
2. X: don't care.

SMBUS ELECTRICAL SPECIFICATION (Test Conditions: $\mathrm{V}+=5.5 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ )

| Symbol | Parameter | Min | Max | Units |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Data, Clock Input Low Voltage | -0.5 | 0.6 | V |  |
| $\mathrm{~V}_{\mathrm{IH}}$ | Data, Clock Input High Voltage | 1.4 | 5.5 |  |  |
| $\mathrm{~V}_{\mathrm{OL}}$ | Data, Clock Output Low Voltage |  | 0.4 |  |  |
| $\mathrm{I}_{\text {LEAK }}$ | Input Leakage |  | $\pm 1$ | $\mathrm{\mu A}$ |  |

## SMBUS AC SPECIFICATIONS

| Symbol | Parameter | Min | Max | Units |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{F}_{\text {SMB }}$ | SMBus Operation Frequency | 10 | 100 | kHz |
| $\mathrm{T}_{\text {BUF }}$ | Bus free time between Stop and Start | 4.7 |  | $\mu \mathrm{~s}$ |
| $\mathrm{~T}_{\text {HD }}$ | Data Hold Time | 300 |  | ns |
| $\mathrm{~T}_{\mathrm{SU}}$ | Data Setup Time | 250 |  |  |
| $\mathrm{~T}_{\text {LOW }}$ | Clock Low Period | 4.7 |  | $\mathrm{\mu s}$ |
| $\mathrm{~T}_{\text {HIGH }}$ | Clock High Period | 4.0 | 50 |  |
| $\mathrm{~T}_{\mathrm{F}}$ | Clock/Data Fall Time |  | 300 | ns |
| $\mathrm{~T}_{\mathrm{R}}$ | Clock/Data Rise Time |  | 1000 |  |

## TIMING DIAGRAMS



Figure 2. Start-Up Timing Sequence

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## DETAILED FUNCTIONAL BLOCK DIAGRAMS



Figure 3. Buck Block Diagram


Figure 4. PWM Flyback Block Diagram


Figure 5. Complete Si9135 Block Diagram

## DESCRIPTION OF OPERATION

## Start-up Sequence

Si9135 is normally controlled by its SMBus interface after $\mathrm{V}_{\text {IN }}$ is applied. Initially, if there is no incoming SMBus control command, it comes up in its default power on sequence, first the LDO 5 V will come up within its tolerance, and then the precision 3.3 V reference will come up. Immediately afterwards, the oscillator will begin and 3.3 V BUCK converter will turn on and then 5 V BUCK converter and at last 12 V FLYBACK converter. If Si9135 receives any SMBus controlling command after LDO 5 V is established, the designated converters will be allowed to turn on or off independently depending on the command received. In the event of all three converters are turned off, the oscillator will be turned off, the total system would only draw $35 \mu \mathrm{~A}$ supply current.
Each converter can soft-start separately. The integrated internal soft-start circuitry for each converter gradually increases the inductor maximum peak current during softstart period (approximately 4 msec ), preventing excessive
currents being drawn from the input during startup. The softstart is controlled by initial default start up sequence or incoming SMBus command.
Si9135 converters a 5.5 V to 30 V input voltage to five outputs, two BUCK (step-down) high current, PWM, switchmode supplies, one at 3.3 V and one at 5 V , one FLYBACK 12 V PWM switch-mode supply, one precision 3.3 V reference and one 5 V Low Drop Out linear regulator output. Switch-mode supply output current capabilities depend on external components (can exceed 10 A ). With typical application shown on the application diagram, the two BUCK converters deliver 4 A and the FLYBACK converters deliver 0.25 A . The recommended load current for precision 3.3 V reference output is less than 1 mA , the recommended load current for 5 V LDO output current is less than 30 mA . In order to maximize the power efficiency, when the 5 V BUCK converter supply is above 4.5 V , the BUCK converter's output is internal connected to LDO output.

## DESCRIPTION OF OPERATION (CONT'D)

## Buck Converter Operation

The 3.3 V and 5 V buck converters are both current-mode PWM and PSM (during light load operation) regulators using high-side bootstrap N -Channel and low-side N-Channel MOSFETs. At light load conditions, the converters switch at a lower frequency than the clock frequency, seen like some clock pulses between the actual switching are skipped, this operating condition is defined as pulse-skipping. The operation of the converter(s) switching at clock frequency is defined as normal operation.

## Normal Operation: Buck Converters

In normal operation, the buck converter high-side MOSFET is turned on with a delay (known as break-before-make time - $t_{\text {BBM }}$ ), after the rising edge of the clock. After a certain on time, the high-side MOSFET is turned off and then after a delay ( $\mathrm{t}_{\mathrm{BBM}}$ ), the low-side MOSFET is turned on until the next rising edge of the clock, or the inductor current reaches zero. The $\mathrm{t}_{\text {BBM }}$ (approximately 25 ns to 60 ns ), has been optimized to guarantee the efficiency is not adversely affected at the high switching frequency and a specified minimum to account for variations of possible MOSFET gate capacitances.
During the normal operation, the high-side MOSFET switch on-time is controlled internally to provide excellent line and load regulation over temperature. Both buck converters should have load, line, regulation to within $0.5 \%$ tolerance.

## Pulse Skipping: Buck Converters

When the buck converter switching frequency is less than the internal clock frequency, its operation mode is defined as pulse skipping mode. During this mode, the high-side MOSFET is turned on until $\mathrm{V}_{\mathrm{CS}}-\mathrm{V}_{\mathrm{FB}}$ reaches 20 mV , or the on time reaches its maximum duty ratio. After the high-side MOSFET is turned off, the low-side MOSFET is turned on after the $\mathrm{t}_{\mathrm{BBM}}$ delay, which will remain on until the inductor current reaches zero. The output voltage will rise slightly above the regulation voltage after this sequence, causing the controller to stay idle for the next one, or several clock cycles. When the output voltage falls slightly below the regulation level, the high-side MOSFET will be turned on again at the next clock cycle. With the converter remaining idle during some clock cycles, the switching losses are reduced in order to preserve conversion efficiency during the light output current condition.

## Current Limit: Buck Converters

When the buck converter inductor current is too high, the voltage across pin CS3(5) and pin FB3(5) exceeds approximately 120 mV , the high-side MOSFET would be turned off instantaneously regardless of the input, or output condition. The Si9135 features clock cycle by clock cycle current limiting capability.

## Flyback Converter Operation

Designed mainly for PCMCIA or EEPROM programming, the Si9135 has a 12 V output non-isolated buck boost converter, called for brevity a flyback. It consists of two N-Channel MOSFET switches that are turned on and off in phase, and two diodes. Similar to the buck converter, during the light load conditions, the flyback converter will switch at a frequency lower than the internal clock frequency, which can be defined as pulse skipping mode (PSM); otherwise, it is operating in normal PWM mode.

## Normal Operation: Flyback Converter

In normal operation mode, the two MOSFETs are turned on at the rising edge of the clock, and then turned off. The on time is controlled internally to provide excellent load, line, and temperature regulation. The flyback converter has load, line and temperature regulation well within $0.5 \%$.

## Pulse Skipping: Flyback Converter

Under the light load conditions, similar to the buck converter, the flyback converter will enter pulse skipping mode. The MOSFETs will be turned on until the inductor current increases to such a level that the voltage across the pin CSP and pin CSN reaches 100 mV , or the on time reaches the maximum duty cycle. After the MOSFETs are turned off, the inductor current will conduct through two diodes until it reaches zero. At this point, the flyback converter output will rise slightly above the regulation level, and the converter will stay idle for one or several clock cycle(s) until the output falls back slightly below the regulation level. The switching losses are reduced by skipping pulses and so the efficiency during light load is preserved.

## Current Limit: Flyback Converter

Similar to the buck converter; when the voltage across pin CSP and pin CSN exceeds 410 mV typical, the two MOSFETs will be turned off regardless of the input and output conditions.

## DESCRIPTION OF OPERATION (CONT'D)

## SMBus Commands

individually or as a group commanded on or off using a code word on the SMBus, as detailed in the SMBus Truth Table. The command sequence is:

1. Receive a start bit, which is a falling edge on the SDA line while the SCL line is high.
2. Receive a one-byte address, which for Si 9135 is 01100000.
3. Send an acknowledge bit.
4. Receive a one-byte command
5. Send an acknowledge bit.
6. Receive a stop bit, which is a rising edge on the SDA line while the SCL line is high.
This is a total of 20 bits, which at the maximum clock frequency of 100 kHz translates into $200 \mu \mathrm{sec}$ before any change in the status of Si9135 ban be accomplished.
If Si9135 receives a command to turn on (respectively, off) a converter that is already on (respectively, off) it shall not falsely command the converter off (respectively, on).
Si9135 must be able to receive a stop command at any time during a command sequence. If Si9135 receives a stop command during a command sequence, it must not change the state of any converter, and must be ready to receive the next command sequence.

## Grounding

There are two separate grounds on the Si9135, analog signal ground (GND) and power ground (PGND). The purpose of two separate grounds is to prevent the high currents on the power devices (both external and internal) from interfering with the analog signals. The internal components of Si 9135 have their grounds tied (internally) together. These two grounds are then tied together (externally) at a single point, to ensure Si9135 noise immunity.
This separation of grounds should be maintained in the external circuitry, with the power ground of all power devices being returned directly to the input capacitors, and the small signal ground being returned to the GND pin of Si9135.

## ON/OFF Function

Logic-low shuts off the appropriate section by disabling the gate drive stage. High-side and low-side gate drivers are turned off when ON/OFF pins are logic-low. Logic-high enables the DH and DL pins.

## Stability

## Buck Converters:

In order to simplify designs, the Si9135 requires no specified external components except load capacitors for stability control. Meanwhile, it achieves excellent regulation and efficiency. The converters are current mode control, with a bandwidth substantially higher than the LC tank dominant pole frequency of the output filter. To ensure stability, the minimum capacitance and maximum ESR values are:

$$
\mathrm{C}_{\text {LOAD }} \geq \frac{\mathrm{V}_{\text {REF }}}{2 \pi \times \mathrm{V}_{\mathrm{OUT}} \times \mathrm{R}_{\mathrm{CS}} \times \mathrm{BW}} \quad \mathrm{ESR} \leq \frac{\mathrm{V}_{\mathrm{OUT}} \times \mathrm{Rcs}_{\mathrm{cs}}}{\mathrm{~V}_{\text {REF }}}
$$

Where $\mathrm{V}_{\text {REF }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}$ is the output voltage ( 5 V or 3.3 V ), Rcs is the current sensing resistor in ohms and $\mathrm{BW}=$ 50 khz .
With the components specified in the application circuit $\left(\mathrm{L}=10 \mu \mathrm{H}, \quad\right.$ RCS $=0.02 \Omega, \mathrm{C}_{\text {OUT }}=330 \mu \mathrm{~F}, \mathrm{ESR}$ approximately $0.1 \Omega$, the converter should have a bandwidth at approximately 50 kHz , with minimum phase margin of $65^{\circ}$, and dc gain above 50 dB .

## Other Outputs

The Si9135 also provides a 3.3 V reference which can be external loaded up to 1 mA , as well as, a 5 V LDO output which can be loaded 30 mA , or even more depending on the system application. When the 5 V buck converter is turned on, the 5 V LDO output is shorted with the 5 V buck converter output, so its loading capability is substantially increased. For stability, the 3.3 V reference output requires a $1 \mu \mathrm{~F}$ capacitor, and 5 V LDO output requires a $4.7 \mu \mathrm{~F}$ capacitor.

## SSOP: 28-LEAD (5.3 MM) (POWER IC ONLY)



| Dim | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: |
|  | Min | Nom | Max |
| A | 1.73 | 1.88 | 1.99 |
| $\mathrm{A}_{1}$ | 0.05 | 0.13 | 0.21 |
| $\mathrm{A}_{2}$ | 1.68 | 1.75 | 1.78 |
| b | 0.25 | 0.30 | 0.38 |
| C | 0.09 | 0.15 | 0.20 |
| D | 10.07 | 10.20 | 10.33 |
| E | 7.60 | 7.80 | 8.00 |
| $E_{1}$ | 5.20 | 5.30 | 5.40 |
| e | 0.65 BSC |  |  |
| L | 0.63 | 0.75 | 0.95 |
| L1 |  | 1.25 BSC |  |
| R | 0.09 | 0.15 | --- |
| $\oslash$ | $0^{\circ}$ | $4^{\circ}$ | $8^{\circ}$ |
| ECN: S-40080—Rev. A, 02-Feb-04 DWG: 5915 |  |  |  |

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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