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## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

### 1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

## 1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

**Table 1.1 Performance outline**

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	62.5 ns ( $f(XIN) = 16$ MHz, $VCC = 3.0$ to $5.5$ V) 100 ns ( $f(XIN) = 10$ MHz, $VCC = 2.7$ to $5.5$ V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 "Product List"
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Input capture circuit)
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 8 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	Internal: 9 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator
	Oscillation stop detection function	Main clock oscillation stop detection function
	Electrical characteristics	Supply voltage
Power consumption		Typ. 8mA ( $VCC = 5.0$ V, ( $f(XIN) = 16$ MHz) Typ. 5mA ( $VCC = 3.0$ V, ( $f(XIN) = 10$ MHz) Typ. 35 $\mu$ A ( $VCC = 3.0$ V, Wait mode, Peripheral clock off) Typ. 0.7 $\mu$ A ( $VCC = 3.0$ V, Stop mode)
Flash memory	Program/erase supply voltage	$VCC = 2.7$ to $5.5$ V
	Program/erase endurance	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

### 1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

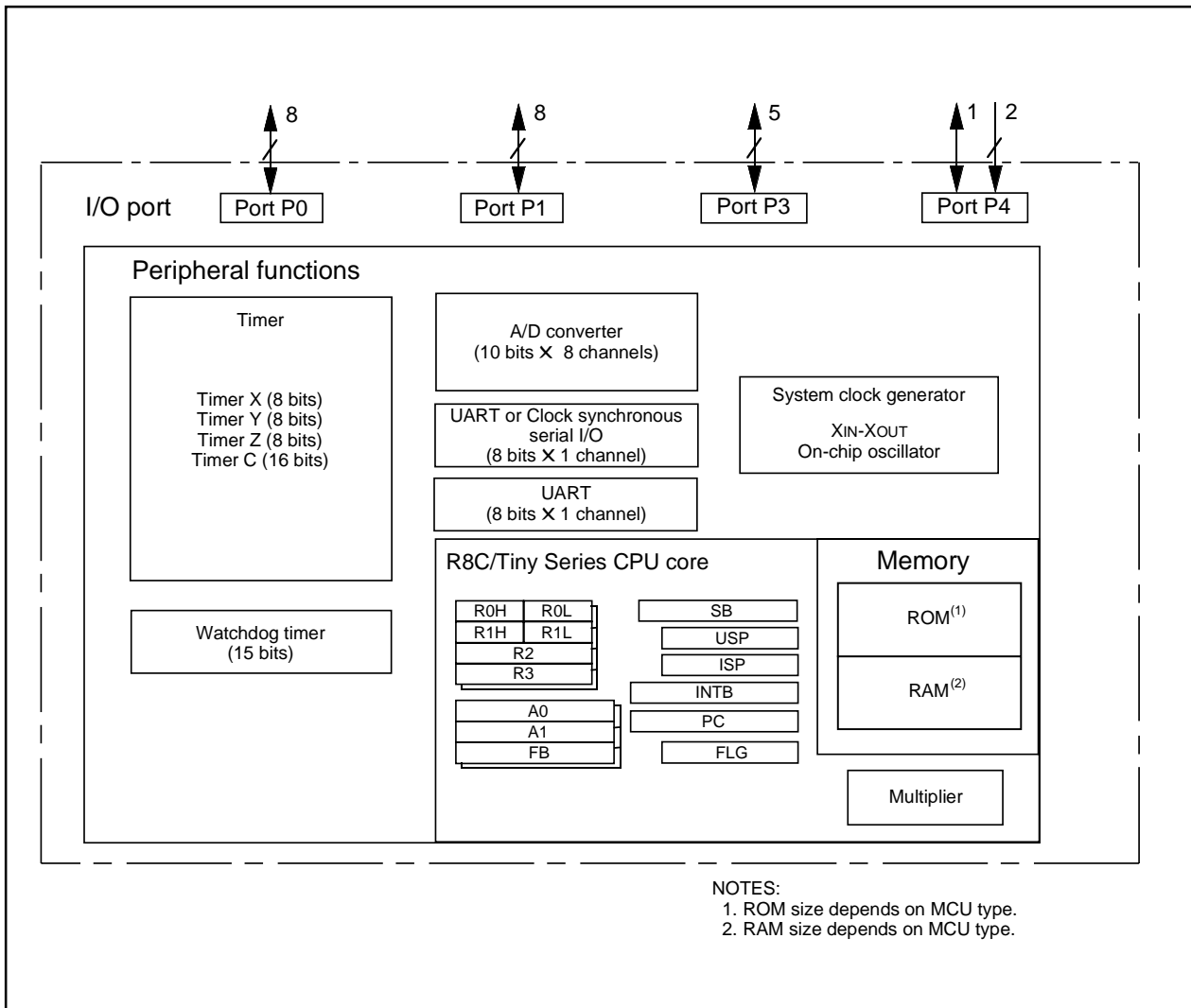


Figure 1.1 Block Diagram

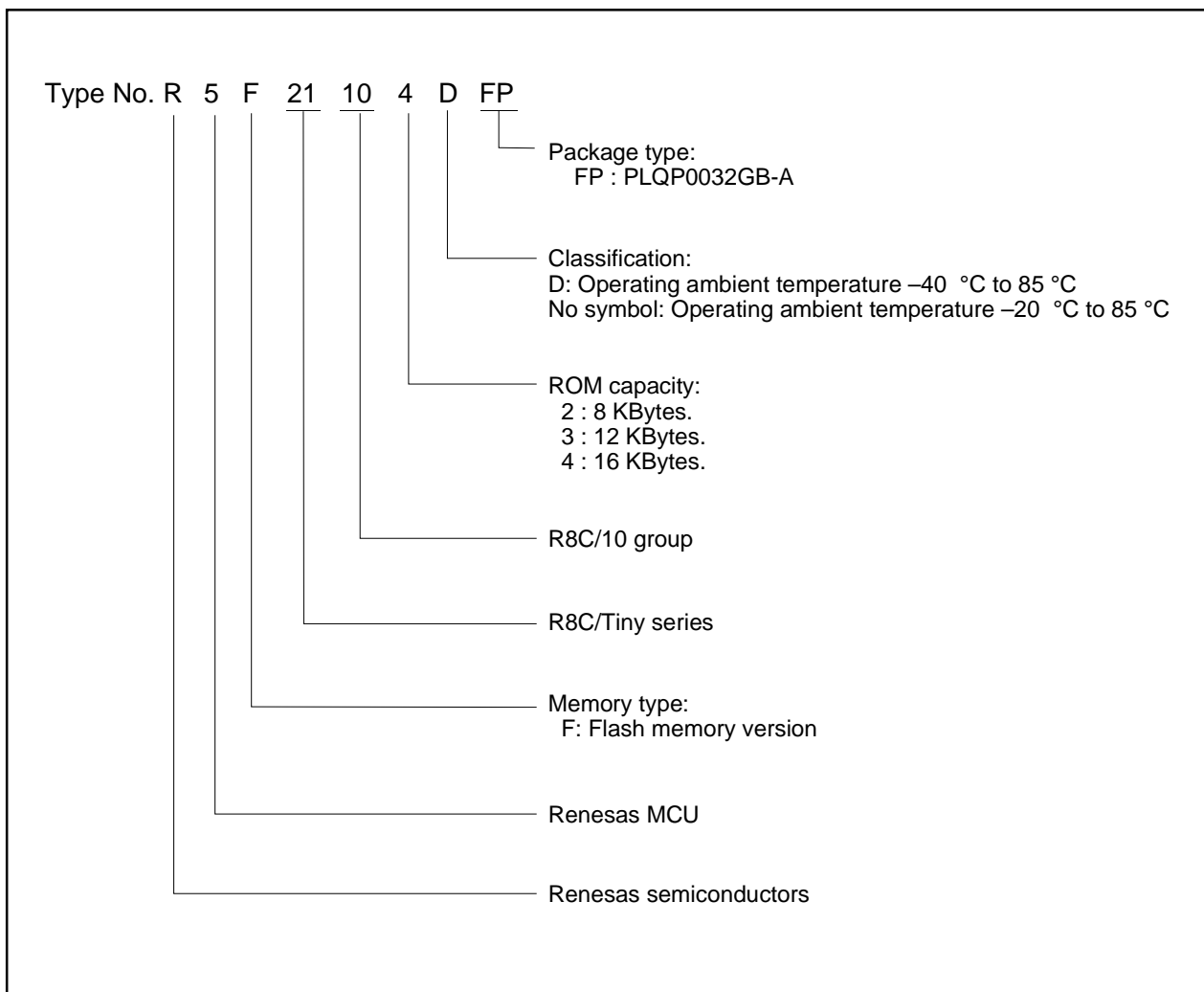
## 1.4 Product Information

Table 1.2 lists the product information.

**Table 1.2 Product Information**

As of January 2006

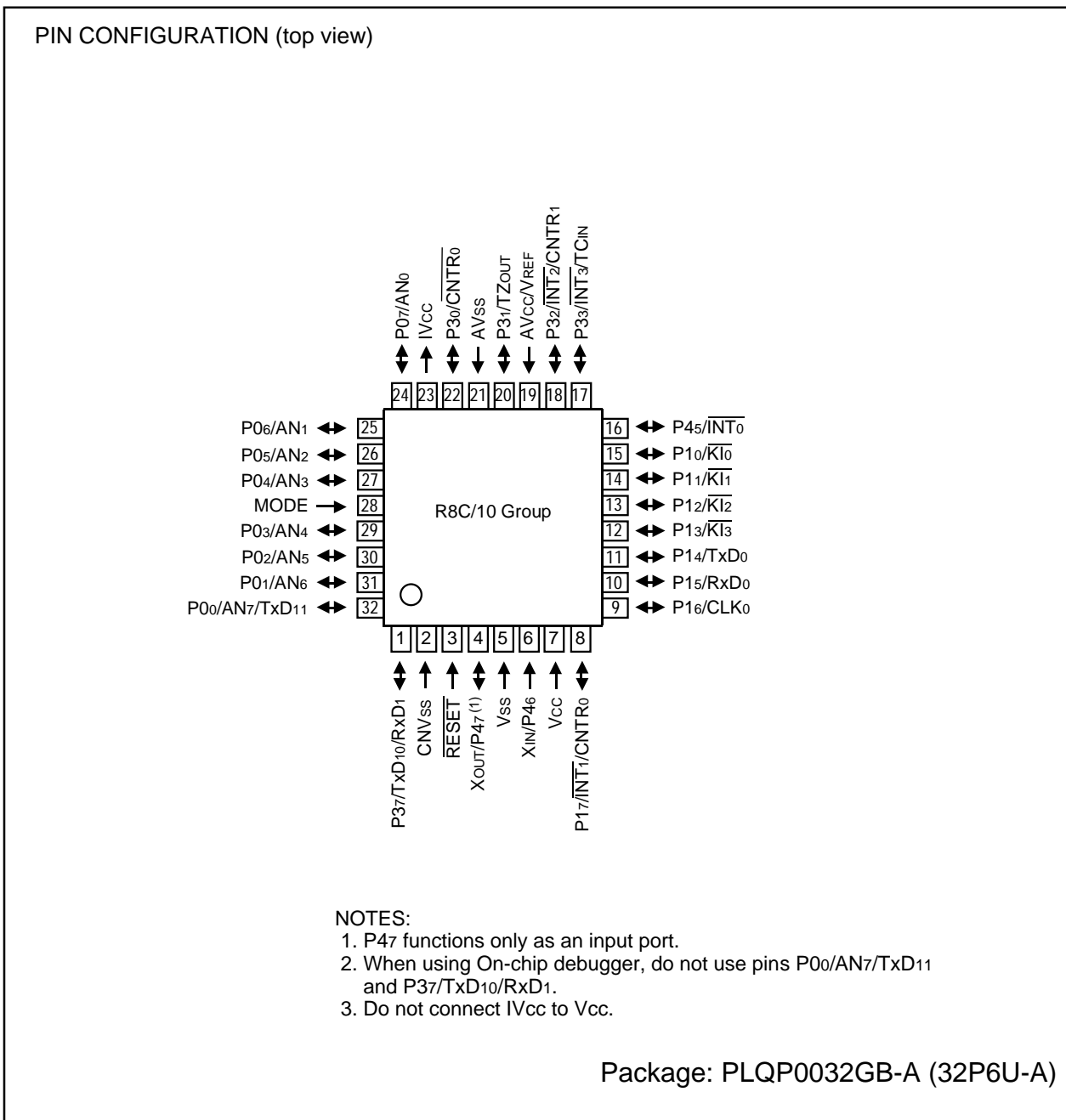
Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21102FP	8K bytes	512 bytes	PLQP0032GB-A	Flash memory version
R5F21103FP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104FP	16K bytes	1K bytes	PLQP0032GB-A	
R5F21102DFP	8K bytes	512 bytes	PLQP0032GB-A	D version
R5F21103DFP	12K bytes	768 bytes	PLQP0032GB-A	
R5F21104DFP	16K bytes	1K bytes	PLQP0032GB-A	



**Figure 1.2 Type No., Memory Size, and Package**

### 1.5 Pin Assignment

Figure 1.3 shows the pin Assignments (top view).



**NOTES:**

1. P47 functions only as an input port.
2. When using On-chip debugger, do not use pins P00/AN7/TxD11 and P37/TxD10/RxD1.
3. Do not connect IVcc to Vcc.

Figure 1.3 Pin Assignments (Top View)

## 1.6 Pin Description

Table 1.3 shows the pin description

**Table 1.3 Pin description**

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 $\mu$ F). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
INT interrupt input	INT $\bar{0}$ to INT $\bar{3}$	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt pins.
Timer X	CNTR $\bar{0}$	I/O	Timer X I/O pin
	CNTR $\bar{0}$	O	Timer X output pin
Timer Y	CNTR $\bar{1}$	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK $\bar{0}$	I/O	Transfer clock I/O pin.
	RxD $\bar{0}$ , RxD $\bar{1}$	I	Serial data input pins.
	TxD $\bar{0}$ , TxD $\bar{10}$ , TxD $\bar{11}$	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN $\bar{0}$ to AN $\bar{7}$	I	Analog input pins for A/D converter
I/O port	P0 $\bar{0}$ to P0 $\bar{7}$ , P1 $\bar{0}$ to P1 $\bar{7}$ , P3 $\bar{0}$ to P3 $\bar{3}$ , P3 $\bar{7}$ , P4 $\bar{5}$	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P1 $\bar{0}$ to P1 $\bar{7}$ also function as LED drive ports.
Input port	P4 $\bar{6}$ , P4 $\bar{7}$	I	Port for input-only.



## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

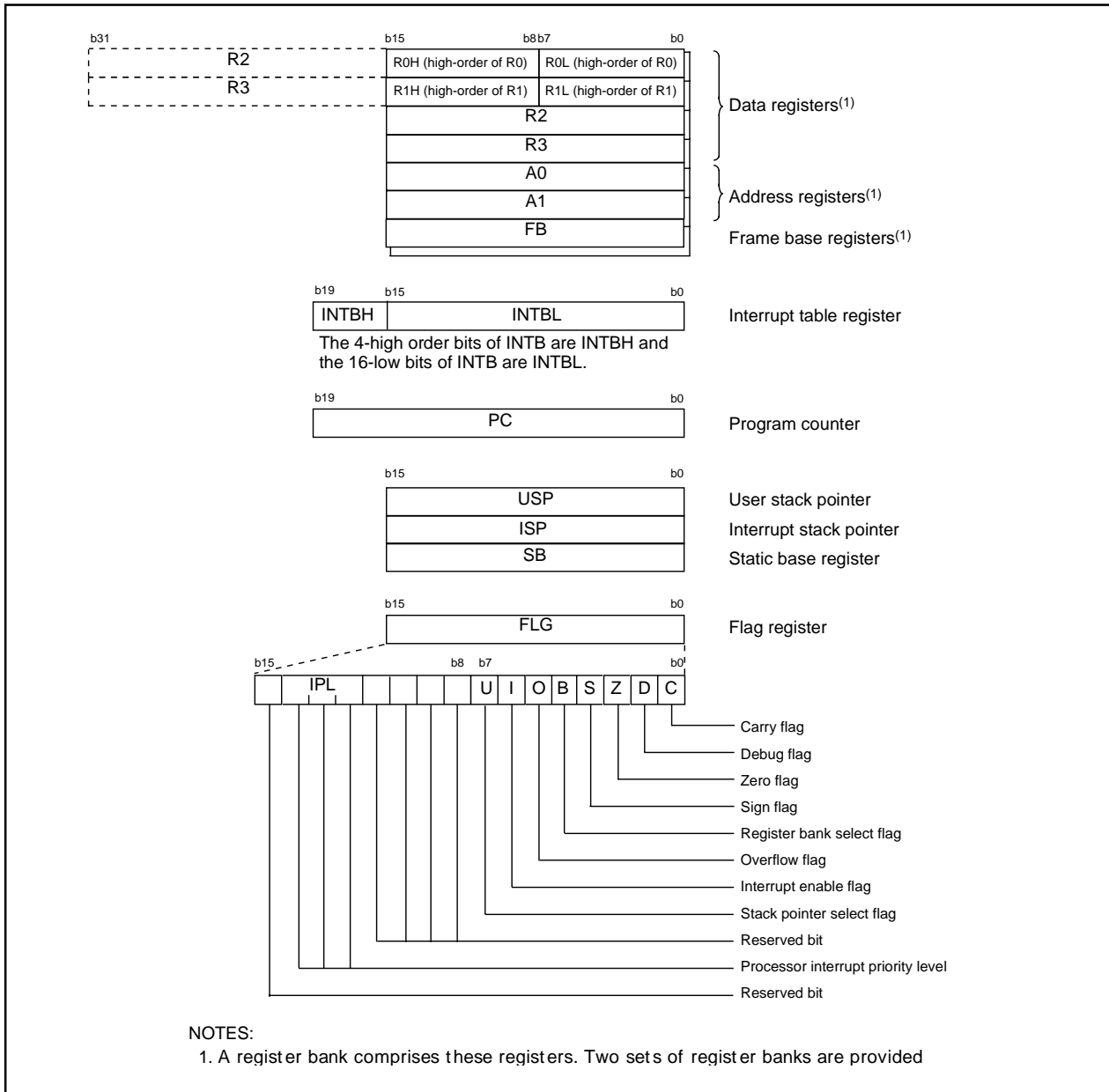


Figure 2.1 CPU Register

### 2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

### 2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

### 2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

### 2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

### 2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

### 3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000<sub>16</sub> to FFFFF<sub>16</sub>.

The internal ROM is allocated lower addresses beginning with address 0FFFF<sub>16</sub>. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000<sub>16</sub> to 0FFFF<sub>16</sub>.

The fixed interrupt vector table is allocated addresses 0FFDC<sub>16</sub> to 0FFFF<sub>16</sub>. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM is allocated addresses 00400<sub>16</sub> to 007FF<sub>16</sub>. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000<sub>16</sub> to 002FF<sub>16</sub>. The peripheral function control registers are located there. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

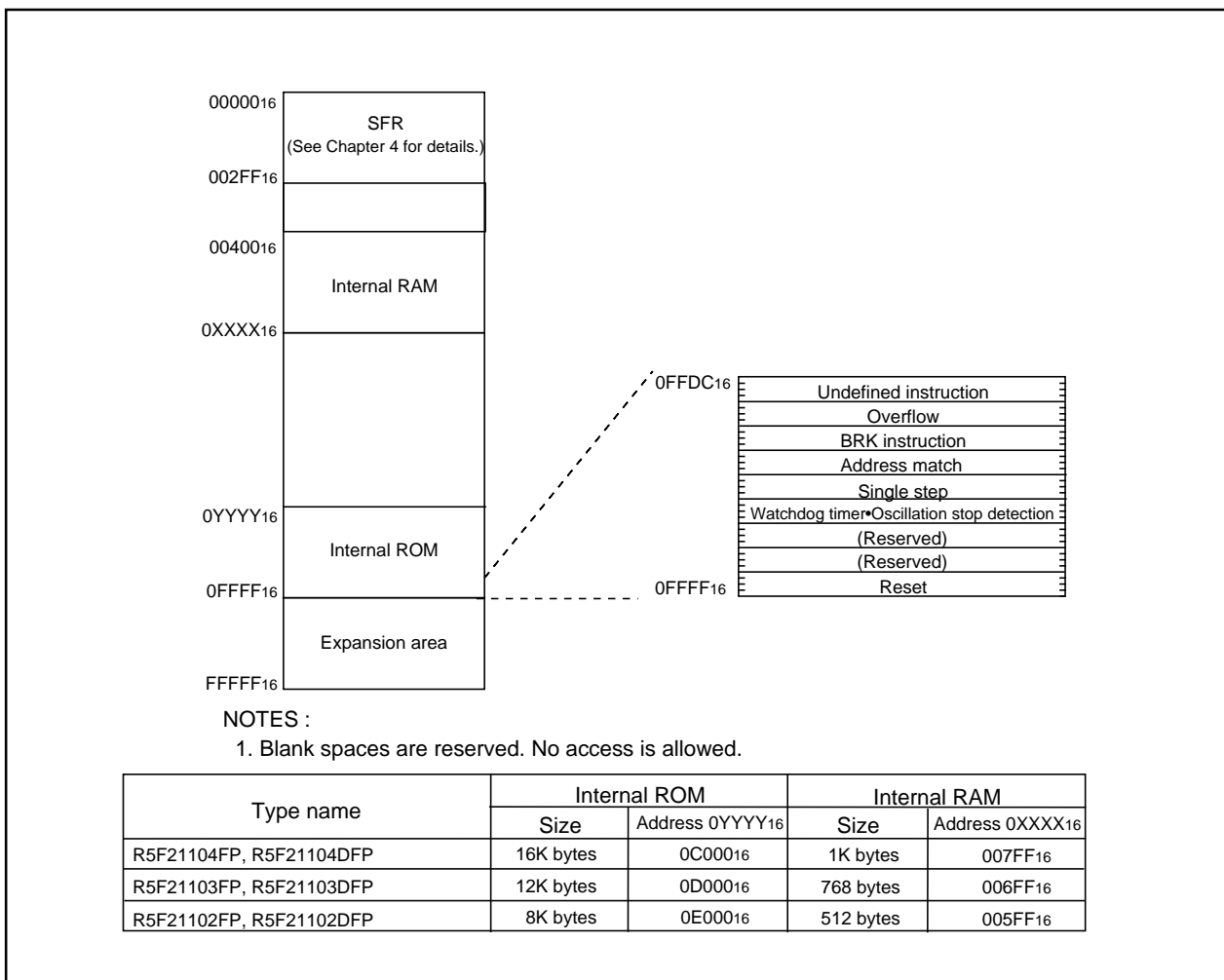


Figure 3.1 Memory Map

## 4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

**Table 4.1 SFR Information(1)(1)**

Address	Register	Symbol	After reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0	PM0	XXXX0X002
0005 <sub>16</sub>	Processor mode register 1	PM1	00XXX0X02
0006 <sub>16</sub>	System clock control register 0	CM0	011010002
0007 <sub>16</sub>	System clock control register 1	CM1	001000002
0008 <sub>16</sub>			
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX002
000A <sub>16</sub>	Protect register	PRCR	00XXX0002
000B <sub>16</sub>			
000C <sub>16</sub>	Oscillation stop detection register	OCD	000001002
000D <sub>16</sub>	Watchdog timer reset register	WDTR	XX16
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX16
000F <sub>16</sub>	Watchdog timer control register	WDC	000111112
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	0016
0011 <sub>16</sub>			0016
0012 <sub>16</sub>			X016
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	0016
0015 <sub>16</sub>			0016
0016 <sub>16</sub>			X016
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>			
001A <sub>16</sub>			
001B <sub>16</sub>			
001C <sub>16</sub>			
001D <sub>16</sub>			
001E <sub>16</sub>	INT0 input filter select register	INT0F	XXXXX0002
001F <sub>16</sub>			
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>			
0027 <sub>16</sub>			
0028 <sub>16</sub>			
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub>			
0039 <sub>16</sub>			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

**NOTES:**

- Blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.2 SFR Information(2)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX0002
004E <sub>16</sub>	AD conversion interrupt control register	ADIC	XXXXX0002
004F <sub>16</sub>			
0050 <sub>16</sub>			
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 <sub>16</sub>	INT2 interrupt control register	INT2IC	XXXXX0002
0056 <sub>16</sub>	Timer X interrupt control register	TXIC	XXXXX0002
0057 <sub>16</sub>	Timer Y interrupt control register	TYIC	XXXXX0002
0058 <sub>16</sub>	Timer Z interrupt control register	TZIC	XXXXX0002
0059 <sub>16</sub>	INT1 interrupt control register	INT1IC	XXXXX0002
005A <sub>16</sub>	INT3 interrupt control register	INT3IC	XXXXX0002
005B <sub>16</sub>	Timer C interrupt control register	TCIC	XXXXX0002
005C <sub>16</sub>			
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X0002
005E <sub>16</sub>			
005F <sub>16</sub>			
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

## NOTES :

- Blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.3 SFR Information(3)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0080 <sub>16</sub>	Timer Y, Z mode register	TYZMR	0016
0081 <sub>16</sub>	Prescaler Y register	PREY	FF16
0082 <sub>16</sub>	Timer Y secondary register	TYSC	FF16
0083 <sub>16</sub>	Timer Y primary register	TYPR	FF16
0084 <sub>16</sub>	Timer Y, Z waveform output control register	PUM	0016
0085 <sub>16</sub>	Prescaler Z register	PREZ	FF16
0086 <sub>16</sub>	Timer Z secondary register	TZSC	FF16
0087 <sub>16</sub>	Timer Z primary register	TZPR	FF16
0088 <sub>16</sub>			
0089 <sub>16</sub>			
008A <sub>16</sub>	Timer Y, Z output control register	TYZOC	0016
008B <sub>16</sub>	Timer X mode register	TXMR	0016
008C <sub>16</sub>	Prescaler X register	PREX	FF16
008D <sub>16</sub>	Timer X register	TX	FF16
008E <sub>16</sub>	Count source set register	TCSS	0016
008F <sub>16</sub>			
0090 <sub>16</sub>	Timer C register	TC	0016
0091 <sub>16</sub>			0016
0092 <sub>16</sub>			
0093 <sub>16</sub>			
0094 <sub>16</sub>			
0095 <sub>16</sub>			
0096 <sub>16</sub>	External input enable register	INTEN	0016
0097 <sub>16</sub>			
0098 <sub>16</sub>	Key input enable register	KIEN	0016
0099 <sub>16</sub>			
009A <sub>16</sub>	Timer C control register 0	TCC0	0016
009B <sub>16</sub>	Timer C control register 1	TCC1	0016
009C <sub>16</sub>	Capture register	TM0	0016
009D <sub>16</sub>			0016
009E <sub>16</sub>			
009F <sub>16</sub>			
00A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	0016
00A1 <sub>16</sub>	UART0 bit rate generator	U0BRG	XX16
00A2 <sub>16</sub>	UART0 transmit buffer register	U0TB	XX16
00A3 <sub>16</sub>			XX16
00A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	000010002
00A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	000000102
00A6 <sub>16</sub>	UART0 receive buffer register	U0RB	XX16
00A7 <sub>16</sub>			XX16
00A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	0016
00A9 <sub>16</sub>	UART1 bit rate generator	U1BRG	XX16
00AA <sub>16</sub>	UART1 transmit buffer register	U1TB	XX16
00AB <sub>16</sub>			XX16
00AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	000010002
00AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	000000102
00AE <sub>16</sub>	UART1 receive buffer register	U1RB	XX16
00AF <sub>16</sub>			XX16
00B0 <sub>16</sub>	UART transmit/receive control register 2	UCON	0016
00B1 <sub>16</sub>			
00B2 <sub>16</sub>			
00B3 <sub>16</sub>			
00B4 <sub>16</sub>			
00B5 <sub>16</sub>			
00B6 <sub>16</sub>			
00B7 <sub>16</sub>			
00B8 <sub>16</sub>			
00B9 <sub>16</sub>			
00BA <sub>16</sub>			
00BB <sub>16</sub>			
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

## NOTES:

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.4 SFR Information(4)<sup>(1)</sup>

Address	Register	Symbol	After reset
00C0 <sub>16</sub>	AD register	AD	XXXXXXXX <sub>2</sub>
00C1 <sub>16</sub>			XXXXXXXX <sub>2</sub>
00C2 <sub>16</sub>			
00C3 <sub>16</sub>			
00C4 <sub>16</sub>			
00C5 <sub>16</sub>			
00C6 <sub>16</sub>			
00C7 <sub>16</sub>			
00C8 <sub>16</sub>			
00C9 <sub>16</sub>			
00CA <sub>16</sub>			
00CB <sub>16</sub>			
00CC <sub>16</sub>			
00CD <sub>16</sub>			
00CE <sub>16</sub>			
00CF <sub>16</sub>			
00D0 <sub>16</sub>			
00D1 <sub>16</sub>			
00D2 <sub>16</sub>			
00D3 <sub>16</sub>			
00D4 <sub>16</sub>	AD control register 2	ADCON2	0016
00D5 <sub>16</sub>			
00D6 <sub>16</sub>	AD control register 0	ADCON0	00000XXX <sub>2</sub>
00D7 <sub>16</sub>	AD control register 1	ADCON1	0016
00D8 <sub>16</sub>			
00D9 <sub>16</sub>			
00DA <sub>16</sub>			
00DB <sub>16</sub>			
00DC <sub>16</sub>			
00DD <sub>16</sub>			
00DE <sub>16</sub>			
00DF <sub>16</sub>			
00E0 <sub>16</sub>	Port P0 register	P0	XX <sub>16</sub>
00E1 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>
00E2 <sub>16</sub>	Port P0 direction register	PD0	0016
00E3 <sub>16</sub>	Port P1 direction register	PD1	0016
00E4 <sub>16</sub>			
00E5 <sub>16</sub>	Port P3 register	P3	XX <sub>16</sub>
00E6 <sub>16</sub>			
00E7 <sub>16</sub>	Port P3 direction register	PD3	0016
00E8 <sub>16</sub>	Port P4 register	P4	XX <sub>16</sub>
00E9 <sub>16</sub>			
00EA <sub>16</sub>	Port P4 direction register	PD4	0016
00EB <sub>16</sub>			
00EC <sub>16</sub>			
00ED <sub>16</sub>			
00EE <sub>16</sub>			
00EF <sub>16</sub>			
00F0 <sub>16</sub>			
00F1 <sub>16</sub>			
00F2 <sub>16</sub>			
00F3 <sub>16</sub>			
00F4 <sub>16</sub>			
00F5 <sub>16</sub>			
00F6 <sub>16</sub>			
00F7 <sub>16</sub>			
00F8 <sub>16</sub>			
00F9 <sub>16</sub>			
03FA <sub>16</sub>			
00FB <sub>16</sub>			
00FC <sub>16</sub>	Pull-up control register 0	PUR0	00XX0000 <sub>2</sub>
00FD <sub>16</sub>	Pull-up control register 1	PUR1	XXXXXXXX <sub>2</sub>
00FE <sub>16</sub>	Port P1 drive capacity control register	DRR	0016
00FF <sub>16</sub>			
01B3 <sub>16</sub>	Flash memory control register 4	FMR4	01000000 <sub>2</sub>
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1	FMR1	0100XX0X <sub>2</sub>
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0	FMR0	00000012

## NOTES:

1. Blank columns, 0100<sub>16</sub> to 01B2<sub>16</sub> and 01B8<sub>16</sub> to 02FF<sub>16</sub> are all reserved. No access is allowed.

X : Undefined

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated value	Unit
V <sub>cc</sub>	Supply voltage	V <sub>cc</sub> =AV <sub>cc</sub>	-0.3 to 6.5	V
AV <sub>cc</sub>	Analog supply voltage	V <sub>cc</sub> =AV <sub>cc</sub>	-0.3 to 6.5	V
V <sub>i</sub>	Input voltage		-0.3 to V <sub>cc</sub> +0.3	V
V <sub>o</sub>	Output voltage		-0.3 to V <sub>cc</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>opr</sub> =25 °C	300	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter	Conditions	Standard			Unit	
			Min.	Typ.	Max.		
V <sub>cc</sub>	Supply voltage		2.7	—	5.5	V	
AV <sub>cc</sub>	Analog supply voltage		—	V <sub>cc</sub> (3)	—	V	
V <sub>ss</sub>	Supply voltage		—	0	—	V	
AV <sub>ss</sub>	Analog supply voltage		—	0	—	V	
V <sub>IH</sub>	"H" input voltage		0.8V <sub>cc</sub>	—	V <sub>cc</sub>	V	
V <sub>IL</sub>	"L" input voltage		0	—	0.2V <sub>cc</sub>	V	
I <sub>OH</sub> (sum)	"H" peak all output currents	Sum of all pins' IOH (peak)	—	—	-60.0	mA	
I <sub>OH</sub> (peak)	"H" peak output current		—	—	-10.0	mA	
I <sub>OH</sub> (avg)	"H" average output current		—	—	-5.0	mA	
I <sub>OL</sub> (sum)	"L" peak all output currents	Sum of all pins' IOL (peak)	—	—	60	mA	
I <sub>OL</sub> (peak)	"L" peak output current	Except P10 to P17	—	—	10	mA	
		P10 to P17	Drive capacity HIGH	—	—	30	mA
			Drive capacity LOW	—	—	10	mA
I <sub>OL</sub> (avg)	"L" average output current	Except P10 to P17	—	—	5	mA	
		P10 to P17	Drive capacity HIGH	—	—	15	mA
			Drive capacity LOW	—	—	5	mA
f (XIN)	Main clock input oscillation frequency	3.0V ≤ V <sub>cc</sub> ≤ 5.5V	0	—	16	MHz	
		2.7V ≤ V <sub>cc</sub> < 3.0V	0	—	10	MHz	

**NOTES:**

1. V<sub>cc</sub> = AV<sub>cc</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V<sub>cc</sub>=AV<sub>cc</sub>.



**Table 5.3 A/D Conversion Characteristics**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bit
—	Absolute accuracy	10 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=5.0$ V	—	—	$\pm 3$	LSB
		8 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=5.0$ V	—	—	$\pm 2$	LSB
		10 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=3.3$ V <sup>(3)</sup>	—	—	$\pm 5$	LSB
		8 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=3.3$ V <sup>(3)</sup>	—	—	$\pm 2$	LSB
$R_{LADDER}$	Ladder resistance		$V_{REF}=V_{CC}$	10	—	40	k $\Omega$
$t_{CONV}$	Conversion time	10 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=5.0$ V	3.3	—	—	$\mu$ s
		8 bit mode	$\phi_{AD}=10$ MHz, $V_{ref}=V_{CC}=5.0$ V	2.8	—	—	$\mu$ s
$V_{REF}$	Reference voltage			—	$V_{CC}$ <sup>(4)</sup>	—	V
$V_{IA}$	Analog input voltage			0	—	$V_{ref}$	V
—	A/D operating clock frequency <sup>(2)</sup>	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

## NOTES:

1.  $V_{CC}=AV_{CC}=2.7$  to  $5.5$ V at  $T_{opr} = -20$  to  $85$  °C /  $-40$  to  $85$  °C, unless otherwise specified.
2. If  $f_{AD}$  exceeds 10 MHz, divide the  $f_{AD}$  and hold A/D operating clock frequency ( $\phi_{AD}$ ) 10 MHz or below.
3. If the  $AV_{CC}$  is less than 4.2V, divide the  $f_{AD}$  and hold A/D operating clock frequency ( $\phi_{AD}$ )  $f_{AD}/2$  or below.
4. Hold  $V_{CC}=V_{ref}$ .

**Table 5.4 Flash Memory Version Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance		100	—	—	times
—	Byte program time		—	50	400	$\mu$ s
—	Block erase time		—	0.4	9	s
$t_{d(SR-ES)}$	Time delay from suspend request until erase suspend		—	—	8	ms
—	Erase Suspend Request Interval		10	—	—	ms
—	Program, Erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, Erase temperature		0	—	60	°C
—	Data hold time <sup>(2)</sup>	Ambient temperature= $55$ °C	20	—	—	year

## NOTES:

1.  $V_{CC1}=AV_{CC}=2.7$  to  $5.5$ V at  $T_{opr} = 0$  to  $60$  °C, unless otherwise specified.
2. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5 Power Circuit Timing Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on <sup>(2)</sup>		1	—	2000	$\mu$ s
$t_{d(R-S)}$	STOP release time <sup>(3)</sup>		—	—	150	$\mu$ s

## NOTES:

1. The measuring condition is  $V_{CC}=AV_{CC}=2.7$  to  $5.5$  V and  $T_{opr}=25$  °C.
2. This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

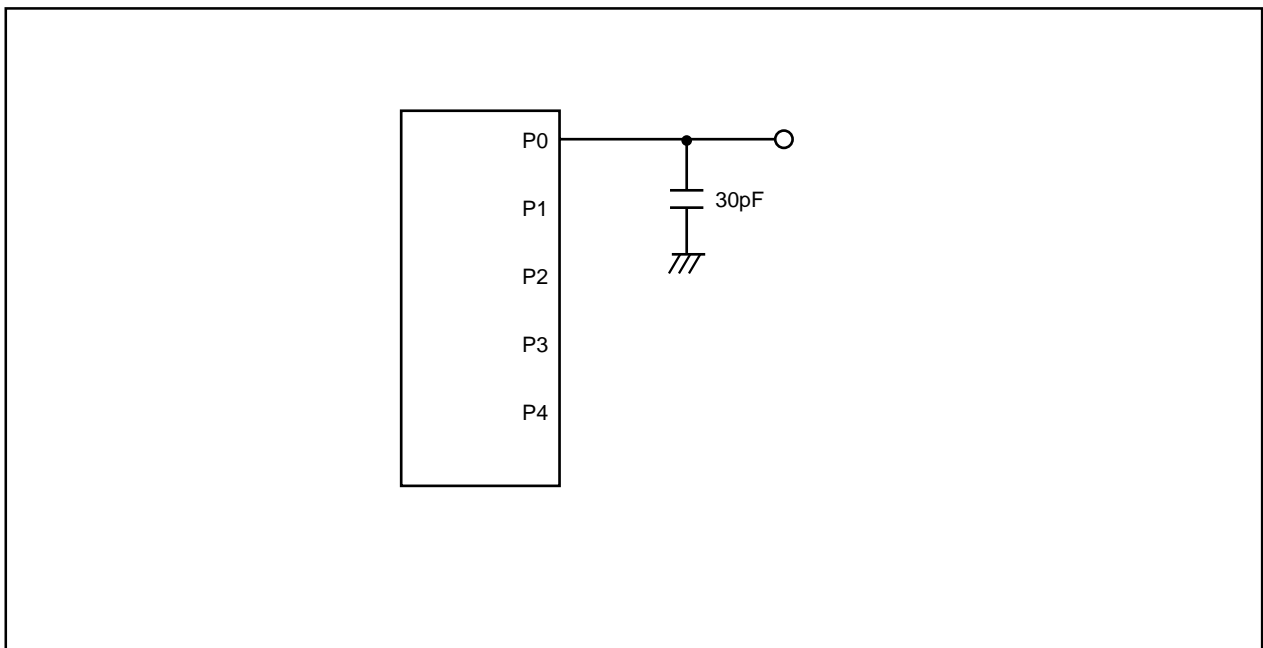


Figure 5.1 Port P0 to P4 measurement circuit

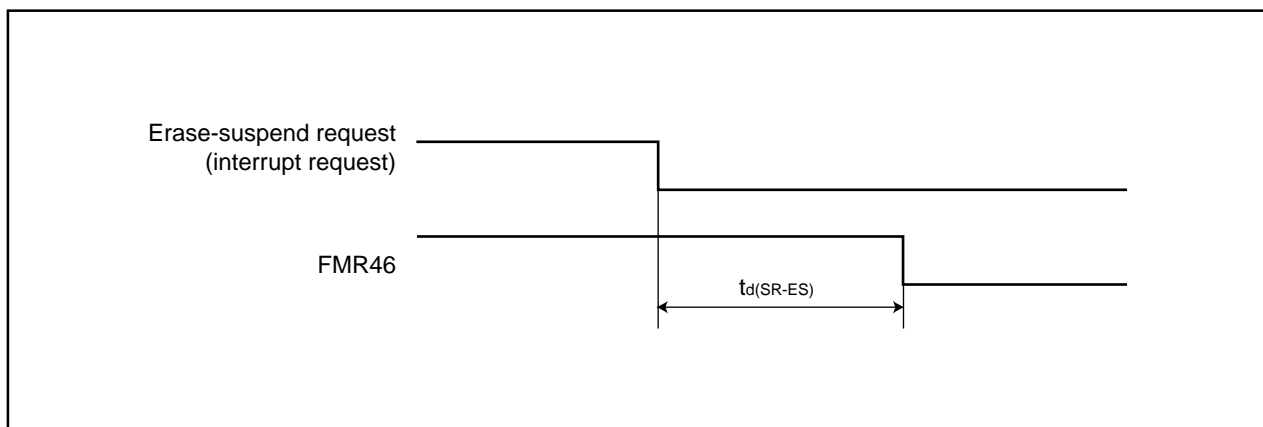


Figure 5.2 Time delay from Suspend Request until Erase Suspend

**Table 5.6 Electrical Characteristics (1) [Vcc=5V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-5mA	Vcc-2.0		Vcc	V
			IOH=-200μA	Vcc-0.3		Vcc	V
	XOUT		Drive capacity HIGH IOH=-1 mA	Vcc-2.0		Vcc	V
			Drive capacity LOW IOH=-500μA	Vcc-2.0		Vcc	V
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 5 mA			2.0	V
			IOL= 200 μA			0.45	V
	P10 to P17		Drive capacity HIGH IOL= 15 mA			2.0	V
			Drive capacity LOW IOL= 5 mA			2.0	V
			Drive capacity LOW IOL= 200 μA			0.45	V
	XOUT		Drive capacity HIGH IOL= 1 mA			2.0	V
Drive capacity LOW IOL=500μA					2.0	V	
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45 RESET		0.2		1.0	V
				0.2		2.2	V
IiH	"H" input current		VI=5V			5.0	μA
IiL	"L" input current		VI=0V			-5.0	μA
RPULLUP	Pull-up resistance		VI=0V	30	50	167	kΩ
RiXIN	Feedback resistance	XIN			1.0		MΩ
fRING	On-chip oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

## NOTES:

1. Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz unless otherwise specified.

**Table 5.7 Electrical Characteristics (2) [V<sub>CC</sub>=5V]**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode X <sub>IN</sub> =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
		High-speed mode X <sub>IN</sub> =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode X <sub>IN</sub> =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
		Medium-speed mode X <sub>IN</sub> =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
		On-chip oscillator mode Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	μA
		Wait mode Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>(1)</sup> Peripheral clock operation	—	40	80	μA
		Wait mode Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>(1)</sup> Peripheral clock off	—	38	76	μA
Stop mode Main clock off, T <sub>opr</sub> = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	μA		

## NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 4.2 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, f(X<sub>IN</sub>)=20MHz unless otherwise specified.

**Timing requirements (Unless otherwise noted:  $V_{CC} = 5V$ ,  $V_{SS} = 0V$  at  $T_{opr} = 25\text{ }^{\circ}C$ ) [ $V_{CC}=5V$ ]****Table 5.8 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(XIN)$	XIN input cycle time	62.5	–	ns
$t_{WH}(XIN)$	XIN input HIGH pulse width	30	–	ns
$t_{WL}(XIN)$	XIN input LOW pulse width	30	–	ns

**Table 5.9 CNTR0 input, CNTR1 input,  $\overline{INT2}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CNTR0)$	CNTR0 input cycle time	100	–	ns
$t_{WH}(CNTR0)$	CNTR0 input HIGH pulse width	40	–	ns
$t_{WL}(CNTR0)$	CNTR0 input LOW pulse width	40	–	ns

**Table 5.10 TCIN input,  $\overline{INT3}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(TCIN)$	TCIN input cycle time	400 <sup>(1)</sup>	–	ns
$t_{WH}(TCIN)$	TCIN input HIGH pulse width	200 <sup>(2)</sup>	–	ns
$t_{WL}(TCIN)$	TCIN input LOW pulse width	200 <sup>(2)</sup>	–	ns

## NOTES:

1. When using the Timer C capture function, adjust the cycle time above ( 1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above ( 1/ Timer C count source frequency x 1.5).

**Table 5.11 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_C(CK)$	CLKi input cycle time	200	–	ns
$t_W(CKH)$	CLKi input HIGH pulse width	100	–	ns
$t_W(CKL)$	CLKi input LOW pulse width	100	–	ns
$t_d(C-Q)$	TxDi output delay time	–	80	ns
$t_h(C-Q)$	TxDi hold time	0	–	ns
$t_{su}(D-C)$	RxDi input setup time	35	–	ns
$t_h(C-D)$	RxDi input hold time	90	–	ns

**Table 5.12 External interrupt  $\overline{INT0}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_W(INH)$	$\overline{INT0}$ input HIGH pulse width	250 <sup>(1)</sup>	–	ns
$t_W(INL)$	$\overline{INT0}$ input LOW pulse width	250 <sup>(2)</sup>	–	ns

## NOTES:

1. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use the  $\overline{INT0}$  input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or the minimum value of standard.

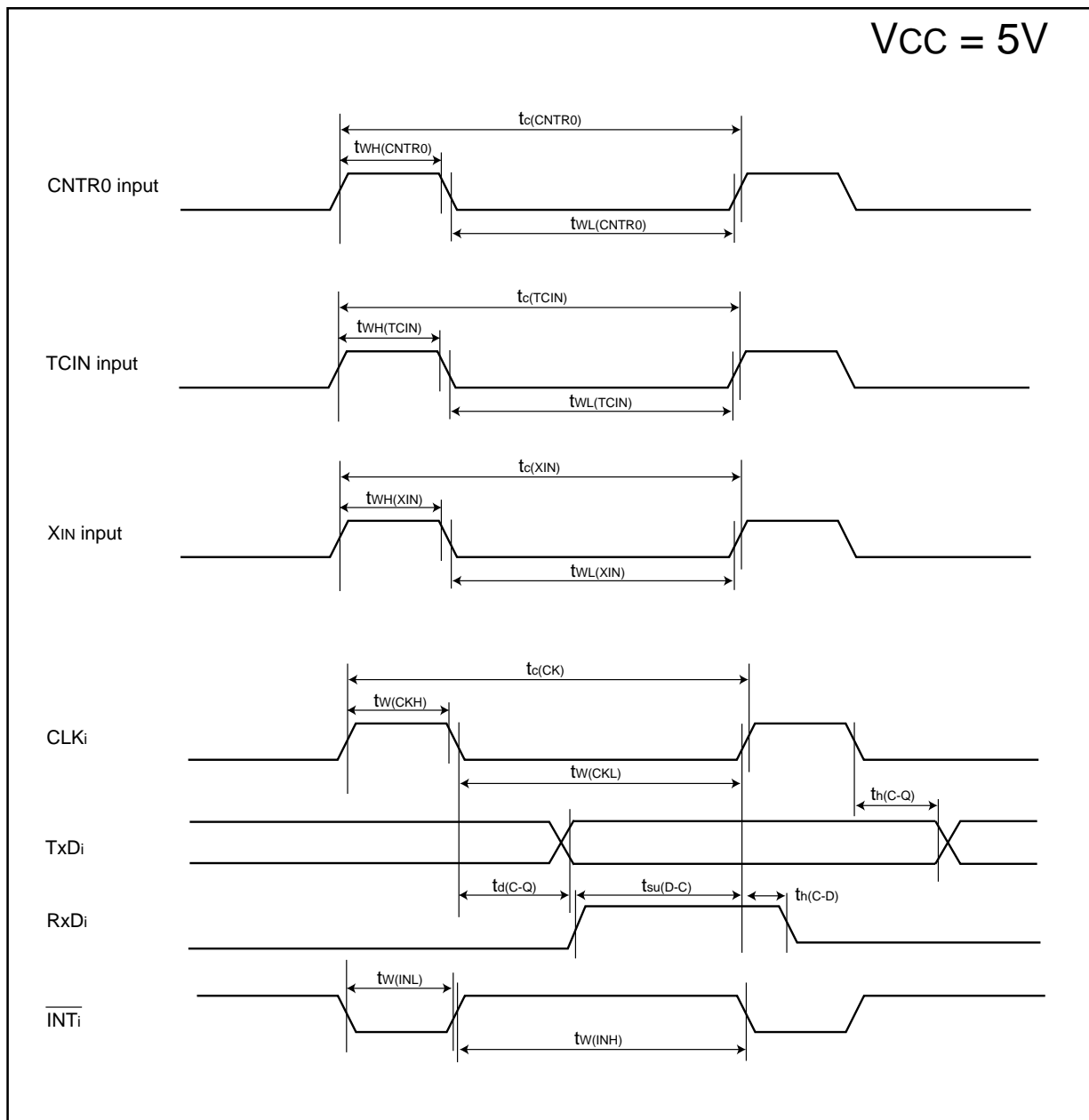


Figure 5.3  $V_{CC}=5V$  timing diagram

**Table 5.13 Electrical Characteristics (3) [Vcc=3V]**

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA		Vcc-0.5	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH=-0.1 mA	Vcc-0.5	—	Vcc	v
			Drive capacity LOW	IOH=-50 μA	Vcc-0.5	—	Vcc	v
VOL	"L" output voltage	Except P10 to P17, XOUT	IOL= 1 mA		—	—	0.5	V
		P10 to P17	Drive capacity HIGH	IOL= 2 mA	—	—	0.5	V
			Drive capacity LOW	IOL= 1 mA	—	—	0.5	v
		XOUT	Drive capacity HIGH	IOL= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	IOL=50 μA	—	—	0.5	V
VT+·VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
IiH	"H" input current			Vi=3V	—	—	4.0	μA
IiL	"L" input current			Vi=0V	—	—	-4.0	μA
RPULLUP	Pull-up resistance			Vi=0V	66	160	500	kΩ
RiXIN	Feedback resistance	XIN			—	3.0	—	MΩ
fRING	On-chip oscillator frequency				40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage			At stop mode	2.0	—	—	V

## NOTES:

1. Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

**Table 5.14 Electrical Characteristics (4) [Vcc=3V]**

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
I <sub>CC</sub>	Power supply current (V <sub>CC1</sub> =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode	X <sub>IN</sub> =16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	7	12	mA
			X <sub>IN</sub> =10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X <sub>IN</sub> =16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
			X <sub>IN</sub> =10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	420	800	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>(1)</sup> Peripheral clock operation	—	37	74	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed <sup>(1)</sup> Peripheral clock off	—	35	70	μA
Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.7	3.0	μA		

## NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V<sub>CC</sub>=AV<sub>CC</sub>=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X<sub>IN</sub>)=10MHz unless otherwise specified.



**Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc=3V]****Table 5.15 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100	–	ns
tWH(XIN)	XIN input HIGH pulse width	40	–	ns
tWL(XIN)	XIN input LOW pulse width	40	–	ns

**Table 5.16 CNTR0 input, CNTR1 input,  $\overline{\text{INT2}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300	–	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120	–	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120	–	ns

**Table 5.17 TCIN input,  $\overline{\text{INT3}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 <sup>(1)</sup>	–	ns
tWH(TCIN)	TCIN input HIGH pulse width	600 <sup>(2)</sup>	–	ns
tWL(TCIN)	TCIN input LOW pulse width	600 <sup>(2)</sup>	–	ns

**NOTES:**

1. When using the Timer C capture function, adjust the cycle time above ( 1 / Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above ( 1 / Timer C count source frequency x 1.5).

**Table 5.18 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300	–	ns
tW(CKH)	CLKi input HIGH pulse width	150	–	ns
tW(CKL)	CLKi input LOW pulse width	150	–	ns
td(C-Q)	TxDi output delay time	–	160	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	55	–	ns
th(C-D)	RxDi input hold time	90	–	ns

**Table 5.19 External interrupt  $\overline{\text{INT0}}$  input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380 <sup>(1)</sup>	–	ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380 <sup>(2)</sup>	–	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input HIGH pulse width to the greater value, either ( 1 / digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the  $\overline{\text{INT0}}$  input filter select bit, use the  $\overline{\text{INT0}}$  input LOW pulse width to the greater value, either ( 1 / digital filter clock frequency x 3) or the minimum value of standard.

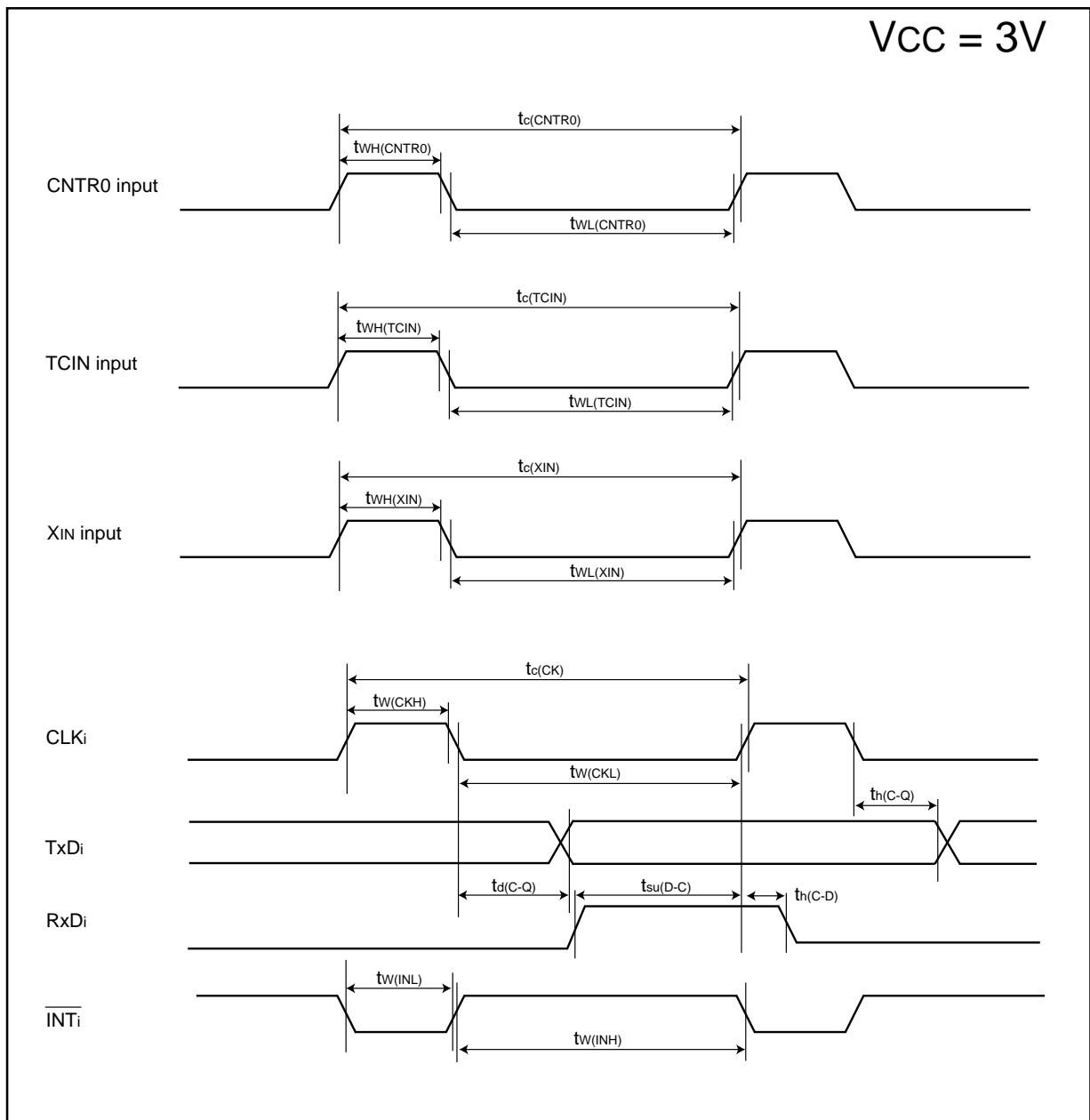
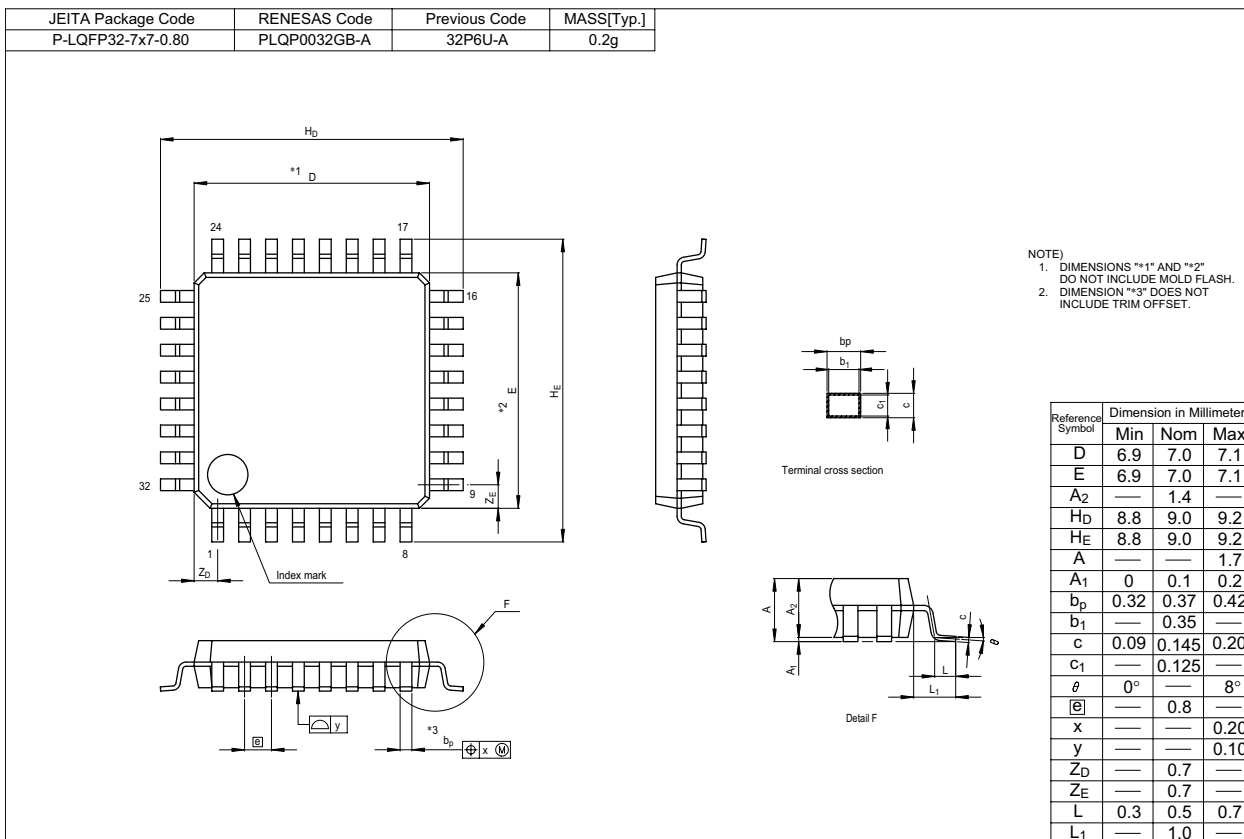


Figure 5.4  $V_{CC}=3V$  timing diagram

### Package Dimensions



REVISION HISTORY

R8C/10 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 12 14	Table 1.1: Shortest instruction execution time and f(XIN) changed Figure 1.3: Pin name changed from TXOUT to CNTR $\bar{0}$ Table 1.3: Pin name changed from TXOUT to CNTR $\bar{0}$ The value of Time C register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 14 15 16 18  19 20 21 22  23 24	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Table 5.2: Note 3 and Note 4 deleted tsamp in Table 5.3 deleted Figure 5.1 added Table 5.7: Vcc changed from "4.2 to 5.5V" to "3.3V to 5.5V", on-chip oscillator changed from "on 100kHz" to "125kHz", XIN=5MHz deleted and XIN=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.8 to Table 5.12 added Figure 5.2 added Table 5.13: Note 1, f(BCLK)=5 MHz changed to 10 MHz Table 5.14: on-chip oscillator changed from "on 100kHz" to "125kHz", XIN=5MHz deleted and XIN=10MHz added in high-speed mode and medium-speed mode, data added and modified Table 5.15 to Table 5.19 added Figure 5.3 added
1.30	Dec 05, 2003	4 15	Table 1.2 : ** deleted Table 5.4 revised
1.40	Sep 30, 2004	All pages 2 5 6 10-13 12 14 15 17 18 19 21 22 23	Words standardized (on-chip oscillator, serial interface, A/D) Table 1.1 revised Figure 1.3, NOTES 3 added Table 1.3 revised One body sentence in chapter 4 added ; Titles 4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised Table 5.2 revised Table 5.3 revised ; Table 5.4 revised Table 5.6 revised Table 5.7 revised Table 5.8 revised ; Table 5.12 revised Table 5.13 revised Table 5.14 revised Table 5.15 revised ; Table 5.17 revised ; Table 5.19 revised
1.50	Apr.27.2005	4 5 10	Table 1.2, Figure 1.2 package name revised Figure 1.3 package name revised Table 4.1 revised

REVISION HISTORY

R8C/10 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.50	Apr.27.2005	12	Table 4.3 revised
		15	Table 5.3 partly revised Table 5.4 partly added Table 5.5 partly revised
		17	Table 5.6 partly revised
		21	Table 5.13 partly revised
		25	Package Dimensions revised
1.60	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2 "Product List" → "Product Informaton" revised
		6	Figure 1.2 Type No., Memory Size, and Package partly revised
		7-8	Table 1.3 Pin description revised 2 Central Processing Unit (CPU) revised Figure 2.1 CPU register revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised
		11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3); 0081 <sub>16</sub> : "Prescaler Y" → "Prescaler Y Register" 0082 <sub>16</sub> : "Timer Y Secondary" → "Timer Y Secondary Register" 0083 <sub>16</sub> : "Timer Y Primary" → "Timer Y Primary Register" 0085 <sub>16</sub> : "Prescaler Z" → "Prescaler Z Register" 0086 <sub>16</sub> : "Timer Z Secondary" → "Timer Z Secondary Register" 0087 <sub>16</sub> : "Timer Z Primary" → "Timer Z Primary Register" 008C <sub>16</sub> : "Prescaler X" → "Prescaler X Register" revised NOTES:1 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		14	Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		15	Table 5.3 A/D Conversion Characteristics; "A/D operation clock frequency" → "A/D operating clock frequency" revised NOTES: 1, 2, 3, 4 revised Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; "Data retention duration" → "Data hold time" revised "Topr" → "Ambient temperature" revised NOTES: 2 added Measuring condition of byte program time and block erase time deleted
		17	Table 5.6 Electrical Characteristics (1) [V <sub>CC</sub> =5V]; "P1 <sub>0</sub> to P1 <sub>7</sub> Except X <sub>OUT</sub> " → "Except P1 <sub>0</sub> to P1 <sub>7</sub> , X <sub>OUT</sub> " revised
		18	Table 5.7 Electrical Characteristics (2) [V <sub>CC</sub> =5V] NOTES: 1, 2 revised Measuring condition: Stop mode "Topr = 25 °C"
		21	Table 5.13 Electrical Characteristics (3) [V <sub>CC</sub> =3V] "P1 <sub>0</sub> to P1 <sub>7</sub> Except X <sub>OUT</sub> " → "Except P1 <sub>0</sub> to P1 <sub>7</sub> , X <sub>OUT</sub> " revised
22	Table 5.14 Electrical Characteristics (4) [V <sub>CC</sub> =3V] NOTES: 1, 2 revised Measuring condition: Stop mode "Topr = 25 °C"		

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