PMF370XN

N-channel TrenchMOS extremely low level FET

5 July 2019 **Product data sheet**

1. General description

Extremely low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Low threshold voltage
- Saves PCB space due to small footprint (40 % smaller than SOT23)
- Suitable for low gate drive sources
- Surface-mounted package

3. Applications

- Driver circuits
- Switching in portable appliances

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	30	V
I_D	drain current	V_{GS} = 4.5 V; T_{sp} = 25 °C		-	-	0.87	A
P_{tot}	total power dissipation	T_{sp} = 25 °C		-	-	0.56	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 25 °C		-	370	440	mΩ

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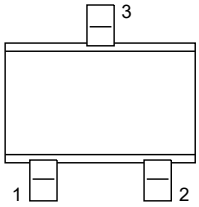
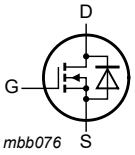
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-70 (SOT323)	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMF370XN	SC-70	plastic surface-mounted package; 3 leads	SOT323

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMF370XN	F6%

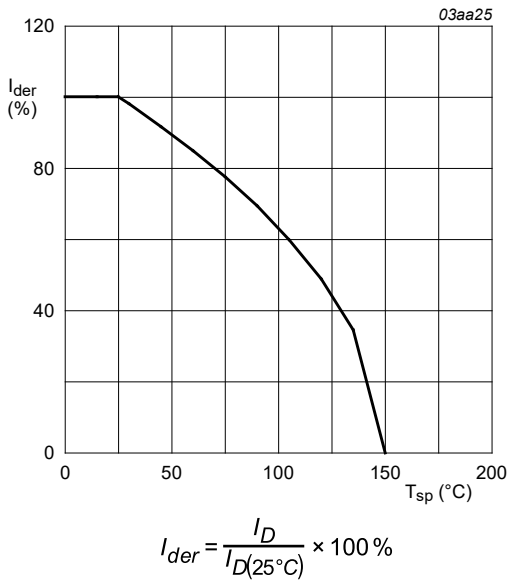
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

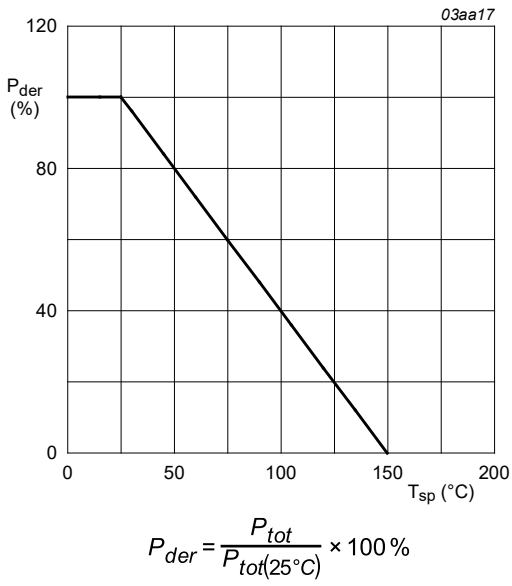
In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	V_{GS} = 4.5 V; T_{sp} = 25 °C		-	0.87	A
		V_{GS} = 4.5 V; T_{sp} = 100 °C		-	0.55	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs		-	1.74	A
P_{tot}	total power dissipation	T_{sp} = 25 °C		-	0.56	W
T_j	junction temperature			-55	150	°C
T_{stg}	storage temperature			-55	150	°C
I_S	source current	T_{sp} = 25 °C		-	0.47	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{sp} = 25 °C		-	0.94	A



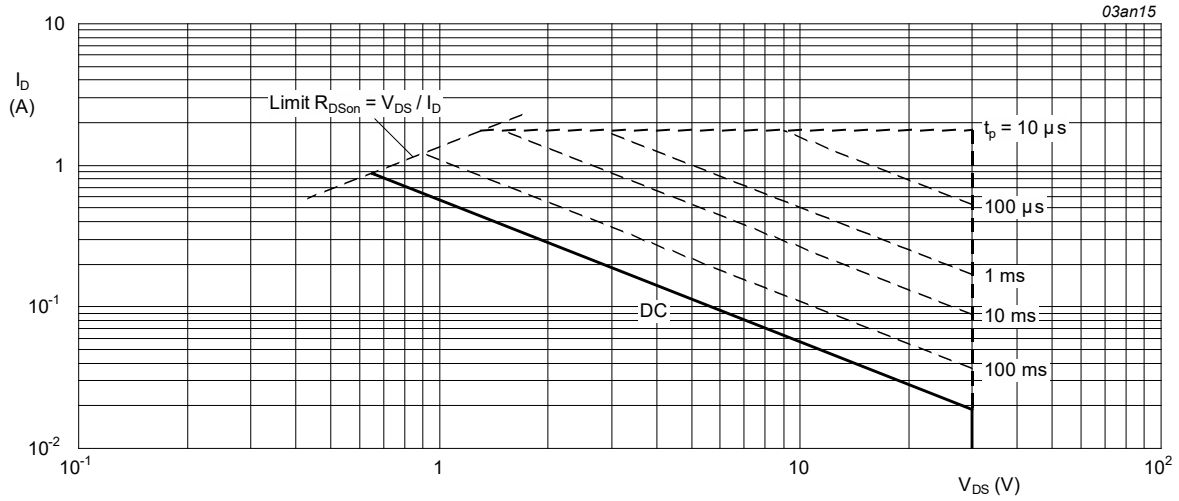
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig. 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25°C; I_{DM}$ is single pulse; $V_{GS} = 4.5V$

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point			-	-	220	K/W

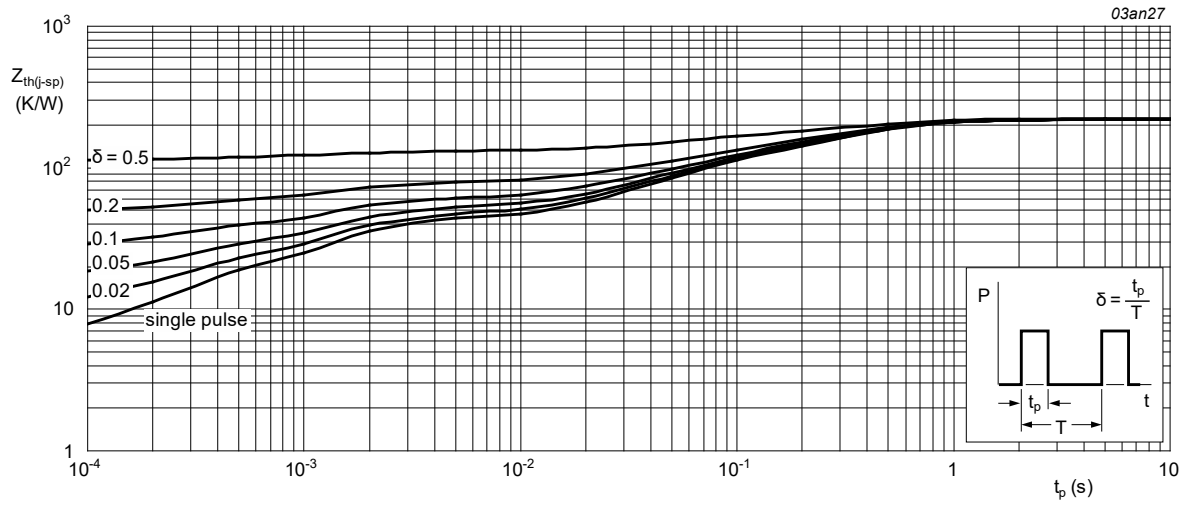
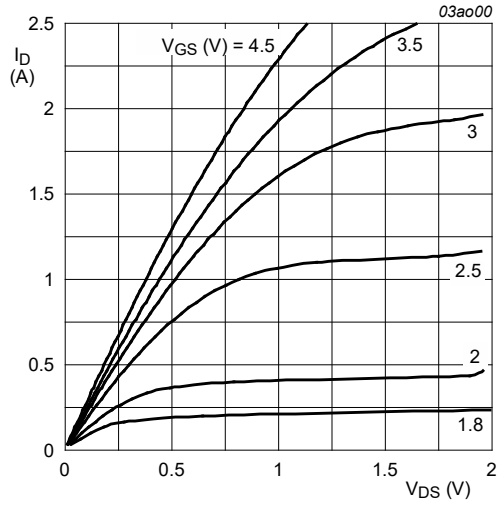


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

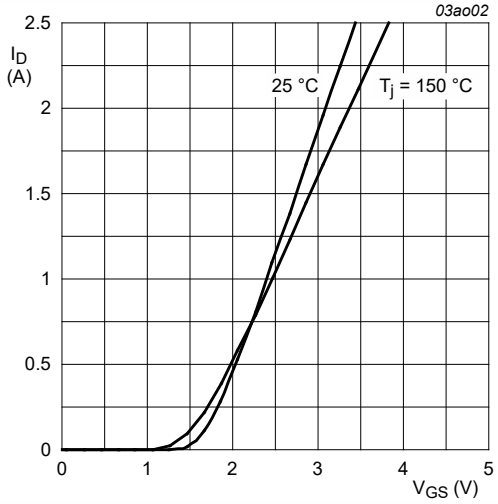
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = -55 °C		-	-	1.8	V
		I_D = 250 µA; V_{DS} = V_{GS}; T_j = 150 °C		0.35	-	-	V
		I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C		0.5	1	1.5	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 70 °C		-	-	2	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C		-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 0.1 A; T_j = 25 °C		-	550	650	mΩ
		V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 150 °C		-	629	748	mΩ
		V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 25 °C		-	370	440	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 1 A; V_{GS} = 4.5 V; T_j = 25 °C		-	0.65	-	nC
Q_{GS}	gate-source charge			-	0.14	-	nC
Q_{GD}	gate-drain charge			-	0.18	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	37	-	pF
C_{oss}	output capacitance			-	8.5	-	pF
C_{rss}	reverse transfer capacitance			-	5.5	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 15 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	6.5	-	ns
t_r	rise time			-	9.5	-	ns
$t_{d(off)}$	turn-off delay time			-	14	-	ns
t_f	fall time			-	5.5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 0.3 A; V_{GS} = 0 V; T_j = 25 °C		-	0.81	1.2	V



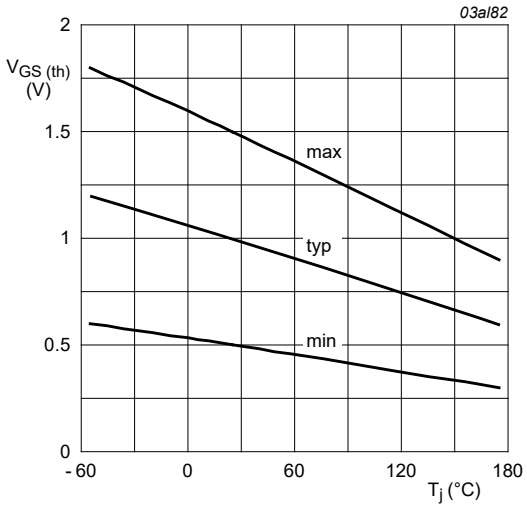
T_j = 25 °C

Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values



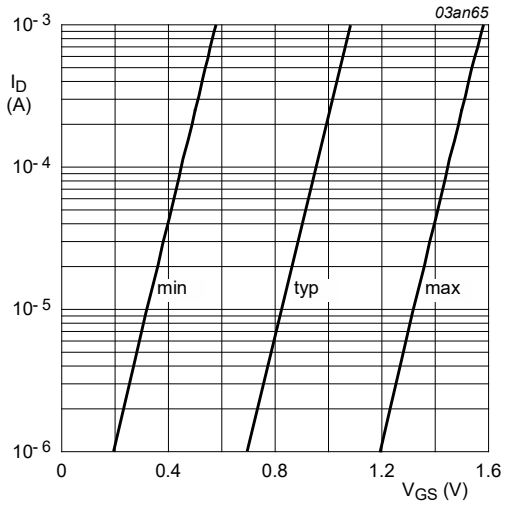
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



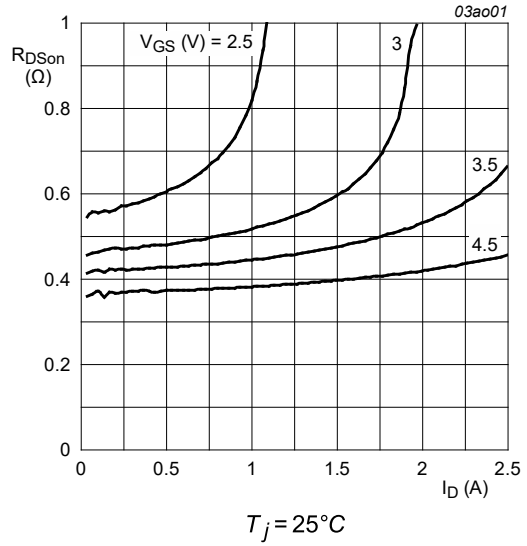
$I_D = 0.25A; V_{DS} = V_{GS}$

Fig. 7. Gate-source threshold voltage as a function of junction temperature



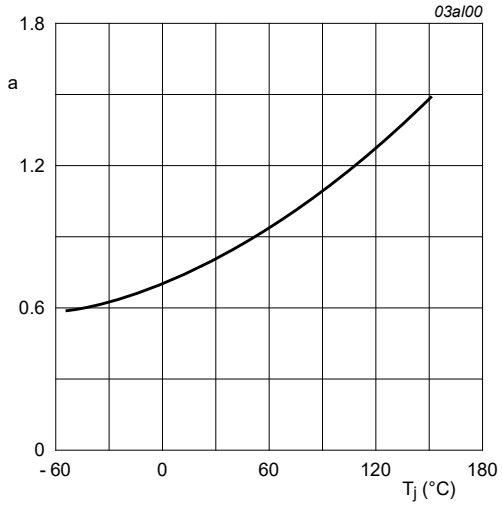
$T_j = 25°C; V_{DS} = 5V$

Fig. 8. Subthreshold drain current as a function of gate-source voltage



$T_j = 25°C$

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

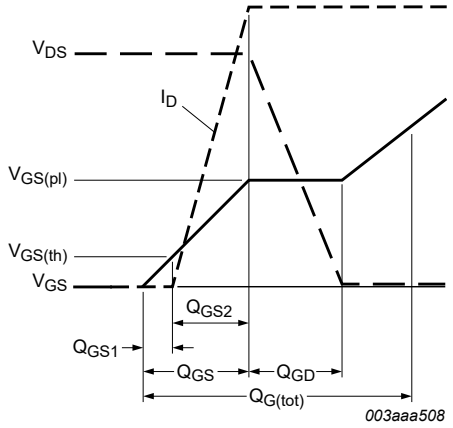
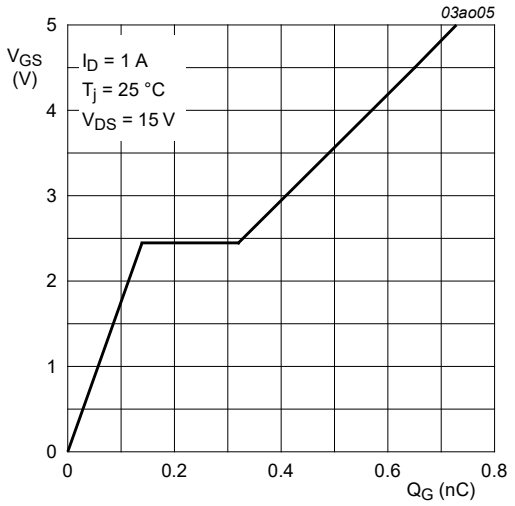
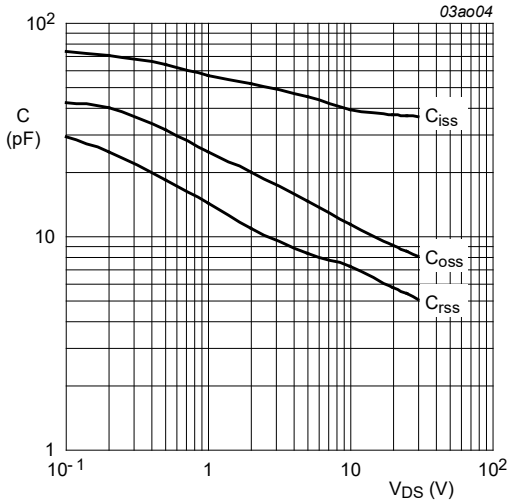


Fig. 11. Gate charge waveform definitions



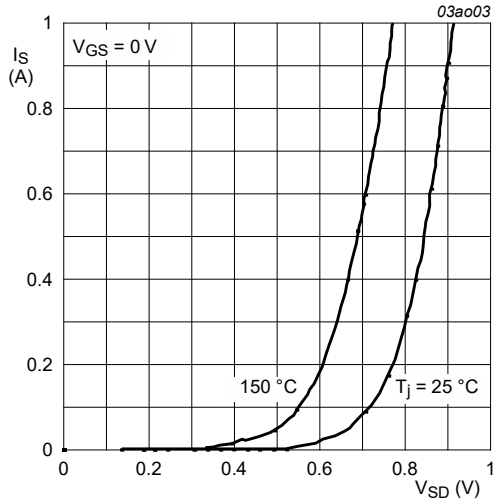
$I_D = 1A; V_{DS} = 15V$

Fig. 12. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V; 1 MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

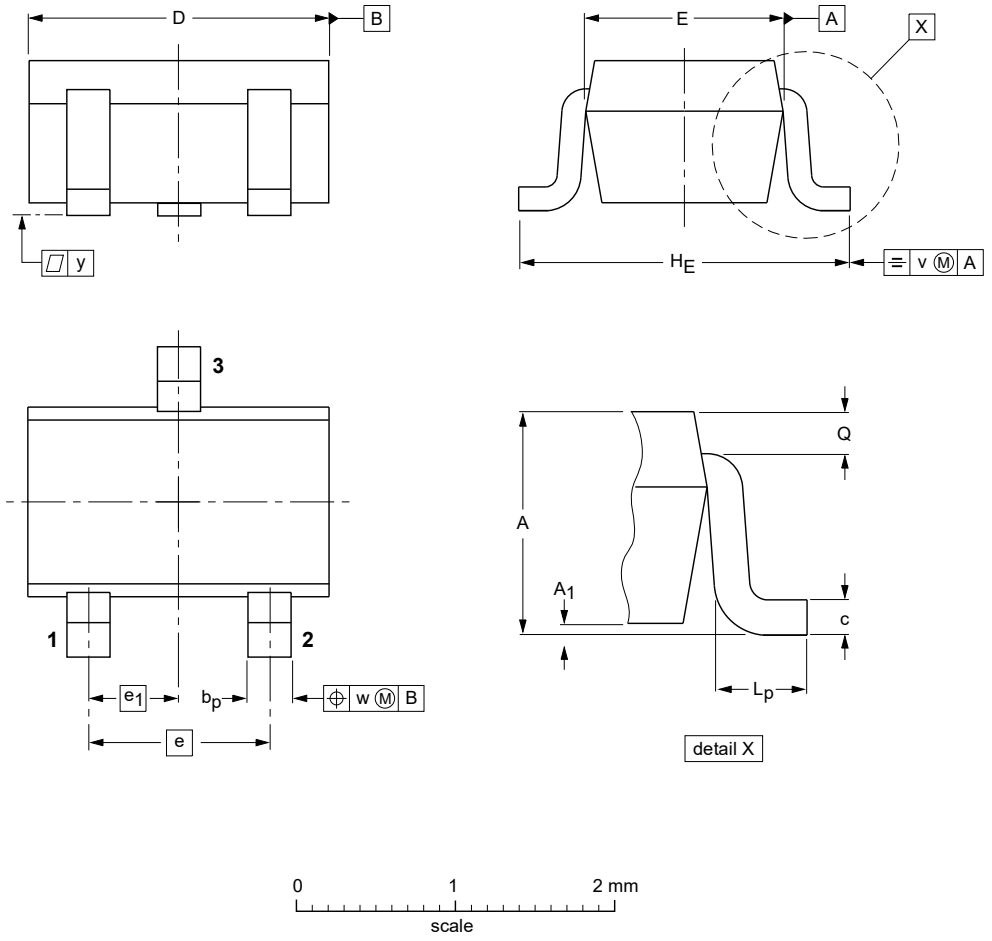


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig. 14. Source current as a function of source-drain voltage; typical values

11. Package outline

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

Fig. 15. Package outline SC-70 (SOT323)

12. Soldering

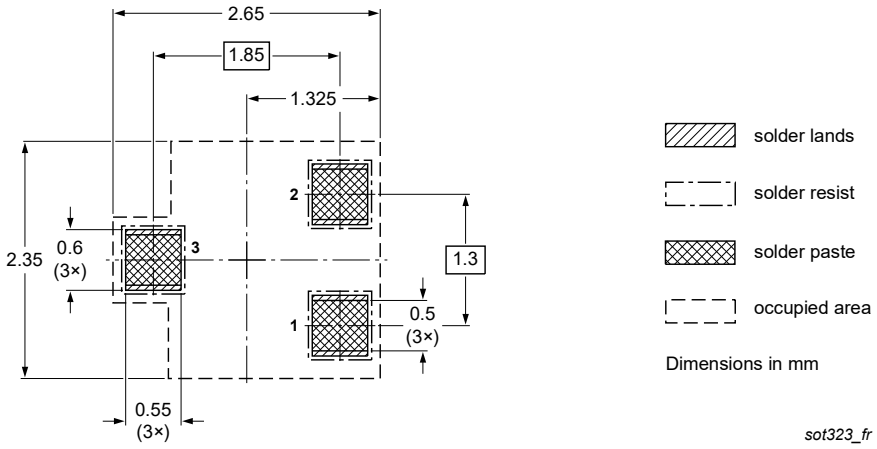


Fig. 16. Reflow soldering footprint for SC-70 (SOT323)

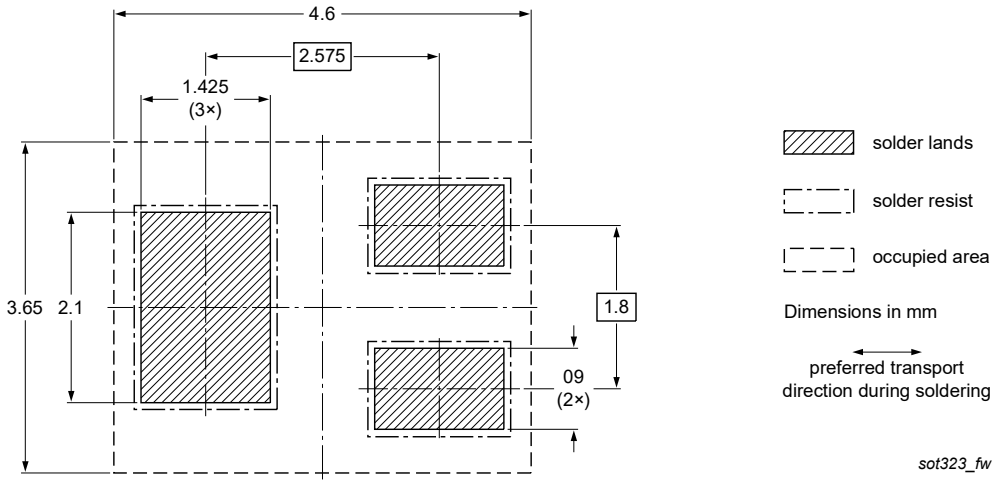


Fig. 17. Wave soldering footprint for SC-70 (SOT323)

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMF370XN v.4	20190705	Product data sheet	-	PMF370XN v.3
Modifications:	• Measurement conditions for $V_{(BR)DSS}$ revised. • Legal texts have been adapted to the new company name where appropriate. • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.			
PMF370XN v.3	20080620	Product data sheet	-	PMF370XN v.2
PMF370XN v.2	20051206	Product data sheet	-	PMF370XN v.1
PMF370XN v.1	20040211	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 5 July 2019

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