



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8K Microwire Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	PE Pin	Word Size	Temp Ranges	Packages
93AA76A	1.8-5.5	No	No	8-bit	I	P, SN, ST, MS, OT
93AA76B	1.8-5.5	No	No	16-bit	I	P, SN, ST, MS, OT
93LC76A	2.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93LC76B	2.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93C76A	4.5-5.5	No	No	8-bit	I, E	P, SN, ST, MS, OT
93C76B	4.5-5.5	No	No	16-bit	I, E	P, SN, ST, MS, OT
93AA76C	1.8-5.5	Yes	Yes	8- or 16-bit	I	P, SN, ST, MS, MC, MN
93LC76C	2.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN
93C76C	4.5-5.5	Yes	Yes	8- or 16-bit	I, E	P, SN, ST, MS, MC, MN

Features:

- Low-Power CMOS Technology
- ORG Pin to Select Word Size for '76C' Version
- 1024 x 8-bit Organization 'A' Devices (no ORG)
- 512 x 16-bit Organization 'B' Devices (no ORG)
- Program Enable Pin to Write-Protect the Entire Array ('76C' version only)
- Self-Timed Erase/Write Cycles (including Auto-Erase)
- Automatic ERAL Before WRAL
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/Busy)
- Sequential Read Function
- 1,000,000 Erase/Write Cycles
- Data Retention > 200 Years
- Pb-free and RoHS Compliant
- Temperature Ranges Supported:
 - Industrial (I) -40°C to +85°C
 - Automotive (E) -40°C to +125°C

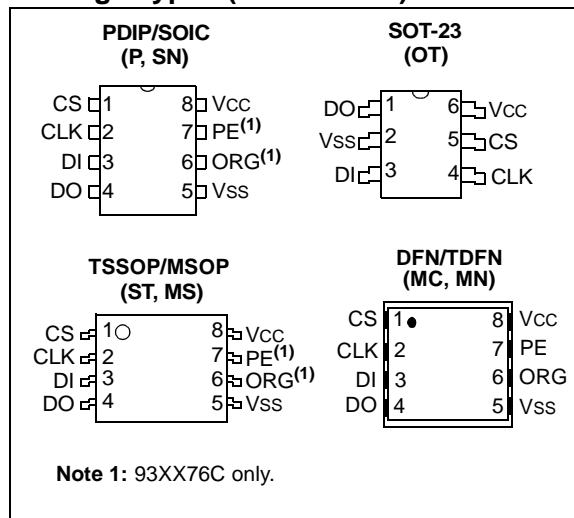
Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable – 93XX76C only
ORG	Memory Configuration – 93XX76C only
Vcc	Power Supply

Description:

The Microchip Technology Inc. 93XX76A/B/C devices are 8Kbit, low-voltage, serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93XX76C are dependent upon external logic levels driving the ORG pin to set word size. The 93XX76A devices provide dedicated 8-bit memory organization, while the 93XX76B devices provide dedicated 16-bit memory organization. A Program Enable (PE) pin allows the user to write-protect the entire memory array. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The 93XX Series is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, 6-lead SOT-23, 8-lead 2x3 DFN/TDFN and 8-lead TSSOP. All packages are Pb-free (Matte Tin) finish.

Package Types (not to scale)



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V _{CC}	7.0V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): T _A = -40°C to +85°C, V _{CC} = +1.8V to 5.5V Automotive (E): T _A = -40°C to +125°C, V _{CC} = +2.5V to 5.5V				
Param. No.	Symbol	Parameter	Min	Typ	Max	Units	Conditions
D1	V _{IH1}	High-level input voltage	2.0	—	V _{CC} +1	V	V _{CC} ≥ 2.7V
	V _{IH2}		0.7 V _{CC}	—	V _{CC} +1	V	V _{CC} < 2.7V
D2	V _{IL1}	Low-level input voltage	-0.3	—	0.8	V	V _{CC} ≥ 2.7V
	V _{IL2}		-0.3	—	0.2 V _{CC}	V	V _{CC} < 2.7V
D3	V _{OL1}	Low-level output voltage	—	—	0.4	V	I _{OL} = 2.1 mA, V _{CC} = 4.5V
	V _{OL2}		—	—	0.2	V	I _{OL} = 100 μA, V _{CC} = 2.5V
D4	V _{OH1}	High-level output voltage	2.4	—	—	V	I _{OH} = -400 μA, V _{CC} = 4.5V
	V _{OH2}		V _{CC} - 0.2	—	—	V	I _{OH} = -100 μA, V _{CC} = 2.5V
D5	I _{LI}	Input leakage current	—	—	±1	μA	V _{IN} = V _{SS} or V _{CC}
D6	I _{LO}	Output leakage current	—	—	±1	μA	V _{OUT} = V _{SS} or V _{CC}
D7	C _{IN} , C _{OUT}	Pin capacitance (all inputs/ outputs)	—	—	7	pF	V _{IN} /V _{OUT} = 0V (Note 1) T _A = 25°C, F _{CLK} = 1 MHz
D8	I _{CC} write	Write current	—	—	3	mA	F _{CLK} = 3 MHz, V _{CC} = 5.5V
			—	500	—	μA	F _{CLK} = 2 MHz, V _{CC} = 2.5V
D9	I _{CC} read	Read current	—	—	1	mA	F _{CLK} = 3 MHz, V _{CC} = 5.5V
			—	—	500	μA	F _{CLK} = 2 MHz, V _{CC} = 3.0V
			—	100	—	μA	F _{CLK} = 2 MHz, V _{CC} = 2.5V
D10	I _{CCS}	Standby current	—	—	1	μA	I – Temp
			—	—	5	μA	E – Temp CLK = CS = 0V ORG = DI = PE = V _{SS} or V _{CC} (Note 2) (Note 3)
D11	V _{POR}	V _{CC} voltage detect	—	1.5	—	V	(Note 1) 93AA76A/B/C, 93LC76A/B/C 93C76A/B/C
			—	3.8	—	V	

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG and PE pins not available on ‘A’ or ‘B’ versions.

3: Ready/Busy status must be cleared from DO; see [Section 3.4 “Data Out \(DO\)”](#).

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

TABLE 1-2: AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			Industrial (I): TA = -40°C to +85°C, VCC = +1.8V to 5.5V Automotive (E): TA = -40°C to +125°C, VCC = +2.5V to 5.5V			
Param. No.	Symbol	Parameter	Min	Max	Units	Conditions
A1	FCLK	Clock frequency	—	3	MHz	4.5V ≤ VCC < 5.5V
				2	MHz	2.5V ≤ VCC < 4.5V
				1	MHz	1.8V ≤ VCC < 2.5V
A2	TCKH	Clock high time	200	—	ns	4.5V ≤ VCC < 5.5V
			250		ns	2.5V ≤ VCC < 4.5V
			450		ns	1.8V ≤ VCC < 2.5V
A3	TCKL	Clock low time	100	—	ns	4.5V ≤ VCC < 5.5V
			200		ns	2.5V ≤ VCC < 4.5V
			450		ns	1.8V ≤ VCC < 2.5V
A4	TCSS	Chip Select setup time	50	—	ns	4.5V ≤ VCC < 5.5V
			100		ns	2.5V ≤ VCC < 4.5V
			250		ns	1.8V ≤ VCC < 2.5V
A5	TCSH	Chip Select hold time	0	—	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip Select low time	250	—	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data input setup time	50	—	ns	4.5V ≤ VCC < 5.5V
			100		ns	2.5V ≤ VCC < 4.5V
			250		ns	1.8V ≤ VCC < 2.5V
A8	TDIH	Data input hold time	50	—	ns	4.5V ≤ VCC < 5.5V
			100		ns	2.5V ≤ VCC < 4.5V
			250		ns	1.8V ≤ VCC < 2.5V
A9	TPD	Data output delay time	—	100	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
				250	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
				400	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	TCZ	Data output disable time	—	100	ns	4.5V ≤ VCC < 5.5V, (Note 1)
				200	ns	1.8V ≤ VCC < 4.5V, (Note 1)
A11	Tsv	Status valid time	—	200	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
				300	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
				500	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF
A12	TWC	Program cycle time	—	5	ms	Erase/Write mode (AA and LC versions)
A13	TWC			2	ms	Erase/Write mode (93C versions)
A14	TEC			6	ms	ERAL mode, 4.5V ≤ VCC ≤ 5.5V
A15	TWL			15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16	—			Endurance	1M	—

Note 1: This parameter is periodically sampled and not 100% tested.

- 2:** This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which may be obtained from Microchip's web site at www.microchip.com.

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

FIGURE 1-1: SYNCHRONOUS DATA TIMING

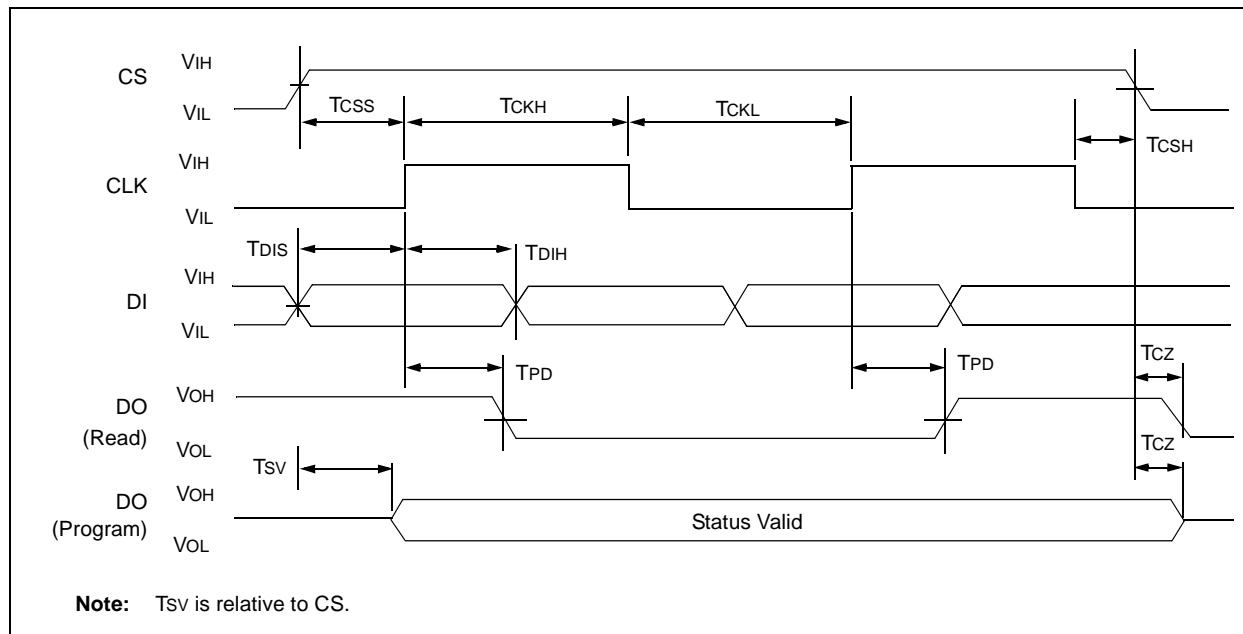


TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX76B OR 93XX76C WITH ORG = 1)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15-D0	29
EWEN	1	00	1 1 x x x x x x x x	—	High-Z	13
ERASE	1	11	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/ $\overline{\text{BSY}}$)	13
ERAL	1	00	1 0 x x x x x x x x	—	(RDY/ $\overline{\text{BSY}}$)	13
WRITE	1	01	X A8 A7 A6 A5 A4 A3 A2 A1 A0	D15-D0	(RDY/ $\overline{\text{BSY}}$)	29
WRAL	1	00	0 1 x x x x x x x x	D15-D0	(RDY/ $\overline{\text{BSY}}$)	29
EWDS	1	00	0 0 x x x x x x x x	—	High-Z	13

TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX76A OR 93XX76C WITH ORG = 0)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7-D0	22
EWEN	1	00	1 1 x x x x x x x x	—	High-Z	14
ERASE	1	11	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/ $\overline{\text{BSY}}$)	14
ERAL	1	00	1 0 x x x x x x x x	—	(RDY/ $\overline{\text{BSY}}$)	14
WRITE	1	01	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7-D0	(RDY/ $\overline{\text{BSY}}$)	22
WRAL	1	00	0 1 x x x x x x x x	D7-D0	(RDY/ $\overline{\text{BSY}}$)	22
EWDS	1	00	0 0 x x x x x x x x	—	High-Z	14

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX76C) is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note: When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation if A0 is a logic high-level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of the driver, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for '93AA' and '93LC' devices or 3.8V for '93C' devices.

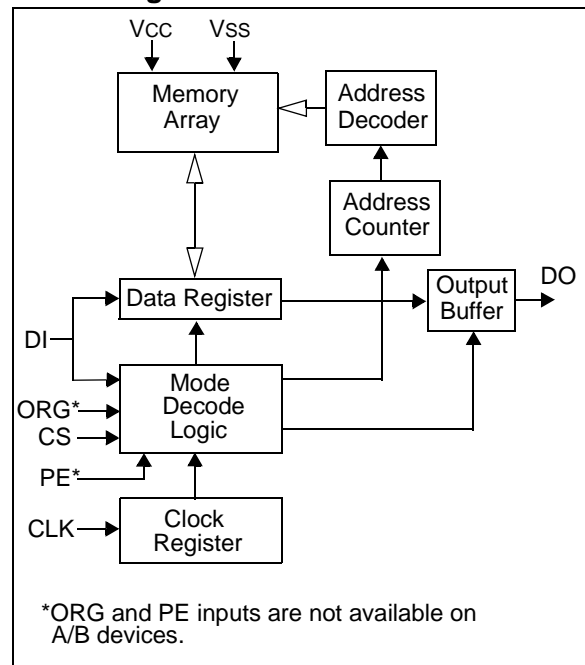
The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Note: To prevent accidental writes to the array in the 93XX76C devices, set the PE pin to a logic low.

Block Diagram



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

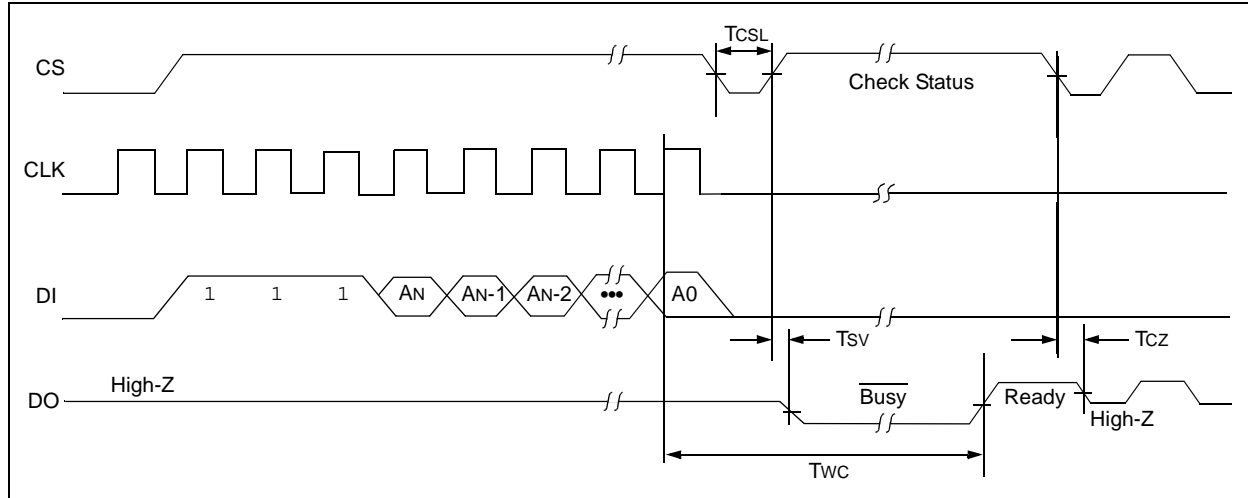
2.4 Erase

The ERASE instruction forces all data bits of the specified address to the logical '1' state. The rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/ $\overline{\text{Busy}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-1: ERASE TIMING



2.5 Erase All (ERAL)

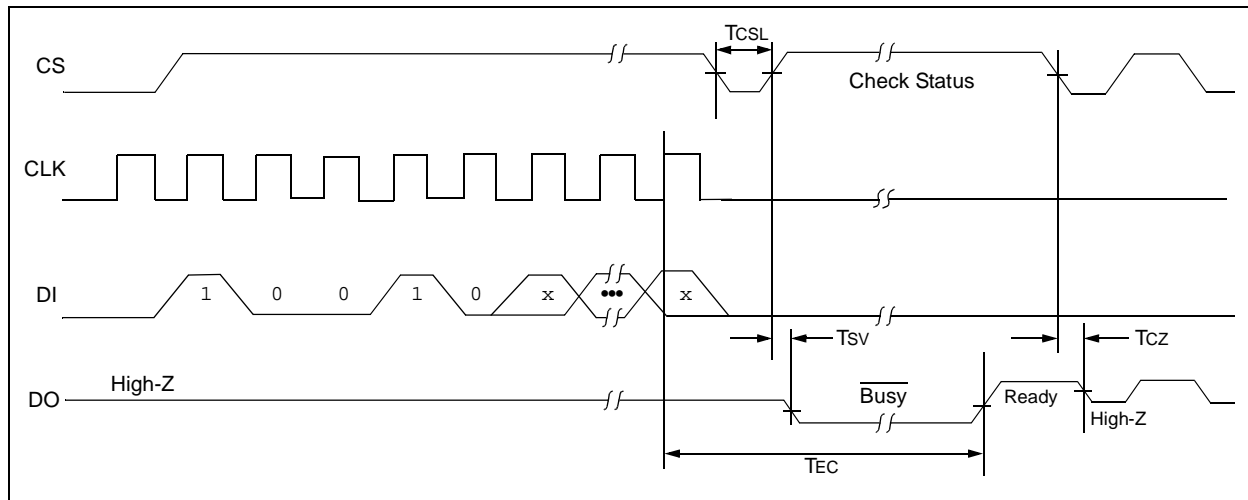
The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed. The rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/ $\overline{\text{Busy}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}).

Note: After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

VCC must be $\geq 4.5\text{V}$ for proper operation of ERAL.

FIGURE 2-2: ERAL TIMING



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX76A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction.

Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING



FIGURE 2-4: EWEN TIMING



2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-version devices) or 16-bit (If ORG pin is high or B-version devices) output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-5: READ TIMING



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

2.8 Write

The WRITE instruction is followed by 8 bits (if ORG is low or A-version devices) or 16 bits (if ORG pin is high or B-version devices) of data which are written into the specified address. The self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/Busy status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note: After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-6: WRITE TIMING



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

2.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command includes an automatic ERAL cycle for the device, so the WRAL instruction does not require an ERAL instruction. However, the chip must be in the EWEN status.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

Note: The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note: After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

VCC must be $\geq 4.5V$ for proper operation of WRAL.

FIGURE 2-7: WRAL TIMING



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	PDIP	SOIC	TSSOP	MSOP	DFN ⁽¹⁾	TDFN ⁽¹⁾	SOT-23	Function
CS	1	1	1	1	1	1	5	Chip Select
CLK	2	2	2	2	2	2	4	Serial Clock
DI	3	3	3	3	3	3	3	Data In
DO	4	4	4	4	4	4	1	Data Out
Vss	5	5	5	5	5	5	2	Ground
ORG	6	6	6	6	6	6	—	Organization/93XX76C only
PE	7	7	7	7	7	7	—	Program Enable/93XX76C only
Vcc	8	8	8	8	8	8	6	Power Supply

Note 1: The exposed pad on the DFN/TDFN package may be connected to Vss or left floating.

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle that is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low-level) and can be continued anytime with respect to Clock High Time (T_{CKH}) and Clock Low Time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don’t care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively, low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and

data bits before an instruction is executed. CLK and DI then become “don’t care” inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum Chip Select Low Time (T_{CSL}) and an erase or write operation has been initiated.

The Status signal is not available on DO, if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

Note: After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

3.5 Organization (ORG)

When the ORG pin is connected to Vcc or logic high, the (x16) memory organization is selected. When the ORG pin is tied to Vss or logic low, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX76A devices are always (x8) organization and 93XX76B devices are always (x16) organization.

3.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is tied to Vcc, the device can be programmed. If the PE pin is tied to Vss, programming will be inhibited. This pin cannot be floated – it must be tied to Vcc or Vss. PE is not available on 93XX76A or 93XX76B. On those devices, programming is always enabled.

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

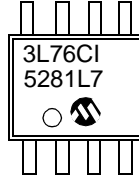
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead MSOP (150 mil)



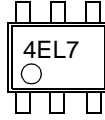
Example:



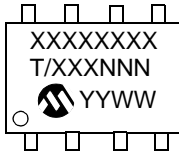
6-Lead SOT-23



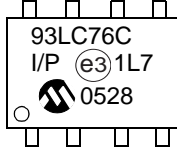
Example:



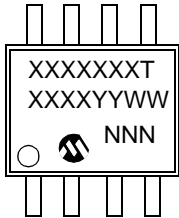
8-Lead PDIP



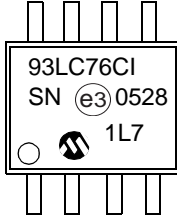
Example:



8-Lead SOIC



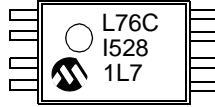
Example:



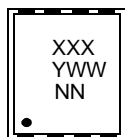
8-Lead TSSOP



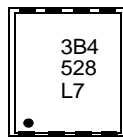
Example:



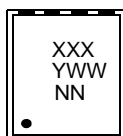
8-Lead 2x3 DFN



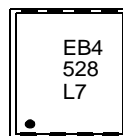
Example:



8-Lead 2x3 TDFN



Example:



93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

Part Number	1st Line Marking Codes							
	TSSOP	MSOP	SOT-23		DFN		TDFN	
			I Temp.	E Temp.	I Temp.	E Temp.	I Temp.	E Temp.
93AA76A	A76A	3A76AT	4BNN	—	—	—	—	—
93AA76B	A76B	3A76BT	4LNN	—	—	—	—	—
93AA76C	A76C	3A76CT	—	—	3B1	—	EB1	—
93LC76A	L76A	3L76AT	4ENN	4FNN	—	—	—	—
93LC76B	L76B	3L76BT	4PNN	4RNN	—	—	—	—
93LC76C	L76C	3L76CT	—	—	3B4	3B5	EB4	EB5
93C76A	C76A	3C76AT	4HNN	4JNN	—	—	—	—
93C76B	C76B	3C76BT	4TNN	4UNN	—	—	—	—
93C76C	C76C	3C76CT	—	—	3B7	3B8	EB7	EB8

Note: T = Temperature grade (I, E)
 NN = Alphanumeric traceability code

Legend: XX...X Part number or part number code
 T Temperature (I, E)
 Y Year code (last digit of calendar year)
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code (2 characters for small packages)
 ⓔ Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator ⓔ, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

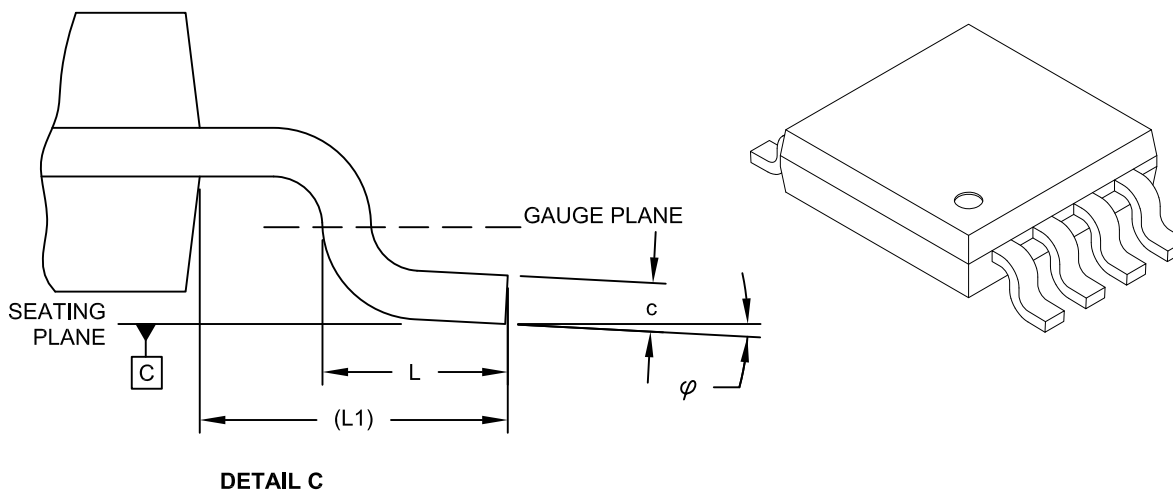
93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

NOTES:

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

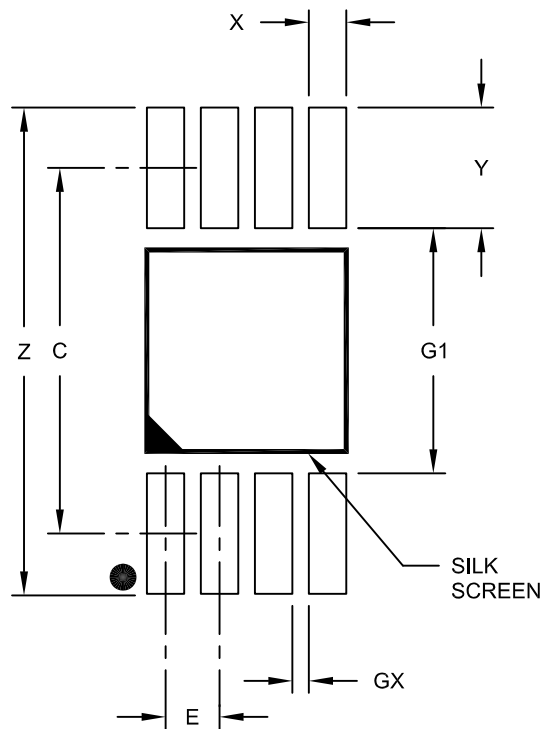
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

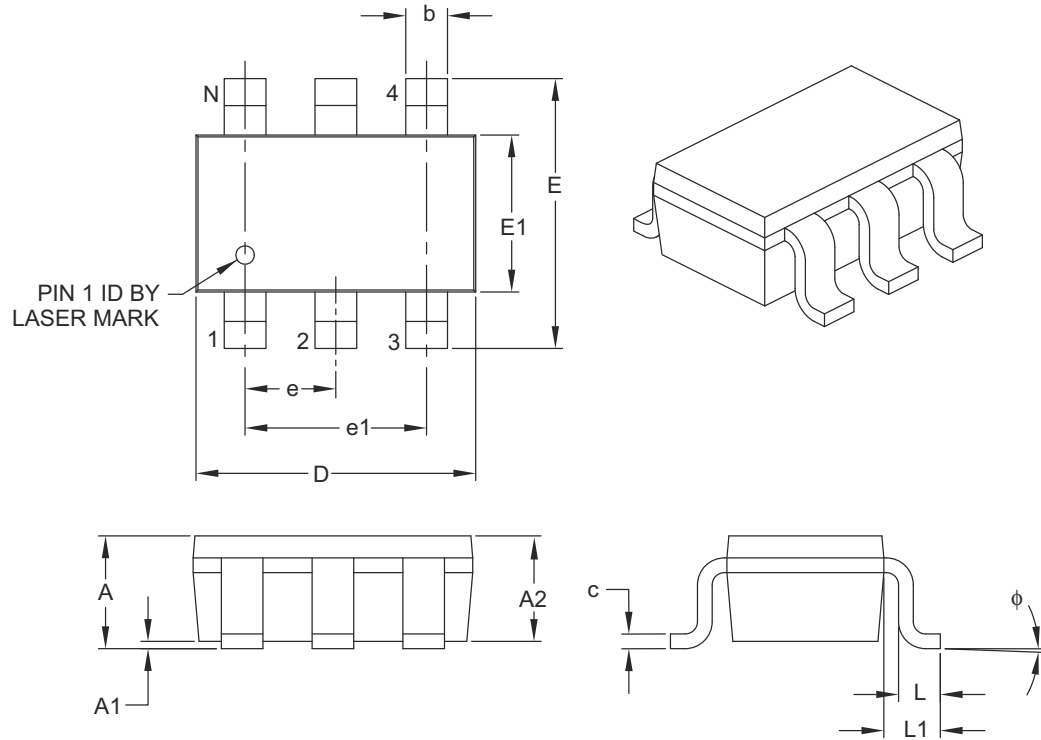
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	φ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

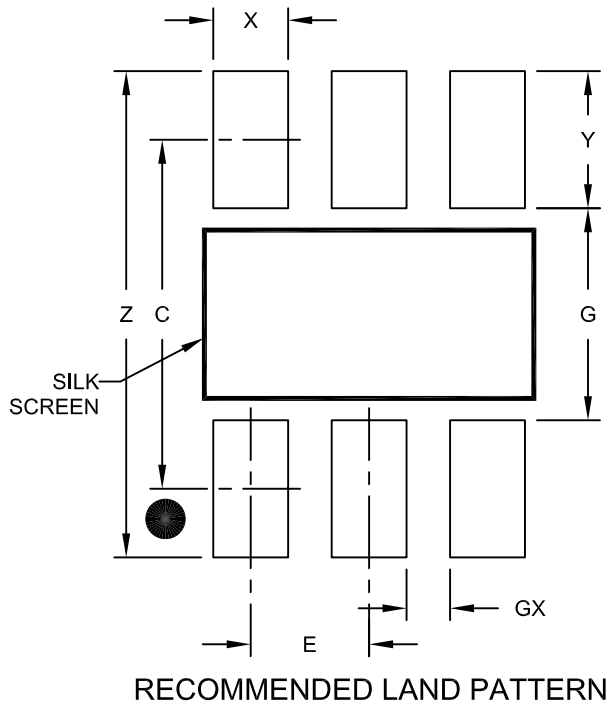
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

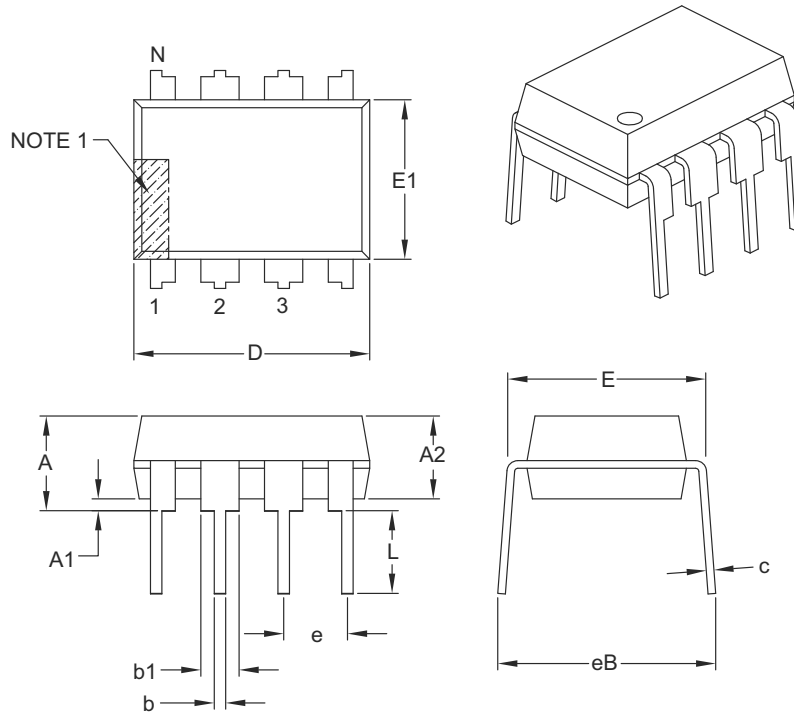
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

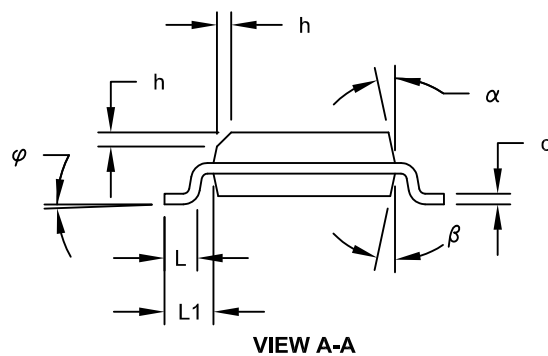
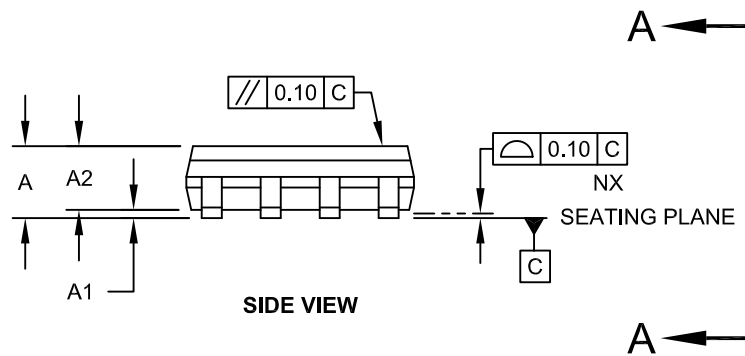
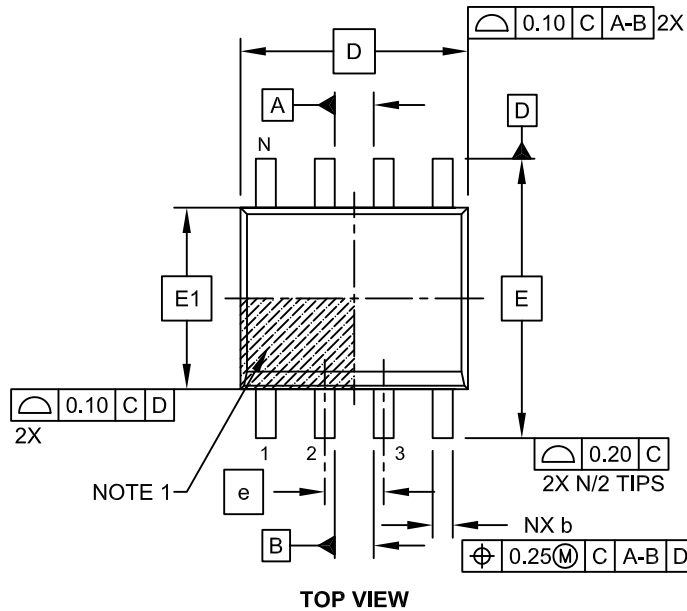
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

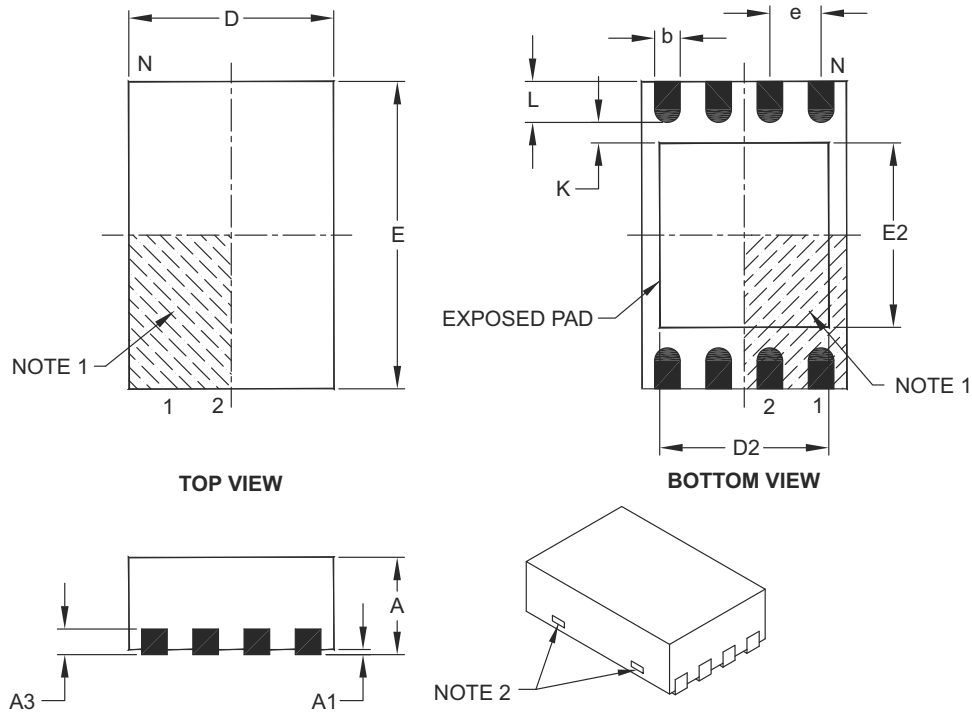
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

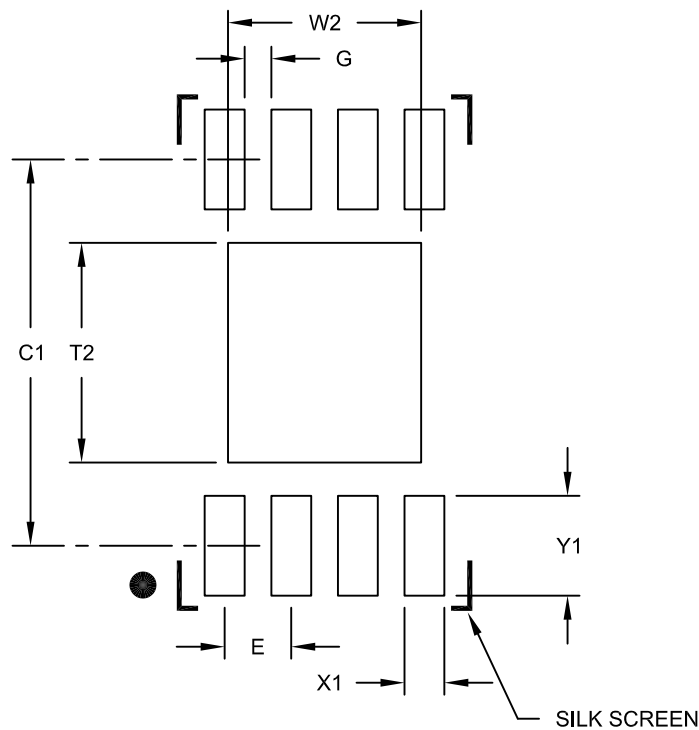
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

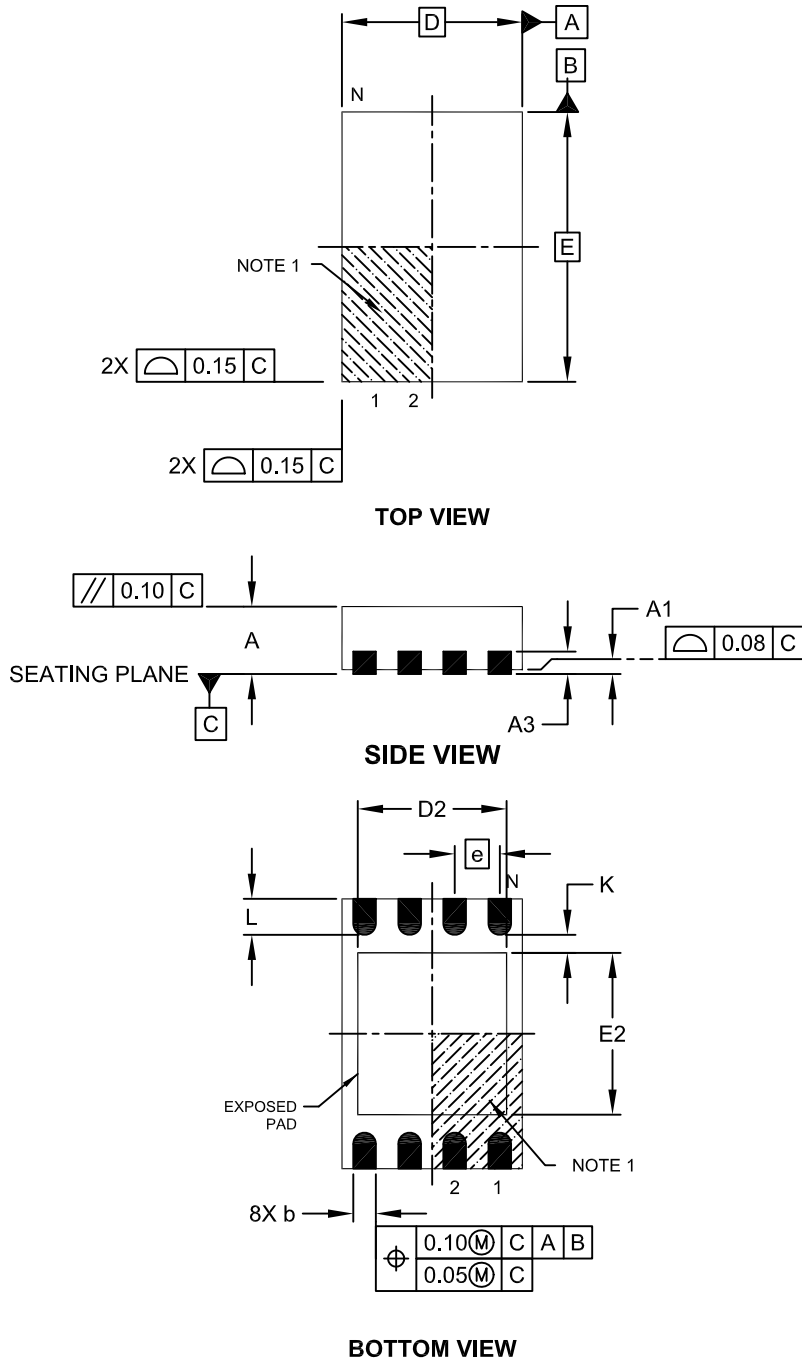
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-129C Sheet 1 of 2

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		0.50 BSC		
Overall Height	A		0.70	0.75	0.80
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Length	D		2.00 BSC		
Overall Width	E		3.00 BSC		
Exposed Pad Length	D2		1.20	-	1.60
Exposed Pad Width	E2		1.20	-	1.60
Contact Width	b		0.20	0.25	0.30
Contact Length	L		0.25	0.30	0.45
Contact-to-Exposed Pad	K		0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		0.50 BSC		
Optional Center Pad Width	W2				1.46
Optional Center Pad Length	T2				1.36
Contact Pad Spacing	C1			3.00	
Contact Pad Width (X8)	X1				0.30
Contact Pad Length (X8)	Y1				0.75
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

APPENDIX A: REVISION HISTORY

Revision A (05/2003)

Initial Release.

Revision B (07/2003)

Revision C (12/2003)

Corrections to Section 1.0, Electrical Characteristics. Section 4.1, 6-Lead SOT-23 package to OT.

Revision D (02/2004)

Corrections to Device Selection Table, Table 1-1, Table 1-2, Section 2.4, Section 2.5, Section 2.8 and Section 2.9. Added note to Figure 2-7.

Revision E (03/2005)

Added DFN package.

Revision F (04/2005)

Added notes throughout.

Revision G (09/2006)

Revised note in Sections 2.8 and 2.9. Replaced DFN package drawing.

Revision H (11/2006)

Updated Package Drawings.

Revision J (10/2007)

Revised Device Selection Table; Revised Pin Function Table; Revised Package Types; Revised Table 3-1; Replaced Package Drawings; Revised Product ID System.

Revision K (5/2008)

Revised Figures 2-1, 2-2, 2-6 and 2-7; Revised Package Marking Information; Replaced Package Drawings.

Revision L (01/2012)

Added TDFN package.

Revision M (04/2012)

Revised Device Selection Table; Added Note to Package Types Diagram; Revised Marking Codes Table; Revised Product ID System.

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93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

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Literature Number: DS21796M

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6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

PRODUCT IDENTIFICATION SYSTEM

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<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>/XX</u>
Device	Tape & Reel	Temperature Range	Package
Device:			
93AA76A:		8K 1.8V Microwire Serial EEPROM (x8)	
93AA76B:		8K 1.8V Microwire Serial EEPROM (x16)	
93AA76C:		8K 1.8V Microwire Serial EEPROM w/ORG	
93LC76A:		8K 2.5V Microwire Serial EEPROM (x8)	
93LC76B:		8K 2.5V Microwire Serial EEPROM (x16)	
93LC76C:		8K 2.5V Microwire Serial EEPROM w/ORG	
93C76A:		8K 5.0V Microwire Serial EEPROM (x8)	
93C76B:		8K 5.0V Microwire Serial EEPROM (x16)	
93C76C:		8K 5.0V Microwire Serial EEPROM w/ORG	
Tape & Reel:			
	Blank =	Standard pinout	
	T =	Tape & Reel	
Temperature Range:			
	I =	-40°C to +85°C	
	E =	-40°C to +125°C	
Package:			
	MS =	Plastic MSOP (Micro Small outline), 8-lead	
	OT =	Plastic SOT-23, 6-lead (Tape & Reel only)	
	P =	Plastic DIP (300 mil body), 8-lead	
	SN =	Plastic SOIC (3.90 mm body), 8-lead	
	ST =	Plastic TSSOP (4.4 mm body), 8-lead	
	MC =	Plastic DFN (2x3x0.90 mm body), 8-lead	
	MNY ⁽¹⁾ =	Plastic TDFN (2x3x0.75 mm body), 8-lead (Tape & Reel only)	
Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.			

Examples:

- a) 93AA76C-I/P: 8K, 1024x8 or 512x16 Serial EEPROM, PDIP package, 1.8V
- b) 93AA76AT-I/OT: 8K, 1024x8 Serial EEPROM, SOT-23 package, tape and reel, 1.8V
- c) 93AA76CT-I/MS: 8K, 1024x8 or 512x16 Serial EEPROM, MSOP package, tape and reel, 1.8V
- a) 93LC76C-I/ST: 8K, 1024x8 or 512x16 Serial EEPROM, TSSOP package, 2.5V
- b) 93LC76BT-I/OT: 8K, 512x16 Serial EEPROM, SOT-23 package, tape and reel, 2.5V
- c) 93LC76CT-E/MNY: 8K, 1024x8 or 512x16 Serial EEPROM, Automotive Temp, TDFN package, tape and reel
- a) 93C76C-I/MS: 8K, 1024x8 or 512x16 Serial EEPROM, MSOP package, 5.0V
- b) 93C76AT-I/OT: 8K, 1024x8 Serial EEPROM, SOT-23 package, tape and reel, 5.0V

93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

NOTES:

Note the following details of the code protection feature on Microchip devices:

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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