Complete 14-Bit CCD/CIS Signal Processor

AD9822

FEATURES

14-bit 15 MSPS ADC
No missing codes guaranteed
3-channel operation up to 15 MSPS
1-channel operation up to 12.5 MSPS
Correlated double sampling
1–6× programmable gain
±350 mV programmable offset
Input clamp circuitry
Internal voltage reference
Multiplexed byte-wide output (8 + 6 format)
3-wire serial digital interface
3 V/5 V digital I/O compatibility
28-Lead SOIC or SSOP
Low power CMOS: 385 mW (typ)
Power-down mode: <1 mW

APPLICATIONS

Flatbed document scanners
Film scanners
Digital color copiers
Multifunction peripherals

GENERAL DESCRIPTION

The AD9822 is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of trilinear color CCD arrays. Each channel consists of an input clamp, correlated double sampler (CDS), offset DAC, and programmable gain amplifier (PGA) multiplexed to a high performance 14-bit ADC.

The CDS amplifiers may be disabled for use with sensors such as contact image sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 14-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface and provide adjustment of the gain, offset, and operating mode.

The AD9822 operates from a single 5 V power supply, consumes 385 mW of power typically, and is packaged in a 28-lead SOIC or SSOP.

FUNCTIONAL BLOCK DIAGRAM

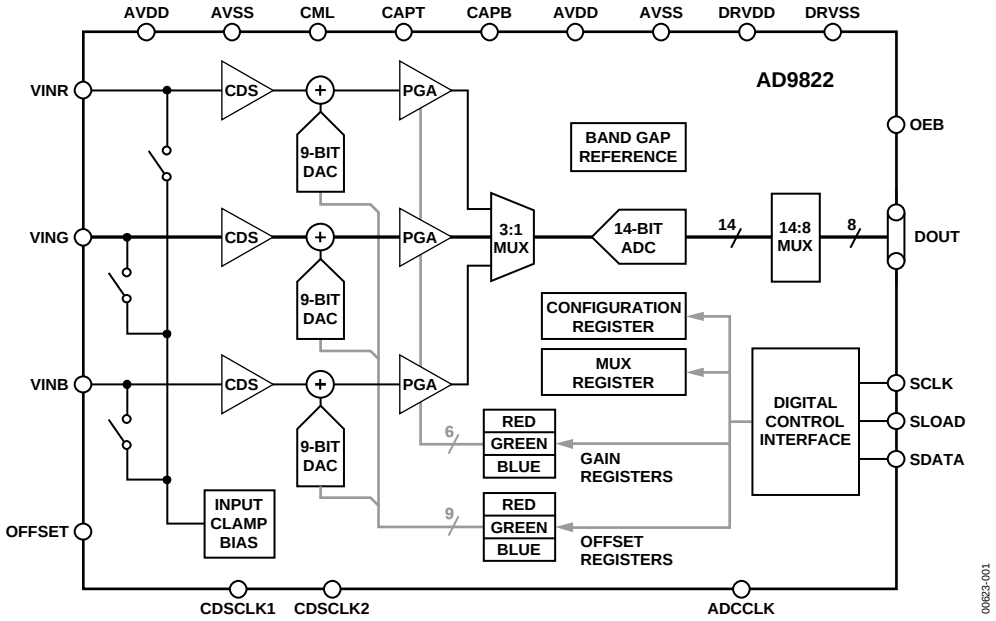

Figure 1.

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703 **© 2005 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

2/05—Rev. A to Rev. B

Changes to Format ... Universal
Changes to Ordering Guide ... 18
Updated Outline Dimensions ... 18

12/99—Rev. 0 to Rev. A

SPECIFICATIONS

ANALOG SPECIFICATIONS

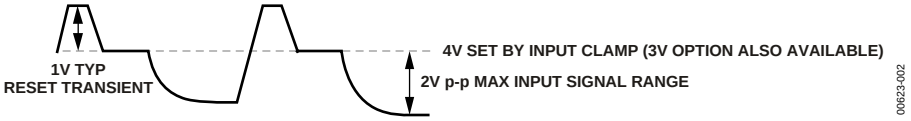
T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS mode, f_{ADCCLK} = 15 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 5 MHz, PGA gain = 1, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
MAXIMUM CONVERSION RATE				
3-Channel Mode with CDS	15			MSPS
1-Channel Mode with CDS	12.5			MSPS
ACCURACY (ENTIRE SIGNAL PATH)				
ADC Resolution		14		Bits
Integral Nonlinearity (INL)		−17.0/+3.5		LSB
INL @ 6 MHz		−10.5/+1.5		LSB
Differential Nonlinearity (DNL)		−0.65/+0.75		LSB
DNL @ 6 MHz	−1.0	−0.6/+0.65	+1.1	LSB
No Missing Codes		14		Bits
No Missing Codes @ 6 MHz	14			Bits
Offset Error	−240	−19	+200	mV
Gain Error	−1.4	+3.5	+6.9	% FSR
ANALOG INPUTS				
Input Signal Range[1]		2.0		V p-p
Allowable Reset Transient[1]		1.0		V
Input Limits[2]	AVSS − 0.3		AVDD + 0.3	V
Input Capacitance		10		pF
Input Bias Current		10		nA
AMPLIFIERS				
PGA Gain at Minimum		1		V/V
PGA Gain at Maximum		5.7		V/V
PGA Gain Resolution[2]		64		Steps
PGA Gain Monotonicity		Guaranteed		
Programmable Offset at Minimum		−350		mV
Programmable Offset at Maximum		+350		mV
Programmable Offset Resolution		512		Steps
Programmable Offset Monotonicity		Guaranteed		
NOISE AND CROSSTALK				
Total Output Noise @ PGA Minimum		1.5		LSB rms
Total Output Noise @ PGA Maximum		6.0		LSB rms
Channel-to-Channel Crosstalk @ 6 MHz		<1		LSB
POWER SUPPLY REJECTION				
AVDD = 5 V ± 0.25 V		0.063	0.9	% FSR
DIFFERENTIAL VREF (@ 25°C)				
CAPT to CAPB (2 V ADC Full-Scale Range)	0.94	1.0	1.06	V
TEMPERATURE RANGE				
Operating	0		+70	°C
Storage	−65		+150	°C
POWER SUPPLIES				
AVDD	4.75	5.0	5.25	V
DRVDD	3.0	5.0	5.25	V
OPERATING CURRENT				
AVDD		73		mA
DRVDD		4		mA
Power-Down Mode Current		150		µA

Parameter	Min	Typ	Max	Unit
POWER DISSIPATION				
3-Channel Mode		385	450	mW
3-Channel Mode @ 6 MHz		335	410	mW
1-Channel Mode		300		mW
1-Channel Mode @ 6 MHz		250		mW

[1] Linear input signal range is from 2 V to 4 V when the CCD's reference level is clamped to 4 V by the AD9822's input clamp.



[2] The PGA gain is approximately linear-in-dB and follows the equation: $Gain = \left[\frac{5.7}{1 + 4.7\left[\frac{63 - G}{63}\right]} \right]$ where *G* is the register value. See Figure 15.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS mode, f_{ADCCLK} = 15 MHz, $f_{CDSCLK1} = f_{CDSCLK2}$ = 5 MHz, C_L = 10 pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.0			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	4.5			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Output Current	I_{OH}		50		µA
Low Level Output Current	I_{OL}		50		µA

TIMING SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK PARAMETERS					
3-Channel Pixel Rate	t_{PRA}	67			ns
1-Channel Pixel Rate	t_{PRB}	80			ns
ADCCLK Pulse Width	t_{ADCLK}	30			ns
CDSCLK1 Pulse Width	t_{C1}	10			ns
CDSCLK2 Pulse Width	t_{C2}	10			ns
CDSCLK1 Falling to CDSCLK2 Rising	t_{C1C2}	0			ns
ADCCLK Falling to CDSCLK2 Rising	t_{ADC2}	0			ns
CDSCLK2 Rising to ADCCLK Rising	t_{C2ADR}	0			ns
CDSCLK2 Falling to ADCCLK Falling	t_{C2ADF}	30	40		ns
CDSCLK2 Falling to CDSCLK1 Rising	t_{C2C1}	30	40		ns
ADCCLK Falling to CDSCLK1 Rising	t_{ADC1}	0			ns
Aperture Delay for CDS Clocks	t_{AD}		2		ns
SERIAL INTERFACE					
Maximum SCLK Frequency	f_{SCLK}	10			MHz
SLOAD to SCLK Setup Time	t_{LS}	10			ns
SCLK to SLOAD Hold Time	t_{LH}	10			ns
SDATA to SCLK Rising Setup Time	t_{DS}	10			ns
SCLK Rising to SDATA Hold Time	t_{DH}	10			ns
SCLK Falling to SDATA Valid	t_{RDV}	10			ns
DATA OUTPUT					
Output Delay	t_{OD}		8		ns
Three-State to Data Valid	t_{DV}		10		ns
Output Enable High to Three-State	t_{HZ}		10		ns
Latency (Pipeline Delay)			3 (Fixed)		Cycles

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Min	Max	Unit
VIN, CAPT, CAPB	AVSS	−0.3	AVDD + 0.3	V
Digital Inputs	AVSS	−0.3	AVDD + 0.3	V
AVDD	AVSS	−0.5	+6.5	V
DRVDD	DRVSS	−0.5	+6.5	V
AVSS	DRVSS	−0.3	+0.3	V
Digital Outputs	DRVSS	−0.3	DRVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

28-Lead 300 Mil SOIC

θ_{JA} = 71.4°C/W

θ_{JC} = 23°C/W

28-Lead 5.3 mm SSOP

θ_{JA} = 109°C/W

θ_{JC} = 39°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

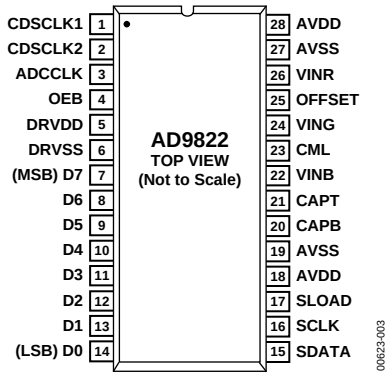


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	CDSCLK1	DI	CDS Reference Level Sampling Clock.
2	CDSCLK2	DI	CDS Data Level Sampling Clock.
3	ADCCLK	DI	ADC Sampling Clock.
4	OEB	DI	Output Enable, Active Low.
5	DRVDD	P	Digital Output Driver Supply.
6	DRVSS	P	Digital Output Driver Ground.
7	D7 (MSB)	DO	Data Output MSB. ADC DB13 High Byte, ADC DB5 Low Byte.
8	D6	DO	Data Output. ADC DB12 High Byte, ADC DB4 Low Byte.
9	D5	DO	Data Output. ADC DB11 High Byte, ADC DB3 Low Byte.
10	D4	DO	Data Output. ADC DB10 High Byte, ADC DB2 Low Byte.
11	D3	DO	Data Output. ADC DB9 High Byte, ADC DB1 Low Byte.
12	D2	DO	Data Output. ADC DB8 High Byte, ADC DB0 Low Byte.
13	D1	DO	Data Output. ADC DB7 High Byte, Don't Care Low Byte.
14	D0 (LSB)	DO	Data Output LSB. ADC DB6 High Byte, Don't Care Low Byte.
15	SDATA	DI/DO	Serial Interface Data Input/Output.
16	SCLK	DI	Serial Interface Clock Input.
17	SLOAD	DI	Serial Interface Load Pulse.
18	AVDD	P	5 V Analog Supply.
19	AVSS	P	Analog Ground.
20	CAPB	AO	ADC Bottom Reference Voltage Decoupling.
21	CAPT	AO	ADC Top Reference Voltage Decoupling.
22	VINB	AI	Analog Input, Blue Channel.
23	CML	AO	Internal Bias Level Decoupling.
24	VING	AI	Analog Input, Green Channel.
25	OFFSET	AO	Clamp Bias Level Decoupling.
26	VINR	AI	Analog Input, Red Channel.
27	AVSS	P	Analog Ground.
28	AVDD	P	5 V Analog Supply.

[1] Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

TERMINOLOGY

Integral Nonlinearity (INL)
Integral nonlinearity error refers to the deviation of each individual code from a line drawn from zero scale through positive full scale. The point used as zero scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1 ½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value; therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

Offset Error
The first ADC code transition should occur at a level ½ LSB above the nominal zero-scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

Gain Error
The last code transition should occur for an analog value 1 ½ LSB below the nominal full-scale voltage. Gain error is the deviation of the actual difference between the first and last code transitions and the ideal difference between the first and last code transitions.

Input Referred Noise
The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB and converted to an equivalent voltage, using the relationship 1 LSB = 4 V/16384 = 244 mV. The noise is then referred to the input of the AD9822 by dividing by the PGA gain.

Channel-to-Channel Crosstalk
In an ideal 3-channel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel crosstalk specification is a measure of the change that occurs in one channel as the other two channels are varied. In the AD9822, one channel is grounded and the other two channels are exercised with full-scale input signals. The change in the output codes from the first channel is measured and compared with the result when all three channels are grounded. The difference is the channel-to-channel crosstalk, stated in LSB.

Aperture Delay
The time delay that occurs from when a sampling edge is applied to the AD9822 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low; therefore, the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

Power Supply Rejection
It specifies the maximum full-scale change that occurs from the initial value when the supplies are varied over the specified limits.

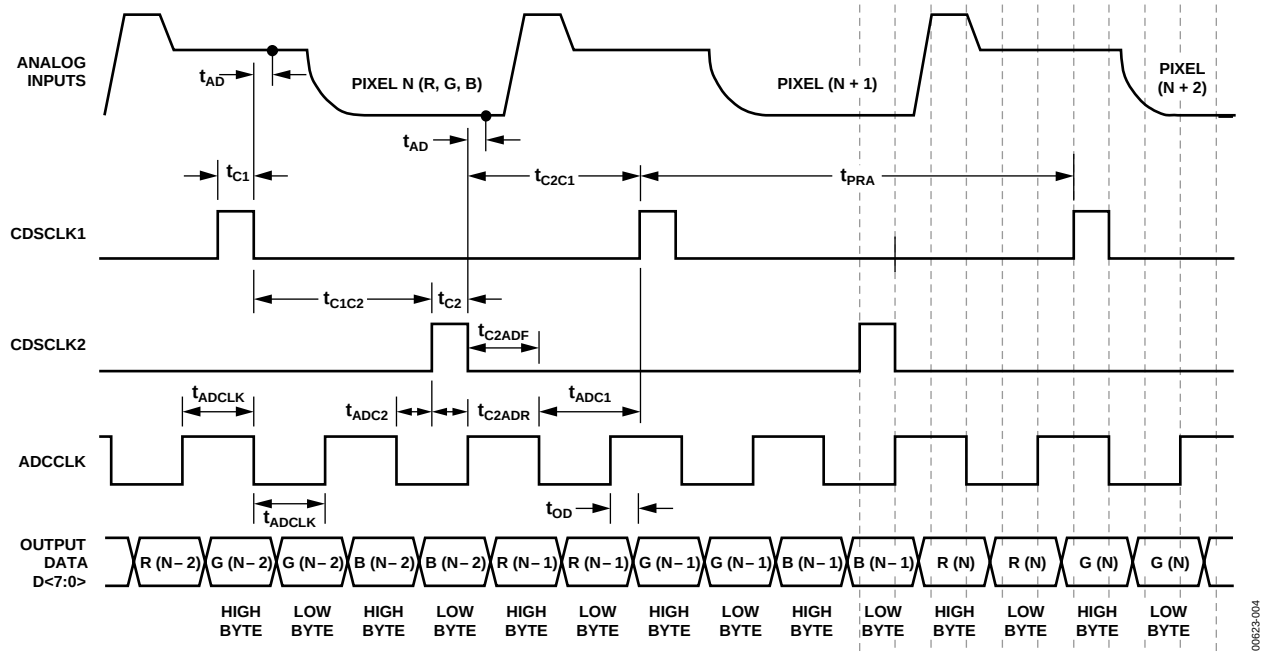


Figure 3. 3-Channel CDS Mode Timing

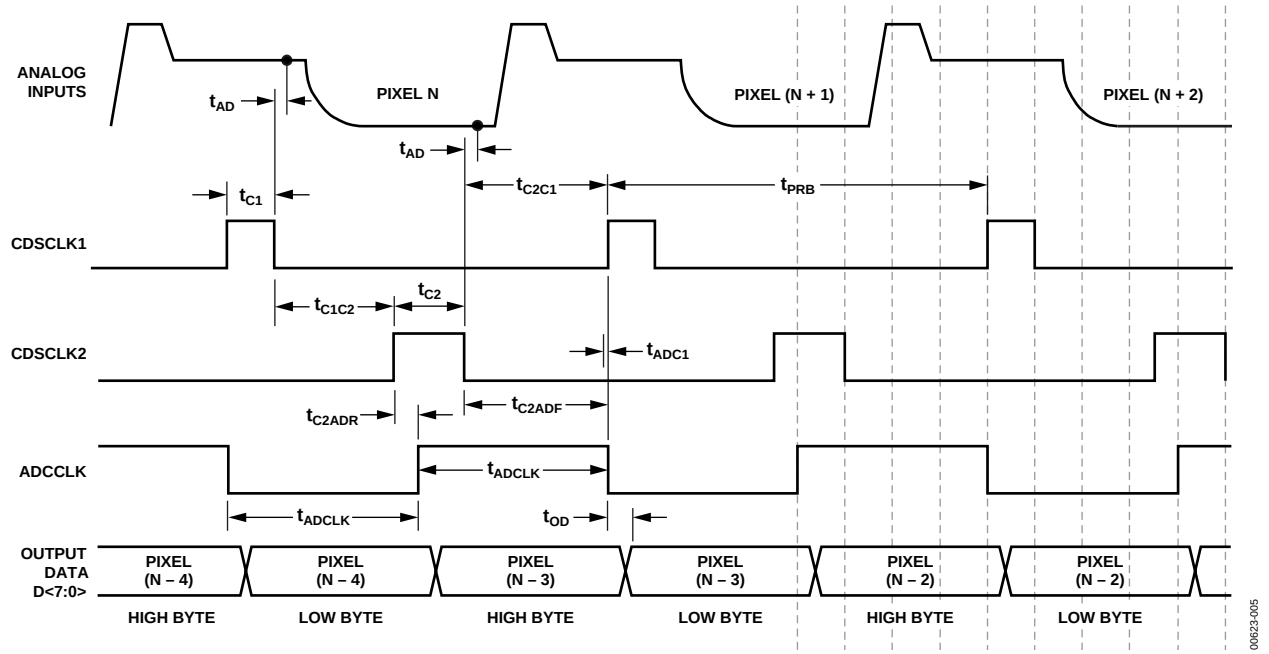


Figure 4. 1-Channel CDS Mode Timing

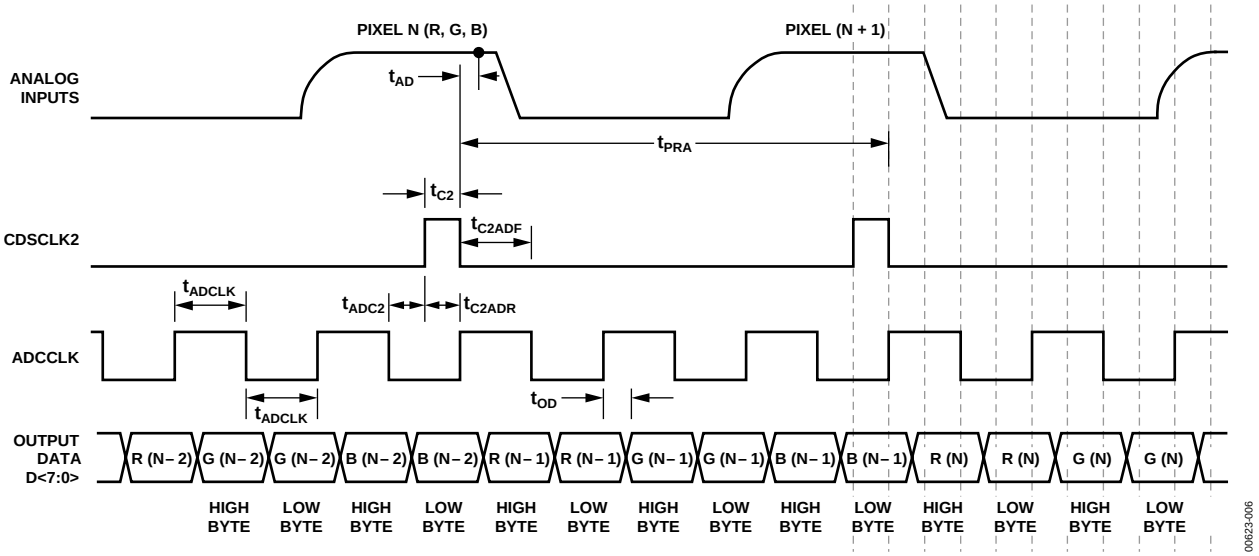


Figure 5. 3-Channel SHA Mode Timing

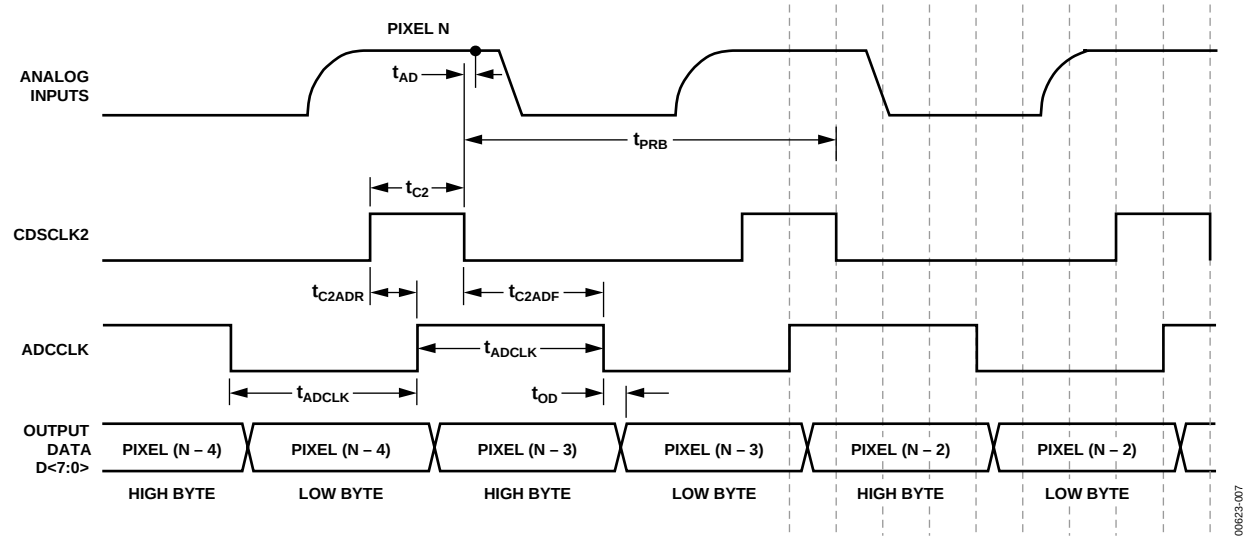


Figure 6. 1-Channel SHA Mode Timing

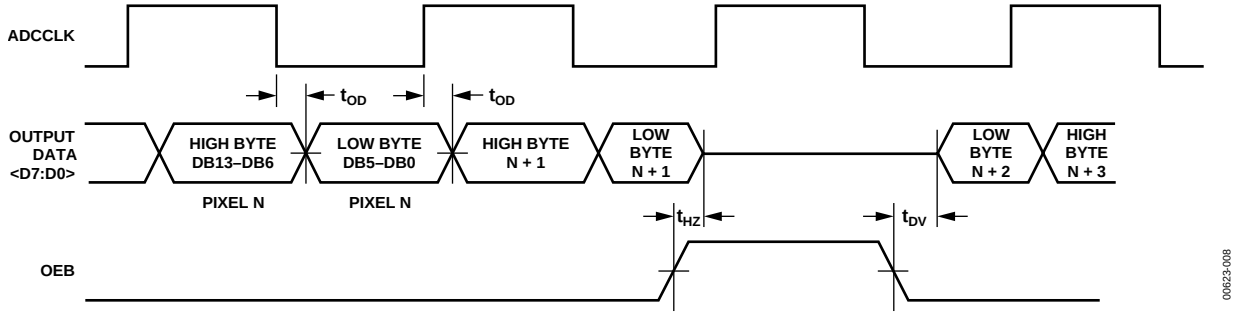


Figure 7. Digital Output Data Timing

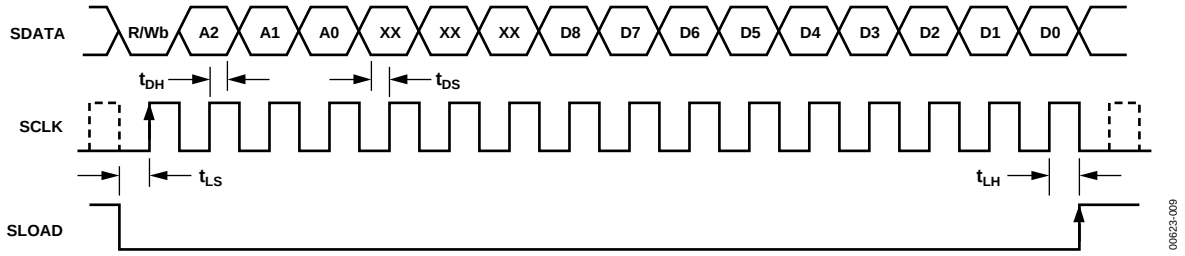


Figure 8. Serial Write Operation Timing

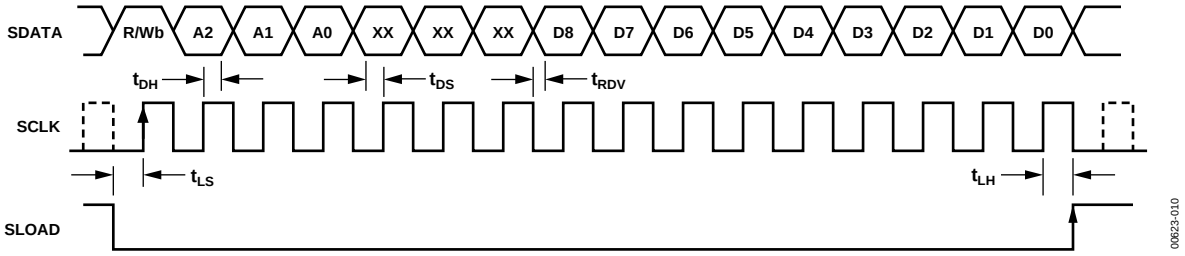


Figure 9. Serial Read Operation Timing

FUNCTIONAL DESCRIPTION

The AD9822 can be operated in four different modes: 3-channel CDS mode, 3-channel SHA mode, 1-channel CDS mode, and 1-channel SHA mode. Each mode is selected by programming the configuration register through the serial interface. For more information on CDS or SHA mode operation, see the Circuit Operation section.

3-CHANNEL CDS MODE

In 3-channel CDS mode, the AD9822 simultaneously samples the red, green, and blue input voltages from the CCD outputs. The sampling points for each CDS are controlled by CDSCLK1 and CDSCLK2 (see Figure 10 and Figure 11). CDSCLK1's falling edge samples the reference level of the CCD waveform, and CDSCLK2's falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD's reference and data levels. The output voltage of each CDS amplifier is then level-shifted by an offset DAC. The voltages are scaled by the three PGAs before being multiplexed through the 14-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The offset and gain values for the red, green, and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register.

Timing for this mode is shown in Figure 3. It is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK. However, this is not required to satisfy the minimum timing constraints. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three clock cycles.

3-CHANNEL SHA MODE

In 3-channel SHA mode, the AD9822 simultaneously samples the red, green, and blue input voltages. The sampling point is controlled by CDSCLK2. CDSCLK2's falling edge samples the input waveforms on each channel. The output voltages from the three SHAs are modified by the offset DACs and then scaled by the three PGAs. The outputs of the PGAs are then multiplexed through the 14-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin (see Figure 12). With the OFFSET pin grounded, a 0 V input corresponds to the ADC's zero-scale output. The OFFSET pin may also be used as a coarse offset adjust pin. A voltage applied to this pin is subtracted from the voltages applied to the red, green, and blue inputs in the first amplifier stage of the AD9822. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 5. CDSCLK1 should be grounded in this mode. Although not required, it is recommended that the falling edge of CDSCLK2 occur coincident with or before the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three ADCCLK cycles.

The offset and gain values for the red, green, and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register.

1-CHANNEL CDS MODE

This mode operates in the same way as the 3-channel CDS mode. The difference is that the multiplexer remains fixed in this mode; therefore, only the channel specified in the MUX register is processed.

Timing for this mode is shown in Figure 4.

1-CHANNEL SHA MODE

This mode operates in the same way as the 3-channel SHA mode, except the multiplexer remains stationary. Only the channel specified in the MUX register is processed.

The input signal is sampled with respect to the voltage applied to the OFFSET pin. With the OFFSET pin grounded, a 0 V input corresponds to the ADC's zero-scale output. The OFFSET pin may also be used as a coarse offset adjust pin. A voltage applied to this pin is subtracted from the voltages applied to the red, green, and blue inputs in the first amplifier stage of the AD9822. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 6. CDSCLK1 should be grounded in this mode of operation.

INTERNAL REGISTER DESCRIPTIONS

Table 6. Internal Register Map

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	VREF	3Ch/1Ch	CDS On	Clamp	Pwr Dn	0	0
MUX	0	0	1	0	RGB/BGR	Red	Green	Blue	0	0	0	0
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Configuration Register

The Configuration Register controls the AD9822's operating mode and bias levels. Bits D8, D1, and D0 should always be set low. Bit D7 sets the full-scale voltage range of the AD9822's ADC to either 4 V (high) or 2 V (low). Bit D6 controls the internal voltage reference. If the AD9822's internal voltage reference is used, this bit is set high. Setting Bit D6 low disables the internal voltage reference, allowing an external voltage reference to be used. Bit D5 configures the AD9822 for either the 3-channel (high) or 1-channel (low) mode of operation. Setting Bit D4 high enables the CDS mode of operation and setting this bit low enables the SHA mode of operation. Bit D3 sets the dc bias level of the AD9822's input clamp. This bit should always be set high for the 4 V clamp bias, unless a CCD with a reset feedthrough transient exceeding 2 V is used. If the 3 V clamp bias level is used, the peak-to-peak input signal range to the AD9822 is reduced to 3 V maximum. Bit D2 controls the power-down mode. Setting Bit D2 high places the AD9822 into a very low power "sleep" mode. All register contents are retained while the AD9822 is in the power-down state.

Table 7. Configuration Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Internal VREF	No. of Channels	CDS Operation	Input Clamp Bias	Power-Down	Set to 0	Set to 0
		1 = Enabled[1]	1 = 3-Ch Mode[1]	1 = CDS Mode[1]	1 = 4 V[1]	1 = On		
		0 = Disabled	0 = 1-Ch Mode	0 = SHA Mode	0 = 3 V	0 = Off (Normal)[1]		

[1] Power-on default value.

MUX Register

The MUX register controls the sampling channel order in the AD9822. Bits D8, D3, D2, D1, and D0 should always be set low. Bit D7 is used when operating in 3-channel mode. Setting Bit D7 high sequences the MUX to sample the red channel first, then the green channel, and then the blue channel. When in this mode, the CDSCLK2 pulse always resets the MUX to sample the red channel first (see Figure 3). When Bit D7 is set low, the channel order is reversed to blue first, green second, and red third. The CDSCLK2 pulse always resets the MUX to sample the blue channel first. Bits D6, D5, and D4 are used when operating in 1-channel mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX remains stationary during 1-channel mode.

Table 8. MUX Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	3-Channel Select	1-Channel Select	1-Channel Select	1-Channel Select	Set to 0	Set to 0	Set to 0	Set to 0
	1 = R-G-B[1]	1 = RED[1]	1 = GREEN	1 = BLUE				
	0 = B-G-R	0 = Off	0 = Off[1]	0 = Off[1]				

[1] Power-on default value.

PGA Gain Registers

There are three PGA registers for individually programming the gain in the red, green, and blue channels. Bits D8, D7, and D6 in each register must be set low, and Bits D5 through D0 control the gain range in 64 increments. See Figure 15 for the PGA gain vs. the PGA register code. The coding for the PGA registers is straight binary, with an all 0s word corresponding to the minimum gain setting (1×) and an all 1s word corresponding to the maximum gain setting (5.7×).

Table 9. PGA Gain Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0		
Set to 0	**Set to 0**	**Set to 0**	**MSB**					**LSB**	**Gain (V/V)**	**Gain (dB)**
0	0	0	0	0	0	0	0	0[1]	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
					•				•	•
					•				•	•
					•				•	•
0	0	0	1	1	1	1	1	0	5.4	14.6
0	0	0	1	1	1	1	1	1	5.7	15.1

[1] Power-on default value.

Offset Registers

There are three PGA registers for individually programming the offset in the red, green, and blue channels. Bits D8 through D0 control the offset range from −350 mV to +350 mV in 512 increments. The coding for the offset registers is sign magnitude, with D8 as the sign bit. Table 10 shows the offset range as a function of the Bits D8 through D0.

Table 10. Offset Register Settings

D8 (MSB)	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Offset (mV)
0	0	0	0	0	0	0	0	0[1]	0
0	0	0	0	0	0	0	0	1	+1.2
					•				•
					•				•
					•				•
0	1	1	1	1	1	1	1	1	+350
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	−1.2
					•				•
					•				•
					•				•
1	1	1	1	1	1	1	1	1	−350

[1] Power-on default value.

CIRCUIT OPERATION

ANALOG INPUTS—CDS MODE

Figure 10 shows the analog input configuration for the CDS mode of operation. Figure 11 shows the internal timing for the sampling switches. The CCD reference level is sampled when CDSCLK1 transitions from high to low, opening S1. The CCD data level is sampled when CDSCLK2 transitions from high to low, opening S2. S3 is then closed, generating a differential output voltage representing the difference between the two sampled levels.

The input clamp is controlled by CDSCLK1. When CDSCLK1 is high, S4 closes and the internal bias voltage is connected to the analog input. The bias voltage charges the external 0.1 µF input capacitor, level-shifting the CCD signal into the AD9822's input common-mode range. The time constant of the input clamp is determined by the internal 5 kΩ resistance and the external 0.1 µF input capacitance.

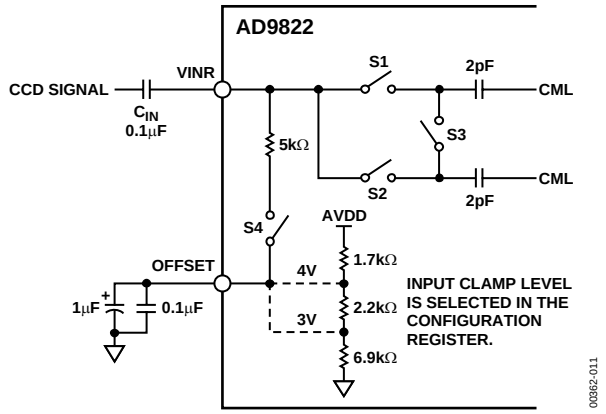


Figure 10. CDS Mode Input Configuration (All Three Channels are Identical)

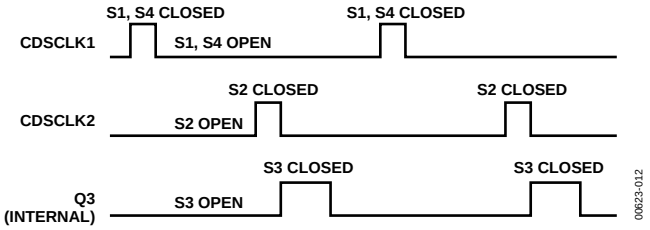


Figure 11. CDS Mode Internal Switch Timing

EXTERNAL INPUT COUPLING CAPACITORS

The recommended value for the input coupling capacitors is 0.1 µF. While it is possible to use a smaller capacitor, this larger value is chosen for several reasons:

- Signal Attenuation: The input coupling capacitor creates a capacitive divider with a CMOS integrated circuit's input capacitance, attenuating the CCD signal level. CIN should be large relative to the IC's 10 pF input capacitance in order to minimize this effect.
- Linearity: Some of the input capacitance of a CMOS IC is junction capacitance, which varies nonlinearly with applied voltage. If the input coupling capacitor is too small, the attenuation of the CCD signal varies nonlinearly with signal level. This degrades the system linearity performance.
- Sampling Errors: The internal 2 pF sample capacitors have a "memory" of the previously sampled pixel. There is a charge redistribution error between CIN and the internal sample capacitors for larger pixel-to-pixel voltage swings. As the value of CIN is reduced, the resulting error in the sampled voltage increases. With a CIN value of 0.1 µF, the charge redistribution error is less than 1 LSB for a full-scale, pixel-to-pixel voltage swing.

ANALOG INPUTS—SHA MODE

Figure 12 shows the analog input configuration for the SHA mode of operation. Figure 13 shows the internal timing for the sampling switches. The input signal is sampled when CDSCLK2 transitions from high to low, opening S1. The voltage on the OFFSET pin is also sampled on the falling edge of CDSCLK2, when S2 opens. S3 is then closed, generating a differential output voltage representing the difference between the sampled input voltage and the OFFSET voltage. The input clamp is disabled during SHA mode operation.

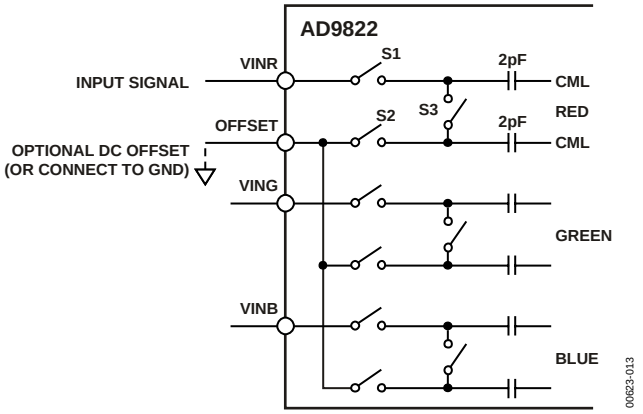


Figure 12. SHA Mode Input Configuration (All Three Channels are Identical)

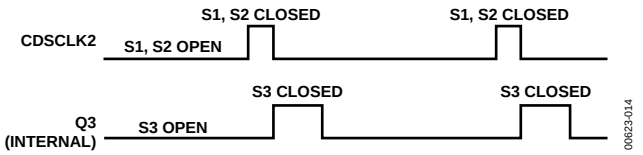


Figure 13. SHA Mode Internal Switch Timing

Figure 14 shows how the OFFSET pin may be used in a CIS application for coarse offset adjustment. Many CIS signals have dc offsets ranging from several hundred millivolts to more than 1 V. By connecting the appropriate dc voltage to the OFFSET pin, the CIS signal is restored to 0. After the large dc offset is removed, the signal can be scaled using the PGA to maximize the ADC's dynamic range.

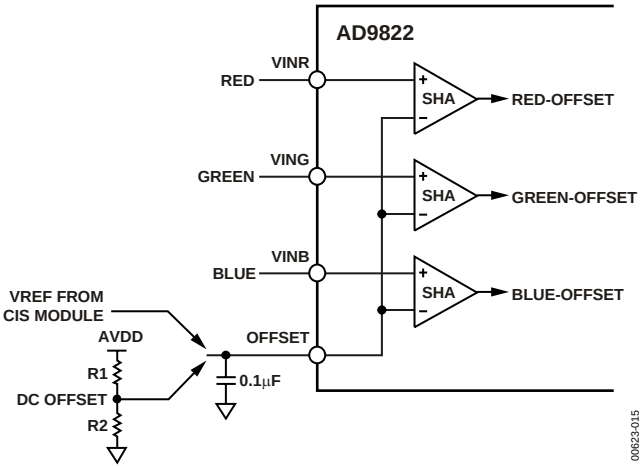


Figure 14. SHA Mode Used with External DC Offset

PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The AD9822 uses one PGA for each channel. Each PGA has a gain range from 1× (0 dB) to 5.8× (15.5 dB), adjustable in 64 steps. Figure 15 shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear-in-dB, the gain in V/V varies nonlinearly with register code, following the equation

$$Gain = \frac{5.7}{1 + 4.7\left[\frac{63 - G}{63}\right]}$$

where G is the decimal value of the gain register contents and varies from 0 to 63.

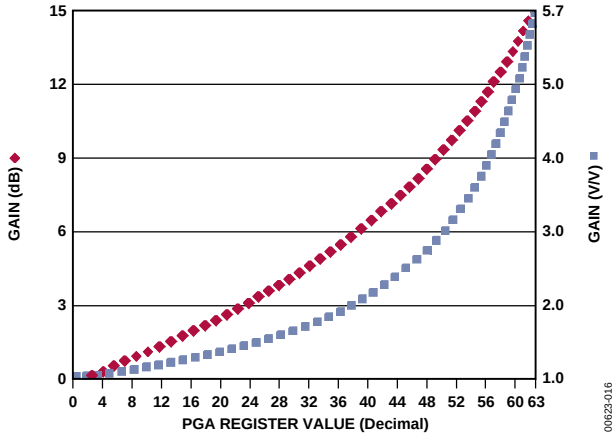


Figure 15. PGA Gain Transfer Function

APPLICATIONS

CIRCUIT AND LAYOUT RECOMMENDATIONS

Figure 16 shows the recommended circuit configuration for 3-channel CDS mode operation. The recommended input coupling capacitor value is 0.1 µF (see the Circuit Operation section). A single ground plane is recommended for the AD9822. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the AD9822. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK (see Figure 3 through Figure 6 for timing). All 0.1 µF decoupling capacitors should be located as close as possible to the AD9822 pins. When operating in single-channel mode, the unused analog inputs should be grounded.

Figure 17 shows the recommended circuit configuration for 3-channel SHA mode. All of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the AD9822 without the use of coupling capacitors. The analog input signals must already be dc-biased between 0 V and 2 V (see the Circuit Operation section).

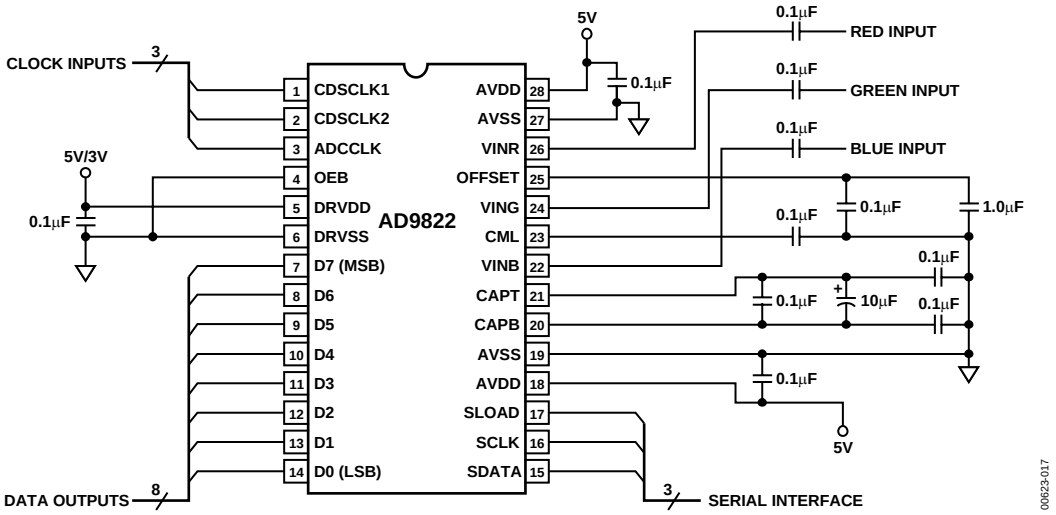


Figure 16. Recommended Circuit Configuration, 3-Channel CDS Mode

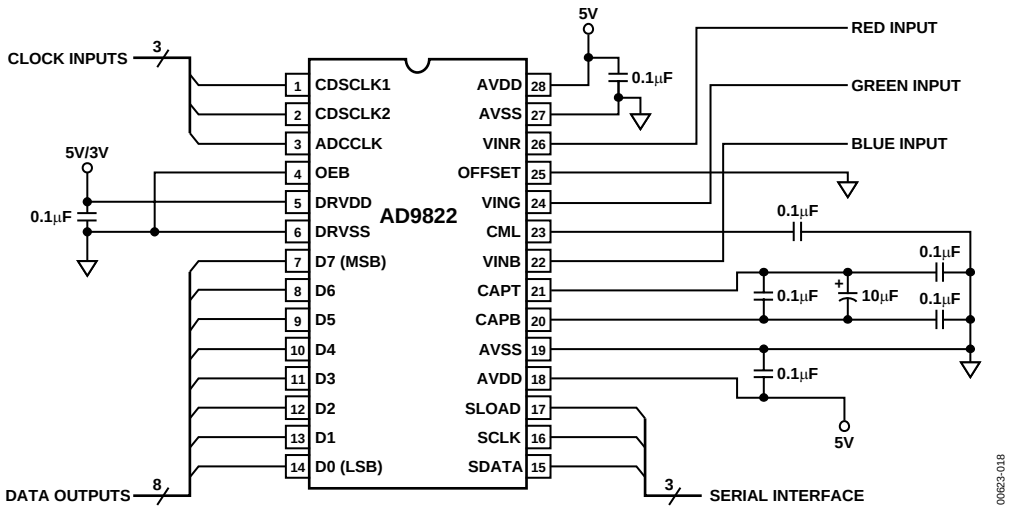
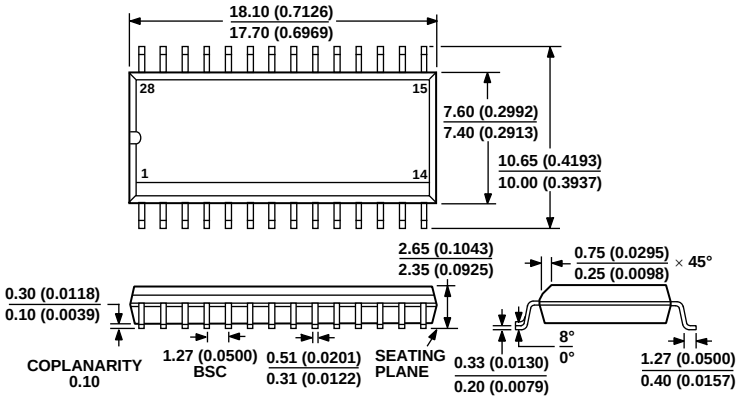


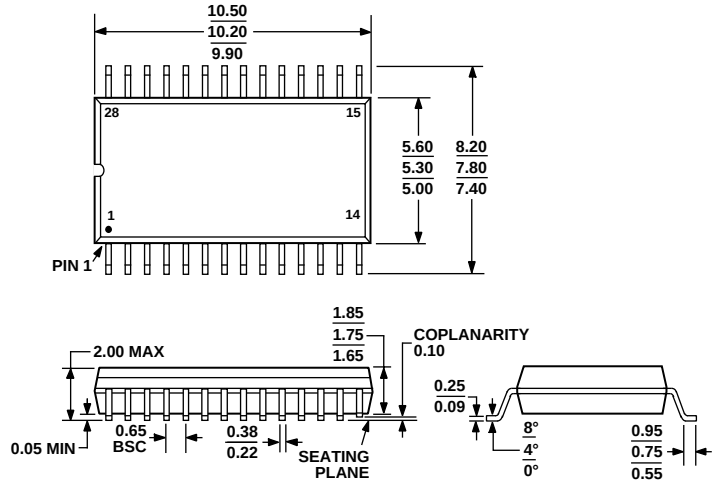
Figure 17. Recommended Circuit Configuration, 3-Channel SHA Mode (Analog Inputs Sampled with Respect to Ground)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 18. 28-Lead Standard Small Outline Package [SOIC]
Wide Body (R-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150AH

Figure 19. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9822JR	0°C to 70°C	28-Lead SOIC	R-28
AD9822JRRL	0°C to 70°C	28-Lead SOIC	R-28
AD9822JRS	0°C to 70°C	28-Lead SSOP	RS-28
AD9822JRSRL	0°C to 70°C	28-Lead SSOP	RS-28
AD9822JRSZ[1]	0°C to 70°C	28-Lead SSOP	RS-28
AD9822JRSZRL[1]	0°C to 70°C	28-Lead SSOP	RS-28

[1] Z = Pb-free part.

NOTES

NOTES

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C00623–0–2/05(B)

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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А