



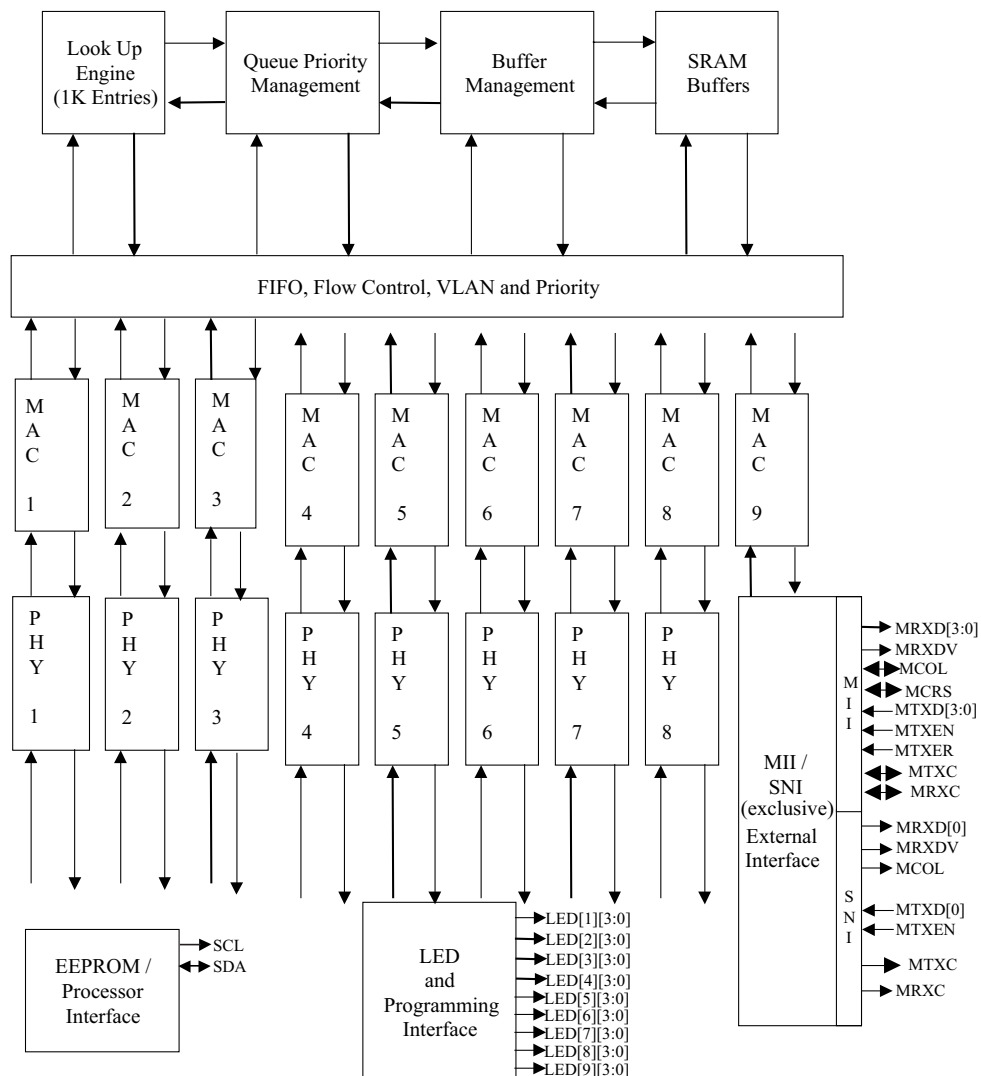
General Description

The KS8999 contains eight 10/100 physical layer transceivers, nine MAC (Media Access Control) units with an integrated layer 2 switch. The device runs in two modes. The first mode is an eight port integrated switch and the second is as a nine port switch with the ninth port available through an MII (Media Independent Interface). Useful configurations include a stand alone eight port switch as well as a eight port switch with a routing element connected to the extra MII port. The additional port is also useful for a public network interfacing. The

KS8999 is designed to reside in an unmanaged design not requiring processor intervention. This is achieved through I/O strapping or EEPROM programming at system reset time. On the media side, the KS8999 supports 10BaseT, 100BaseTX and 100BaseFX as specified by the IEEE 802.3 committee. Physical signal transmission and reception are enhanced through use of analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Functional Diagram



Features

- 9 port (8+1) 10/100 integrated switch with eight physical layer transceivers and one MII/SNI interface
- Advanced Ethernet Switch with internal frame buffer
 - 128K Byte of SRAM on chip for frame buffering
 - 2.0Gbps high performance memory bandwidth
 - Wire speed reception and transmission
 - Integrated address look-up engine, supports 1K absolute MAC addresses
 - Automatic address learning, address aging and address migration
- Advanced Switch Features
 - Supports 802.1p priority and port based priority
 - Supports port based VLAN
 - Supports 1536 byte frame for VLAN tag
 - Supports DiffServ priority, 802.1p based priority or port based priority and broadcast storm protection
- Proven transceiver technology for UTP and fiber operation
 - 10BaseT, 100BaseTX and 100BaseFX modes of operation
 - Supports for UTP or fiber on all 8-ports
 - Indicators for link, activity, full/half-duplex and speed
 - Hardware based 10/100, full/half, flow control and auto-negotiation
 - Individual port forced modes (full duplex, 100BaseTX) when auto-negotiation is disabled
 - Full duplex IEEE 802.3x flow control
 - Half-duplex back pressure flow control
- Supports MDI/MDI-X auto crossover
- External MAC interface (MII or 7-wire) for router applications
- Unmanaged operation via strapping or EEPROM at system reset time (see Reset Reference Circuit section)
- Comprehensive LED support
- Single 2.0V power supply with options for 2.5V and 3.3V I/O
- 900 mA (1.80W) including physical transmit drivers
- Supports both commercial and industry temperature
 - Commercial temperature range: 0°C to +70°C (KS8999)
 - Industrial temperature range: –40°C to +85°C (KS8999I)
- Supports lead free products:
 - Commercial temperature range: 0°C to +70°C (KSZ8999)
 - Industrial temperature range: –40°C to +85°C (KSZ8999I)
- Available in 208-pin PQFP package

Ordering Information

| Part Number | Temperature Range | Package |
|-------------|-------------------|--------------|
| KS8999 | 0°C to +70°C | 208-Pin PQFP |
| KS8999I | –40°C to +85°C | 208-Pin PQFP |
| KSZ8999 | 0°C to +70°C | 208-Pin PQFP |
| KSZ8999I | –40°C to +85°C | 208-Pin PQFP |

Revision History

| Revision | Date | Summary of Changes |
|----------|-----------|---|
| 1.00 | 11/27/00 | Preliminary Release |
| 1.01 | 03/30/01 | Update maximum frame size Update EEPROM priority descriptions Update I/O pin definition Update I/O descriptions Update Electrical Characteristics |
| 1.02 | 04/20/01 | Correct timing information |
| 1.03 | 05/11/01 | Add MDI/MDI-X description |
| 1.04 | 06/22/01 | Change electrical requirements |
| 1.05 | 0/6/25/01 | Correct I/O descriptions |
| 1.06 | 07/25/01 | Update PLL clock information Update timing information |
| 1.07 | 08/09/01 | Correct LED[6][1:0] to float configuration Add reverse and forward timing Correct optional CPU timing |
| 1.08 | 1/14/02 | Update Optional CPU interface Correct I/O description for MCOL and MCRS Correct pin 174 and 175 description |
| 1.09 | 6/18/02 | Correct default to floating for pin 174 Change pin 87 TEST[3] to AUTOMDIX for enable/disable of auto MDI-MDIX function |
| 1.10 | 2/27/03 | Add KS8999I industrial temperature Update non-periodic blinking in Mode 1 of LED[1:9][0] Add MRXD[0] description |
| 1.11 | 5/12/03 | Changed Vcc from 2.00 to 2.10 (typical) Added FEF disable to T[4] pin #173 |
| 1.12 | 8/29/03 | Convert to new format. |
| 1.13 | 1/19/05 | Correct pin type description. Correct selection of reference oscillator/crystal spec. Insert recommended reset circuit. |
| 1.14 | 1/31/05 | Added lead free and Industrial temperature packages. |

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System Level Applications

The KS8999 can be configured to fit either in an eight port 10/100 application or as a nine port 10/100 network interface with an extra MII/7-wire port. This MII/7-wire port can be connected to an external processor and used for routing

purposes or public network access. The major benefits of using the KS8999 are the lower power consumption, unmanaged operation, flexible configuration, built in frame buffering, VLAN abilities and traffic priority control. Two such applications are depicted below.

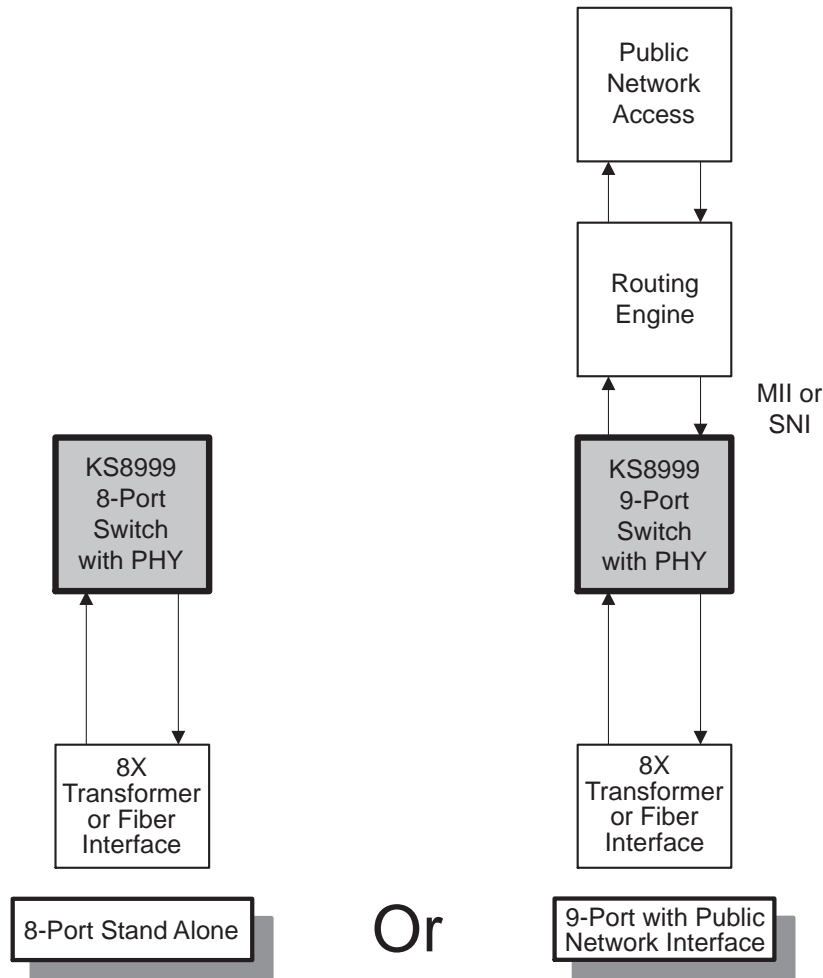


Figure 1. System Applications

Pin Description

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|----------|--------------------------|------|--|
| 1 | VDD_RX | Pwr | | 2.0V for equalizer |
| 2 | GND_RX | GND | | Ground for equalizer |
| 3 | GND_RX | GND | | Ground for equalizer |
| 4 | VDD_RX | Pwr | | 2.0V for equalizer |
| 5 | RXP[3] | I | 3 | Physical receive signal + (differential) |
| 6 | RXM[3] | I | 3 | Physical receive signal - (differential) |
| 7 | AOUT2 | O | | Factory test output |
| 8 | DOOUT2 | O | | Factory test output |
| 9 | TXP[3] | O | 3 | Physical transmit signal + (differential) |
| 10 | TXM[3] | O | 3 | Physical transmit signal - (differential) |
| 11 | QH[5] | Opd | | Factory test pin – leave open for normal operation |
| 12 | QH[4] | Opd | | Factory test pin – leave open for normal operation |
| 13 | QH[3] | Opd | | Factory test pin – leave open for normal operation |
| 14 | QH[2] | Opd | | Factory test pin – leave open for normal operation |
| 15 | GND_TX | GND | | Ground for transmit circuitry |
| 16 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 17 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 18 | GND-ISO | GND | | Analog ground |
| 19 | TXP[4] | O | 4 | Physical transmit signal + (differential) |
| 20 | TXM[4] | O | 4 | Physical transmit signal - (differential) |
| 21 | GND_TX | GND | | Ground for transmit circuitry |
| 22 | RXP[4] | I | 4 | Physical receive signal + (differential) |
| 23 | RXM[4] | I | 4 | Physical receive signal - (differential) |
| 24 | GND_RX | GND | | Ground for equalizer |
| 25 | VDD_RX | Pwr | | 2.0V for equalizer |
| 26 | ISET | | | Set physical transmit output current |
| 27 | GND-ISO | GND | | Analog ground |
| 28 | VDD_RX | Pwr | | 2.0V for equalizer |
| 29 | GND_RX | GND | | Ground for equalizer |
| 30 | RXP[5] | I | 5 | Physical receive signal + (differential) |
| 31 | RXM[5] | I | 5 | Physical receive signal - (differential) |
| 32 | GND_TX | GND | | Ground for transmit circuitry |
| 33 | TXP[5] | O | 5 | Physical transmit signal + (differential) |
| 34 | TXM[5] | O | 5 | Physical transmit signal - (differential) |

Note 1. Pwr = power supply
 GND = ground
 I = input
 O = output
 I/O = bi-directional
 Ipu = input w/ internal pull-up
 Ipd = input w/ internal pull-down
 Opu = output w/ internal pull-up
 Opd = output w/ internal pull-down
 Ipd/O = input w/ internal pull-down during reset, output pin otherwise
 Ipu/O = input w/ internal pull-up during reset, output pin otherwise

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|----------|--------------------------|------|---|
| 35 | GND-ISO | GND | | Analog ground |
| 36 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 37 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 38 | GND_TX | GND | | Ground for transmit circuitry |
| 39 | QL[2] | Opd | | Factory test pin – leave open for normal operation |
| 40 | QL[3] | Opd | | Factory test pin – leave open for normal operation |
| 41 | QL[4] | Opd | | Factory test pin – leave open for normal operation |
| 42 | QL[5] | Opd | | Factory test pin – leave open for normal operation |
| 43 | TXP[6] | O | 6 | Physical transmit signal + (differential) |
| 44 | TXM[6] | O | 6 | Physical transmit signal - (differential) |
| 45 | DOUT | O | | Factory test output – leave open for normal operation |
| 46 | AOUT | O | | Factory test output – leave open for normal operation |
| 47 | RXP[6] | I | 6 | Physical receive signal + (differential) |
| 48 | RXM[6] | I | 6 | Physical receive signal - (differential) |
| 49 | VDD_RX | Pwr | | 2.0V for equalizer |
| 50 | GND_RX | GND | | Ground for equalizer |
| 51 | GND_RX | GND | | Ground for equalizer |
| 52 | VDD_RX | Pwr | | 2.0V for equalizer |
| 53 | GND-ISO | GND | | Analog ground |
| 54 | RXP[7] | I | 7 | Physical receive signal + (differential) |
| 55 | RXM[7] | I | 7 | Physical receive signal - (differential) |
| 56 | GND_TX | GND | | Ground for transmit circuitry |
| 57 | TXP[7] | O | 7 | Physical transmit signal + (differential) |
| 58 | TXM[7] | O | 7 | Physical transmit signal - (differential) |
| 59 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 60 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 61 | TXP[8] | O | 8 | Physical transmit signal + (differential) |
| 62 | TXM[8] | O | 8 | Physical transmit signal - (differential) |
| 63 | GND_TX | GND | | Ground for transmit circuitry |
| 64 | RXP[8] | I | 8 | Physical receive signal + (differential) |
| 65 | RXM[8] | I | 8 | Physical receive signal - (differential) |
| 66 | GND_RX | GND | | Ground for equalizer |
| 67 | VDD_RX | Pwr | | 2.0V for equalizer |
| 68 | FXSD[5] | lpd | 5 | Fiber signal detect |
| 69 | FXSD[6] | lpd | 6 | Fiber signal detect |

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 Opd = output w/ internal pull-down
 Ipd/O = input w/ internal pull-down during reset, output pin otherwise
 Ipu/O = input w/ internal pull-up during reset, output pin otherwise

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|----------|--------------------------|------|--|
| 70 | FXSD[7] | lpd | 7 | Fiber signal detect |
| 71 | FXSD[8] | lpd | 8 | Fiber signal detect |
| 72 | GND_RCV | GND | | Ground for clock recovery circuit |
| 73 | GND_RCV | GND | | Ground for clock recovery circuit |
| 74 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 75 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 76 | GND_RCV | GND | | Ground for clock recovery circuit |
| 77 | GND_RCV | GND | | Ground for clock recovery circuit |
| 78 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 79 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 80 | BTOUT2 | O | | Factory test pin – leave open for normal operation |
| 81 | CTOUT2 | O | | Factory test pin – leave open for normal operation |
| 82 | RLPBK | I | | Enable loop back for testing – pull-down/float for normal operation |
| 83 | MUX[1] | I | | Factory test pin – float for normal operation |
| 84 | MUX[2] | I | | Factory test pin – float for normal operation |
| 85 | TEST[1] | I | | Factory test pin – float for normal operation |
| 86 | TEST[2] | I | | Factory test pin – float for normal operation |
| 87 | AUTOMDIX | I | | Auto MDI/MDIX enable and disable – pull-up/float enable; pull-down disable |
| 88 | T[1] | lpu | | Factory test pin – float for normal operation |
| 89 | T[2] | lpd | | Factory test pin – float for normal operation |
| 90 | T[3] | lpd | | Factory test pin – float for normal operation |
| 91 | EN1P | lpd | | Enable 802.1p for all ports |
| 92 | SDA | lpd/O | | Serial data from EEPROM or processor |
| 93 | SCL | lpd/O | | Clock for EEPROM or from processor |
| 94 | VDD | Pwr | | 2.0V for core digital circuitry |
| 95 | GND | GND | | Ground for digital circuitry |
| 96 | MTXEN | lpd | 9 | MII transmit enable |
| 97 | MTXD[3] | lpd | 9 | MII transmit bit 3 |
| 98 | MTXD[2] | lpd | 9 | MII transmit bit 2 |
| 99 | MTXD[1] | lpd | 9 | MII transmit bit 1 |
| 100 | MTXD[0] | lpd | 9 | MII transmit bit 0 |
| 101 | MTXER | lpd | 9 | MII transmit error |
| 102 | MTXC | lpd/O | 9 | MII transmit clock |
| 103 | MCOL | lpd/O | 9 | MII collision detected |
| 104 | MCRS | lpd/O | 9 | MII carrier sense |

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 Opd = output w/ internal pull-down
 lpd/O = input w/ internal pull-down during reset, output pin otherwise
 lpu/O = input w/ internal pull-up during reset, output pin otherwise

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|-----------|--------------------------|------|---|
| 105 | VDD-IO | Pwr | | 2.0V, 2.5V or 3.3V for I/O circuitry |
| 106 | GND | GND | | Ground for digital circuitry |
| 107 | GND | GND | | Ground for digital circuitry |
| 108 | VDD | Pwr | | 2.0V for core digital circuitry |
| 109 | BIST | lpd | | Built in self test – tie low for normal operation |
| 110 | RST# | I | | Reset – active low |
| 111 | LED[1][3] | lpu/O | 1 | LED indicator 3 |
| 112 | LED[1][2] | lpu/O | 1 | LED indicator 2 |
| 113 | LED[1][1] | lpu/O | 1 | LED indicator 1 |
| 114 | LED[1][0] | lpu/O | 1 | LED indicator 0 |
| 115 | LED[2][3] | lpu/O | 2 | LED indicator 3 |
| 116 | LED[2][2] | lpu/O | 2 | LED indicator 2 |
| 117 | LED[2][1] | lpu/O | 2 | LED indicator 1 |
| 118 | LED[2][0] | lpu/O | 2 | LED indicator 0 |
| 119 | MRXDV | Opd | 9 | MII receive data valid |
| 120 | MRXD[3] | Opu | 9 | MII receive bit 3 |
| 121 | MRXD[2] | Opu | 9 | MII receive bit 2 |
| 122 | MRXD[1] | Opu | 9 | MII receive bit 1 |
| 123 | MRXD[0] | Opu | 9 | MII receive bit 0 |
| 124 | MRXC | lpu/O | 9 | MII receive clock |
| 125 | VDD-IO | Pwr | | 2.0V, 2.5V or 3.3V for I/O circuitry |
| 126 | GND | GND | | Ground for digital circuitry |
| 127 | LED[3][3] | lpu/O | 3 | LED indicator 3 |
| 128 | LED[3][2] | lpu/O | 3 | LED indicator 2 |
| 129 | LED[3][1] | lpu/O | 3 | LED indicator 1 |
| 130 | LED[3][0] | lpu/O | 3 | LED indicator 0 |
| 131 | LED[4][3] | lpu/O | 4 | LED indicator 3 |
| 132 | LED[4][2] | lpu/O | 4 | LED indicator 2 |
| 133 | LED[4][1] | lpu/O | 4 | LED indicator 1 |
| 134 | LED[4][0] | lpu/O | 4 | LED indicator 0 |
| 135 | VDD | Pwr | | 2.0V for core digital circuitry |
| 136 | GND | GND | | Ground for digital circuitry |
| 137 | LED[5][3] | lpu/O | 5 | LED indicator 3 |
| 138 | LED[5][2] | lpu/O | 5 | LED indicator 2 |
| 139 | LED[5][1] | lpu/O | 5 | LED indicator 1 |

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 Opd = output w/ internal pull-down
 lpd/O = input w/ internal pull-down during reset, output pin otherwise
 lpu/O = input w/ internal pull-up during reset, output pin otherwise

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|------------|--------------------------|------|--|
| 140 | LED[5][0] | lpu/O | 5 | LED indicator 0 |
| 141 | LED[6][3] | lpu/O | 6 | LED indicator 3 |
| 142 | LED[6][2] | lpu/O | 6 | LED indicator 2 |
| 143 | LED[6][1] | lpu/O | 6 | LED indicator 1 |
| 144 | LED[6][0] | lpu/O | 6 | LED indicator 0 |
| 145 | LED[7][3] | lpu/O | 7 | LED indicator 3 |
| 146 | LED[7][2] | lpu/O | 7 | LED indicator 2 |
| 147 | LED[7][1] | lpu/O | 7 | LED indicator 1 |
| 148 | VDD-IO | Pwr | | 2.0V, 2.5V or 3.3V for I/O circuitry |
| 149 | LED[7][0] | lpu/O | 7 | LED indicator 0 |
| 150 | LED[8][3] | lpu/O | 8 | LED indicator 3 |
| 151 | LED[8][2] | lpu/O | 8 | LED indicator 2 |
| 152 | LED[8][1] | lpu/O | 8 | LED indicator 1 |
| 153 | LED[8][0] | lpu/O | 8 | LED indicator 0 |
| 154 | GND | GND | | Ground for digital circuitry |
| 155 | GND | GND | | Ground for digital circuitry |
| 156 | IO_SWM | lpu | | Factory test pin – tie high for normal operation |
| 157 | VDD | Pwr | | 2.0V for core digital circuitry |
| 158 | LED[9][3] | lpu/O | 9 | LED indicator 3 |
| 159 | LED[9][2] | lpu/O | 9 | LED indicator 2 |
| 160 | LED[9][1] | lpu/O | 9 | LED indicator 1 |
| 161 | LED[9][0] | lpu/O | 9 | LED indicator 0 |
| 162 | MIIS[1] | lpd | 9 | MII mode select bit 1 |
| 163 | MIIS[0] | lpd | 9 | MII mode select bit 0 |
| 164 | MODESEL[3] | lpd | | Selects LED and test modes |
| 165 | MODESEL[2] | lpd | | Selects LED and test modes |
| 166 | MODESEL[1] | lpd | | Selects LED and test modes |
| 167 | MODESEL[0] | lpd | | Selects LED and test modes |
| 168 | TESTEN | lpd | | Factory test pin – tie low for normal operation |
| 169 | SCANEN | lpd | | Factory test pin – tie low for normal operation |
| 170 | PRSV | lpd | | Reserve 6KB buffer for priority frames |
| 171 | CFGMODE | lpu | | Configures programming interface for EEPROM or processor |
| 172 | T[5] | I | | Factory test pin – float for normal operation |
| 173 | T[4] | lpdthevillage | | F/D = normal operation (default) U = disable FEF |
| 174 | Reserve | I | | Reserved – floating for normal operation |

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Opd = output w/ internal pull-down
lpd/O = input w/ internal pull-down during reset, output pin otherwise
lpu/O = input w/ internal pull-up during reset, output pin otherwise

| Pin Number | Pin Name | Type ^(Note 1) | Port | Pin Function |
|------------|-----------|--------------------------|------|--|
| 175 | Reserve | I | | Reserved - floating for normal operation |
| 176 | X1 | I | | Crystal or clock input |
| 177 | X2 | O | | Connect to crystal |
| 178 | VDD_PLLTX | Pwr | | 2.0 V for phase locked loop circuit |
| 179 | GND_PLLTX | GND | | Ground for phase locked loop circuit |
| 180 | CTOUT | O | | Factory test pin – leave open for normal operation |
| 181 | BTOUT | O | | Factory test pin – leave open for normal operation |
| 182 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 183 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 184 | GND_RCV | GND | | Ground for clock recovery circuit |
| 185 | GND_RCV | GND | | Ground for clock recovery circuit |
| 186 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 187 | VDD_RCV | Pwr | | 2.0V for clock recovery circuit |
| 188 | GND_RCV | GND | | Ground for clock recovery circuit |
| 189 | GND_RCV | GND | | Ground for clock recovery circuit |
| 190 | FXSD[1] | lpd | 1 | Fiber signal detect |
| 191 | FXSD[2] | lpd | 2 | Fiber signal detect |
| 192 | FXSD[3] | lpd | 3 | Fiber signal detect |
| 193 | FXSD[4] | lpd | 4 | Fiber signal detect |
| 194 | VDD_RX | Pwr | | 2.0V for equalizer |
| 195 | GND_RX | GND | | Ground for equalizer |
| 196 | RXP[1] | I | 1 | Physical receive signal + (differential) |
| 197 | RXM[1] | I | 1 | Physical receive signal - (differential) |
| 198 | GND_TX | GND | | Ground for transmit circuitry |
| 199 | TXP[1] | O | 1 | Physical transmit signal + (differential) |
| 200 | TXM[1] | O | 1 | Physical transmit signal - (differential) |
| 201 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 202 | VDD_TX | Pwr | | 2.0V for transmit circuitry |
| 203 | TXP[2] | O | 2 | Physical transmit signal + (differential) |
| 204 | TXM[2] | O | 2 | Physical transmit signal - (differential) |
| 205 | GND_TX | GND | | Ground for transmit circuitry |
| 206 | RXP[2] | I | 2 | Physical receive signal + (differential) |
| 207 | RXM[2] | I | 2 | Physical receive signal - (differential) |
| 208 | GND-ISO | GND | | Analog ground |

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GND = ground
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lpu = input w/ internal pull-up
lpd = input w/ internal pull-down
Opu = output w/ internal pull-up
Opd = output w/ internal pull-down
lpd/O = input w/ internal pull-down during reset, output pin otherwise
lpu/O = input w/ internal pull-up during reset, output pin otherwise

I/O Grouping

| Group Name | Description |
|------------|-----------------------------|
| PHY | Physical Interface |
| MII | Media Independent Interface |
| SNI | Serial Network Interface |
| IND | LED Indicators |
| UP | Unmanaged Programmable |
| CTRL | Control and Miscellaneous |
| TEST | Test (Factory) |
| PWR | Power and Ground |

I/O Descriptions

| Group | I/O Names | Active Status | Description |
|-------|----------------------|---------------|--|
| PHY | RXP[1:8] RXM[1:8] | Analog | Differential inputs (receive) for connection to media (transformer or fiber module) |
| | TXP[1:8] TXM[1:8] | Analog | Differential outputs (transmit) for connection to media (transformer or fiber module) |
| | FXSD[1:8] | H | Fiber signal detect – connect to fiber signal detect output on fiber module with appropriate voltage divider if needed. Tie low for copper mode. |
| | ISET | Analog | Transmit Current Set. Connecting an external reference resistor to set transmitter output current. This pin connects to a 3K Ω 1% resistor to ground if a transformer with 1:1 turn ratio is used. |
| MII | MRXD[0:3] | H | Four bit wide data bus for receiving MAC frames |
| | MRXDV | H | Receive data valid |
| | MCOL | H | Receive collision detection |
| | MCRS | H | Carrier sense |
| | MTXD[0:3] | H | Four bit wide data bus for transmitting MAC frames |
| | MTXEN | H | Transmit enable |
| | MTXER | H | Transmit error |
| | MRXC | Clock | MII receive clock |
| | MTXC | Clock | MII transmit clock |
| SNI | MTXD[0] | H | Serial transmit data |
| | MTXEN | H | Transmit enable |
| | MRXD[0] | H | Serial receive data |
| | MRXDV | H | Receive carrier sense/data valid |
| | MCOL | H | Collision detection |
| | MRXC | Clock | SNI receive clock |
| | MTXC | Clock | SNI transmit clock |
| IND | LED[1:9][0] | L | Output (after reset) Mode 0: Speed (on = 100/off = 10) Mode 1: 10/100 + link + activity 10Mb link activity = slow blink (non-periodic blinking) 100Mb link activity = fast blink (non-periodic blinking) Mode 2: Collision (on = collision/off = no collision) Mode 3: Speed (on = 100/off = 10) |

| Group | I/O Names | Active Status | Description(Notes 1) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|--------------|---------------|--|--------------------------|--|--|--|--|---|---|---|---|-----------|---|---|---|---|------------|---|---|---|---|------------|---|---|---|---|------------|---|---|---|---|------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|---|---|---|---|--------------------------|
| | LED[1:9][1] | L | Output (after reset) Mode 0: Full Duplex (on = full/off = half) Mode 1: Full Duplex (on = full/off = half) Mode 2: Full Duplex (on = full/off = half) Mode 3: Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED[1:9][2] | L | Output (after reset) Mode 0: Collision (on = collision/off = no collision) Mode 1: Transmit Activity (on during transmission) Mode 2: Link activity (10Mb mode) Mode 3: Full Duplex + Collision (constant on = full duplex; intermittent on = collision; off = half-duplex with no collision) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED[1:9][3] | L | Output (after reset) Mode 0: Link + Activity When LED is solid "on", it indicates the link is on for both 10 or 100BaseTX, but no data is transmitting or receiving. When LED is solid "off", it indicates the link is off. When LED is blinking, it indicates data is transmitting or receiving for either 10 or 100 BaseTX Mode 1: Receive Activity (on = receiving/off = not receiving) Mode 2: Link activity (100Mb mode) Mode 3: Link + Activity (see description above) <i>Note: Mode is set by MODESEL[3:0]; please see description in UP (unmanaged programming) section.</i> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| UP | MODESEL[3:0] | H | Mode select at reset time. LED mode is selected by using the table below. Note that under normal operation MODESEL[3:2] must be tied low. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="4">MODESEL</th> <th></th> </tr> <tr> <th>3</th> <th>2</th> <th>1</th> <th>0</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>LED mode 0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>LED mode 1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>LED mode 2</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>LED mode 3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Used for factory testing</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Used for factory testing</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Used for factory testing</td> </tr> </tbody> </table> | MODESEL | | | | | 3 | 2 | 1 | 0 | Operation | 0 | 0 | 0 | 0 | LED mode 0 | 0 | 0 | 0 | 1 | LED mode 1 | 0 | 0 | 1 | 0 | LED mode 2 | 0 | 0 | 1 | 1 | LED mode 3 | 0 | 1 | 0 | 0 | Used for factory testing | 0 | 1 | 0 | 1 | Used for factory testing | 0 | 1 | 1 | 0 | Used for factory testing | 0 | 1 | 1 | 1 | Used for factory testing | 1 | 0 | 0 | 0 | Used for factory testing | 1 | 0 | 0 | 1 | Used for factory testing | 1 | 0 | 1 | 0 | Used for factory testing | 1 | 0 | 1 | 1 | Used for factory testing | 1 | 1 | 0 | 0 | Used for factory testing | 1 | 1 | 0 | 1 | Used for factory testing | 1 | 1 | 1 | 0 | Used for factory testing | 1 | 1 | 1 | 1 | Used for factory testing |
| MODESEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 2 | 1 | 0 | Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | LED mode 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | LED mode 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | LED mode 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | LED mode 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | Used for factory testing | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED[1][3] | | Programs auto-negotiation on port 1 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED[1][2] | | Programs auto-negotiation on port 2 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED[1][1] | | Programs auto-negotiation on port 3 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See "Reference Circuits" section.

| Group | I/O Names | Active Status | Description ^(Note 1) |
|-------|-----------|---------------|--|
| | LED[1][0] | | Programs auto-negotiation on port 4 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) |
| | LED[2][3] | | Programs auto-negotiation on port 5 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) |
| | LED[2][2] | | Programs auto-negotiation on port 6 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) |
| | LED[2][1] | | Programs auto-negotiation on port 7 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) |
| | LED[2][0] | | Programs auto-negotiation on port 8 D = Disable auto-negotiation, F/U = Enable auto-negotiation (default) |
| | LED[3][3] | | Programs port speed on port 1. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[3][2] | | Programs port speed on port 2. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[3][1] | | Programs port speed on port 3. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[3][0] | | Programs port speed on port 4. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[4][3] | | Programs port speed on port 5. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[4][2] | | Programs port speed on port 6. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[4][1] | | Programs port speed on port 7. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[4][0] | | Programs port speed on port 8. This is only effective if auto-negotiation is disabled. D = 10Mbps, F/U = 100Mbps (default) |
| | LED[5][3] | | Programs port duplex (full/ half) on port 1. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |
| | LED[5][2] | | Programs port duplex (full/ half) on port 2. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |
| | LED[5][1] | | Programs port duplex (full/ half) on port 3. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |
| | LED[5][0] | | Programs port duplex (full/ half) on port 4. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |
| | LED[9][3] | | Programs port duplex (full/ half) on port 5. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |
| | LED[9][2] | | Programs port duplex (full/ half) on port 6. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) |

Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See "Reference Circuits" section.

| Group | I/O Names | Active Status | Description(Notes 1) | | | | | | | | | | | | |
|-------|-----------------------|---------------|--|------|----------------|-----|--|-----|-----------------------|-----|-------------|-----|-------------|-----|-------------------|
| | LED[9][1] | | Programs port duplex (full / half) on port 7. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) | | | | | | | | | | | | |
| | LED[9][0] | | Programs port duplex (full / half) on port 8. This is only effective if auto-negotiation is disabled or if this end has auto-negotiation enabled and the far end has auto-negotiation disabled. D = Full-duplex, F/U = Half-duplex (default) | | | | | | | | | | | | |
| | LED[6][3] | | Programs back-off aggressiveness for half-duplex mode D = Less aggressive back-off, F/U = More aggressive back-off (default) | | | | | | | | | | | | |
| | LED[6][2] | | Programs retries for frames that encounter collisions. D = Drop frame after 16 collisions, F/U = Continue sending frame regardless of the number of collisions (default) | | | | | | | | | | | | |
| | LED[6][1:0] | | Reserved – use float configuration | | | | | | | | | | | | |
| | LED[7][3] | | Programs flow control D = No flow control, F/U = Flow control enabled (default) | | | | | | | | | | | | |
| | LED[7][2] | | Programs broadcast storm protection. D = 5% broadcast frames allowed, F/U = Unlimited broadcast frames (default) | | | | | | | | | | | | |
| | LED[7][1] | | Programs buffer sharing feature. D = Equal amount of buffers per port (113 buffers), F/U = Share buffers up to 512 buffers on a single port (default) | | | | | | | | | | | | |
| | LED[7][0] | | Reserved – use float configuration | | | | | | | | | | | | |
| | LED[8][3] | | Programs address aging. D = Aging disabled, F/U = Enable 5 minute aging (default) | | | | | | | | | | | | |
| | LED[8][2] | | Programs frame length enforcement. D = Max length for VLAN is 1522 bytes and without VLAN is 1518 bytes F/U = Max length is 1536 bytes (default) | | | | | | | | | | | | |
| | LED[8][1] | | Reserved | | | | | | | | | | | | |
| | LED[8][0] | | Programs half-duplex back pressure. D = No half-duplex back pressure, F/U = Half-duplex back pressure enabled (default) | | | | | | | | | | | | |
| | MRXD[3] | | Programs port 9 speed D = 10Mbps, F/U = 100Mbps (default) | | | | | | | | | | | | |
| | MRXD[2] | | Programs port 9 duplex D = Half-duplex, F/U = Full duplex (default) | | | | | | | | | | | | |
| | MRXD[1] | | Programs port 9 flow control D = Flow control, F/U = No flow control (default) | | | | | | | | | | | | |
| | MRXD[0] | | D = reserved, F/U = normal operation (default) | | | | | | | | | | | | |
| CTRL | EN1P | H | Enable 802.1p for all ports – this enables QoS based on the priority field in the layer 2 header. | | | | | | | | | | | | |
| | | | 0 = 802.1p selected by port in EEPROM 1 = Use 802.1p priority field unless disabled in EEPROM <i>Note: This is also controlled by the EEPROM registers (registers 4-12 bit 4). The values in the EEPROM supercede this pin. Also, if the priority selection is unaltered in the EEPROM registers (register 3 bits 0-7) then values above 3 are considered high priority and less than 4 are low priority.</i> | | | | | | | | | | | | |
| | MIIS[1:0] | H | MII mode selection – allows the MII to run in the following modes <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MIIS</th> <th>Operating mode</th> </tr> </thead> <tbody> <tr> <td>1 0</td> <td></td> </tr> <tr> <td>0 0</td> <td>Disable MII interface</td> </tr> <tr> <td>0 1</td> <td>Reverse MII</td> </tr> <tr> <td>1 0</td> <td>Forward MII</td> </tr> <tr> <td>1 1</td> <td>7 wire mode (SNI)</td> </tr> </tbody> </table> | MIIS | Operating mode | 1 0 | | 0 0 | Disable MII interface | 0 1 | Reverse MII | 1 0 | Forward MII | 1 1 | 7 wire mode (SNI) |
| MIIS | Operating mode | | | | | | | | | | | | | | |
| 1 0 | | | | | | | | | | | | | | | |
| 0 0 | Disable MII interface | | | | | | | | | | | | | | |
| 0 1 | Reverse MII | | | | | | | | | | | | | | |
| 1 0 | Forward MII | | | | | | | | | | | | | | |
| 1 1 | 7 wire mode (SNI) | | | | | | | | | | | | | | |

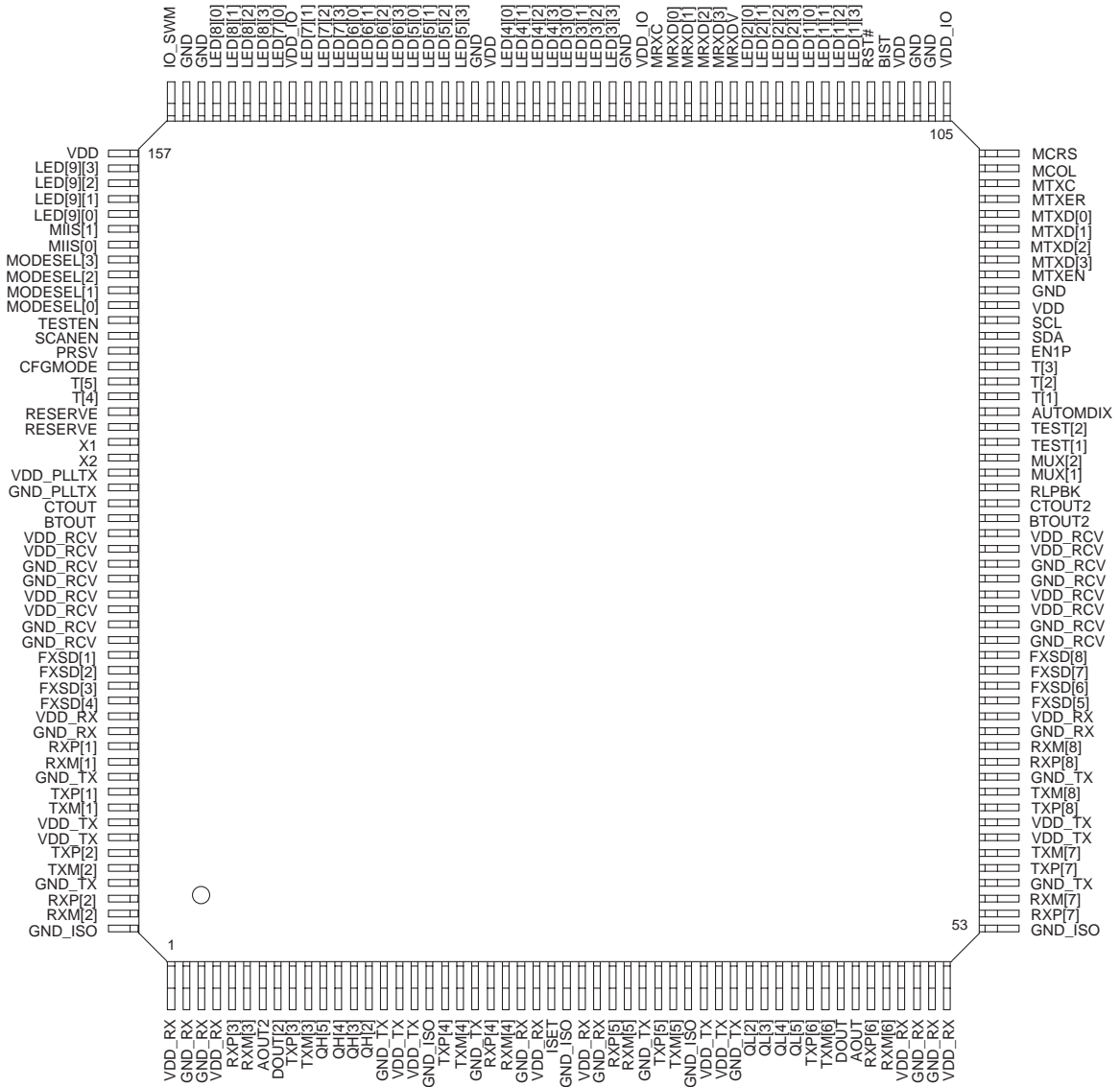
Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up.
See "Reference Circuits" section.

| Group | I/O Names | Active Status | Description ^(Note 1) |
|-------|---------------|---------------|---|
| | PRSV | H | Priority buffer reserve – reserves 6KB of buffer space for the priority traffic if enabled. 0 = No priority reserve 1 = Reserve 6KB for priority traffic <i>Note: This is also controlled by the EEPROM registers (register 2 bit 1). The value in the EEPROM supercedes this pin.</i> |
| | CFGMODE | H | Selects between EEPROM or processor for programming interface. 0 = Processor interface 1 = EEPROM interface or not programmed on this interface (SCL / SDA not used) |
| | X1 | Clock | External crystal or clock input |
| | X2 | Clock | Used when other polarity of crystal is needed. This is unused for a normal clock input. |
| | SCL | Clock | Clock for EEPROM |
| | SDA | I/O | Serial data for EEPROM |
| | RST# | L | System reset |
| TEST | TESTEN | H | Factory test input – tie low for normal operation |
| | SCANEN | H | Factory test input – tie low for normal operation |
| | MUX[1:2] | H | Factory test input – leave open for normal operation |
| | AOUT | H | Factory test output – leave open for normal operation |
| | DOUT | H | Factory test output – leave open for normal operation |
| | AOUT2 | H | Factory test output – leave open for normal operation |
| | DOUT2 | H | Factory test output – leave open for normal operation |
| | BTOUT | H | Factory test output – leave open for normal operation |
| | CTOUT | H | Factory test output – leave open for normal operation |
| | BTOUT2 | H | Factory test output – leave open for normal operation |
| | CTOUT2 | H | Factory test output – leave open for normal operation |
| | TEST[1:2] | H | Factory test inputs – leave open for normal operation |
| | AUTOMDIX | H | F/U = Enable Auto MDI/MDIX (normal operation) D = Disable Auto MDI/MDIX |
| | T[1:3] & T[5] | H | Factory test inputs – leave open (float) for normal operation |
| | T[4] | H | F/D = normal operation (default) U = Disable FEF |
| | QH[2:5] | H | Factory test outputs – leave open for normal operation |
| | QL[2:5] | H | Factory test outputs – leave open for normal operation |
| | IO_SWM | H | Factory test input – tie high for normal operation |
| | RLPBK | H | Factory test input – tie low for normal operation |
| | BIST | H | Factory test input – tie low for normal operation |
| PWR | VDD_RX | | 2.0V for equalizer |
| | GND_RX | | Ground for equalizer |
| | VDD_TX | | 2.0V for transmit circuitry |
| | GND_TX | | Ground for transmit circuitry |
| | VDD_RCV | | 2.0V for clock recovery circuitry |
| | GND_RCV | | Ground for clock recovery |
| | VDD_PLLTX | | 2.0V for phase locked loop circuitry |

Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See "Reference Circuits" section.

| Group | I/O Names | Active Status | Description |
|-------|-----------|---------------|--|
| | GND_PLLTX | | Ground for phase locked loop circuitry |
| | GND-ISO | | Analog ground |
| | VDD | | 2.0V for core digital circuitry |
| | VDD-IO | | 2.0V, 2.5V or 3.3V for I/O circuitry |
| | GND | | Ground for digital circuitry |

Pin Configuration



208-Pin PQFP (PQ)

Functional Overview: Physical Layer Transceiver

100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, then transmitted in MLT3 current output. The output current is set by an external 1% 3.01k Ω resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies to the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitters. The wave-shaped 10BaseT output is also incorporated into the 100BaseTX transmitter.

100BaseTX Receive

The 100BaseTX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. This is an ongoing process and can self adjust to the environmental changes such as temperature variations. The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive. The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is provided as the input data to the MAC.

PLL Clock Synthesizer

The KS8999 generates 125MHz, 62.5MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal.

Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled by the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

100BaseFX Operation

100BaseFX operation is very similar to 100BaseTX operation with the differences being that the scrambler/de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

100BaseFX Signal Detection

The physical port runs in 100BaseFX mode if FXSDx > 0.6V. FXSDx is considered 'low' when 0.6V < FXSDx < 1.25V and considered 'high' when FXSDx > 1.25V. If FXSDx goes into 'low' state, the link is considered lost and the link active LED will go off. For FXSDx in the high state, the link is considered active. When FXSDx is below .6V then 100BaseFX mode is disabled. (see application note for detailed information).

100BaseFX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module which occurs when FXSDx is below 1.2V and above 0.6V. When this occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames.

10BaseT Transmit

The output 10BaseT driver is incorporated into the 100BaseT driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude.

10BaseT Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8999 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

Power Save Mode

The KS8999 will turn off everything except for the Energy Detect and PLL circuits when the cable is not installed on an individual port basis. In other words, the KS8999 will shutdown most of the internal circuits to save power if there is no link.

MDI/MDI-X Auto Crossover

The KS8999 supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection.

The auto MDI/MDI-X is achieved by the Micrel device listening for the far end transmission channel and assigning transmit/receive pairs accordingly. Auto MDI/MDI-X can be disabled by pulling the pin 87 (AUTOMDIX) to low.

Auto-Negotiation

The KS8999 conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8999 is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted below.

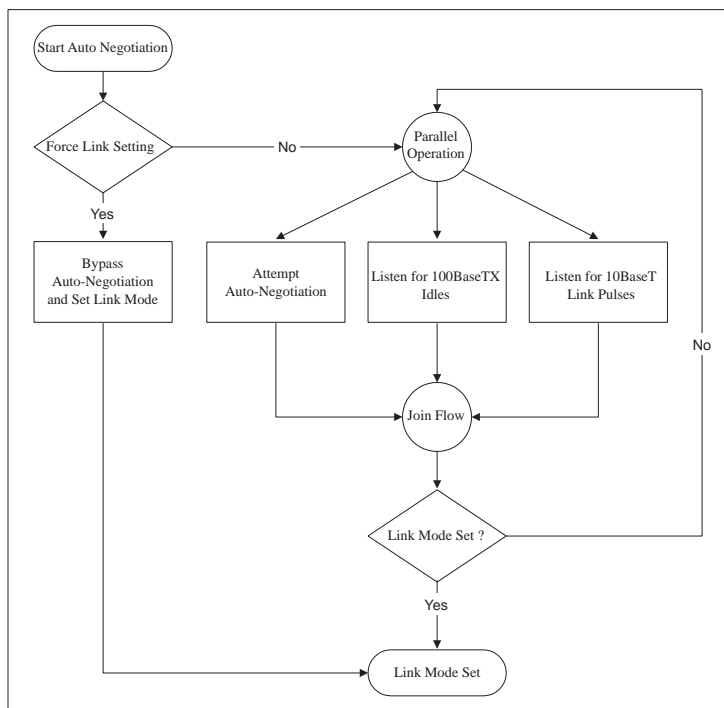


Figure 2. Auto-Negotiation

Functional Overview: Switch Core

Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains 1K full CAM with 48-bit address plus switching information. The KS8999 is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine will update its table with a new entry if the following conditions are met:

- The received packet's SA does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will insert the qualified SA into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If it happens, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will then remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 seconds. This feature can be enabled or disabled by external pull-up or pull-down resistors.

Forwarding

The KS8999 will forward packets as follows:

- If the DA look-up results is a "match", the KS8999 will use the destination port information to determine where the packet goes.
- If the DA look-up result is a "miss", the KS8999 will forward the packet to all other ports except the port that received the packet.
- All the multicast and broadcast packets will be forwarded to all other ports except the source port.

The KS8999 will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KS8999 will intercept these packets and do the appropriate actions.
- "Local" packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as "local".

Switching Engine

The KS8999 has a very high performance switching engine to move data to and from the MAC's, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8999 has an internal buffer for frames that is 32Kx32 (128KB). This resource could be shared between the nine ports and is programmed at system reset time by using the unmanaged program mode (I/O strapping).

Each buffer is sized at 128B and therefore there are a total of 1024 buffers available. Two different modes are available for buffer allocation. One mode equally allocates the buffers to all the ports (113 buffers per port). The other mode adaptively allocates buffers up to 512 to a single port based on loading. Selection is achieved by using LED[7][1] in the unmanaged programming description.

MAC Operation

The KS8999 strictly abides by IEEE 802.3 standard to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bit time IPG is measured from MCRS and the next MTXEN.

Backoff Algorithm

The KS8999 implements the IEEE Std 802.3 binary exponential back-off algorithm, and optional “aggressive mode” back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration.

Late Collision

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet will be dropped.

Illegal Frames

The KS8999 discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes. Since the KS8999 supports VLAN tags, the maximum sizing is adjusted when these tags are present.

Flow Control

The KS8999 supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8999 receives a pause control frame, the KS8999 will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8999 will be transmitted.

On the transmit side, the KS8999 has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8999 will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8999 will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8999 will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent flow control mechanism from being activated and deactivated too many times.

The KS8999 will flow control all ports if the receive queue becomes full.

Half Duplex Back Pressure

Half duplex back pressure option (Note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full duplex mode. If back pressure is required, the KS8999 will send preambles to defer other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

Broadcast Storm Protection

The KS8999 has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus will use too many switch resources (bandwidth and available space in transmit queues). The KS8999 will discard broadcast packets if the number of those packets exceeds the threshold (configured by strapping during reset and EEPROM settings) in a preset period of time. If the preset period expires it will then resume receiving broadcast packets until the threshold is reached. The options are 5% of network line rate for the maximum broadcast receiving threshold or unlimited (feature off).

MII Interface Operation

The MII (Media Independent Interface) operates in either a MAC or PHY mode. In the MAC mode, the KS8999 MII acts like a MAC and in the PHY mode, it acts like a PHY device. This interface is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. There are two distinct groups, one being for transmission and the other for receiving. The table below describes the signals used in this interface in MAC and PHY modes.

| PHY Mode Connection | | Description | MAC Mode Connection | |
|---------------------------------|--------------------|---------------------|----------------------|--------------------|
| External MAC Controller Signals | KS8999 PHY Signals | | External PHY Signals | KS8999 MAC Signals |
| MTXEN | MTXEN | Transmit enable | MTXEN | MRXDV |
| MTXER | MTXER | Transmit error | MTXER | Not used |
| MTXD3 | MTXD[3] | Transmit data bit 3 | MTXD3 | MRXD[3] |
| MTXD2 | MTXD[2] | Transmit data bit 2 | MTXD2 | MRXD[2] |
| MTXD1 | MTXD[1] | Transmit data bit 1 | MTXD1 | MRXD[1] |
| MTXD0 | MTXD[0] | Transmit data bit 0 | MTXD0 | MRXD[0] |
| MTXC | MTXC | Transmit clock | MTXC | MTXC |
| MCOL | MCOL | Collision detection | MCOL | MCOL |
| MCRS | MCRS | Carrier sense | MCRS | MCRS |
| MRXDV | MRXDV | Receive data valid | MRXDV | SMTXEN |
| MRXER | Not used | Receive error | MRXER | MTXER |
| MRXD3 | MRXD[3] | Receive data bit 3 | MRXD3 | MTXD[3] |
| MRXD2 | MRXD[2] | Receive data bit 2 | MRXD2 | MTXD[2] |
| MRXD1 | MRXD[1] | Receive data bit 1 | MRXD1 | MTXD[1] |
| MRXD0 | MRXD[0] | Receive data bit 0 | MRXD0 | MTXD[0] |
| MRXC | MRXC | Receive clock | MRXC | MRXC |

Table 1. MII Signals

This interface is a nibble wide data interface and therefore runs at _ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII interface for the KS8999 for PHY mode operation and MTXER is not represented for MAC mode. Normally this would indicate a receive / transmit error coming from the physical layer /MAC device, but is not appropriate for this configuration. If the connecting device has a MRXER pin, this should be tied low on the other device for reverse or if it has a MTXER pin in the forward mode it should also be tied low on the other device.

The following explains the KS8999 in PHY mode and MAC mode of operation:

KS8999 PHY Mode

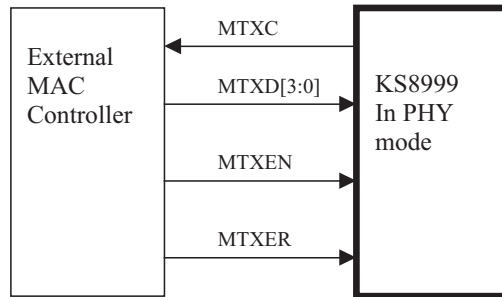


Figure 3. Data Sent from External MAC Controller to KS8999 PHY Mode

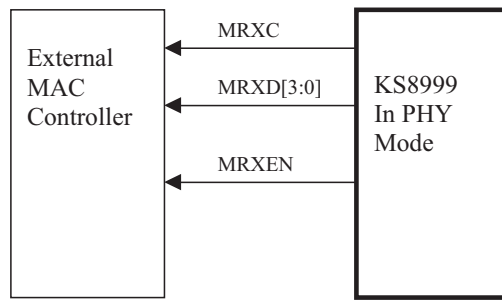


Figure 4. Data Sent from PHY Mode to External MAC Controller

KS8999 MAC Mode

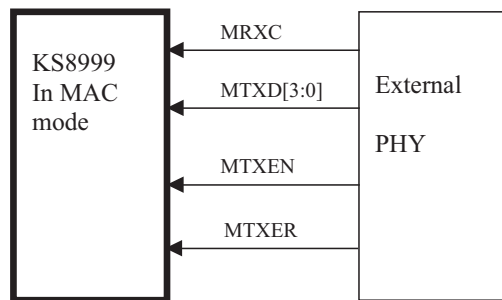


Figure 5. Data Sent from PHY Device to KS8999 MAC Mode

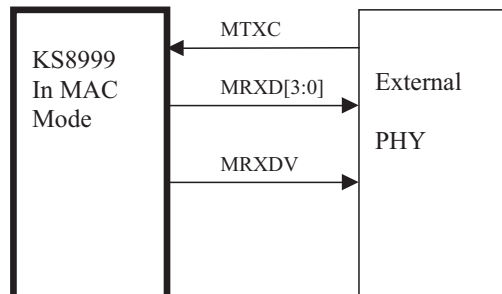


Figure 6. Data Sent from KS8999 PHY Mode to External PHY Device

SNI Interface (7-wire) Operation

The SNI (Serial Network Interface) is compatible with some controllers used for network layer protocol processing. KS8999 acts like a PHY device to external controllers. This interface can be directly connected to these types of devices. The signals are divided into two groups, one being for transmission and the other being the receive side. The signals involved are described in the table below.

| SNI Signal | Description | KS8999 SNI Signal | KS8999 Input/Output |
|------------|----------------------|-------------------|---------------------|
| TXEN | Transmit enable | MTXEN | Input |
| TXD | Serial transmit data | MTXD[0] | Input |
| TXC | Transmit clock | MTXC | Output |
| COL | Collision detection | MCOL | Output |
| CRS | Carrier sense | MRXDV | Output |
| RXD | Serial receive data | MRXD[0] | Output |
| RXC | Receive clock | MRXC | Output |

Table 2. SNI Signals

This interface is a bit wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that conveys when the data is valid. For half-duplex operation there is a signal that indicate a collision has occurred during transmission.

Programmable Features

Priority Schemes

The KS8999 can determine priority through three different means at the ingress point. The first method is a simple per port method, the second is via the 802.1p frame tag and the third is by viewing the DSCP (TOS) field in the IPv4 header. Of course for the priority to be effective, the high and low priority queues must be enabled on the destination port or egress point.

Per Port Method

General priority can be specified on a per port basis. In this type of priority all traffic from the specified input port is considered high priority in the destination queue. This can be useful in IP phone applications mixed with other data types of traffic where the IP phone connects to a specific port. The IP phone traffic would be high priority (outbound) to the wide area network. The inbound traffic to the IP phone is all of the same priority to the IP phone.

802.1p Method

This method works well when used with ports that have mixed data and media flows. The inbound port examines the priority field in the tag and determines the high or low priority. Priority profiles are setup in the Priority Classification Control in the EEPROM.

IPv4 DSCP Method

This is another per frame way of determining outbound priority. The DSCP (Differentiated Services Code Point – RFC#2474) method uses the TOS field in the IP header to determine high and low priority on a per code point basis. Each fully decoded code point can have either a high or low priority. A larger spectrum of priority flows can be defined with this larger code space. More specific to implementation, the most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high and if 0, the priority is low.

Other Priority Considerations

When setting up the priority scheme, one should consider other available controls to regulate the traffic. One of these is Priority Control Scheme (register 2 bits 2-3) which controls the interleaving of high and low priority frames. Options allow from a 2:1 ratio up to a setting that sends all the high priority first. This setting controls all ports globally. Another global feature is Priority Buffer Reserve (register 2 bit 1). If this is set, there is a 6KB (10%) buffer dedicated to high priority traffic, otherwise if cleared the buffer is shared between all traffic.

On an individual port basis there are controls that enable DSCP, 802.1p, port based and high/low priority queues. These are contained in registers 4-12 bits 5-3 and 0. It should be noted that there is a special pin that generally enables the 802.1p priority for all ports (pin 91). When this pin is active (high) all ports will have the 802.1p priority enabled unless specifically disabled by EEPROM programming (bit 4 of registers 4-12). Default high priority is a value greater than 4 in the VLAN tag with low priority being 3 or less.

The table below briefly summarizes priority features. For more detailed settings see the EEPROM register description.

| Register(s) | Bit(s) | Global/Port | Description |
|-------------|--------|-------------|--|
| | | | General |
| 2 | 3-2 | Global | Priority Control Scheme: Transmit buffer high/low interleave control |
| 2 | 1 | Global | Priority Buffer Reserve: Reserves 6KB of the buffer for high priority traffic |
| 4-12 | 0 | Port | Enable Port Queue Split: Splits the transmit queue on the desired port for high and low priority traffic |
| | | | DSCP Priority |
| 4-12 | 5 | Port | Enable Port DSCP: Looks at DSCP field in IP header to decide high or low priority |
| 40-47 | 7-0 | Global | DSCP Priority Points: Fully decoded 64 bit register used to determine priority from DSCP field (6 bits) in the IP header |
| | | | 802.1p Priority |
| 4-12 | 4 | Port | Enable Port 802.1p Priority: Uses the 802.1p priority tag (3 bits) to determine frame priority |
| 3 | 7-0 | Global | Priority Classification: Determines which tag values have high priority |
| | | | Per Port Priority |
| 4-12 | 3 | Port | Enable Port Priority: Determines which ports have high or low priority traffic |

Table 3. Priority Control

VLAN Operation

The VLAN's are setup by programming the VLAN Mask Registers in the EEPROM. The perspective of the VLAN is from the input port and which output ports it sees directly through the switch. For example if port 1 only participated in a VLAN with ports 2 and 9 then one would set bits 0 and 7 in register 13 (Port 1 VLAN Mask Register). Note that different ports can be setup independently. An example of this would be where a router is connected to port 9 and each of the other ports would work autonomously. In this configuration ports 1 through 8 would only set the mask for port 9 and port 9 would set the mask for ports 1 through 8. In this way, the router could see all ports and each of the other individual ports would only communicate with the router.

All multicast and broadcast frames adhere to the VLAN configuration. Unicast frame treatment is a function of register 2 bit 0. If this bit is set then unicast frames only see ports within their VLAN. If this bit is cleared unicast frames can traverse VLAN's. VLAN tags can be added or removed on a per port basis. Further, there are provisions to specify the tag value to be inserted on a per port basis.

The table below briefly summarizes VLAN features. For more detailed settings see the EEPROM register description.

| Register(s) | Bit(s) | Global/Port | Description |
|-------------|--------|-------------|---|
| 4-12 | 2 | Port | Insert VLAN Tags: If specified, will add VLAN tags to frames without existing tags |
| 4-12 | 1 | Port | Strip VLAN Tags: If specified, will remove VLAN tags from frames if they exist |
| 2 | 0 | Global | VLAN Enforcement: Allows unicast frames to adhere or ignore the VLAN configuration |
| 13-21 | 7-0 | Port | VLAN Mask Registers: Allows configuration of individual VLAN grouping. |
| 22-39 | 7-0 | Port | VLAN Tag Insertion Values: Specifies the VLAN tag to be inserted if enabled (see above) |

Table 4. VLAN Control

Station MAC Address (control frames only)

The MAC source address can be programmed as used in flow control frames. The table below briefly summarizes this programmable feature.

| Register(s) | Bit(s) | Global/Port | Description |
|-------------|--------|-------------|--|
| 48-53 | 7-0 | Global | Station MAC Address: Used as source address for MAC control frames as used in full duplex flow control mechanisms. |

Table 5. Misc. Control

EEPROM Operation

The EEPROM interface utilizes 2 pins that provide a clock and a serial data path. As part of the initialization sequence, the KS8999 reads the contents of the EEPROM and loads the values into the appropriate registers. Note that the first two bytes in the EEPROM must be “55” and “99” respectively for the loading to occur properly. If these first two values are not correct, all other data will be ignored.

Data start and stop conditions are signaled on the data line as a state transition during clock high time. A high to low transition indicates start of data and a low to high transition indicates a stop condition. The actual data that traverses the serial line changes during the clock low time.

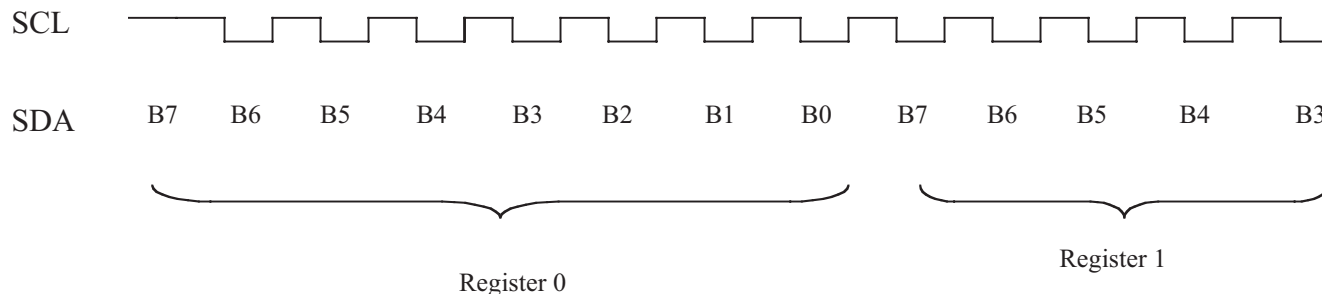
The KS8999 EEPROM interface is compatible with the Atmel AT24C01A part. Address A0, A1 and A2 are fixed to 000. Further timing and data sequences can be found in the Atmel AT24C01A specification.

Optional CPU Interface

Instead of using an EEPROM to program the KS8999, one can use an external processor. To utilize this feature, the CFGMODE pin (only available on the 208 pin package) needs to be pulled low. This makes the KS8999 serial and clock interface into a slave rather than a master. In this mode, clock and data are sourced from the processor.

Due to timing constraints, the maximum clock speed that the processor can generate is 8MHz. Data timing is referenced to the rising edge of the clock and are 10ns for setup and 60ns for hold. The processor needs to supply the exact number of clock cycles and data bits to program the KS8999 properly. KS8999 won't start until all of the registers are programmed. Bits are loaded from high order (bit 7) to low order (bit 0) starting with register 0 and finishing with register 53.

| | | |
|----------------------------|---------------------------------|----------------------------|
| Register 0: | Skip clock on first bit 7 | SCL clock cycle: 7 |
| Register 1 to Register 53: | provide clock on bit 7 to bit 0 | SCL clock cycle: 424 |
| | | Total SCL clock cycle: 431 |



EEPROM Memory Map

| Address | Name | Description | Default (chip) Value |
|---|------|---|----------------------|
| 0 | 7-0 | Signature byte 1. Value = "55" | 0x55 |
| 1 | 7-0 | Signature byte 2. Value = "99" | 0x99 |
| General Control Register | | | |
| 2 | 7-4 | Reserved – set to zero | 0000 |
| 2 | 3-2 | Priority control scheme (all ports) 00 = Transmit all high priority before any low priority 01 = Transmit high and low priority at a 10:1 ratio 10 = Transmit high and low priority at a 5:1 ratio 11 = Transmit high and low priority at a 2:1 ratio | 00 |
| 2 | 1 | Priority buffer reserve for high priority traffic 1 = Reserve 6KB of buffer space for high priority 0 = None reserved | 0 |
| 2 | 0 | VLAN enforcement 1 = All unicast frames adhere to VLAN configuration 0 = Unicast frames ignore VLAN configuration | 0 |
| Priority Classification Control – 802.1p tag field | | | |
| 3 | 7 | 1 = State "111" is high priority 0 = State "111" is low priority | 1 |
| 3 | 6 | 1 = State "110" is high priority 0 = State "110" is low priority | 1 |
| 3 | 5 | 1 = State "101" is high priority 0 = State "101" is low priority | 1 |
| 3 | 4 | 1 = State "100" is high priority 0 = State "100" is low priority | 1 |
| 3 | 3 | 1 = State "011" is high priority 0 = State "011" is low priority | 0 |
| 3 | 2 | 1 = State "010" is high priority 0 = State "010" is low priority | 0 |
| 3 | 1 | 1 = State "001" is high priority 0 = State "001" is low priority | 0 |
| 3 | 0 | 1 = State "000" is high priority 0 = State "000" is low priority | 0 |
| Port 1 Control Register | | | |
| 4 | 7-6 | Reserved – set to zero | 00 |
| 4 | 5 | TOS priority classification enable for port 1 1 = Enable 0 = Disable | 0 |
| 4 | 4 | 802.1p priority classification enable for port 1 1 = Enable 0 = Disable | 0 |
| 4 | 3 | Port based priority classification for port 1 1 = High priority 0 = Low priority | 0 |
| 4 | 2 | Insert VLAN tags for port 1 if non-existent 1 = Enable 0 = Disable | 0 |
| 4 | 1 | Strip VLAN tags for port 1 if existent 1 = Enable 0 = Disable | 0 |

| Address | Name | Description | Default (chip) Value |
|--------------------------------|------|--|----------------------|
| 4 | 0 | Enable high and low output priority queues for port 1 1 = Enable 0 = Disable | 0 |
| Port 2 Control Register | | | |
| 5 | 7-6 | Reserved – set to zero | 00 |
| 5 | 5 | TOS priority classification enable for port 2 1 = Enable 0 = Disable | 0 |
| 5 | 4 | 802.1p priority classification enable for port 2 1 = Enable 0 = Disable | 0 |
| 5 | 3 | Port based priority classification for port 2 1 = High priority 0 = Low priority | 0 |
| 5 | 2 | Insert VLAN tags for port 2 if non-existent 1 = Enable 0 = Disable | 0 |
| 5 | 1 | Strip VLAN tags for port 2 if existent 1 = Enable 0 = Disable | 0 |
| 5 | 0 | Enable high and low output priority queues for port 2 1 = Enable 0 = Disable | 0 |
| Port 3 Control Register | | | |
| 6 | 7-6 | Reserved – set to zero | 00 |
| 6 | 5 | TOS priority classification enable for port 3 1 = Enable 0 = Disable | 0 |
| 6 | 4 | 802.1p priority classification enable for port 3 1 = Enable 0 = Disable | 0 |
| 6 | 3 | Port based priority classification for port 3 1 = High priority 0 = Low priority | 0 |
| 6 | 2 | Insert VLAN tags for port 3 if non-existent 1 = Enable 0 = Disable | 0 |
| 6 | 1 | Strip VLAN tags for port 3 if existent 1 = Enable 0 = Disable | 0 |
| 6 | 0 | Enable high and low output priority queues for port 3 1 = Enable 0 = Disable | 0 |
| Port 4 Control Register | | | |
| 7 | 7-6 | Reserved – set to zero | 00 |
| 7 | 5 | TOS priority classification enable for port 4 1 = Enable 0 = Disable | 0 |
| 7 | 4 | 802.1p priority classification enable for port 4 1 = Enable 0 = Disable | 0 |

| Address | Name | Description | Default (chip) Value |
|--------------------------------|------|--|----------------------|
| 7 | 3 | Port based priority classification for port 4 1 = High priority 0 = Low priority | 0 |
| 7 | 2 | Insert VLAN tags for port 4 if non-existent 1 = Enable 0 = Disable | 0 |
| 7 | 1 | Strip VLAN tags for port 4 if existent 1 = Enable 0 = Disable | 0 |
| 7 | 0 | Enable high and low output priority queues for port 4 1 = Enable 0 = Disable | 0 |
| Port 5 Control Register | | | |
| 8 | 7-6 | Reserved – set to zero | 00 |
| 8 | 5 | TOS priority classification enable for port 5 1 = Enable 0 = Disable | 0 |
| 8 | 4 | 802.1p priority classification enable for port 5 1 = Enable 0 = Disable | 0 |
| 8 | 3 | Port based priority classification for port 5 1 = High priority 0 = Low priority | 0 |
| 8 | 2 | Insert VLAN tags for port 5 if non-existent 1 = Enable 0 = Disable | 0 |
| 8 | 1 | Strip VLAN tags for port 5 if existent 1 = Enable 0 = Disable | 0 |
| 8 | 0 | Enable high and low output priority queues for port 5 1 = Enable 0 = Disable | 0 |
| Port 6 Control Register | | | |
| 9 | 7-6 | Reserved – set to zero | 00 |
| 9 | 5 | TOS priority classification enable for port 6 1 = Enable 0 = Disable | 0 |
| 9 | 4 | 802.1p priority classification enable for port 6 1 = Enable 0 = Disable | 0 |
| 9 | 3 | Port based priority classification for port 6 1 = High priority 0 = Low priority | 0 |
| 9 | 2 | Insert VLAN tags for port 6 if non-existent 1 = Enable 0 = Disable | 0 |
| 9 | 1 | Strip VLAN tags for port 6 if existent 1 = Enable 0 = Disable | 0 |
| 9 | 0 | Enable high and low output priority queues for port 6 1 = Enable 0 = Disable | 0 |

| Address | Name | Description | Default (chip) Value |
|--------------------------------|------|--|----------------------|
| Port 7 Control Register | | | |
| 10 | 7-6 | Reserved – set to zero | 00 |
| 10 | 5 | TOS priority classification enable for port 7 1 = Enable 0 = Disable | 0 |
| 10 | 4 | 802.1p priority classification enable for port 7 1 = Enable 0 = Disable | 0 |
| 10 | 3 | Port based priority classification for port 7 1 = High priority 0 = Low priority | 0 |
| 10 | 2 | Insert VLAN tags for port 7 if non-existent 1 = Enable 0 = Disable | 0 |
| 10 | 1 | Strip VLAN tags for port 7 if existent 1 = Enable 0 = Disable | 0 |
| 10 | 0 | Enable high and low output priority queues for port 7 1 = Enable 0 = Disable | 0 |
| Port 8 Control Register | | | |
| 11 | 7-6 | Reserved – set to zero | 00 |
| 11 | 5 | TOS priority classification enable for port 8 1 = Enable 0 = Disable | 0 |
| 11 | 4 | 802.1p priority classification enable for port 8 1 = Enable 0 = Disable | 0 |
| 11 | 3 | Port based priority classification for port 8 1 = High priority 0 = Low priority | 0 |
| 11 | 2 | Insert VLAN tags for port 8 if non-existent 1 = Enable 0 = Disable | 0 |
| 11 | 1 | Strip VLAN tags for port 8 if existent 1 = Enable 0 = Disable | 0 |
| 11 | 0 | Enable high and low output priority queues for port 8 1 = Enable 0 = Disable | 0 |
| Port 9 Control Register | | | |
| 12 | 7-6 | Reserved – set to zero | 00 |
| 12 | 5 | TOS priority classification enable for port 9 1 = Enable 0 = Disable | 0 |
| 12 | 4 | 802.1p priority classification enable for port 9 1 = Enable 0 = Disable | 0 |
| 12 | 3 | Port based priority classification for port 9 1 = High priority 0 = Low priority | 0 |

| Address | Name | Description | Default (chip) Value |
|----------------------------------|------|--|----------------------|
| 12 | 2 | Insert VLAN tags for port 9 if non-existent 1 = Enable 0 = Disable | 0 |
| 12 | 1 | Strip VLAN tags for port 9 if existent 1 = Enable 0 = Disable | 0 |
| 12 | 0 | Enable high and low output priority queues for port 9 1 = Enable 0 = Disable | 0 |
| Port 1 VLAN Mask Register | | | |
| 13 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 1 0 = Port 9 not in the same VLAN as port 1 | 1 |
| 13 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 1 0 = Port 8 not in the same VLAN as port 1 | 1 |
| 13 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 1 0 = Port 7 not in the same VLAN as port 1 | 1 |
| 13 | 4 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 1 0 = Port 6 not in the same VLAN as port 1 | 1 |
| 13 | 3 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 1 0 = Port 5 not in the same VLAN as port 1 | 1 |
| 13 | 2 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 1 0 = Port 4 not in the same VLAN as port 1 | 1 |
| 13 | 1 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 1 0 = Port 3 not in the same VLAN as port 1 | 1 |
| 13 | 0 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 1 0 = Port 2 not in the same VLAN as port 1 | 1 |
| Port 2 VLAN Mask Register | | | |
| 14 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 2 0 = Port 9 not in the same VLAN as port 2 | 1 |
| 14 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 2 0 = Port 8 not in the same VLAN as port 2 | 1 |
| 14 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 2 0 = Port 7 not in the same VLAN as port 2 | 1 |
| 14 | 4 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 2 0 = Port 6 not in the same VLAN as port 2 | 1 |
| 14 | 3 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 2 0 = Port 5 not in the same VLAN as port 2 | 1 |
| 14 | 2 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 2 0 = Port 4 not in the same VLAN as port 2 | 1 |

| Address | Name | Description | Default (chip) Value |
|----------------------------------|------|--|----------------------|
| 14 | 1 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 2 0 = Port 3 not in the same VLAN as port 2 | 1 |
| 14 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 2 0 = Port 1 not in the same VLAN as port 2 | 1 |
| Port 3 VLAN Mask Register | | | |
| 15 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 3 0 = Port 9 not in the same VLAN as port 3 | 1 |
| 15 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 3 0 = Port 8 not in the same VLAN as port 3 | 1 |
| 15 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 3 0 = Port 7 not in the same VLAN as port 3 | 1 |
| 15 | 4 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 3 0 = Port 6 not in the same VLAN as port 3 | 1 |
| 15 | 3 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 3 0 = Port 5 not in the same VLAN as port 3 | 1 |
| 15 | 2 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 3 0 = Port 4 not in the same VLAN as port 3 | 1 |
| 15 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 3 0 = Port 2 not in the same VLAN as port 3 | 1 |
| 15 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 3 0 = Port 1 not in the same VLAN as port 3 | 1 |
| Port 4 VLAN Mask Register | | | |
| 16 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 4 0 = Port 9 not in the same VLAN as port 4 | 1 |
| 16 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 4 0 = Port 8 not in the same VLAN as port 4 | 1 |
| 16 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 4 0 = Port 7 not in the same VLAN as port 4 | 1 |
| 16 | 4 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 4 0 = Port 6 not in the same VLAN as port 4 | 1 |
| 16 | 3 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 4 0 = Port 5 not in the same VLAN as port 4 | 1 |
| 16 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 4 0 = Port 3 not in the same VLAN as port 4 | 1 |
| 16 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 4 0 = Port 2 not in the same VLAN as port 4 | 1 |

| Address | Name | Description | Default (chip) Value |
|----------------------------------|------|--|----------------------|
| 16 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 4 0 = Port 1 not in the same VLAN as port 4 | 1 |
| Port 5 VLAN Mask Register | | | |
| 17 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 5 0 = Port 9 not in the same VLAN as port 5 | 1 |
| 17 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 5 0 = Port 8 not in the same VLAN as port 5 | 1 |
| 17 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 5 0 = Port 7 not in the same VLAN as port 5 | 1 |
| 17 | 4 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 5 0 = Port 6 not in the same VLAN as port 5 | 1 |
| 17 | 3 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 5 0 = Port 4 not in the same VLAN as port 5 | 1 |
| 17 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 5 0 = Port 3 not in the same VLAN as port 5 | 1 |
| 17 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 5 0 = Port 2 not in the same VLAN as port 5 | 1 |
| 17 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 5 0 = Port 1 not in the same VLAN as port 5 | 1 |
| Port 6 VLAN Mask Register | | | |
| 18 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 6 0 = Port 9 not in the same VLAN as port 6 | 1 |
| 18 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 6 0 = Port 8 not in the same VLAN as port 6 | 1 |
| 18 | 5 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 6 0 = Port 7 not in the same VLAN as port 6 | 1 |
| 18 | 4 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 6 0 = Port 5 not in the same VLAN as port 6 | 1 |
| 18 | 3 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 6 0 = Port 4 not in the same VLAN as port 6 | 1 |
| 18 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 6 0 = Port 3 not in the same VLAN as port 6 | 1 |
| 18 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 6 0 = Port 2 not in the same VLAN as port 6 | 1 |
| 18 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 6 0 = Port 1 not in the same VLAN as port 6 | 1 |

| Address | Name | Description | Default (chip) Value |
|----------------------------------|------|--|----------------------|
| Port 7 VLAN Mask Register | | | |
| 19 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 7 0 = Port 9 not in the same VLAN as port 7 | 1 |
| 19 | 6 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 7 0 = Port 8 not in the same VLAN as port 7 | 1 |
| 19 | 5 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 7 0 = Port 6 not in the same VLAN as port 7 | 1 |
| 19 | 4 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 7 0 = Port 5 not in the same VLAN as port 7 | 1 |
| 19 | 3 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 7 0 = Port 4 not in the same VLAN as port 7 | 1 |
| 19 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 7 0 = Port 3 not in the same VLAN as port 7 | 1 |
| 19 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 7 0 = Port 2 not in the same VLAN as port 7 | 1 |
| 19 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 7 0 = Port 1 not in the same VLAN as port 7 | 1 |
| Port 8 VLAN Mask Register | | | |
| 20 | 7 | Port 9 inclusion 1 = Port 9 in the same VLAN as port 8 0 = Port 9 not in the same VLAN as port 8 | 1 |
| 20 | 6 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 8 0 = Port 7 not in the same VLAN as port 8 | 1 |
| 20 | 5 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 8 0 = Port 6 not in the same VLAN as port 8 | 1 |
| 20 | 4 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 8 0 = Port 5 not in the same VLAN as port 8 | 1 |
| 20 | 3 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 8 0 = Port 4 not in the same VLAN as port 8 | 1 |
| 20 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 8 0 = Port 3 not in the same VLAN as port 8 | 1 |
| 20 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 8 0 = Port 2 not in the same VLAN as port 8 | 1 |
| 20 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 8 0 = Port 1 not in the same VLAN as port 8 | 1 |

| Address | Name | Description | Default (chip) Value |
|--|------|--|----------------------|
| Port 9 VLAN Mask Register | | | |
| 21 | 7 | Port 8 inclusion 1 = Port 8 in the same VLAN as port 9 0 = Port 8 not in the same VLAN as port 9 | 1 |
| 21 | 6 | Port 7 inclusion 1 = Port 7 in the same VLAN as port 9 0 = Port 7 not in the same VLAN as port 9 | 1 |
| 21 | 5 | Port 6 inclusion 1 = Port 6 in the same VLAN as port 9 0 = Port 6 not in the same VLAN as port 9 | 1 |
| 21 | 4 | Port 5 inclusion 1 = Port 5 in the same VLAN as port 9 0 = Port 5 not in the same VLAN as port 9 | 1 |
| 21 | 3 | Port 4 inclusion 1 = Port 4 in the same VLAN as port 9 0 = Port 4 not in the same VLAN as port 9 | 1 |
| 21 | 2 | Port 3 inclusion 1 = Port 3 in the same VLAN as port 9 0 = Port 3 not in the same VLAN as port 9 | 1 |
| 21 | 1 | Port 2 inclusion 1 = Port 2 in the same VLAN as port 9 0 = Port 2 not in the same VLAN as port 9 | 1 |
| 21 | 0 | Port 1 inclusion 1 = Port 1 in the same VLAN as port 9 0 = Port 1 not in the same VLAN as port 9 | 1 |
| Port 1 VLAN Tag Insertion Value Registers | | | |
| 22 | 7-5 | User priority [2:0] | 000 |
| 22 | 4 | CFI | 0 |
| 22 | 3-0 | VID [11:8] | 0x0 |
| 23 | 7-0 | VID [7:0] | 0x00 |
| Port 2 VLAN Tag Insertion Value Registers | | | |
| 24 | 7-5 | User priority [2:0] | 000 |
| 24 | 4 | CFI | 0 |
| 24 | 3-0 | VID [11:8] | 0x0 |
| 25 | 7-0 | VID [7:0] | 0x00 |
| Port 3 VLAN Tag Insertion Value Registers | | | |
| 26 | 7-5 | User priority [2:0] | 000 |
| 26 | 4 | CFI | 0 |
| 26 | 3-0 | VID [11:8] | 0x0 |
| 27 | 7-0 | VID [7:0] | 0x00 |
| Port 4 VLAN Tag Insertion Value Registers | | | |
| 28 | 7-5 | User priority [2:0] | 000 |
| 28 | 4 | CFI | 0 |
| 28 | 3-0 | VID [11:8] | 0x0 |
| 29 | 7-0 | VID [7:0] | 0x00 |

| Address | Name | Description | Default (chip) Value |
|--|------|---------------------|----------------------|
| Port 5 VLAN Tag Insertion Value Registers | | | |
| 30 | 7-5 | User priority [2:0] | 000 |
| 30 | 4 | CFI | 0 |
| 30 | 3-0 | VID [11:8] | 0x0 |
| 31 | 7-0 | VID [7:0] | 0x00 |
| Port 6 VLAN Tag Insertion Value Registers | | | |
| 32 | 7-5 | User priority [2:0] | 000 |
| 32 | 4 | CFI | 0 |
| 32 | 3-0 | VID [11:8] | 0x0 |
| 33 | 7-0 | VID [7:0] | 0x00 |
| Port 7 VLAN Tag Insertion Value Registers | | | |
| 34 | 7-5 | User priority [2:0] | 000 |
| 34 | 4 | CFI | 0 |
| 34 | 3-0 | VID [11:8] | 0x0 |
| 35 | 7-0 | VID [7:0] | 0x00 |
| Port 8 VLAN Tag Insertion Value Registers | | | |
| 36 | 7-5 | User priority [2:0] | 000 |
| 36 | 4 | CFI | 0 |
| 36 | 3-0 | VID [11:8] | 0x0 |
| 37 | 7-0 | VID [7:0] | 0x00 |
| Port 9 VLAN Tag Insertion Value Registers | | | |
| 38 | 7-5 | User priority [2:0] | 000 |
| 38 | 4 | CFI | 0 |
| 38 | 3-0 | VID [11:8] | 0x0 |
| 39 | 7-0 | VID [7:0] | 0x00 |
| Diff Serv Code Point Registers | | | |
| 40 | 7-0 | DSCP[63:56] | 0x00 |
| 41 | 7-0 | DSCP[55:48] | 0x00 |
| 42 | 7-0 | DSCP[47:40] | 0x00 |
| 43 | 7-0 | DSCP[39:32] | 0x00 |
| 44 | 7-0 | DSCP[31:24] | 0x00 |
| 45 | 7-0 | DSCP[23:16] | 0x00 |
| 46 | 7-0 | DSCP[15:8] | 0x00 |
| 47 | 7-0 | DSCP[7:0] | 0x00 |
| Station MAC Address Registers (all ports – MAC control frames only) | | | |
| 48 | 7-0 | MAC address [47:40] | 0x00 |
| 49 | 7-0 | MAC address [39:32] | 0x40 |
| 50 | 7-0 | MAC address [31:24] | 0x05 |
| 51 | 7-0 | MAC address [23:16] | 0x43 |
| 52 | 7-0 | MAC address [15:8] | 0x5E |
| 53 | 7-0 | MAC address [7:0] | 0xFE |

Note: The MAC address is reset to the value in the above table, but can set to any value via the EEPROM interface. This MAC address is used as the source address in MAC control frames that execute flow control between link peers.

Absolute Maximum Ratings (Note 1)

| | | |
|---|-------|-----------------|
| Supply Voltage (V_{DD_RX} , V_{DD_TX} , V_{DD_RCV} , V_{DD} , V_{DD_PLLTX}) | | -0.5V to +2.3V |
| (V_{DDIO}) | | -0.5V to +3.8V |
| Input Voltage | | -0.5V to +4.0V |
| Output Voltage | | -0.5V to +4.0V |
| Lead Temperature (soldering, 10 sec.) | | 270°C |
| Storage Temperature (T_S) | | -55°C to +150°C |

Operating Ratings (Note 2)

| | | |
|---|-------|----------------------------------|
| Supply Voltage (V_{DD_RX} , V_{DD_TX} , V_{DD_RCV} , V_{DD} , V_{DD_PLLTX}) | | +2.0V to +2.3V |
| (V_{DDIO}) | | +2.0V to +2.3V or +3.0V to +3.6V |
| Ambient Temperature (T_A) Commercial | | -0°C to +70°C |
| Industrial | | -40°C to +85°C |
| Package Thermal Resistance, (Note 3) PQFP (θ_{JA}) No Air Flow | | 39.1°C/W |

Electrical Characteristics (KS8999) (Note 4)

$V_{DD} = 2.0V$ to $2.3V$; $T_A = 0^\circ C$ to $+70^\circ C$; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|----------------|-----------|------|------|------|-------|
| V_{DD} | Supply Voltage | | 2.00 | 2.10 | 2.30 | V |

Supply Current (including TX output driver current)

| 100BaseTX Operation—Total | | | | 0.64 | 0.85 | A |
|---------------------------|-------------------------|--|--|------|------|---|
| I_{DX} | 100BaseTX (Transmitter) | | | 0.35 | 0.40 | A |
| I_{DA} | 100BaseTX (Analog) | | | 0.18 | 0.25 | A |
| I_{DD} | 100BaseTX (Digital) | | | 0.11 | 0.20 | A |
| 10BaseT Operation—Total | | | | 1.04 | 1.32 | A |
| I_{DX} | 100BaseTX (Transmitter) | | | 0.84 | 0.95 | A |
| I_{DA} | 100BaseTX (Analog) | | | 0.11 | 0.17 | A |
| I_{DD} | 100BaseTX (Digital) | | | 0.09 | 0.20 | A |

TTL Inputs

| | | | | | | |
|----------|--------------------|----------------------------|--------------------------|--|--------------------------|---------|
| V_{IH} | Input High Voltage | | $(1/2 V_{DDIO})$ +0.4 | | | V |
| V_{IL} | Input Low Voltage | | | | $(1/2 V_{DDIO})$ -0.4 | V |
| I_{IN} | Input Current | $V_{IN} = GND \sim V_{DD}$ | -10 | | 10 | μA |

TTL Outputs

| | | | | | | |
|------------|--------------------------|-----------------|--------------------|--|------|---------|
| V_{OH} | Output High Voltage | $I_{OH} = -4mA$ | V_{DDIO} -0.4 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 4mA$ | | | +0.4 | V |
| $ I_{OZ} $ | Output Tri-State Leakage | | | | 10 | μA |

100BaseTX Transmit (measured differentially after 1:1 transformer)

| | | | | | | |
|------------|----------------------------------|--|------|--|------|----|
| V_O | Peak Differential Output Voltage | 50 Ω from each output to V_{DD} | 0.95 | | 1.05 | V |
| V_{IMB} | Output Voltage Imbalance | 50 Ω from each output to V_{DD} | | | 2 | % |
| t_r, t_f | Rise/Fall Time | | 3 | | 5 | ns |
| | Rise/Fall Time Imbalance | | 0 | | 0.5 | ns |

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).

Note 3. No HS (heat spreader) in package.

Note 4. Specification for packaged product only.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|----------------------------------|---|-----|------|------|-------|
| 100BaseTX Transmit (measured differentially after 1:1 transformer) | | | | | | |
| | Duty Cycle Distortion | | | | ±0.5 | ns |
| | Overshoot | | | | 5 | % |
| V _{SET} | Reference Voltage of ISET | | | 0.75 | | V |
| | Output Jitters | Peak-to-peak | | 0.7 | 1.4 | ns |
| 10BaseTX Receive | | | | | | |
| V _{SQ} | Squelch Threshold | 5MHz square wave | | 400 | | mV |
| 10BaseT Transmit (measured differentially after 1:1 transformer) | | | | | | |
| V _P | Peak Differential Output Voltage | 50Ω from each output to V _{DD} | | 2.3 | | V |
| | Jitters Added | 50Ω from each output to V _{DD} | | | ±3.5 | ns |
| | Rise/Fall Times | | | 28 | | ns |

Timing Diagrams

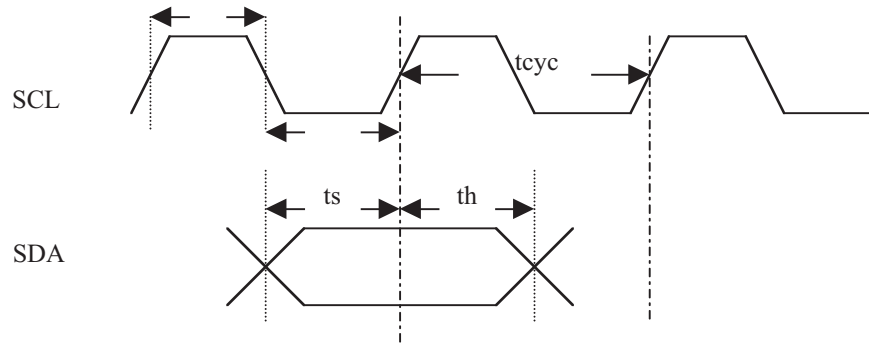


Figure 7. EEPROM Input Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|-------------|-----|-------|-----|-------|
| t_{CYC} | Clock Cycle | | 16384 | | ns |
| t_S | Set-Up Time | 20 | | | ns |
| t_H | Hold Time | 20 | | | ns |

Table 5. EEPROM Input Timing Parameters

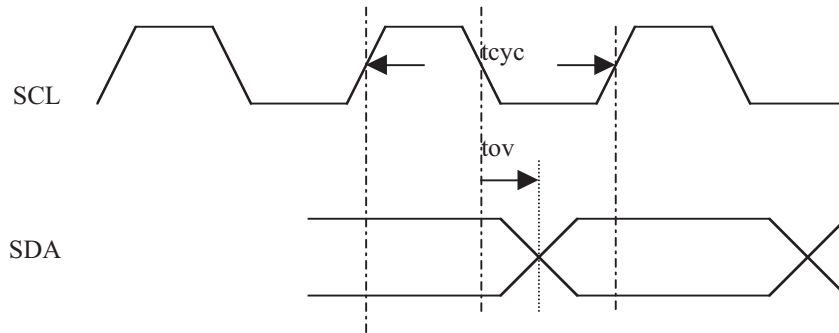


Figure 8. EEPROM Output Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|--------------|------|-------|------|-------|
| t_{CYC} | Clock Cycle | | 16384 | | ns |
| t_{OV} | Output Valid | 4096 | 4112 | 4128 | ns |

Table 6. EEPROM Output Timing Parameters

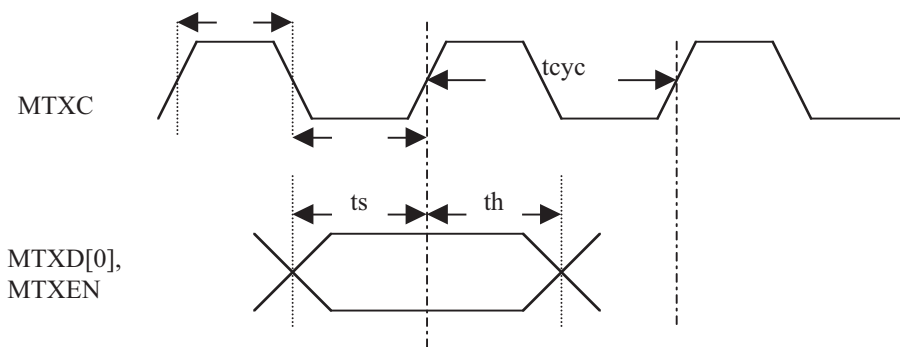


Figure 9. SNI (7-wire) Input Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|-------------|-----|-----|-----|-------|
| t_{cyc} | Clock Cycle | | 100 | | ns |
| t_s | Set-Up Time | 10 | | | ns |
| t_h | Hold Time | 0 | | | ns |

Table 7. SNI (7-wire) Input Parameters

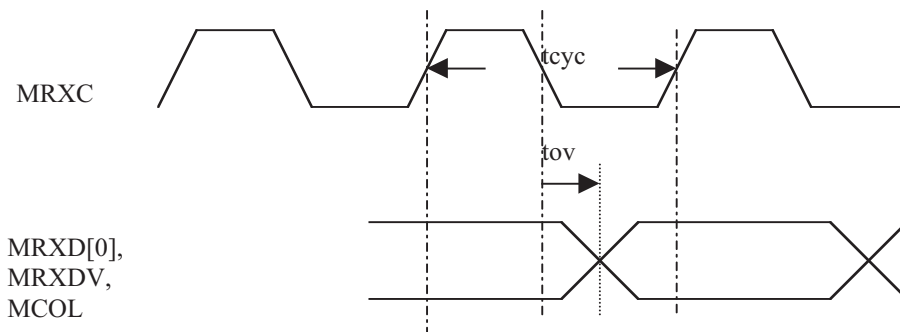


Figure 10. SNI (7-wire) Output Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|--------------|-----|-----|-----|-------|
| t_{cyc} | Clock Cycle | | 100 | | ns |
| t_{ov} | Output Valid | 0 | 3 | 6 | ns |

Table 8. SNI (7-wire) Output Timing Parameters

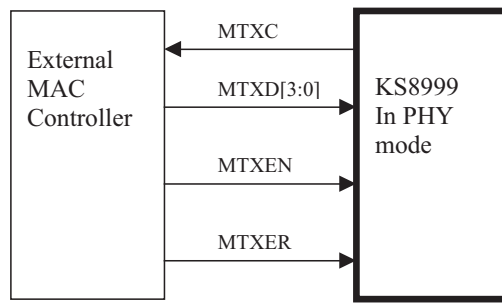


Figure 11. KS8999 PHY Mode—Data Sent from External MAC Controller to KS8999

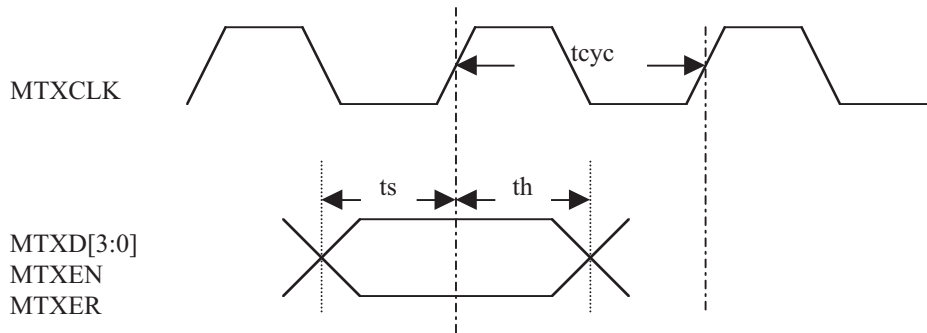


Figure 12. KS8999 PHY Mode Receive Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|-------|
| t_{CYC} | Clock Cycle (100BaseT) | | 40 | | ns |
| t_{CYC} | Clock Cycle (10BaseT) | | 400 | | ns |
| t_s | Set-Up Time | 10 | | | ns |
| t_H | Hold Time | 0 | | | ns |

Table 9. MII Timing in KS8999 PHY and MAC Mode Timing Parameters

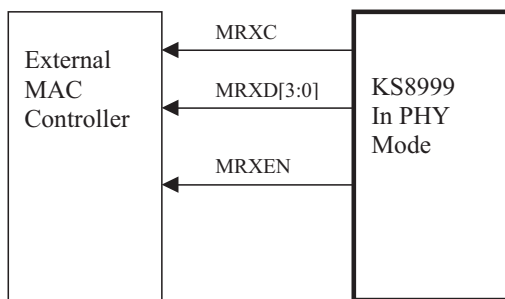


Figure 13. KS8999 PHY Mode—Data Sent from KS8999 PHY Mode to External MAC Controller

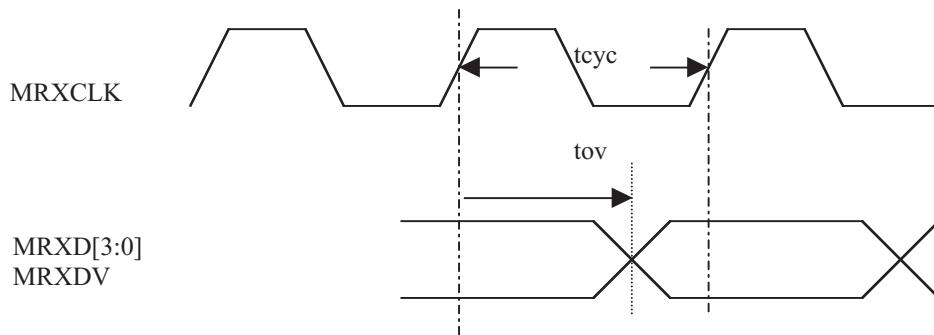


Figure 14. KS8999 PHY Mode Transmit Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|-------|
| t_{CYC} | Clock Cycle (100BaseT) | | 40 | | ns |
| t_{CYC} | Clock Cycle (10BaseT) | | 400 | | ns |
| t_{OV} | Output Valid | 18 | 25 | 28 | ns |

Table 10. KS8999 PHY Mode Transmit Timing Parameters

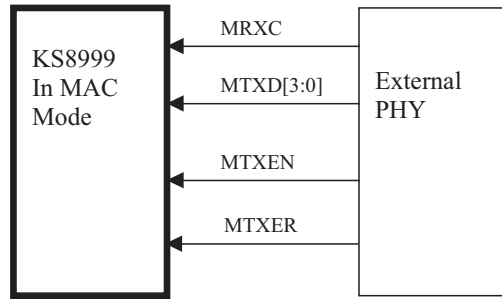


Figure 15. KS8999 MAC Mode—Data Sent from External PHY Device to KS8999

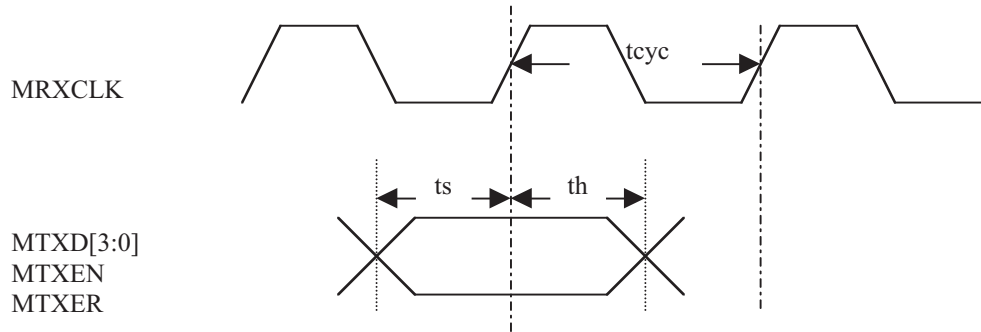


Figure 16. KS8999 MAC Mode Receive Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|-------|
| t_{CYC} | Clock Cycle (100BaseT) | | 40 | | ns |
| t_{CYC} | Clock Cycle (10BaseT) | | 400 | | ns |
| t_S | Output Valid | 10 | | | ns |
| t_H | Output Valid | 5 | | | ns |

Table 11. KS8999 PHY Mode Transmit Timing Parameters

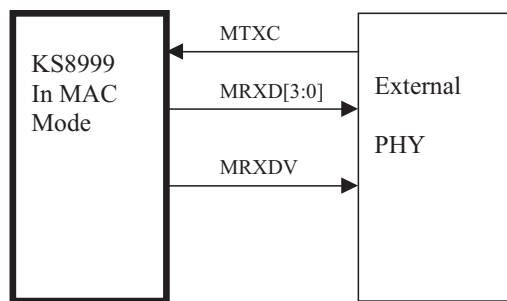


Figure 17. KS8999 MAC Mode Timing—Data Sent from KS8999 MAC mode to External PHY Device

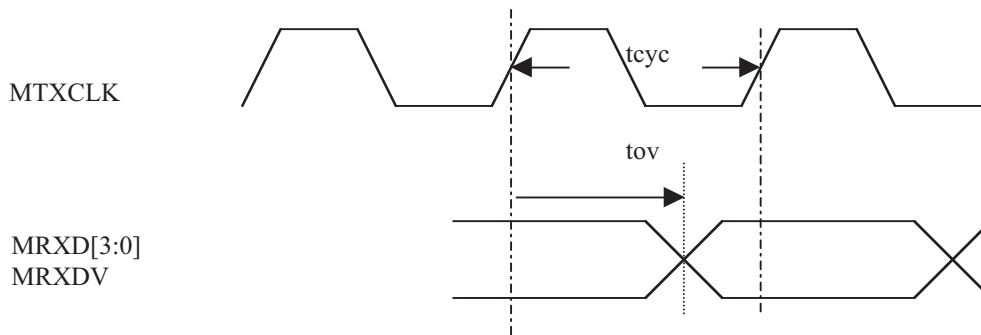


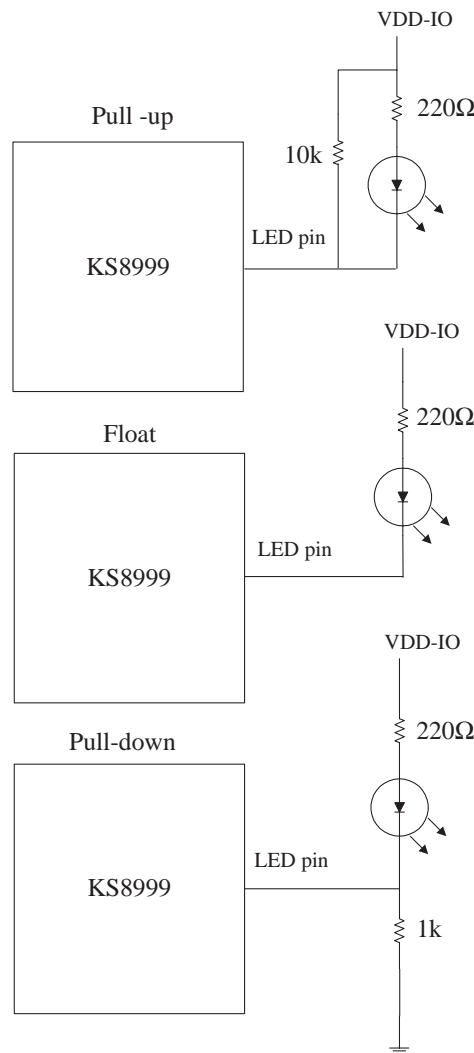
Figure 18. KS8999 MAC Mode Transmit Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|-------|
| t_{CYC} | Clock Cycle (100BaseT) | | 40 | | ns |
| t_{CYC} | Clock Cycle (10BaseT) | | 400 | | ns |
| t_{OV} | Output Valid | 7 | 11 | 16 | ns |

Table 12. KS8999 MAC Mode Transmit Timing Parameters

Reference Circuits

See “I/O Description” section for pull-up/pull-down and float information.



Reference circuits for unmanaged programming through LED ports
 Note: For brighter LED operation use VDD-IO = 3.3V

Figure 19. Unmanaged Programming Circuit

Reset Reference Circuit

Micrel recommends the following discrete reset circuit as shown in Figure 20 when powering up the KS8999 device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 21.

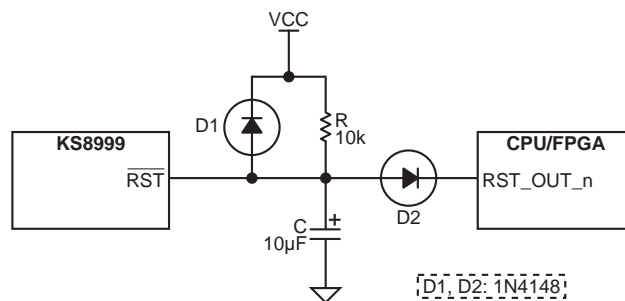


Figure 20. Recommended Reset Circuit.

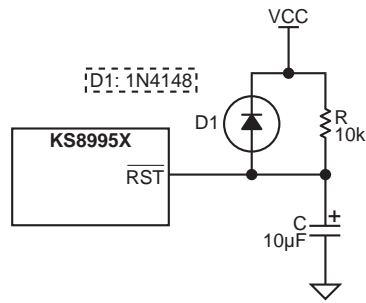


Figure 21. Recommended Circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the KS8999 device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.

4B/5B Coding

In 100BaseTX and 100BaseFX the data and frame control are encoded in the transmitter (and decoded in the receiver) using a 4B/5B code. The extra code space is required to encode extra control (frame delineation) points. It is also used to reduce run length as well as supply sufficient transitions for clock recovery. The table below provides the translation for the 4B/5B coding.

| Code Type | 4B Code | 5B Code | Value |
|-----------|-------------|---------|------------------------|
| Data | 0000 | 11110 | Data value 0 |
| | 0001 | 01001 | Data value 1 |
| | 0010 | 10100 | Data value 2 |
| | 0011 | 10101 | Data value 3 |
| | 0100 | 01010 | Data value 4 |
| | 0101 | 01011 | Data value 5 |
| | 0110 | 01110 | Data value 6 |
| | 0111 | 01111 | Data value 7 |
| | 1000 | 10010 | Data value 8 |
| | 1001 | 10011 | Data value 9 |
| | 1010 | 10110 | Data value A |
| | 1011 | 10111 | Data value B |
| | 1100 | 11010 | Data value C |
| | 1101 | 11011 | Data value D |
| | 1110 | 11100 | Data value E |
| | 1111 | 11101 | Data value F |
| Control | Not defined | 11111 | Idle |
| | 0101 | 11000 | Start delimiter part 1 |
| | 0101 | 10001 | Start delimiter part 2 |
| | Not defined | 01101 | End delimiter part 1 |
| | Not defined | 00111 | End delimiter part 2 |
| | Not defined | 00100 | Transmit error |
| Invalid | Not defined | 00000 | Invalid code |
| | Not defined | 00001 | Invalid code |
| | Not defined | 00010 | Invalid code |
| | Not defined | 00011 | Invalid code |
| | Not defined | 00101 | Invalid code |
| | Not defined | 00110 | Invalid code |
| | Not defined | 01000 | Invalid code |
| | Not defined | 01100 | Invalid code |
| | Not defined | 10000 | Invalid code |
| | Not defined | 11001 | Invalid code |

Table 13. 4B/5B Coding

MLT3 Coding

For 100BaseTX operation the NRZI (Non-Return to Zero Invert on ones) signal is line coded as MLT3. The net result of using MLT3 is to reduce the EMI (Electro Magnetic Interference) of the signal over twisted pair media. In NRZI coding, the level changes from high to low or low to high for every "1" bit. For a "0" bit there is no transition. MLT3 line coding transitions through three distinct levels. For every transition of the NRZI signal the MLT3 signal either increments or decrements depending on the current state of the signal. For instance if the MLT3 level is at its lowest point the next two NRZI transitions will change the MLT3 signal initially to the middle level followed by the highest level (second NRZI transition). On the next NRZI change, the MLT3 level will decrease to the middle level. On the following transition of the NRZI signal the MLT3 level will move to the lowest level where the cycle repeats. The diagram below describes the level changes. Note that in the actual 100BaseTX circuit there is a scrambling circuit and that scrambling is not shown in this diagram.

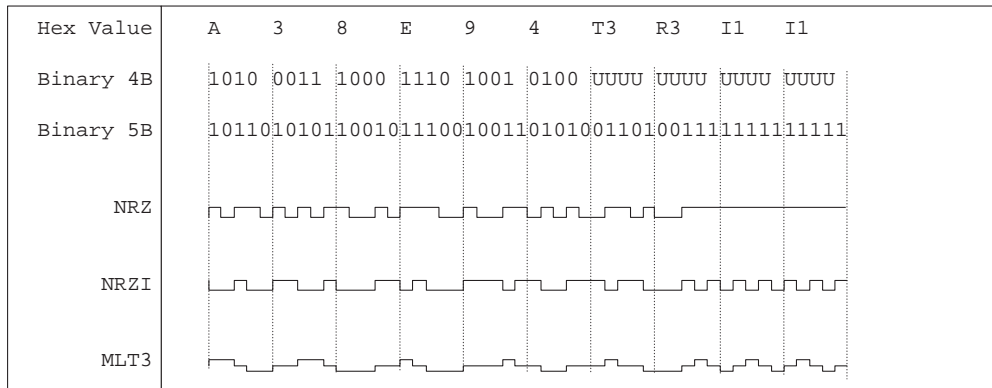


Figure 20. MLT3 coding

MAC Frame

The MAC (Media Access Control) fields are described in the table below.

| Field | Octect Length | Description |
|---------------|---------------|---------------------------------------|
| Preamble/SFD | 8 | Preamble and Start of Frame Delimiter |
| DA | 6 | 48-bit Destination MAC Address |
| SA | 6 | 48-bit Source MAC Address |
| Length | 2 | Frame Length |
| Protocol/Data | 46 to 1500 | Higher Layer Protocol and Frame Data |
| Frame CRC | 4 | 32-bit Cyclical Redundancy Check |
| ESD | 1 | End of Stream Delimiter |
| Idle | Variable | Inter Frame Idles |

Table 14. MAC Frame

Selection of Isolation Transformer^(Note 1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

| Characteristics Name | Value | Test Condition |
|----------------------------------|--------------|---------------------|
| Turns Ratio | 1 CT : 1 CT | |
| Open-Circuit Inductance (min.) | 350 μ H | 100mV, 100 KHz, 8mA |
| Leakage Inductance (max.) | 0.4 μ H | 1MHz (min.) |
| Inter-Winding Capacitance (max.) | 12pF | |
| D.C. Resistance (max.) | 0.9 Ω | |
| Insertion Loss (max.) | 1.0dB | 0MHz to 65MHz |
| HIPOT (min.) | 1500Vrms | |

Note 1. The IEEE 802.3u standard for 100BaseTX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

Selection of Reference Oscillator/Crystal

An oscillator or crystal with the following typical characteristics is recommended.

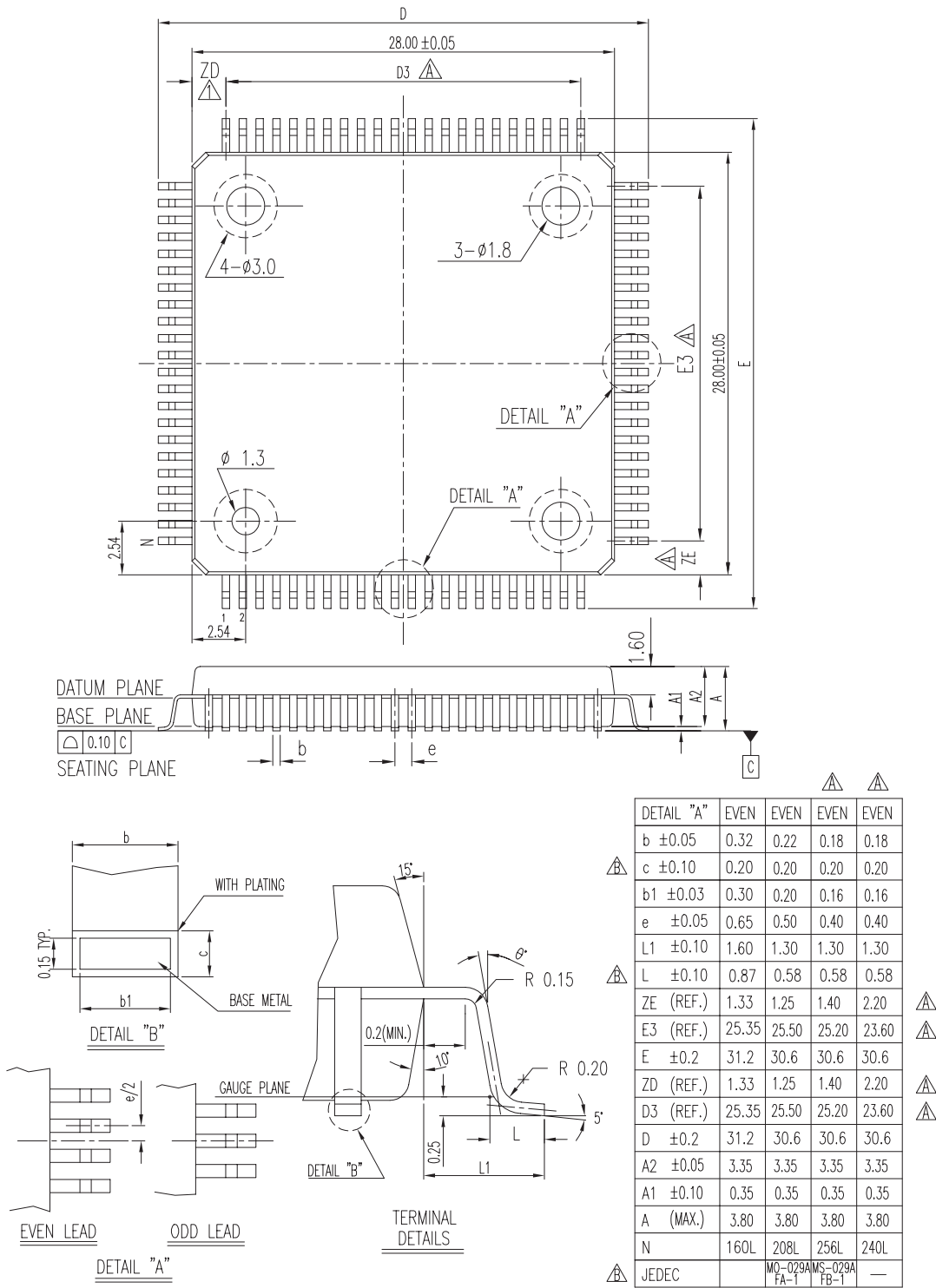
| Characteristics Name | Value | Test Condition |
|-----------------------------|----------|----------------|
| Frequency | 25.00000 | MHz |
| Maximum Frequency Tolerance | \pm 50 | ppm |
| Maximum Jitter | 150 | ps(pk-pk) |

The following transformer vendors provide compatible magnetic parts for Micrel's device:

| 4-Port Integrated | | Auto MDIX | Number of Port | Single Port | | Auto MDIX | Number of Port |
|-------------------|-------------|-----------|----------------|-------------|--------------|-----------|----------------|
| Vendor | Part | | | Vendor | Part | | |
| Pulse | H1164 | Yes | 4 | Pulse | H1102 | Yes | 1 |
| Bel Fuse | 558-5999-Q9 | Yes | 4 | Bel Fuse | S558-5999-U7 | Yes | 1 |
| YCL | PH406466 | Yes | 4 | YCL | PT163020 | Yes | 1 |
| Transpower | HB826-2 | Yes | 4 | Transpower | HB726 | Yes | 1 |
| Delta | LF8731 | Yes | 4 | Delta | LF8505 | Yes | 1 |

Table 15. Qualified Magnetics Vendor Lists

Package Information



208-Pin PQFP (PQ)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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