

# 8-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-8L MB89630R Series

### MB89635R/T635R/636R/637R/T637R MB89P637/W637/PV630

#### ■ OUTLINE

The MB89630R series has been developed as a general-purpose version of the F<sup>2</sup>MC\*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

\*: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

#### ■ FEATURES

- High-speed operating capability at low voltage
- Minimum execution time: 0.4  $\mu$ s@3.5 V, 0.8  $\mu$ s@2.7 V
- F<sup>2</sup>MC-8L family CPU core

Instruction set optimized for controllers

{ Multiplication and division instructions  
16-bit arithmetic operations  
Test and branch instructions  
Bit manipulation instructions, etc.

- Five types of timers
  - 8-bit PWM timer: 2 channels (Also usable as a reload timer)
  - 8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
  - 16-bit timer/counter
  - 21-bit timebase timer
- UART
  - CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  - Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  - Start by an external input capable

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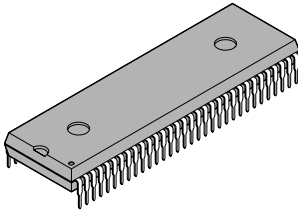
# MB89630R Series

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- External interrupt: 4 channels  
Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes  
Stop mode (Oscillation stops to minimize the current consumption.)  
Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)  
Subclock mode  
Watch mode
- Bus interface function  
With hold and ready function

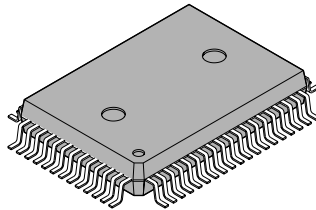
## ■ PACKAGE

64-pin Plastic SH-DIP



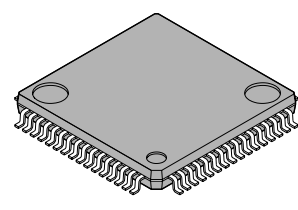
(DIP-64P-M01)

64-pin Plastic QFP



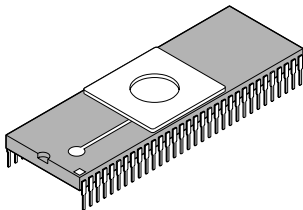
(FPT-64P-M06)

64-pin Plastic QFP



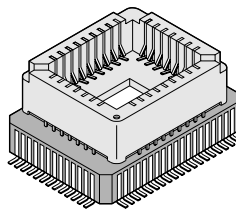
(FPT-64P-M09)

64-pin Ceramic SH-DIP



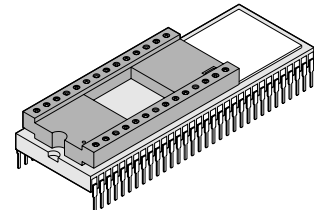
(DIP-64C-A06)

64-pin Ceramic MQFP



(MQP-64C-P01)

64-pin Ceramic MDIP



(MDP-64C-P02)

# MB89630R Series

## ■ PRODUCT LINEUP

| Part number<br>Item                 | MB89635R                                                                                                                                                                                                                                                                                                                                               | MB89636R                                | MB89637R                                | MB89T635R                | MB89T637R     | MB89P637                                                                                          | MB89W637         | MB89PV630                                                                     |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|-----------------------------------------|--------------------------|---------------|---------------------------------------------------------------------------------------------------|------------------|-------------------------------------------------------------------------------|
| Classification                      | Mass-produced products<br>(mask ROM products)                                                                                                                                                                                                                                                                                                          |                                         |                                         | External ROM<br>products |               | One-time<br>PROM<br>product                                                                       | EPROM<br>product | Piggyback/<br>evaluation<br>product (for<br>evaluation<br>and<br>development) |
| ROM size                            | 16 K × 8 bits<br>(internal<br>mask ROM)                                                                                                                                                                                                                                                                                                                | 24 K × 8 bits<br>(internal<br>mask ROM) | 32 K × 8 bits<br>(internal<br>mask ROM) | Fixed to external ROM    |               | 32 K × 8 bits<br>(Internal PROM, to be<br>programmed with<br>general-purpose<br>EPROM programmer) |                  | 32 K × 8 bits<br>(external<br>ROM)                                            |
| RAM size                            | 512 × 8 bits                                                                                                                                                                                                                                                                                                                                           | 768 × 8 bits                            | 1024 × 8 bits                           | 512 × 8 bits             | 1024 × 8 bits |                                                                                                   |                  | 1 K × 8 bits                                                                  |
| CPU functions                       | The number of instructions: 136<br>Instruction bit length: 8 bits<br>Instruction length: 1 to 3 bytes<br>Data bit length: 1, 8, 16 bits<br>Minimum execution time: 0.4 to 6.4 μs/10 MHz, 61 μs@32.768 kHz<br>Interrupt processing time: 3.6 to 57.6 μs/10 MHz, 562.5 μs@32.768 kHz                                                                     |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| Ports                               | Input ports: 5 (All also serve as peripherals.)<br>Output ports (N-ch open-drain): 8 (All also serve as peripherals.)<br>I/O ports (N-ch open-drain): 4 (All also serve as peripherals.)<br>Output ports (CMOS): 8 (All also serve as bus control.)<br>I/O ports (CMOS): 28 (27 ports also serve as bus pins and peripherals.)<br>Total: 53            |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| Clock timer                         | 21 bits × 1 (in main clock)/15 bits × 1 (at 32.768 kHz)                                                                                                                                                                                                                                                                                                |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| 8-bit PWM<br>timer                  | 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 μs to 3.3 ms) × 2<br>channels<br>7/8-bit resolution PWM operation (conversion cycle: 51.2 μs to 839 ms) × 2 channels                                                                                                                                                  |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| 8-bit pulse<br>width count<br>timer | 8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 μs)<br>8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 μs)<br>8-bit pulse width measurement operation (capable of continuous measurement, and<br>measurement of “H” pulse width/ “L” pulse width/ from ↑ to ↑/from ↓ to ↓) |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| 16-bit timer/<br>counter            | 16-bit timer operation (operating clock cycle: 0.4 μs)<br>16-bit event counter operation (rising edge/falling edge/both edge selectable)                                                                                                                                                                                                               |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| 8-bit serial I/O                    | 8 bits<br>LSB first/MSB first selectable<br>One clock selectable from four transfer clocks<br>(one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs)                                                                                                                                                                         |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| UART                                | Capable of switching two I/O systems by software<br>Transfer data length (6, 7, and 8 bits)<br>Transfer rate (300 to 62500 bps. at 10 MHz oscilation)                                                                                                                                                                                                  |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |
| 10-bit A/D<br>converter             | 10-bit resolution × 8 channels<br>A/D conversion mode (conversion time: 13.2 μs)<br>Sense mode (conversion time: 7.2 μs)<br>Capable of continuous activation by an external activation or an internal timer                                                                                                                                            |                                         |                                         |                          |               |                                                                                                   |                  |                                                                               |

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# MB89630R Series

(Continued)

| Part number<br>Item      | MB89635R                                                                                                                                                                                                       | MB89636R | MB89637R | MB89T635R | MB89T637R      | MB89P637 | MB89W637 | MB89PV630                          |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|-----------|----------------|----------|----------|------------------------------------|
| External interrupt input | 4 independent channels (edge selection, interrupt vector, source flag).<br>Rising edge/falling edge selectable<br>Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.) |          |          |           |                |          |          |                                    |
| Standby mode             | Sleep mode, stop mode, watch mode, and subclock mode                                                                                                                                                           |          |          |           |                |          |          |                                    |
| Process                  | CMOS                                                                                                                                                                                                           |          |          |           |                |          |          |                                    |
| Operating voltage*       | 2.2 V to 6.0 V                                                                                                                                                                                                 |          |          |           | 2.7 V to 6.0 V |          |          |                                    |
| EPROM for use            |                                                                                                                                                                                                                |          |          |           |                |          |          | MBM27C256A-20CZ<br>MBM27C256A-20TV |

\* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)  
In the case of the MB89PV630, the voltage varies with the restrictions of the EPROM for use.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package     | MB89635R<br>MB89T635R | MB89636R<br>MB89637R<br>MB89T637R | MB89P637 | MB89W637 | MB89PV630 |
|-------------|-----------------------|-----------------------------------|----------|----------|-----------|
| DIP-64P-M01 | ○                     | ○                                 | ○        | ×        | ×         |
| FPT-64P-M06 | ○                     | ○                                 | ○        | ×        | ×         |
| FPT-64P-M09 | ○                     | ○                                 | ×        | ×        | ×         |
| DIP-64C-A06 | ×                     | ×                                 | ×        | ○        | ×         |
| MQP-64C-P01 | ×                     | ×                                 | ×        | ×        | ○         |
| MDP-64C-P02 | ×                     | ×                                 | ×        | ×        | ○         |

○ : Available    ×: Not available

\* : To convert pin pitches, an adapter socket (manufacturer: Sun Hayato Co., Ltd.) is available.  
64SD-64QF2-8L: For conversion from (DIP-64P-M01, DIP-64C-A06, or MDP-64C-P02) to FPT-64P-M09  
Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403  
FAX (81)-3-5396-9106

Note: For more information about each package, see section “■ Package Dimensions.”

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

On the MB89P637/W637, the program area starts from address 8007<sub>H</sub> but on the MB89PV630 and MB89637R starts from 8000<sub>H</sub>.

- On the MB89P637/W637, addresses 8000<sub>H</sub> to 8006<sub>H</sub> comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000<sub>H</sub> to 8006<sub>H</sub> could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637/W637.
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

### 2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM. However, the current consumption in sleep/stop modes is the same. (For more information, see sections “■ Electrical Characteristics” and “■ Example Characteristics.”)

### 3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section “■ Mask Options.”

Take particular care on the following points:

- A pull-up resistor cannot be set for P50 to P53 on the MB89P637 and MB89W637.
- Options are fixed on the MB89PV630, MB89T635R, and MB89T637R.

### 4. Differences between the MB89630 and MB89630R Series

- Memory access area

There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R.

The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

| Address                                | Memory area   |                   |
|----------------------------------------|---------------|-------------------|
|                                        | MB89636       | MB89636R          |
| 0000 <sub>H</sub> to 007F <sub>H</sub> | I/O area      | I/O area          |
| 0080 <sub>H</sub> to 037F <sub>H</sub> | RAM area      | RAM area          |
| 0380 <sub>H</sub> to 047F <sub>H</sub> | External area | Access prohibited |
| 0480 <sub>H</sub> to 7FFF <sub>H</sub> |               | External area     |
| 8000 <sub>H</sub> to 9FFF <sub>H</sub> |               | Access prohibited |
| A000 <sub>H</sub> to FFFF <sub>H</sub> | ROM area      | ROM area          |

# MB89630R Series

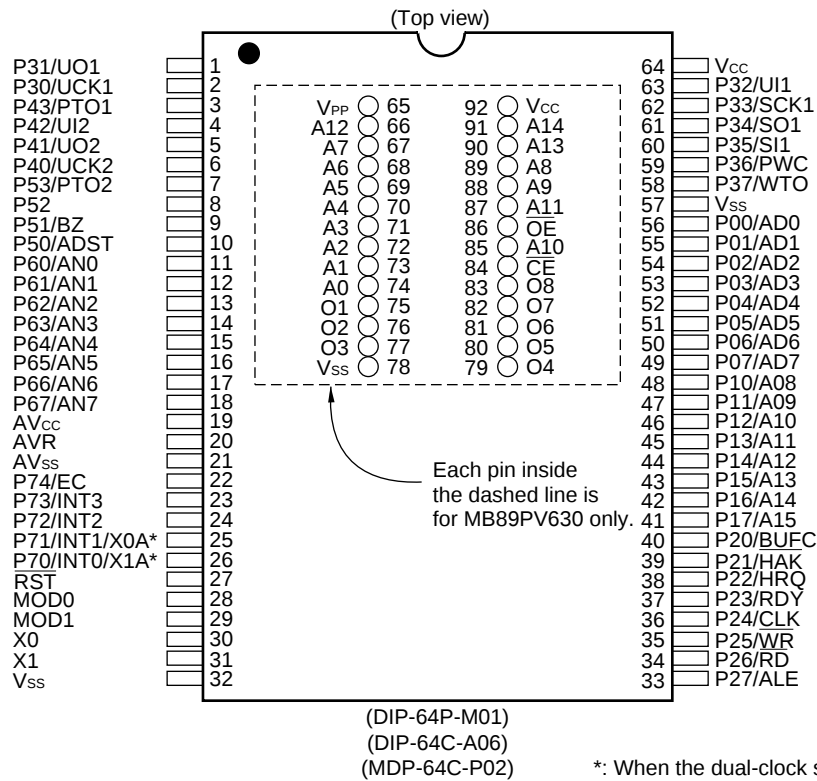
- Other specifications  
Both MB89630 series and MB89630R is the same.
- Electrical specifications/electrical characteristics  
Electrical specifications of the MB89630R series are the same as that of the MB89630 series.  
Electrical characteristics of both the series are much the same.

## ■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

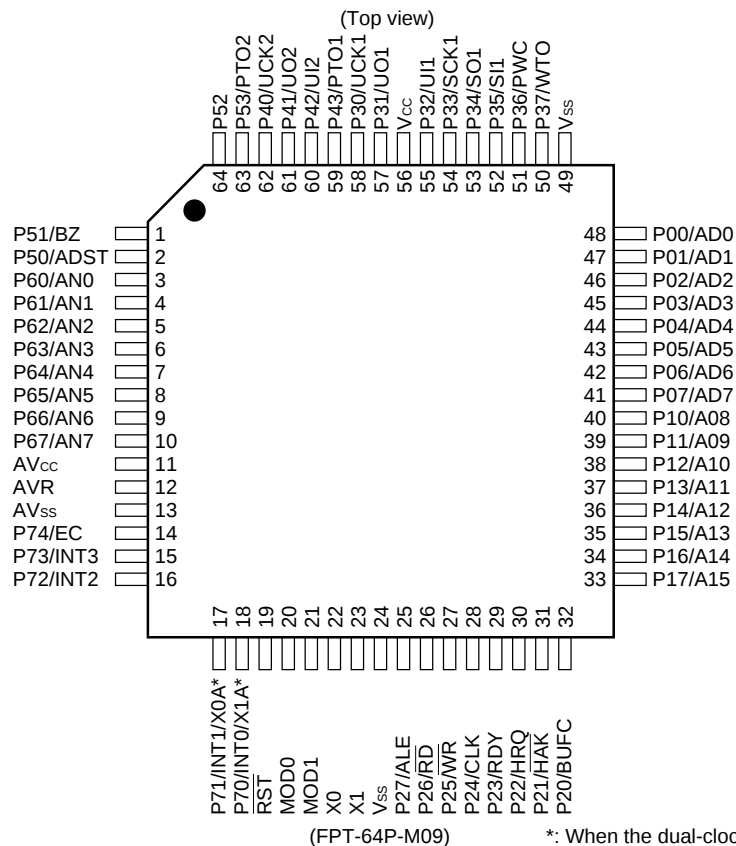
- The MB89630R series is the reduction version of the MB89630 series.
- The the MB89630 and MB89630R series consist of the following products:

|                 |          |           |          |          |           |          |          |           |
|-----------------|----------|-----------|----------|----------|-----------|----------|----------|-----------|
| MB89630 series  | MB89635  | MB89T635  | MB89636  | MB89637  | MB89T637  | MB89P637 | MB89W637 | MB89PV630 |
| MB89630R series | MB89635R | MB89T635R | MB89636R | MB89637R | MB89T637R |          |          |           |

## PIN ASSIGNMENT

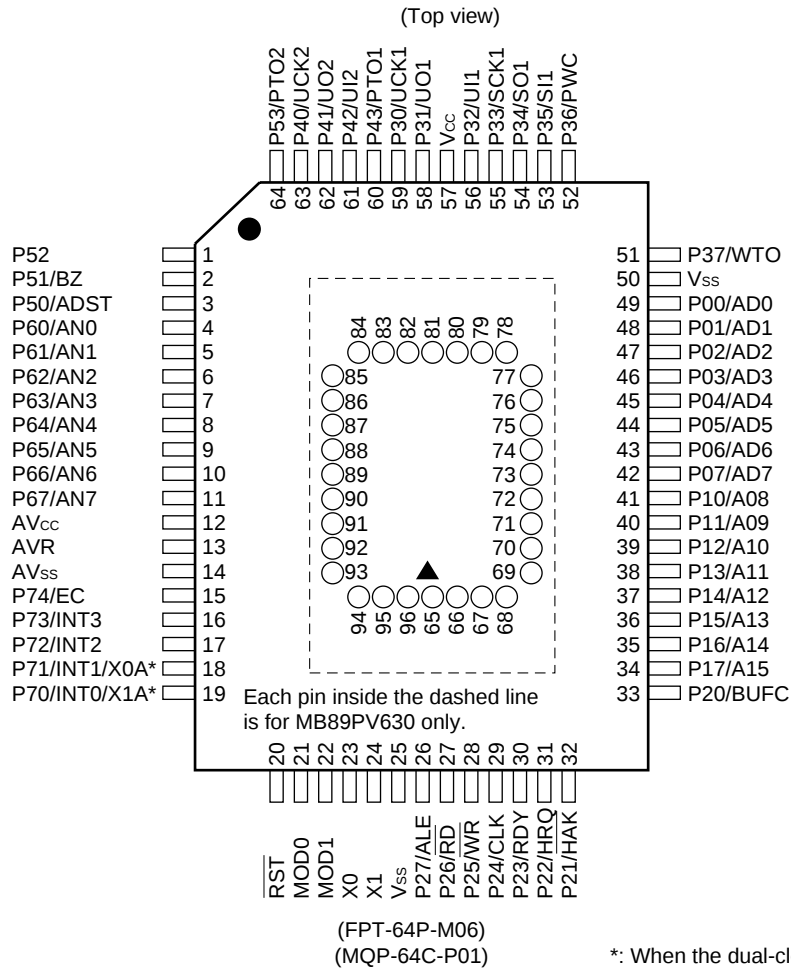


\*: When the dual-clock system is selected.



\*: When the dual-clock system is selected.

# MB89630R Series



## • Pin assignment on package top (MB89PV630 only)

| Pin no. | Pin name        | Pin no. | Pin name        | Pin no. | Pin name               | Pin no. | Pin name               |
|---------|-----------------|---------|-----------------|---------|------------------------|---------|------------------------|
| 65      | N.C.            | 73      | A2              | 81      | N.C.                   | 89      | $\overline{\text{OE}}$ |
| 66      | V <sub>PP</sub> | 74      | A1              | 82      | O4                     | 90      | N.C.                   |
| 67      | A12             | 75      | A0              | 83      | O5                     | 91      | A11                    |
| 68      | A7              | 76      | N.C.            | 84      | O6                     | 92      | A9                     |
| 69      | A6              | 77      | O1              | 85      | O7                     | 93      | A8                     |
| 70      | A5              | 78      | O2              | 86      | O8                     | 94      | A13                    |
| 71      | A4              | 79      | O3              | 87      | $\overline{\text{CE}}$ | 95      | A14                    |
| 72      | A3              | 80      | V <sub>SS</sub> | 88      | A10                    | 96      | V <sub>CC</sub>        |

N.C.: Internally connected. Do not use.

## ■ PIN DESCRIPTION

| Pin no.            |          |                  | Pin name            | Circuit type | Function                                                                                                                                                                                                                               |
|--------------------|----------|------------------|---------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SH-DIP*1<br>MDIP*2 | QFP2*3   | QFP1*4<br>MQFP*5 |                     |              |                                                                                                                                                                                                                                        |
| 30                 | 22       | 23               | X0                  | A            | Main clock crystal oscillator pins                                                                                                                                                                                                     |
| 31                 | 23       | 24               | X1                  |              |                                                                                                                                                                                                                                        |
| 28                 | 20       | 21               | MOD0                | D            | Operating mode selection pins<br>Connect directly to V <sub>CC</sub> or V <sub>SS</sub> .                                                                                                                                              |
| 29                 | 21       | 22               | MOD1                |              |                                                                                                                                                                                                                                        |
| 27                 | 19       | 20               | RST                 | C            | Reset I/O pin<br>This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type.<br>“L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”. |
| 56 to 49           | 48 to 41 | 49 to 42         | P00/AD0 to P07/AD7  | F            | General-purpose I/O ports<br>When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.                                                                                    |
| 48 to 41           | 40 to 33 | 41 to 34         | P10/A08 to P17/A157 | F            | General-purpose I/O ports<br>When an external bus is used, these ports function as an upper address output.                                                                                                                            |
| 40                 | 32       | 33               | P20/BUFC            | H            | General-purpose output port<br>When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.                                                                                                |
| 39                 | 31       | 32               | P21/HAK             | H            | General-purpose output port<br>When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.                                                                                                     |
| 38                 | 30       | 31               | P22/HRQ             | F            | General-purpose output port<br>When an external bus is used, this port can also be used as a hold request input by setting the BCTR.                                                                                                   |
| 37                 | 29       | 30               | P23/RDY             | F            | General-purpose output port<br>When an external bus is used, this port functions as a ready input.                                                                                                                                     |
| 36                 | 28       | 29               | P24/CLK             | H            | General-purpose output port<br>When an external bus is used, this port functions as a clock output.                                                                                                                                    |
| 35                 | 27       | 28               | P25/WR              | H            | General-purpose output port<br>When an external bus is used, this port functions as a write signal output.                                                                                                                             |
| 34                 | 26       | 27               | P26/RD              | H            | General-purpose output port<br>When an external bus is used, this port functions as a read signal output.                                                                                                                              |

\*1: DIP-64P-M01, DIP-64C-A06

\*2: MDP-64C-P02

\*3: FPT-64P-M09

\*4: FPT-64P-M06

\*5: MQP-M64C-P01

(Continued)

# MB89630R Series

(Continued)

| Pin no.            |        |                  | Pin name | Circuit type | Function                                                                                                                                        |
|--------------------|--------|------------------|----------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| SH-DIP*1<br>MDIP*2 | QFP2*3 | QFP1*4<br>MQFP*5 |          |              |                                                                                                                                                 |
| 33                 | 25     | 26               | P27/ALE  | H            | General-purpose output port<br>When an external bus is used, this port functions as an address latch signal output.                             |
| 2                  | 58     | 59               | P30/UCK1 | G            | General-purpose I/O port<br>Also serves as the clock I/O 1 for the UART.<br>This port is a hysteresis input type.                               |
| 1                  | 57     | 58               | P31/UO1  | F            | General-purpose I/O port<br>Also serves as the data output 1 for the UART.                                                                      |
| 63                 | 55     | 56               | P32/UI1  | G            | General-purpose I/O port<br>Also serves as the data input 1 for the UART.<br>This port is a hysteresis input type.                              |
| 62                 | 54     | 55               | P33/SCK1 | G            | General-purpose I/O port<br>Also serves as the data input for the 8-bit serial I/O.<br>This port is a hysteresis input type.                    |
| 61                 | 53     | 54               | P34/SO1  | F            | General-purpose I/O port<br>Also serves as the data output for the 8-bit serial I/O.                                                            |
| 60                 | 52     | 53               | P35/SI1  | G            | General-purpose I/O port<br>Also serves as the data input for the 8-bit serial I/O.<br>This port is a hysteresis input type.                    |
| 59                 | 51     | 52               | P36/PWC  | G            | General-purpose I/O port<br>Also serves as the measured pulse input for the 8-bit pulse width counter.<br>This port is a hysteresis input type. |
| 58                 | 50     | 51               | P37/WTO  | F            | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit pulse width counter.                                                 |
| 6                  | 62     | 63               | P40/UCK2 | G            | General-purpose I/O port<br>Also serves as the clock I/O 2 for the UART.<br>This port is a hysteresis input type.                               |
| 5                  | 61     | 62               | P41/UO2  | F            | General-purpose I/O port<br>Also serves as the data output 2 for the UART.                                                                      |
| 4                  | 60     | 61               | P42/UI2  | G            | General-purpose I/O port<br>Also serves as the data input 2 for the UART.<br>This port is a hysteresis input type.                              |
| 3                  | 59     | 60               | P43/PTO1 | F            | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit PWM timer.                                                           |
| 10                 | 2      | 3                | P50/ADST | K            | General-purpose I/O port<br>Also serves as an A/D converter external activation.<br>This port is a hysteresis input type.                       |

\*1: DIP-64P-M01, DIP-64C-A06

\*2: MDP-64C-P02

\*3: FPT-64P-M09

\*4: FPT-64P-M06

\*5: MQP-M64C-P01

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| Pin no.                                    |                    |                                          | Pin name                      | Circuit type | Function                                                                                                                                                                                             |
|--------------------------------------------|--------------------|------------------------------------------|-------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SH-DIP <sup>*1</sup><br>MDIP <sup>*2</sup> | QFP2 <sup>*3</sup> | QFP1 <sup>*4</sup><br>MQFP <sup>*5</sup> |                               |              |                                                                                                                                                                                                      |
| 9                                          | 1                  | 2                                        | P51/BZ                        | J            | General-purpose I/O port<br>Also serves as a buzzer output.                                                                                                                                          |
| 8                                          | 64                 | 1                                        | P52                           | J            | General-purpose I/O port                                                                                                                                                                             |
| 7                                          | 63                 | 64                                       | P53/PTO2                      | J            | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit PWM timer.                                                                                                                |
| 11 to 18                                   | 3 to 10            | 4 to 11                                  | P60/AN0 to<br>P67/AN7         | I            | N-ch open-drain output ports<br>Also serve as an A/D converter analog input.                                                                                                                         |
| 26,<br>25                                  | 18,<br>17          | 19,<br>18                                | P70/INT0/X1A,<br>P71/INT1/X0A | B/E          | Input-only ports<br>These ports are a hysteresis input type.<br>Also serve as an external interrupt input (at single-clock operation).<br>Subclock crystal oscillator pins (at dual-clock operation) |
| 24,<br>23                                  | 16,<br>15          | 17,<br>16                                | P72/INT2,<br>P73/INT3         | E            | Input-only ports<br>Also serve as an external interrupt input.<br>These ports are a hysteresis input type.                                                                                           |
| 22                                         | 14                 | 15                                       | P74/EC                        | E            | General-purpose input port<br>Also serves as the external clock input for the 16-bit timer/counter.<br>This port is a hysteresis input type.                                                         |
| 64                                         | 56                 | 57                                       | V <sub>CC</sub>               | —            | Power supply pin                                                                                                                                                                                     |
| 32, 57                                     | 24, 49             | 25, 50                                   | V <sub>SS</sub>               | —            | Power supply (GND) pin                                                                                                                                                                               |
| 19                                         | 11                 | 12                                       | AV <sub>CC</sub>              | —            | A/D converter power supply pin                                                                                                                                                                       |
| 20                                         | 12                 | 13                                       | AVR                           | —            | A/D converter reference voltage input pin                                                                                                                                                            |
| 21                                         | 13                 | 14                                       | AV <sub>SS</sub>              | —            | A/D converter power supply pin<br>Use this pin at the same voltage as V <sub>SS</sub> .                                                                                                              |

\*1: DIP-64P-M01, DIP-64C-A06

\*2: MDP-64C-P02

\*3: FPT-64P-M09

\*4: FPT-64P-M06

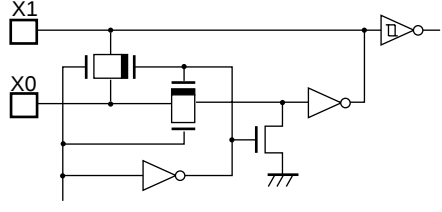
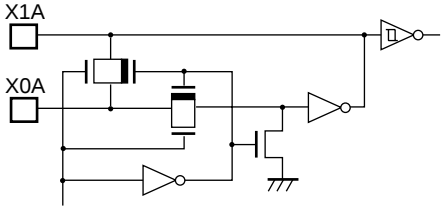
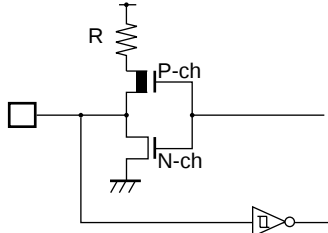
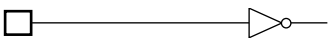
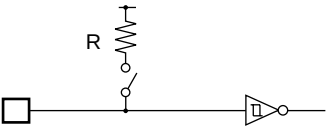
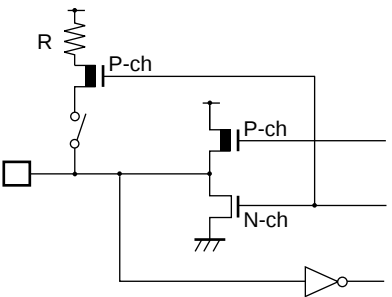
\*5: MQP-M64C-P01

# MB89630R Series

- External EPROM pins (MB89PV630 only)

| Pin no. |                      | Pin name               | I/O | Function                                                 |
|---------|----------------------|------------------------|-----|----------------------------------------------------------|
| MDIP    | MQFP                 |                        |     |                                                          |
| 65      | 66                   | V <sub>PP</sub>        | O   | “H” level output pin                                     |
| 66      | 67                   | A12                    | O   | Address output pins                                      |
| 67      | 68                   | A7                     |     |                                                          |
| 68      | 69                   | A6                     |     |                                                          |
| 69      | 70                   | A5                     |     |                                                          |
| 70      | 71                   | A4                     |     |                                                          |
| 71      | 72                   | A3                     |     |                                                          |
| 72      | 73                   | A2                     |     |                                                          |
| 73      | 74                   | A1                     |     |                                                          |
| 74      | 75                   | A0                     |     |                                                          |
| 75      | 77                   | O1                     | I   | Data input pins                                          |
| 76      | 78                   | O2                     |     |                                                          |
| 77      | 79                   | O3                     |     |                                                          |
| 78      | 80                   | V <sub>SS</sub>        | O   | Power supply (GND) pin                                   |
| 79      | 82                   | O4                     | I   | Data input pins                                          |
| 80      | 83                   | O5                     |     |                                                          |
| 81      | 84                   | O6                     |     |                                                          |
| 82      | 85                   | O7                     |     |                                                          |
| 83      | 86                   | O8                     |     |                                                          |
| 84      | 87                   | $\overline{\text{CE}}$ | O   | ROM chip enable pin<br>Outputs “H” during standby.       |
| 85      | 88                   | A10                    | O   | Address output pin                                       |
| 86      | 89                   | $\overline{\text{OE}}$ | O   | ROM output enable pin<br>Outputs “L” at all times.       |
| 87      | 91                   | A11                    | O   | Address output pins                                      |
| 88      | 92                   | A9                     |     |                                                          |
| 89      | 93                   | A8                     |     |                                                          |
| 90      | 94                   | A13                    | O   |                                                          |
| 91      | 95                   | A14                    | O   |                                                          |
| 92      | 96                   | V <sub>CC</sub>        | O   |                                                          |
| —       | 65<br>76<br>81<br>90 | N.C.                   | —   | Internally connected pins<br>Be sure to leave them open. |

## ■ I/O CIRCUIT TYPE

| Type | Circuit                                                                                                         | Remarks                                                                                                                                                                                                                                                                                                                                               |
|------|-----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A    |  <p>Standby control signal</p> | <ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (main clock)</li> <li>External clock input selection versions of MB89PV630, MB89P637, MB89W637, MB89635R, MB89T635R, MB89636R, MB89637R, and MB89T637R</li> <li>At an oscillation feedback resistor of approximately <math>1\text{ M}\Omega@5.0\text{ V}</math></li> </ul> |
| B    |  <p>Standby control signal</p> | <ul style="list-style-type: none"> <li>Crystal or ceramic oscillation type (subclock)</li> <li>MB89PV630, MB89P637, MB89W637, MB89635R, MB89636R, and MB89637R with dual-clock system</li> <li>At an oscillation feedback resistor of approximately <math>4.5\text{ M}\Omega@5.0\text{ V}</math></li> </ul>                                           |
| C    |                               | <ul style="list-style-type: none"> <li>At an output pull-up resistor (P-ch) of approximately <math>50\text{ k}\Omega@5.0\text{ V}</math></li> <li>Hysteresis input</li> </ul>                                                                                                                                                                         |
| D    |                              |                                                                                                                                                                                                                                                                                                                                                       |
| E    |                              | <ul style="list-style-type: none"> <li>Hysteresis input</li> <li>Pull-up resistor optional (except P70 and P71)</li> </ul>                                                                                                                                                                                                                            |
| F    |                              | <ul style="list-style-type: none"> <li>CMOS output</li> <li>CMOS input</li> <li>Pull-up resistor optional (except P22 and P23)</li> </ul>                                                                                                                                                                                                             |

(Continued)

# MB89630R Series

(Continued)

| Type | Circuit | Remarks                                                                                                                          |
|------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| G    |         | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Pull-up resistor optional</li> </ul> |
| H    |         | <ul style="list-style-type: none"> <li>• CMOS output</li> </ul>                                                                  |
| I    |         | <ul style="list-style-type: none"> <li>• Analog input</li> </ul>                                                                 |
| J    |         | <ul style="list-style-type: none"> <li>• CMOS input</li> <li>• Pull-up resistor optional</li> </ul>                              |
| K    |         | <ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-up resistor optional</li> </ul>                        |

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply ( $AV_{CC}$  and  $AVR$ ) and analog input from exceeding the digital power supply ( $V_{CC}$ ) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be  $AV_{CC} = DAVC = V_{CC}$  and  $AV_{SS} = AVR = V_{SS}$  even if the A/D and D/A converters are not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Fluctuations

Although  $V_{CC}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.

# MB89630R Series

## ■ PROGRAMMING TO THE EPROM ON THE MB89P637

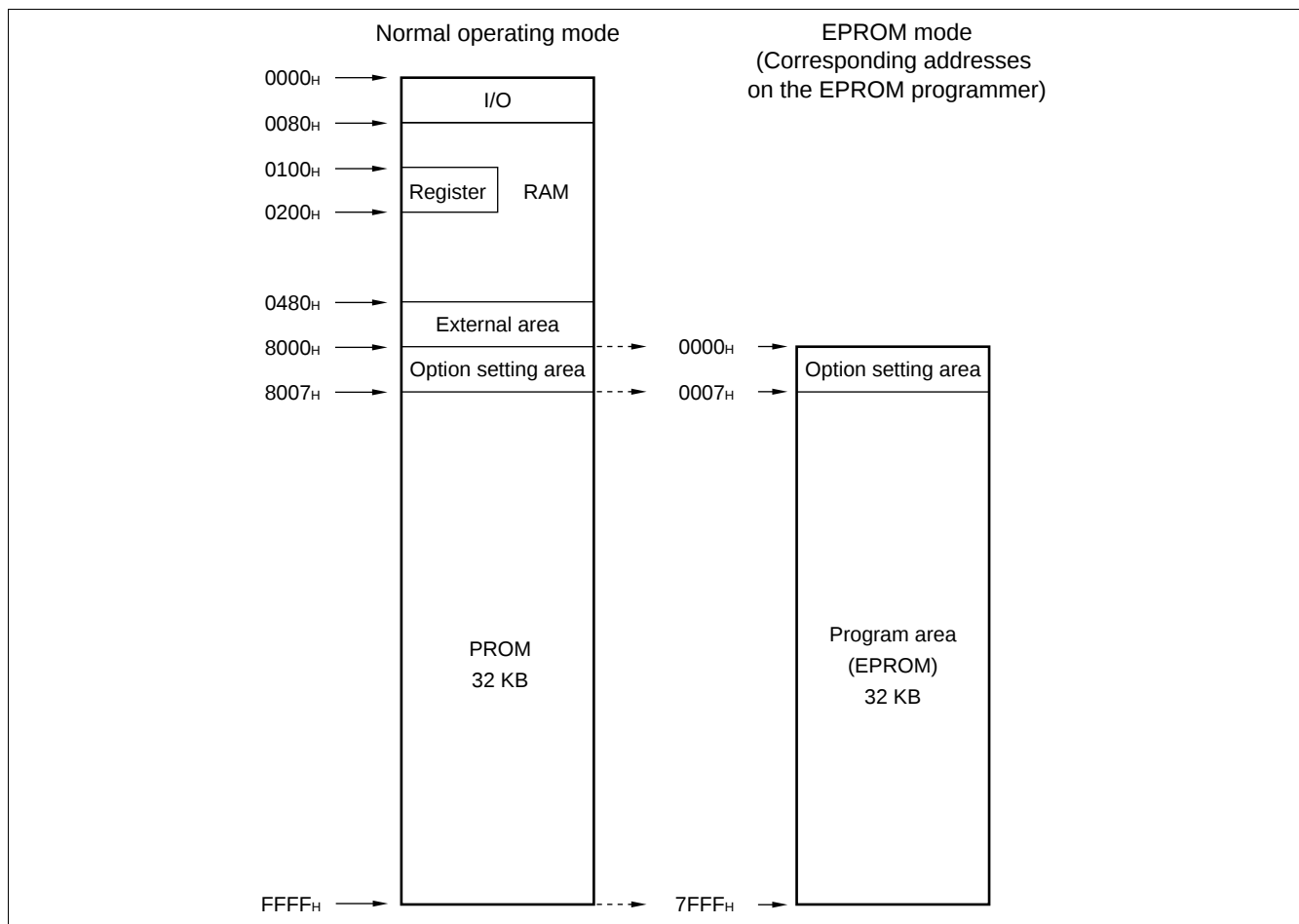
The MB89P637 is an OTPROM version of the MB89630 series.

### 1. Features

- 32-Kbytes PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

### 2. Memory Space

Memory space in each mode is illustrated below.



### 3. Programming to the EPROM

In EPROM mode, the MB89P637 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter.

However, the electronic signature mode cannot be used.

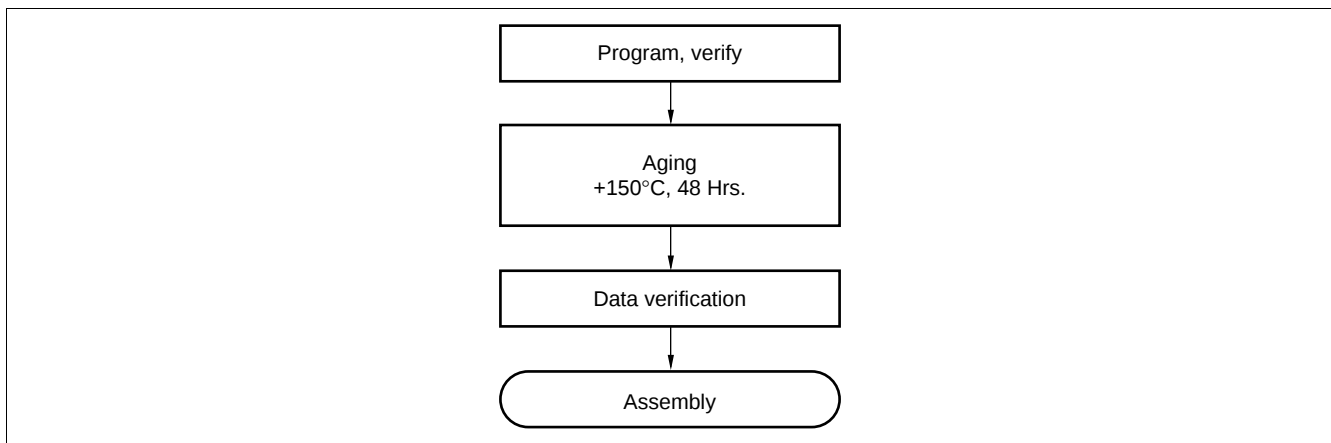
When the operating ROM area for a single chip is 32 Kbytes (8007H to FFFFH) the EPROM can be programmed as follows:

- **Programming procedure**

- (1) Set the EPROM programmer to the MBM27C256A-20CZ and MBM27C256A-20TV.
- (2) Load program data into the EPROM programmer at 0007<sub>H</sub> to 7FFF<sub>H</sub>. (Note that addresses 8000<sub>H</sub> to FFFF<sub>H</sub> in the operating mode assign to 0000<sub>H</sub> to 7FFF<sub>H</sub> in EPROM mode).
- (3) Load option data into addresses 0000<sub>H</sub> to 0006<sub>H</sub> of the EPROM programmer.  
(For information about each corresponding option, see "8. OTPROM Option Bit Map.")
- (4) Program with the EPROM programmer.

## 4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



## 5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## 6. Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm<sup>2</sup> is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/cm<sup>2</sup> for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure time will be much longer than with UV source at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

# MB89630R Series

## 7. EPROM Programmer Socket Adapter

|                                                   |                  |                  |
|---------------------------------------------------|------------------|------------------|
| Part No.                                          | MB89P637-SH      | MB89P637PF       |
| Package                                           | SH-DIP-64        | QFP-64           |
| Compatible socket adapter<br>Sun Hayato Co., Ltd. | ROM-64SD-28DP-8L | ROM-64QF-28DP-8L |

Inquiry: Sun Hayato Co., Ltd.: TEL : (81)-3-3986-0403  
FAX : (81)-3-5396-9106

## 8. OTPROM Option Bit Map

| Address           | Bit 7                                   | Bit 6                                   | Bit 5                                   | Bit 4                                   | Bit 3                                   | Bit 2                                   | Bit 1                                                       | Bit 0                                        |
|-------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-------------------------------------------------------------|----------------------------------------------|
| 0000 <sub>H</sub> | Vacancy                                 | Vacancy                                 | Vacancy                                 | Single/dual-<br>clock system            | Reset pin<br>output                     | Power-on<br>reset                       | Oscillation stabilization ( $f_{CH}$ )                      |                                              |
|                   | Readable<br>and writable                | Readable<br>and writable                | Readable<br>and writable                | 1: Dual clock<br>0: Single clock        | 1: Yes<br>0: No                         | 1: Yes<br>0: No                         | 11:2 <sup>18</sup> / $f_{CH}$ 01:2 <sup>17</sup> / $f_{CH}$ |                                              |
|                   |                                         |                                         |                                         |                                         |                                         |                                         | 10:2 <sup>14</sup> / $f_{CH}$ 00:2 <sup>4</sup> / $f_{CH}$  |                                              |
| 0001 <sub>H</sub> | P07<br>Pull-up<br>1: No<br>0: Yes       | P06<br>Pull-up<br>1: No<br>0: Yes       | P05<br>Pull-up<br>1: No<br>0: Yes       | P04<br>Pull-up<br>1: No<br>0: Yes       | P03<br>Pull-up<br>1: No<br>0: Yes       | P02<br>Pull-up<br>1: No<br>0: Yes       | P01<br>Pull-up<br>1: No<br>0: Yes                           | P00<br>Pull-up<br>1: No<br>0: Yes            |
| 0002 <sub>H</sub> | P17<br>Pull-up<br>1: No<br>0: Yes       | P16<br>Pull-up<br>1: No<br>0: Yes       | P15<br>Pull-up<br>1: No<br>0: Yes       | P14<br>Pull-up<br>1: No<br>0: Yes       | P13<br>Pull-up<br>1: No<br>0: Yes       | P12<br>Pull-up<br>1: No<br>0: Yes       | P11<br>Pull-up<br>1: No<br>0: Yes                           | P10<br>Pull-up<br>1: No<br>0: Yes            |
| 0003 <sub>H</sub> | P37<br>Pull-up<br>1: No<br>0: Yes       | P36<br>Pull-up<br>1: No<br>0: Yes       | P35<br>Pull-up<br>1: No<br>0: Yes       | P34<br>Pull-up<br>1: No<br>0: Yes       | P33<br>Pull-up<br>1: No<br>0: Yes       | P32<br>Pull-up<br>1: No<br>0: Yes       | P31<br>Pull-up<br>1: No<br>0: Yes                           | P30<br>Pull-up<br>1: No<br>0: Yes            |
| 0004 <sub>H</sub> | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | P43<br>Pull-up<br>1: No<br>0: Yes       | P42<br>Pull-up<br>1: No<br>0: Yes       | P41<br>Pull-up<br>1: No<br>0: Yes                           | P40<br>Pull-up<br>1: No<br>0: Yes            |
| 0005 <sub>H</sub> | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | P74<br>Pull-up<br>1: No<br>0: Yes       | P73<br>Pull-up<br>1: No<br>0: Yes       | P72<br>Pull-up<br>1: No<br>0: Yes       | Vacancy<br><br>Readable<br>and writable                     | Vacancy<br><br>Readable<br>and writable      |
| 0006 <sub>H</sub> | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable | Vacancy<br><br>Readable<br>and writable                     | Reserved bit<br><br>Readable<br>and writable |

Note: Each bit is set to '1' as the initialized value.

## ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20CZ, MBM27C256A-20TV

### 2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

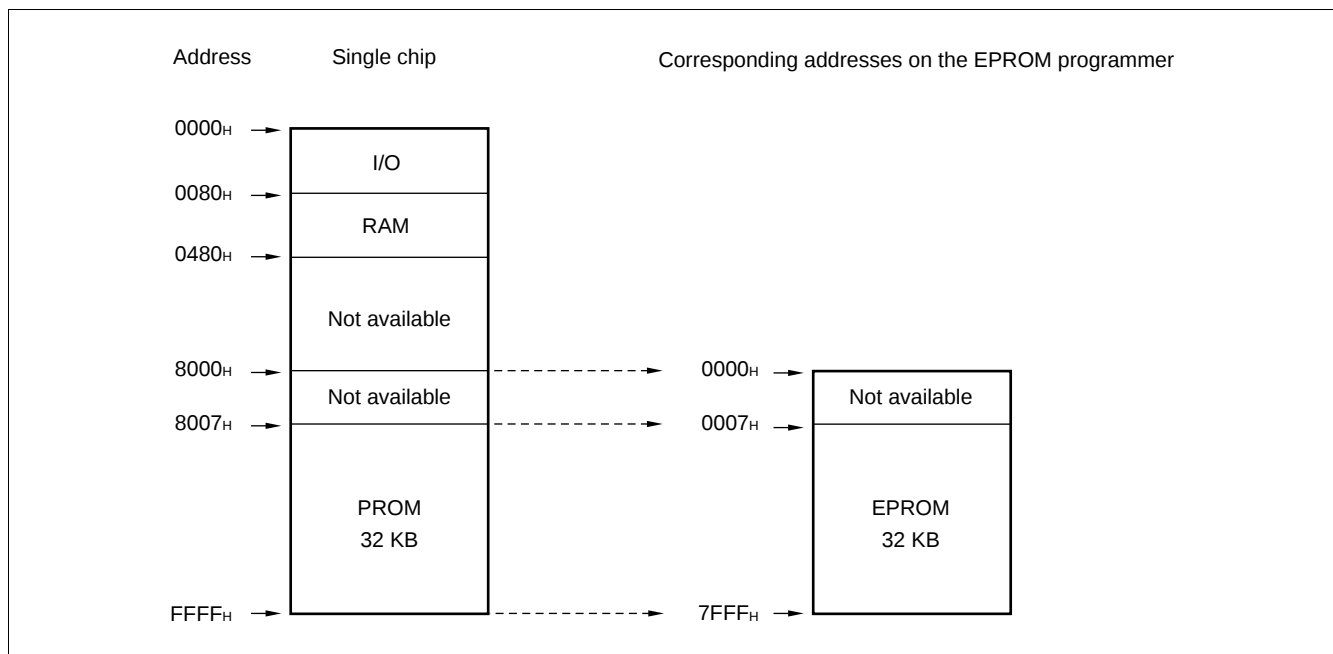
| Package            | Adapter socket part number |
|--------------------|----------------------------|
| LCC-32 (Rectangle) | ROM-32LC-28DP-YG           |

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403

FAX: (81)-3-5396-9106

### 3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.

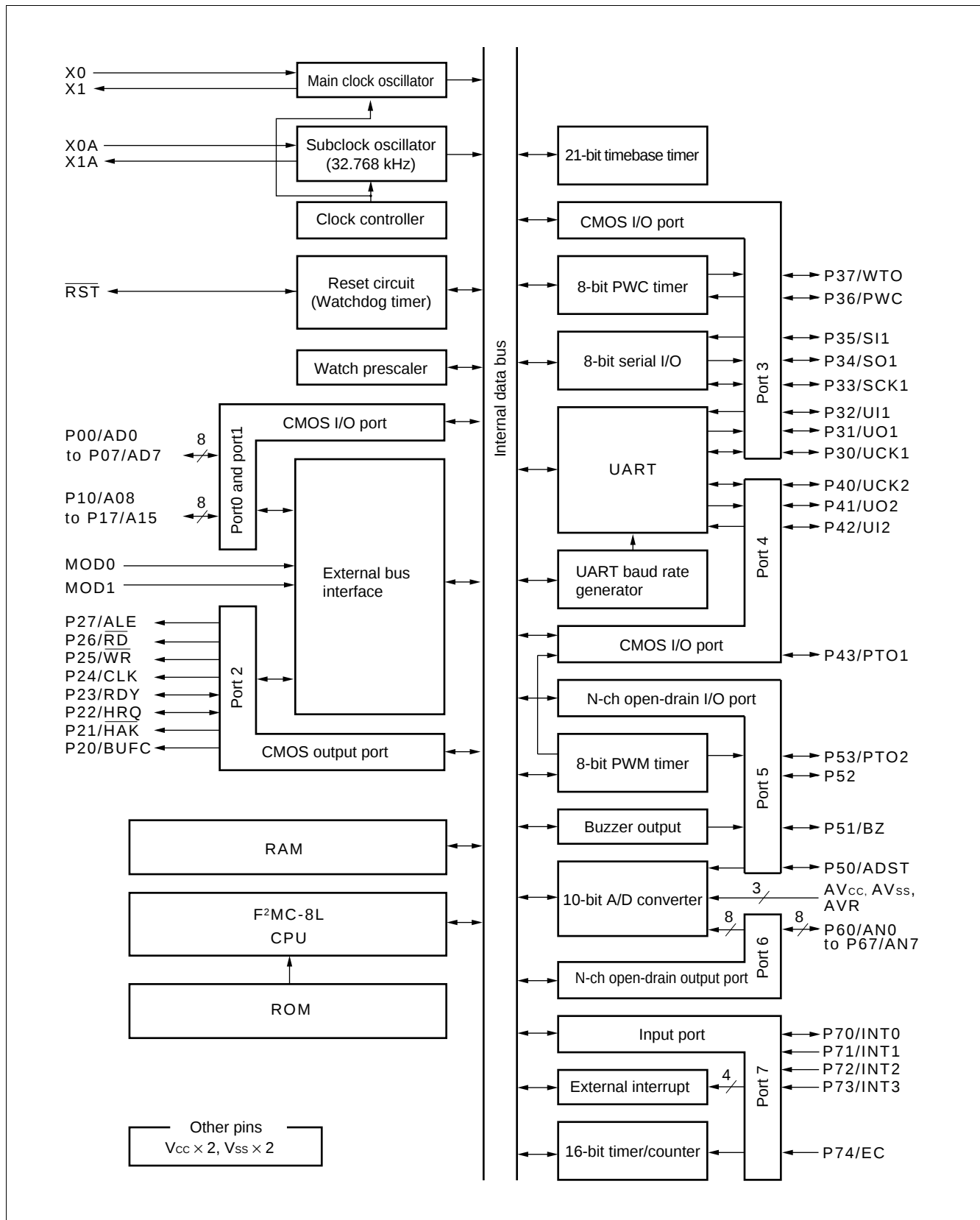


### 4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007<sub>H</sub> to 7FFF<sub>H</sub>.
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

# MB89630R Series

## ■ BLOCK DIAGRAM

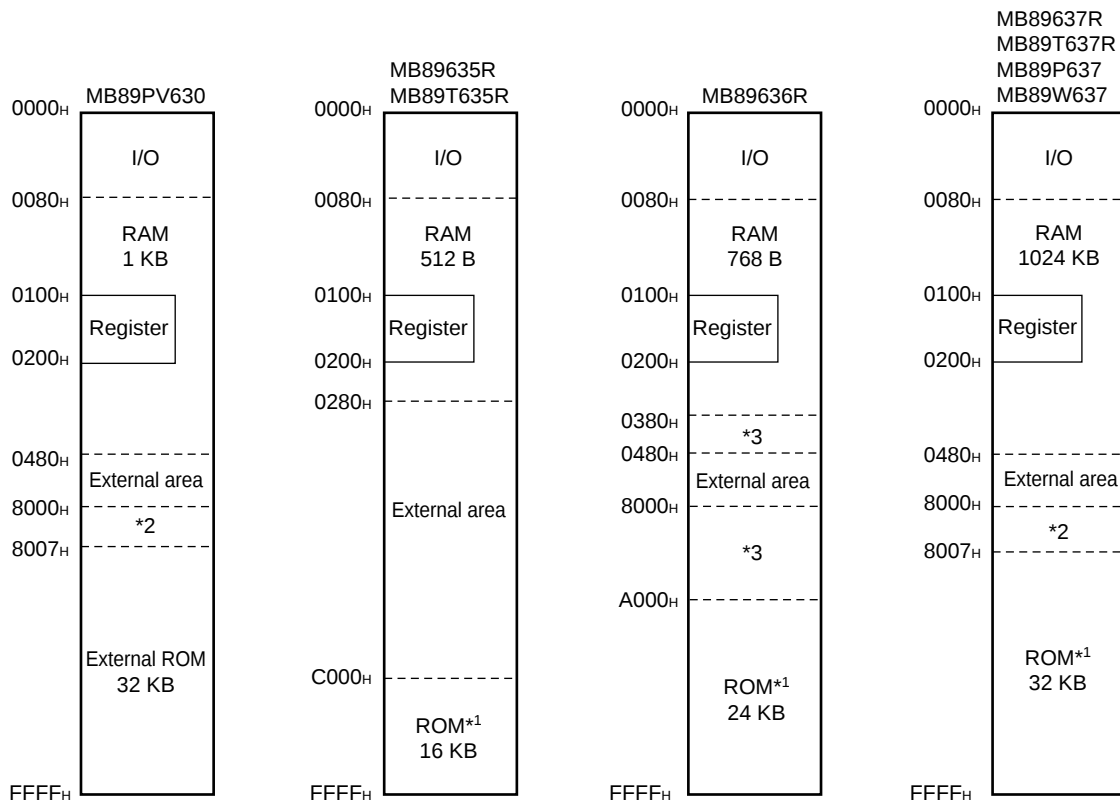


## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89630R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630R series is structured as illustrated below.

#### • Memory space



\*1: The ROM area is an external area depending on the mode.

The internal ROM cannot be used on the MB89T635R and MB89T637R.

\*2: Addresses 8000H to 8006H for the MB89P637 and MB89W637 comprise an option area, do not use this area for the MB89PV630 and MB89637R.

\*3: The access is forbidden in the external bus mode.

# MB89630R Series

## 2. Registers

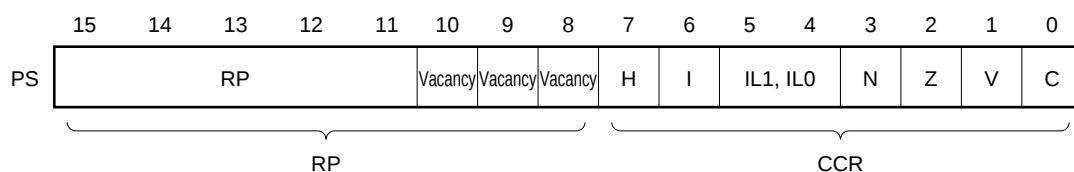
The F<sup>2</sup>MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

|                            |                                                                                                                                                                     |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Program counter (PC):      | A 16-bit register for indicating the instruction storage positions                                                                                                  |
| Accumulator (A):           | A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.           |
| Temporary accumulator (T): | A16-bit register which performs arithmetic operations with the accumulator<br>When the instruction is an 8-bit data processing instruction, the lower byte is used. |
| Index register (IX):       | A16-bit register for index modification                                                                                                                             |
| Extra pointer (EP):        | A16-bit pointer for indicating a memory address                                                                                                                     |
| Stack pointer (SP):        | A16-bit register for indicating a stack area                                                                                                                        |
| Program status (PS):       | A16-bit register for storing a register pointer, a condition code                                                                                                   |

| 16 bits |                         | Initial value                                                        |
|---------|-------------------------|----------------------------------------------------------------------|
| PC      | : Program counter       | FFFD <sub>H</sub>                                                    |
| A       | : Accumulator           | Indeterminate                                                        |
| T       | : Temporary accumulator | Indeterminate                                                        |
| IX      | : Index register        | Indeterminate                                                        |
| EP      | : Extra pointer         | Indeterminate                                                        |
| SP      | : Stack pointer         | Indeterminate                                                        |
| PS      | : Program status        | I-flag = 0, IL1, IL0 = 11<br>The other bit values are indeterminate. |

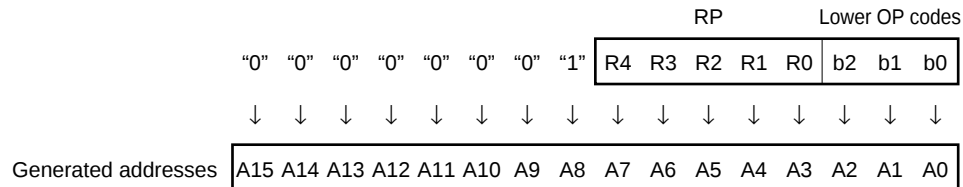
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

### • Structure of the program status register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for conversion of actual addresses of the general-purpose register area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

**H-flag:** Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

**I-flag:** Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | High-low                                                                            |
|-----|-----|-----------------|-------------------------------------------------------------------------------------|
| 0   | 0   | 1               | High                                                                                |
| 0   | 1   |                 |  |
| 1   | 0   | 2               |                                                                                     |
| 1   | 1   | 3               |                                                                                     |

**N-flag:** Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

**Z-flag:** Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

**V-flag:** Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow doesnot occur.

**C-flag:** Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.  
Set to the shift-out value in the case of a shift instruction.

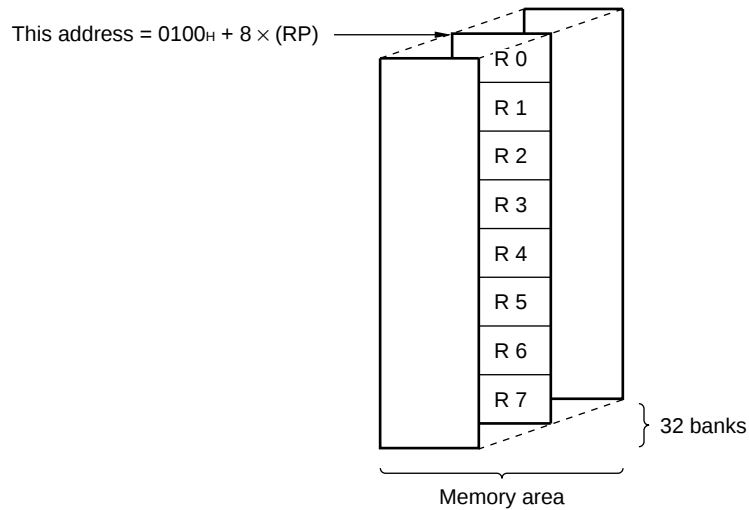
# MB89630R Series

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89653A (RAM  $512 \times 8$  bits). The bank currently in use is indicated by the register bank pointer (RP).

## • Register bank configuraiton



## ■ I/O MAP

| Address         | Read/write | Register name | Register description               |
|-----------------|------------|---------------|------------------------------------|
| 00 <sub>H</sub> | (R/W)      | PDR0          | Port 0 data register               |
| 01 <sub>H</sub> | (W)        | DDR0          | Port 0 data direction register     |
| 02 <sub>H</sub> | (R/W)      | PDR1          | Port 1 data register               |
| 03 <sub>H</sub> | (W)        | DDR1          | Port 1 data direction register     |
| 04 <sub>H</sub> | (R/W)      | PDR2          | Port 2 data register               |
| 05 <sub>H</sub> | (W)        | BCTR          | External bus pin control register  |
| 06 <sub>H</sub> | Vacancy    |               |                                    |
| 07 <sub>H</sub> | (R/W)      | SYCC          | System clock control register      |
| 08 <sub>H</sub> | (R/W)      | STBC          | System clock control register      |
| 09 <sub>H</sub> | (R/W)      | WDTE          | Watchdog timer control register    |
| 0A <sub>H</sub> | (R/W)      | TBCR          | Timebase timer control register    |
| 0B <sub>H</sub> | (R/W)      | WPCR          | Watch prescaler control register   |
| 0C <sub>H</sub> | (R/W)      | CHG3          | Port 3 switching register          |
| 0D <sub>H</sub> | (R/W)      | PDR3          | Port 3 data register               |
| 0E <sub>H</sub> | (W)        | DDR3          | Port 3 data direction register     |
| 0F <sub>H</sub> | (R/W)      | PDR4          | Port 4 data register               |
| 10 <sub>H</sub> | (W)        | DDR4          | Port 4 data direction register     |
| 11 <sub>H</sub> | (R/W)      | BUZR          | Buzzer register                    |
| 12 <sub>H</sub> | (R/W)      | PDR5          | Port 5 data register               |
| 13 <sub>H</sub> | (R/W)      | PDR6          | Port 6 data register               |
| 14 <sub>H</sub> | (R)        | PDR7          | Port 7 data register               |
| 15 <sub>H</sub> | (R/W)      | PCR1          | PWC pulse width control register 1 |
| 16 <sub>H</sub> | (R/W)      | PCR2          | PWC pulse width control register 2 |
| 17 <sub>H</sub> | (R/W)      | RLBR          | PWC reload buffer register         |
| 18 <sub>H</sub> | (R/W)      | TMCR          | 16-bit timer control register      |
| 19 <sub>H</sub> | (R/W)      | TCHR          | 16-bit timer count register (H)    |
| 1A <sub>H</sub> | (R/W)      | TCLR          | 16-bit timer count register (L)    |
| 1B <sub>H</sub> | Vacancy    |               |                                    |
| 1C <sub>H</sub> | (R/W)      | SMR1          | Serial mode register               |
| 1D <sub>H</sub> | (R/W)      | SDR1          | Serial data register               |
| 1E <sub>H</sub> | Vacancy    |               |                                    |
| 1F <sub>H</sub> | Vacancy    |               |                                    |

(Continued)

# MB89630R Series

(Continued)

| Address                            | Read/write | Register name | Register description                                                                |
|------------------------------------|------------|---------------|-------------------------------------------------------------------------------------|
| 20 <sub>H</sub>                    | (R/W)      | ADC1          | A/D converter control register 1                                                    |
| 21 <sub>H</sub>                    | (R/W)      | ADC2          | A/D converter control register 2                                                    |
| 22 <sub>H</sub>                    | (R/W)      | ADDH          | A/D converter data register (H)                                                     |
| 23 <sub>H</sub>                    | (R/W)      | ADDL          | A/D converter data register (L)                                                     |
| 24 <sub>H</sub>                    | (R/W)      | EIC1          | External interrupt control register 1                                               |
| 25 <sub>H</sub>                    | (R/W)      | EIC2          | External interrupt control register 2                                               |
| 26 <sub>H</sub>                    | Vacancy    |               |                                                                                     |
| 27 <sub>H</sub>                    | Vacancy    |               |                                                                                     |
| 28 <sub>H</sub>                    | (R/W)      | CNTR1         | PWM timer control register 1                                                        |
| 29 <sub>H</sub>                    | (R/W)      | CNTR2         | PWM timer control register 2                                                        |
| 2A <sub>H</sub>                    | (R/W)      | CNTR3         | PWM timer control register 3                                                        |
| 2B <sub>H</sub>                    | (W)        | COMR1         | PWM timer compare register 1                                                        |
| 2C <sub>H</sub>                    | (W)        | COMR2         | PWM timer compare register 2                                                        |
| 2D <sub>H</sub>                    | (R/W)      | SMC           | UART serial mode control register                                                   |
| 2E <sub>H</sub>                    | (R/W)      | SRC           | UART serial rate control register                                                   |
| 2F <sub>H</sub>                    | (R/W)      | SSD           | UART serial status/data register                                                    |
| 30 <sub>H</sub>                    | (R)<br>(W) | SIDR<br>SODR  | UART serial input data control register<br>UART serial output data control register |
| 31 <sub>H</sub> to 7B <sub>H</sub> | Vacancy    |               |                                                                                     |
| 7C <sub>H</sub>                    | (W)        | ILR1          | Interrupt level setting register 1                                                  |
| 7D <sub>H</sub>                    | (W)        | ILR2          | Interrupt level setting register 2                                                  |
| 7E <sub>H</sub>                    | (W)        | ILR3          | Interrupt level setting register 3                                                  |
| 7F <sub>H</sub>                    | Vacancy    |               |                                                                                     |

Note: Do not use vacancies.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

(AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V)

| Parameter                              | Symbol             | Value                 |                       | Unit | Remarks                                            |
|----------------------------------------|--------------------|-----------------------|-----------------------|------|----------------------------------------------------|
|                                        |                    | Min.                  | Max.                  |      |                                                    |
| Power supply voltage                   | V <sub>CC</sub>    | V <sub>SS</sub> − 0.3 | V <sub>SS</sub> + 7.0 | V    | *                                                  |
|                                        | AV <sub>CC</sub>   | V <sub>SS</sub> − 0.3 | V <sub>SS</sub> + 7.0 | V    | *                                                  |
| A/D converter reference input voltage  | AVR                | V <sub>SS</sub> − 0.3 | V <sub>SS</sub> + 7.0 | V    | AVR must not exceed "AV <sub>CC</sub> + 0.3 V".    |
| Input voltage                          | V <sub>I</sub>     | V <sub>SS</sub> − 0.3 | V <sub>CC</sub> + 0.3 | V    | Except P50 to P53                                  |
|                                        | V <sub>I2</sub>    | V <sub>SS</sub> − 0.3 | V <sub>SS</sub> + 7.0 | V    | P50 to P53                                         |
| Output voltage                         | V <sub>O</sub>     | V <sub>SS</sub> − 0.3 | V <sub>CC</sub> + 0.3 | V    | Except P50 to P53                                  |
|                                        | V <sub>O2</sub>    | V <sub>SS</sub> − 0.3 | V <sub>SS</sub> + 7.0 | V    | P50 to P53                                         |
| "L" level maximum output current       | I <sub>OL</sub>    | —                     | 20                    | mA   |                                                    |
| "L" level average output current       | I <sub>OLAV</sub>  | —                     | 4                     | mA   | Average value (operating current × operating rate) |
| "L" level total maximum output current | ΣI <sub>OL</sub>   | —                     | 100                   | mA   |                                                    |
| "L" level total average output current | ΣI <sub>OLAV</sub> | —                     | 40                    | mA   | Average value (operating current × operating rate) |
| "H" level maximum output current       | I <sub>OH</sub>    | —                     | −20                   | mA   |                                                    |
| "H" level average output current       | I <sub>OHAV</sub>  | —                     | −4                    | mA   | Average value (operating current × operating rate) |
| "H" level total maximum output current | ΣI <sub>OH</sub>   | —                     | −50                   | mA   |                                                    |
| "H" level total average output current | ΣI <sub>OHAV</sub> | —                     | −20                   | mA   | Average value (operating current × operating rate) |
| Power consumption                      | P <sub>D</sub>     | —                     | 500                   | mW   |                                                    |
| Operating temperature                  | T <sub>A</sub>     | −40                   | +85                   | °C   |                                                    |
| Storage temperature                    | T <sub>stg</sub>   | −55                   | +150                  | °C   |                                                    |

\* : Use AV<sub>CC</sub> and V<sub>CC</sub> set at the same voltage.

Take care so that AV<sub>CC</sub> does not exceed V<sub>CC</sub>, such as when power is turned on.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB89630R Series

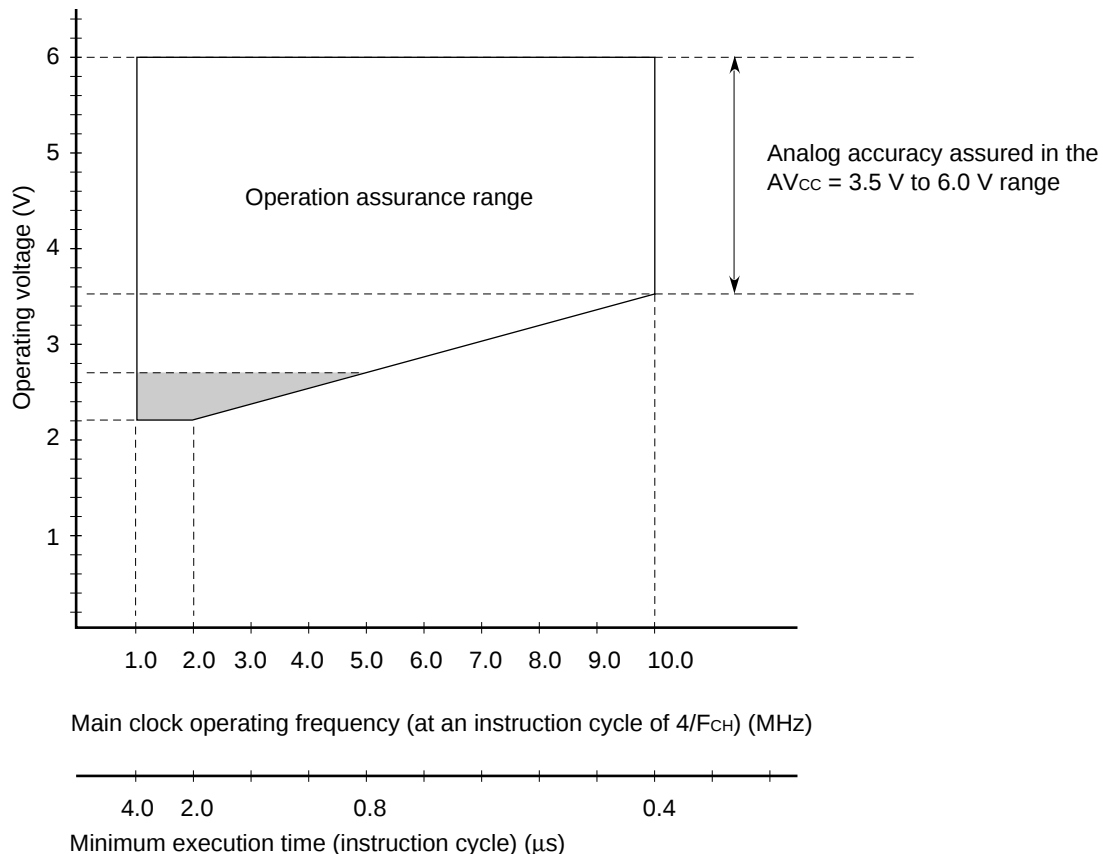
## 2. Recommended Operating Conditions

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ )

| Parameter                             | Symbol    | Value |           | Unit | Remarks                                                           |
|---------------------------------------|-----------|-------|-----------|------|-------------------------------------------------------------------|
|                                       |           | Min.  | Max       |      |                                                                   |
| Power supply voltage                  | $V_{CC}$  | 2.2*  | 6.0*      | V    | Normal operation assurance range* MB89635R/637R                   |
|                                       |           | 2.7*  | 6.0*      | V    | Normal operation assurance range* MB89PV630/P637/W637/T635R/T637R |
|                                       | $AV_{CC}$ | 1.5   | 6.0       | V    | Retains the RAM state in stop mode                                |
| A/D converter reference input voltage | $AVR$     | 3.0   | $AV_{CC}$ | V    |                                                                   |
| Operating temperature                 | $T_A$     | -40   | +85       | °C   |                                                                   |

\* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

**Figure 1 Operating Voltage vs. Main Clock Operating Frequency**



Note: The shaded area is assured only for the MB89635R/636R/637R.

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of  $4/F_{CH}$ . Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB89630R Series

## 3. DC Characteristics

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                                           | Symbol     | Pin name                                                                                             | Condition                     | Value          |      |                | Unit          | Remarks                          |
|-----------------------------------------------------|------------|------------------------------------------------------------------------------------------------------|-------------------------------|----------------|------|----------------|---------------|----------------------------------|
|                                                     |            |                                                                                                      |                               | Min.           | Typ. | Max.           |               |                                  |
| “H” level input voltage                             | $V_{IH1}$  | P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53                                | —                             | $0.7 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             | P51 to P53 with pull-up resistor |
|                                                     | $V_{IH2}$  | P51 to P53                                                                                           |                               | $0.7 V_{CC}$   | —    | $V_{SS} + 6.0$ | V             | Without pull-up resistor         |
|                                                     | $V_{IHS}$  | $\overline{RST}$ , MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42, P50, P72 to P74                    |                               | $0.8 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             | P50 with pull-up resistor        |
|                                                     | $V_{IHS2}$ | P50, P70, P71                                                                                        |                               | $0.8 V_{CC}$   | —    | $V_{SS} + 6.0$ | V             | Without pull-up resistor         |
| “L” level input voltage                             | $V_{IL}$   | P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43                                            | —                             | $V_{SS} - 0.3$ | —    | $0.3 V_{CC}$   | V             |                                  |
|                                                     | $V_{ILS}$  | P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$ , MOD0, MOD1             |                               | $V_{SS} - 0.3$ | —    | $0.2 V_{CC}$   | V             |                                  |
| Open-drain output pin application voltage           | $V_D$      | P50 to P53                                                                                           |                               | $V_{SS} - 0.3$ | —    | $V_{SS} + 6.0$ | V             |                                  |
| “H” level output voltage                            | $V_{OH}$   | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43                                           | $I_{OH} = -2.0\text{ mA}$     | 4.0            | —    | —              | V             |                                  |
| “L” level output voltage                            | $V_{OL}$   | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, $\overline{RST}$ | $I_{OL} = 4.0\text{ mA}$      | —              | —    | 0.4            | V             |                                  |
| Input leakage current (Hi-z output leakage current) | $I_{LI}$   | P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1       | $0.0\text{ V} < V_I < V_{CC}$ | —              | —    | $\pm 5$        | $\mu\text{A}$ | Without pull-up resistor         |

(Continued)

# MB89630R Series

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter              | Symbol            | Pin name                                                               | Condition                                                                                                               | Value                                                                                |      |      | Unit          | Remarks                              |  |
|------------------------|-------------------|------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------|------|---------------|--------------------------------------|--|
|                        |                   |                                                                        |                                                                                                                         | Min.                                                                                 | Typ. | Max. |               |                                      |  |
| Pull-up resistance     | R <sub>PULL</sub> | P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74 | V <sub>I</sub> = 0.0 V                                                                                                  | 25                                                                                   | 50   | 100  | kΩ            | With pull-up resistor                |  |
| Power supply current*1 | I <sub>CC1</sub>  | V <sub>CC</sub>                                                        | F <sub>CH</sub> = 10 MHz<br>V <sub>CC</sub> = 5.0 V<br>t <sub>inst</sub> *2 = 0.4 μs                                    | —                                                                                    | 12   | 20   | mA            |                                      |  |
|                        | I <sub>CC2</sub>  |                                                                        | F <sub>CH</sub> = 10 MHz<br>V <sub>CC</sub> = 3.0 V<br>t <sub>inst</sub> *2 = 6.4 μs                                    | —                                                                                    | 1.0  | 2    | mA            | MB89635R/T635R/636R/637R/T637R/PV630 |  |
|                        |                   |                                                                        | —                                                                                                                       | 1.5                                                                                  | 2.5  | mA   | MB89P637/W637 |                                      |  |
|                        | I <sub>CCS1</sub> |                                                                        | Sleep mode                                                                                                              | F <sub>CH</sub> = 10 MHz<br>V <sub>CC</sub> = 5.0 V<br>t <sub>inst</sub> *2 = 0.4 μs | —    | 3    | 7             | mA                                   |  |
|                        | I <sub>CCS2</sub> |                                                                        |                                                                                                                         | F <sub>CH</sub> = 10 MHz<br>V <sub>CC</sub> = 3.0 V<br>t <sub>inst</sub> *2 = 6.4 μs | —    | 0.5  | 1.5           | mA                                   |  |
|                        | I <sub>CCL</sub>  |                                                                        | F <sub>CL</sub> = 32.768 kHz,<br>V <sub>CC</sub> = 3.0 V<br>Subclock mode                                               | —                                                                                    | 50   | 100  | μA            | MB89635R/T635R/636R/637R/T637R/PV630 |  |
|                        |                   |                                                                        |                                                                                                                         | —                                                                                    | 500  | 700  | μA            | MB89P637/W637                        |  |
|                        | I <sub>CCLS</sub> |                                                                        | F <sub>CL</sub> = 32.768 kHz,<br>V <sub>CC</sub> = 3.0 V<br>Subclock sleep mode                                         | —                                                                                    | 25   | 50   | μA            |                                      |  |
|                        | I <sub>CCT</sub>  |                                                                        | F <sub>CL</sub> = 32.768 kHz,<br>V <sub>CC</sub> = 3.0 V<br>• Watch mode<br>• Main clock stop mode at dual-clock system | —                                                                                    | 3    | 15   | μA            |                                      |  |
|                        | I <sub>CCH</sub>  |                                                                        | T <sub>A</sub> = +25°C<br>• Subclock stop mode<br>• Main clock stop mode at single-clock system                         | —                                                                                    | —    | 1    | μA            |                                      |  |

(Continued)

# MB89630R Series

(Continued)

( $AV_{CC} = V_{CC} = 5.0\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter              | Symbol   | Pin name                                                      | Condition                                                                                         | Value |      |      | Unit          | Remarks |
|------------------------|----------|---------------------------------------------------------------|---------------------------------------------------------------------------------------------------|-------|------|------|---------------|---------|
|                        |          |                                                               |                                                                                                   | Min.  | Typ. | Max. |               |         |
| Power supply current*1 | $I_A$    | $AV_{CC}$                                                     | $F_{CH} = 10\text{ MHz}$ ,<br>when A/D<br>conversion<br>operates.                                 | —     | 6    | —    | mA            |         |
|                        | $I_{AH}$ |                                                               | $F_{CH} = 10\text{ MHz}$ ,<br>$T_A = +25^\circ\text{C}$ ,<br>when A/D<br>conversion in<br>a stop. | —     | —    | 1    | $\mu\text{A}$ |         |
| Input capacitance      | $C_{IN}$ | Other than $AV_{CC}$ ,<br>$AV_{SS}$ , $V_{CC}$ , and $V_{SS}$ | $f = 1\text{ MHz}$                                                                                | —     | 10   | —    | pF            |         |

\*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

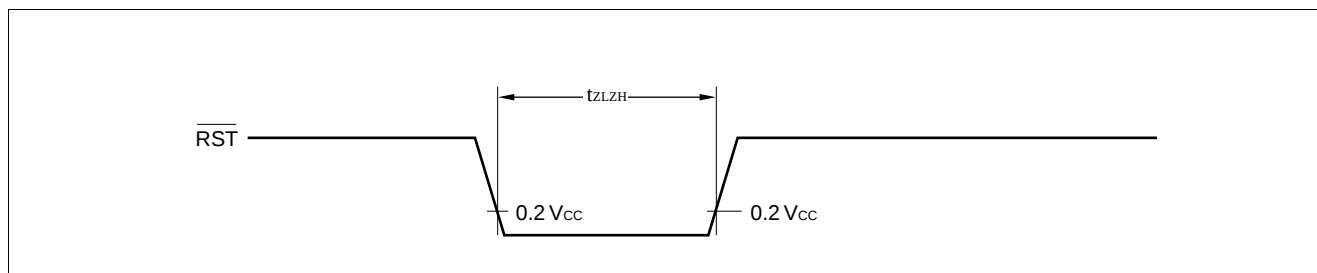
\*2: For information on  $t_{inst}$ , see “(4) Instruction Cycle” in “4. AC Characteristics.”

## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                               | Symbol     | Condition | Value          |      | Unit | Remarks |
|-----------------------------------------|------------|-----------|----------------|------|------|---------|
|                                         |            |           | Min.           | Max. |      |         |
| $\overline{\text{RST}}$ “L” pulse width | $t_{ZLZH}$ | —         | $48\ t_{HCYL}$ | —    | ns   |         |



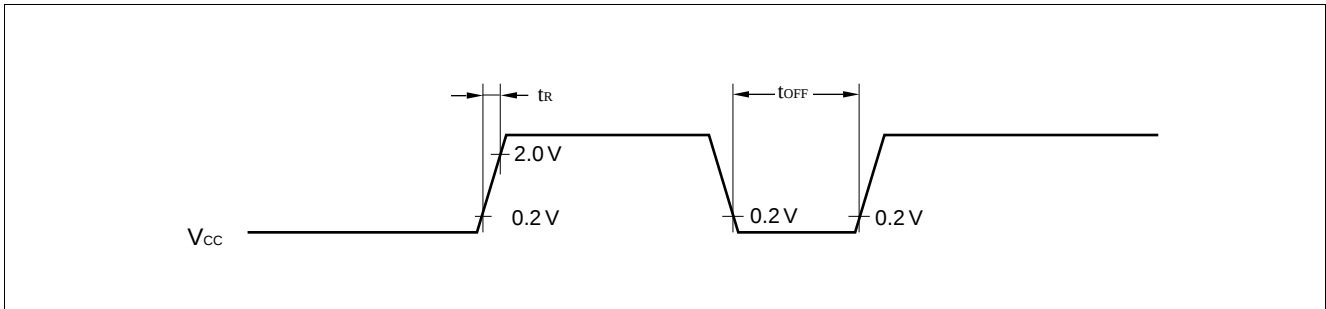
## (2) Specification for Power-on Reset

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                 | Symbol    | Condition | Value |      | Unit | Remarks                                        |
|---------------------------|-----------|-----------|-------|------|------|------------------------------------------------|
|                           |           |           | Min.  | Max. |      |                                                |
| Power supply rising time  | $t_R$     | —         | —     | 50   | ms   | Power-on reset function only                   |
| Power supply cut-off time | $t_{OFF}$ |           | 1     | —    | ms   | Min. interval time for the next power-on reset |

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



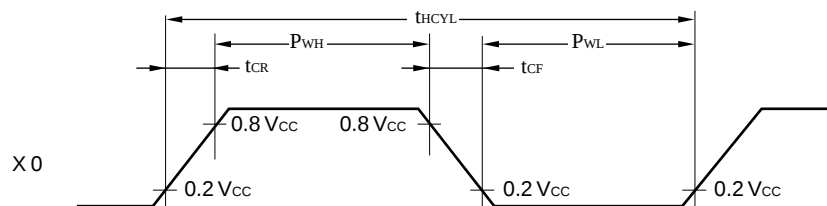
## (3) Clock Timing

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

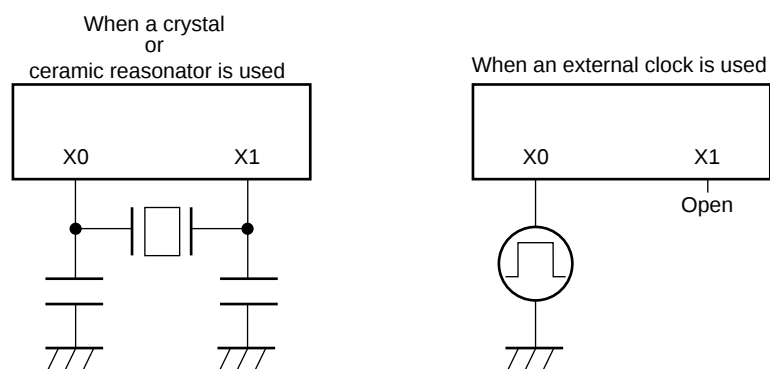
| Parameter                       | Symbol                 | Pin name | Condition | Value |        |      | Unit          | Remarks        |
|---------------------------------|------------------------|----------|-----------|-------|--------|------|---------------|----------------|
|                                 |                        |          |           | Min.  | Typ.   | Max. |               |                |
| Clock frequency                 | $F_{CH}$               | X0, X1   | —         | 1     | —      | 10   | MHz           |                |
|                                 | $F_{CL}$               | X0A, X1A |           | —     | 32.768 | —    | kHz           |                |
| Clock cycle time                | $t_{HCYL}$             | X0, X1   |           | 100   | —      | 1000 | ns            |                |
|                                 | $t_{LCYL}$             | X0A, X1A |           | —     | 30.5   | —    | $\mu\text{s}$ |                |
| Input clock pulse width         | $P_{WH}$<br>$P_{WL}$   | X0       |           | 20    | —      | —    | ns            | External clock |
|                                 | $P_{WLH}$<br>$P_{WLL}$ | X0A      |           | —     | 15.2   | —    | $\mu\text{s}$ | External clock |
| Input clock rising/falling time | $t_{CR}$<br>$t_{CF}$   | X0       |           | —     | —      | 10   | ns            | External clock |

# MB89630R Series

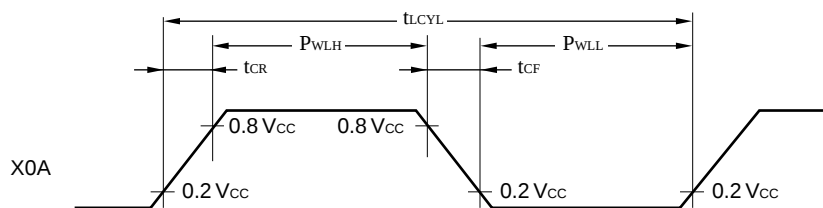
## • Main clock timing condition



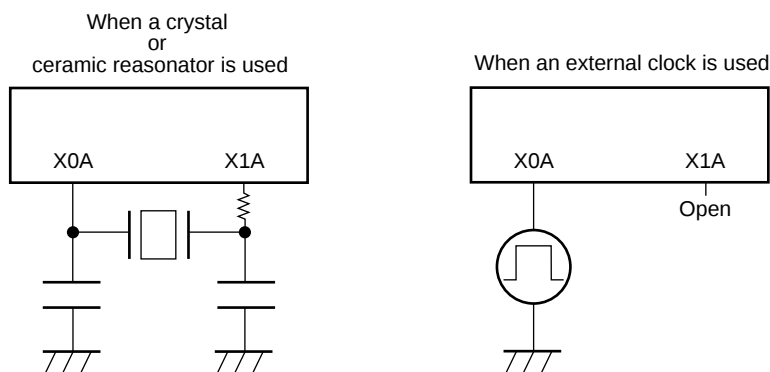
## • Main clock configurations



## • Subclock timing condition



## • Subclock configurations



## (4) Instruction Cycle

| Parameter                                     | Symbol     | Value (typical)                                     | Unit    | Remarks                                                                    |
|-----------------------------------------------|------------|-----------------------------------------------------|---------|----------------------------------------------------------------------------|
| Instruction cycle<br>(minimum execution time) | $t_{inst}$ | $4/F_{CH}$ , $8/F_{CH}$ , $16/F_{CH}$ , $64/F_{CH}$ | $\mu s$ | $(4/F_{CH}) t_{inst} = 0.4 \mu s$ , operating at $F_{CH} = 10 \text{ MHz}$ |
|                                               |            | $2/F_{CL}$                                          | $\mu s$ | $t_{inst} = 61.036 \mu s$ , operating at $F_{CL} = 32.768 \text{ kHz}$     |

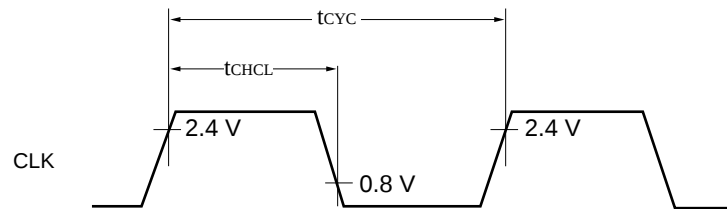
Note: Operating at 10 MHz, the cycle varies with the set execution time.

## (5) Clock Output Timing

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                                   | Symbol     | Pin name | Condition | Value                            |                  | Unit    | Remarks |
|---------------------------------------------|------------|----------|-----------|----------------------------------|------------------|---------|---------|
|                                             |            |          |           | Min.                             | Max.             |         |         |
| Clock time                                  | $t_{CYC}$  | CLK      | —         | $1/2 t_{inst}^*$                 | —                | $\mu s$ |         |
| CLK $\uparrow \rightarrow$ CLK $\downarrow$ | $t_{CHCL}$ | CLK      |           | $1/4 t_{inst}^* - 70 \text{ ns}$ | $1/4 t_{inst}^*$ | $\mu s$ |         |

\* : For information on  $t_{inst}$ , see “(4) Instruction Cycle.”



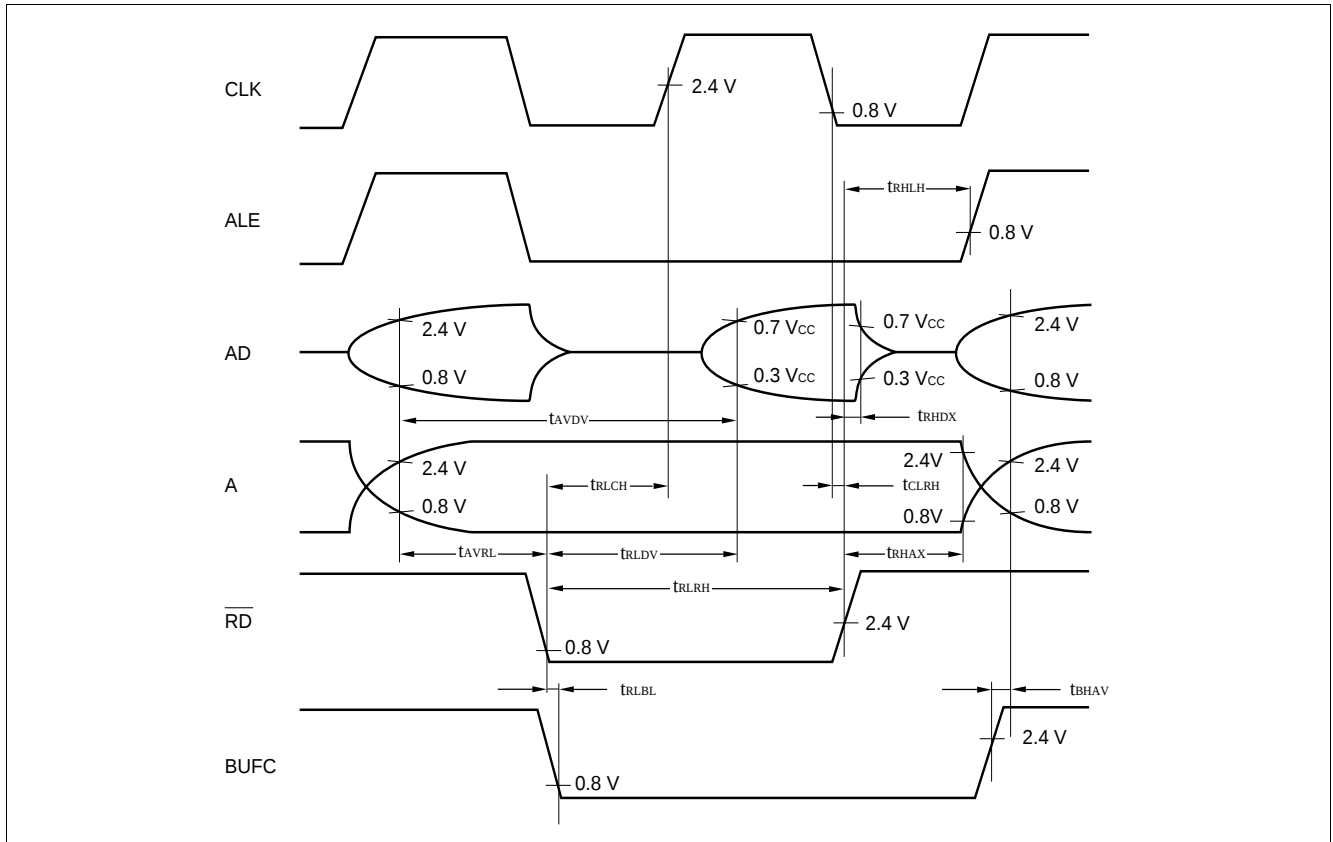
# MB89630R Series

## (6) Bus Read Timing

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , 10 MHz,  $V_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                                                                 | Symbol             | Pin name                                           | Condition | Value                                   |      | Unit          | Remarks |
|---------------------------------------------------------------------------|--------------------|----------------------------------------------------|-----------|-----------------------------------------|------|---------------|---------|
|                                                                           |                    |                                                    |           | Min.                                    | Max. |               |         |
| Valid address $\rightarrow \overline{\text{RD}} \downarrow$ time          | $t_{\text{AVRL}}$  | $\overline{\text{RD}}$ , A15 to A08,<br>AD7 to AD0 | —         | $1/4 t_{\text{inst}}^* - 64 \text{ ns}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{RD}}$ pulse width                                        | $t_{\text{RLRH}}$  | $\overline{\text{RD}}$                             |           | $1/2 t_{\text{inst}}^* - 20 \text{ ns}$ | —    | $\mu\text{s}$ |         |
| Valid address $\rightarrow$ data read time                                | $t_{\text{AVDV}}$  | AD7 to AD0,<br>A15 to A08                          |           | $1/2 t_{\text{inst}}^*$                 | 200  | $\mu\text{s}$ | No wait |
| $\overline{\text{RD}} \downarrow \rightarrow$ data read time              | $t_{\text{RLDV}}$  | $\overline{\text{RD}}$ , AD7 to AD0                |           | $1/2 t_{\text{inst}}^* - 80 \text{ ns}$ | 120  | $\mu\text{s}$ | No wait |
| $\overline{\text{RD}} \uparrow \rightarrow$ data hold time                | $t_{\text{RHDX}}$  | AD7 to AD0,<br>$\overline{\text{RD}}$              |           | 0                                       | —    | $\mu\text{s}$ |         |
| $\overline{\text{RD}} \uparrow \rightarrow \text{ALE} \uparrow$ time      | $t_{\text{RHLH}}$  | $\overline{\text{RD}}$ , ALE                       |           | $1/4 t_{\text{inst}}^* - 40 \text{ ns}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{RD}} \uparrow \rightarrow$ address loss time             | $t_{\text{RHAX}}$  | $\overline{\text{RD}}$ , A15 to A08                |           | $1/4 t_{\text{inst}}^* - 40 \text{ ns}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{RD}} \downarrow \rightarrow \text{CLK} \uparrow$ time    | $t_{\text{RLCH}}$  | $\overline{\text{RD}}$ , CLK                       |           | $1/4 t_{\text{inst}}^* - 40 \text{ ns}$ | —    | $\mu\text{s}$ |         |
| CLK $\downarrow \rightarrow \overline{\text{RD}} \uparrow$ time           | $t_{\text{CLR H}}$ | $\overline{\text{RD}}$ , CLK                       |           | 0                                       | —    | ns            |         |
| $\overline{\text{RD}} \downarrow \rightarrow \text{BUFC} \downarrow$ time | $t_{\text{RLBL}}$  | $\overline{\text{RD}}$ , BUFC                      |           | -5                                      | —    | $\mu\text{s}$ |         |
| BUFC $\uparrow \rightarrow$ valid address time                            | $t_{\text{BHAV}}$  | A15 to A08,<br>AD7 to AD0,<br>BUFC                 |           | 5                                       | —    | $\mu\text{s}$ |         |

\* : For information on  $t_{\text{inst}}$ , see “(4) Instruction Cycle.”



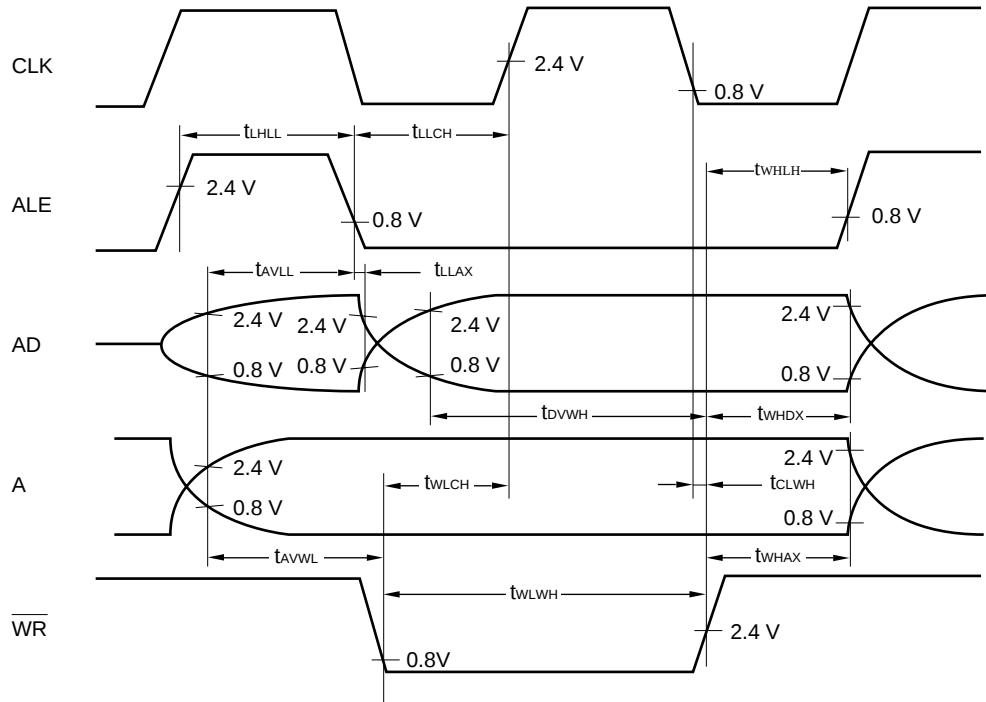
## (7) Bus Write Timing

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $F_{CH} = 10 \text{ MHz}$ ,  $A_{VSS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                                                         | Symbol     | Pin name                            | Condition | Value                                    |      | Unit          | Remarks |
|-------------------------------------------------------------------|------------|-------------------------------------|-----------|------------------------------------------|------|---------------|---------|
|                                                                   |            |                                     |           | Min.                                     | Max. |               |         |
| Valid address $\rightarrow$ ALE $\downarrow$ time                 | $t_{AVLL}$ | AD7 to AD0,<br>ALE                  | —         | $1/4 t_{inst}^{*1} - 64 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| ALE $\downarrow$ time $\rightarrow$ address loss time             | $t_{LLAX}$ | A15 to A08                          |           | 5                                        | —    | ns            |         |
| Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time  | $t_{AVWL}$ | $\overline{\text{WR}}$ , ALE        |           | $1/4 t_{inst}^{*1} - 60 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{WR}}$ pulse width                                | $t_{WLWH}$ | $\overline{\text{WR}}$              |           | $1/2 t_{inst}^{*1} - 20 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| Write data $\rightarrow \overline{\text{WR}} \uparrow$ time       | $t_{DVWH}$ | AD7 to AD0, $\overline{\text{WR}}$  |           | $1/2 t_{inst}^{*1} - 60 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{WR}} \uparrow \rightarrow$ address loss time     | $t_{WHAX}$ | $\overline{\text{WR}}$ , A15 to A08 |           | $1/4 t_{inst}^{*1} - 40 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{WR}} \uparrow \rightarrow$ data hold time        | $t_{WHDX}$ | AD7 to AD0, $\overline{\text{WR}}$  |           | $1/4 t_{inst}^{*1} - 40 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{WR}} \uparrow \rightarrow$ ALE $\uparrow$ time   | $t_{WHLH}$ | $\overline{\text{WR}}$ , ALE        |           | $1/4 t_{inst}^{*1} - 40 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| $\overline{\text{WR}} \downarrow \rightarrow$ CLK $\uparrow$ time | $t_{WLCH}$ | $\overline{\text{WR}}$ , CLK        |           | $1/4 t_{inst}^{*1} - 40 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| CLK $\downarrow \rightarrow \overline{\text{WR}} \uparrow$ time   | $t_{CLWH}$ | $\overline{\text{WR}}$ , CLK        |           | 0                                        | —    | ns            |         |
| ALE pulse width                                                   | $t_{LHLL}$ | ALE                                 |           | $1/4 t_{inst}^{*1} - 35 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |
| ALE $\downarrow \rightarrow$ CLK $\uparrow$ time                  | $t_{LLCH}$ | ALE, CLK                            |           | $1/4 t_{inst}^{*1} - 30 \text{ ns}^{*2}$ | —    | $\mu\text{s}$ |         |

\*1: For information on  $t_{inst}$ , see “(4) Instruction Cycle.”

\*2: This characteristics are also applicable to the bus read timing.



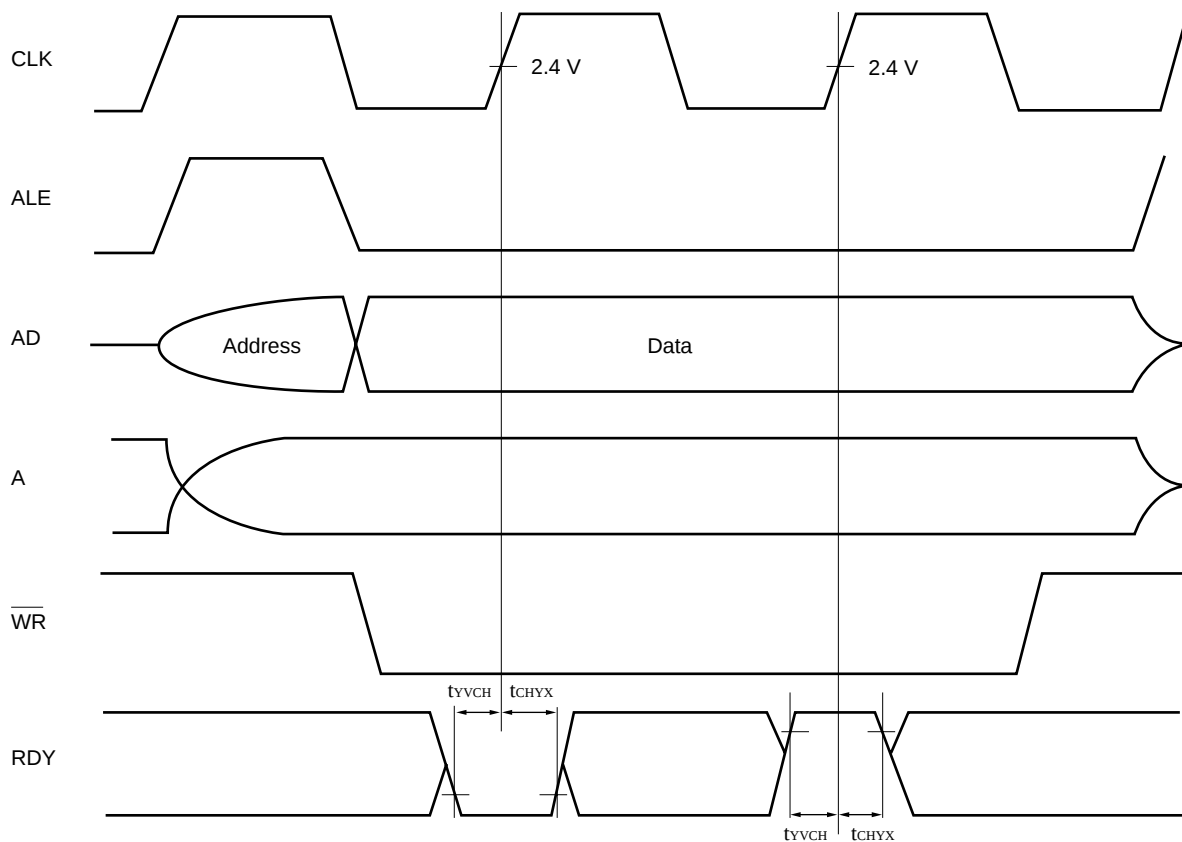
# MB89630R Series

## (8) Ready Input Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $F_{CH} = 10\text{ MHz}$ ,  $A_{VSS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                                   | Symbol     | Pin name | Condition | Value |      | Unit | Remarks |
|---------------------------------------------|------------|----------|-----------|-------|------|------|---------|
|                                             |            |          |           | Min.  | Max. |      |         |
| RDY valid $\rightarrow$ CLK $\uparrow$ time | $t_{YVCH}$ | RDY, CLK | —         | 60    | —    | ns   | *       |
| CLK $\uparrow \rightarrow$ RDY loss time    | $t_{CHYX}$ |          |           | 0     | —    | ns   | *       |

\* : This characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

## (9) Serial I/O Timing

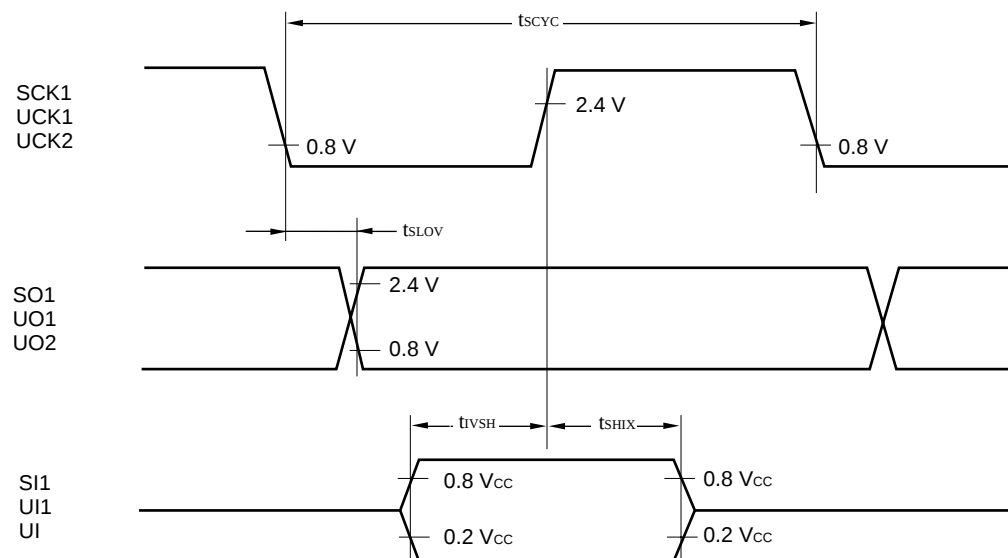
(V<sub>CC</sub> = 5.0 V $\pm$ 10%, F<sub>CH</sub> = 10 MHz, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

| Parameter                                                                                    | Symbol            | Pin name                            | Condition                       | Value                   |      | Unit | Remarks |
|----------------------------------------------------------------------------------------------|-------------------|-------------------------------------|---------------------------------|-------------------------|------|------|---------|
|                                                                                              |                   |                                     |                                 | Min.                    | Max. |      |         |
| Serial clock cycle time                                                                      | t <sub>SCYC</sub> | SCK1, UCK1,<br>UCK2                 | Internal<br>shift clock<br>mode | 2 t <sub>inst</sub> *   | —    | μs   |         |
| SCK1 ↓ → SO1 time<br>UCK1 ↓ → UO1 time<br>UCK2 ↓ → UO2 time                                  | t <sub>SLOV</sub> | SCK1, SO1<br>UCK1, UO1<br>UCK2, UO2 |                                 | -200                    | 200  | ns   |         |
| Valid SI1 → SCK1 ↑<br>Valid UI1 → UCK1 ↑<br>Valid UI2 → UCK2 ↑                               | t <sub>IVSH</sub> | SI1, SCK1<br>UI1, UCK1<br>UI2, UCK2 |                                 | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| SCK1 ↑ → valid SI1 hold time<br>UCK1 ↑ → valid UI1 hold time<br>UCK2 ↑ → valid UI2 hold time | t <sub>SHIX</sub> | SCK1, SI1<br>UCK1, UI1<br>UCK2, UI2 |                                 | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| Serial clock "H" pulse width                                                                 | t <sub>SHSL</sub> | SCK1, UCK1,<br>UCK2                 | External<br>shift clock<br>mode | 1 t <sub>inst</sub> *   | —    | μs   |         |
| Serial clock "L" pulse width                                                                 | t <sub>SLSH</sub> | SCK1, UCK1,<br>UCK2                 |                                 | 1 t <sub>inst</sub> *   | —    | μs   |         |
| SCK1 ↓ → SO1 time<br>UCK1 ↓ → UO1 time<br>UCK2 ↓ → UO2 time                                  | t <sub>SLOV</sub> | SCK1, SO1<br>UCK1, UO1<br>UCK2, UO2 |                                 | 0                       | 200  | ns   |         |
| Valid SI1 → SCK1 ↑<br>Valid UI1 → UCK1 ↑<br>Valid UI2 → UCK2 ↑                               | t <sub>IVSH</sub> | SI1, SCK1<br>UI1, UCK1<br>UI2, UCK2 |                                 | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| SCK1 ↓ → valid SI1 hold time<br>UCK1 ↓ → valid UI1 hold time<br>UCK2 ↓ → valid UI2 hold time | t <sub>SHIX</sub> | SCK1, SI1<br>UCK1, UI1<br>UCK2, UI2 |                                 | 1/2 t <sub>inst</sub> * | —    | μs   |         |

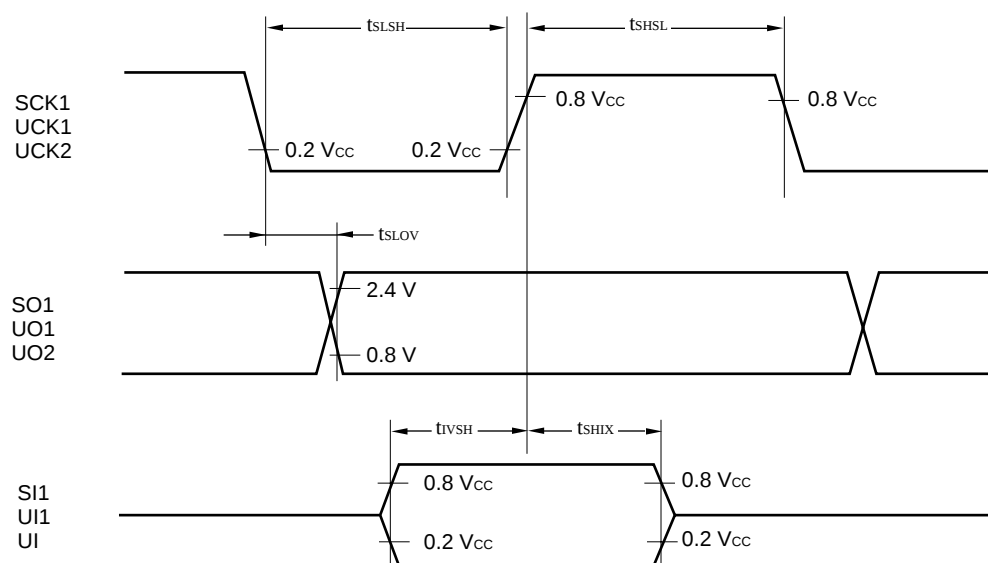
\* : For information on t<sub>inst</sub>, see "(4) Instruction Cycle."

# MB89630R Series

## • Internal shift clock mode



## • External shift clock mode

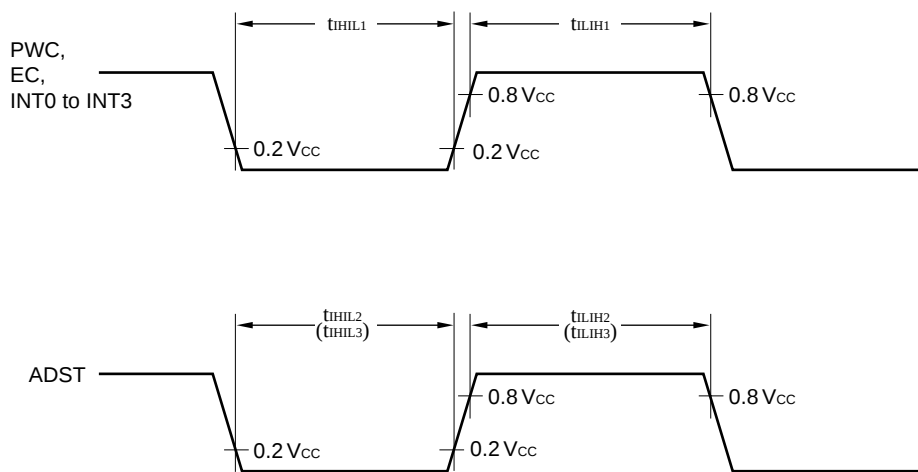


## (10) Peripheral Input Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                          | Symbol     | Pin name              | Value             |      | Unit          | Remarks    |
|------------------------------------|------------|-----------------------|-------------------|------|---------------|------------|
|                                    |            |                       | Min.              | Max. |               |            |
| Peripheral input "H" pulse width 1 | $t_{LIH1}$ | PWC, INT0 to INT3, EC | $2\ t_{inst}^*$   | —    | $\mu\text{s}$ |            |
| Peripheral input "L" pulse width 1 | $t_{HIL1}$ |                       | $2\ t_{inst}^*$   | —    | $\mu\text{s}$ |            |
| Peripheral input "H" pulse width 2 | $t_{LIH2}$ | ADST                  | $2^8\ t_{inst}^*$ | —    | $\mu\text{s}$ | A/D mode   |
| Peripheral input "L" pulse width 2 | $t_{HIL2}$ |                       | $2^8\ t_{inst}^*$ | —    | $\mu\text{s}$ | A/D mode   |
| Peripheral input "H" pulse width 3 | $t_{LIH3}$ | ADST                  | $2^8\ t_{inst}^*$ | —    | $\mu\text{s}$ | Sense mode |
| Peripheral input "L" pulse width 3 | $t_{HIL3}$ |                       | $2^8\ t_{inst}^*$ | —    | $\mu\text{s}$ | Sense mode |

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."



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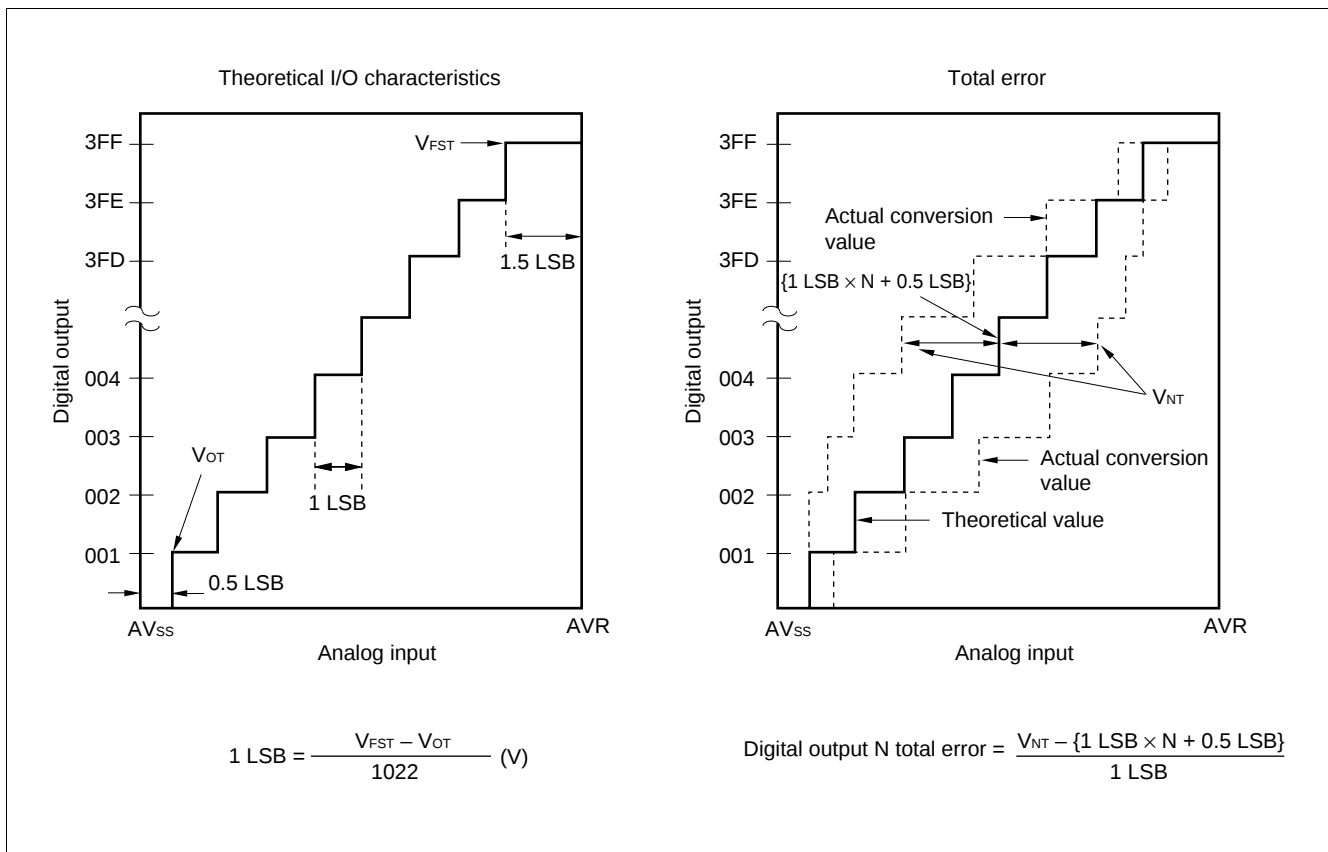
## 5. A/D Converter Electrical Characteristics

( $AV_{CC} = V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$ ,  $F_{CH} = 10 \text{ MHz}$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

| Parameter                        | Symbol    | Pin name   | Value                       |                             |                             | Unit          | Remarks               |
|----------------------------------|-----------|------------|-----------------------------|-----------------------------|-----------------------------|---------------|-----------------------|
|                                  |           |            | Min.                        | Typ.                        | Max.                        |               |                       |
| Resolution                       | —         | —          | —                           | —                           | 10                          | bit           | At $AV_{CC} = V_{CC}$ |
| Linearity error                  |           |            | —                           | —                           | $\pm 2.0$                   | LSB           |                       |
| Differential linearity error     |           |            | —                           | —                           | $\pm 1.5$                   | LSB           |                       |
| Total error                      |           |            | —                           | —                           | $\pm 3.0$                   | LSB           |                       |
| Zero transition voltage          | $V_{OT}$  | AN0 to AN7 | $AV_{SS} - 1.5 \text{ LSB}$ | $AV_{SS} + 0.5 \text{ LSB}$ | $AV_{SS} + 2.5 \text{ LSB}$ | mV            |                       |
| Full-scale transition voltage    | $V_{FST}$ |            | $AVR - 3.5 \text{ LSB}$     | $AVR - 1.5 \text{ LSB}$     | $AVR + 0.5 \text{ LSB}$     | mV            |                       |
| Interchannel disparity           | —         | —          | —                           | —                           | 4                           | LSB           |                       |
| A/D mode conversion time         |           |            | —                           | 13.2                        | —                           | $\mu\text{s}$ |                       |
| Analog port input current        | $I_{AIN}$ | AN0 to AN7 | —                           | —                           | 10                          | $\mu\text{A}$ |                       |
| Analog input voltage             | —         |            | 0.0                         | —                           | AVR                         | V             |                       |
| Reference voltage                |           | 0.0        | —                           | $AV_{CC}$                   | V                           |               |                       |
| Reference voltage supply current | $I_R$     | —          | —                           | 200                         | —                           | $\mu\text{A}$ | AVR = 5.0 V           |

## 6. A/D Converter Glossary

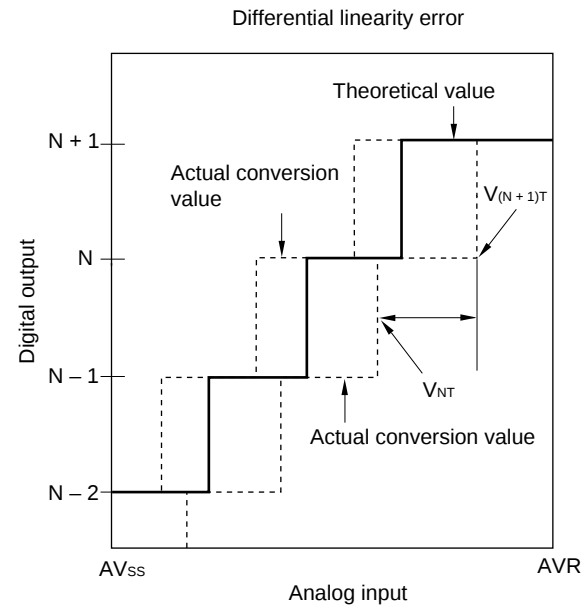
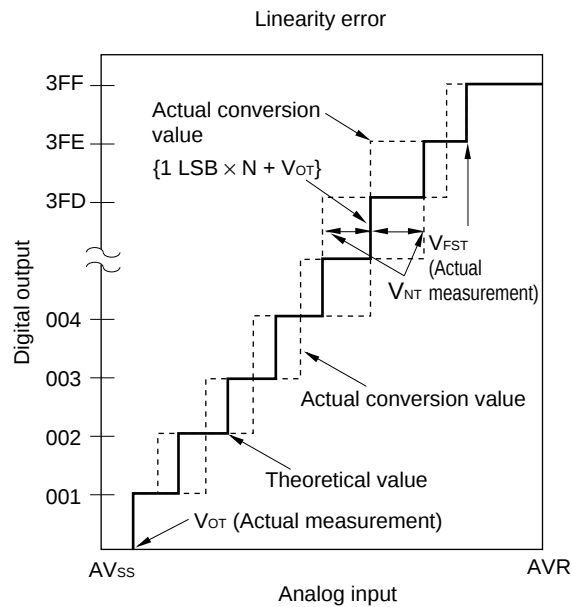
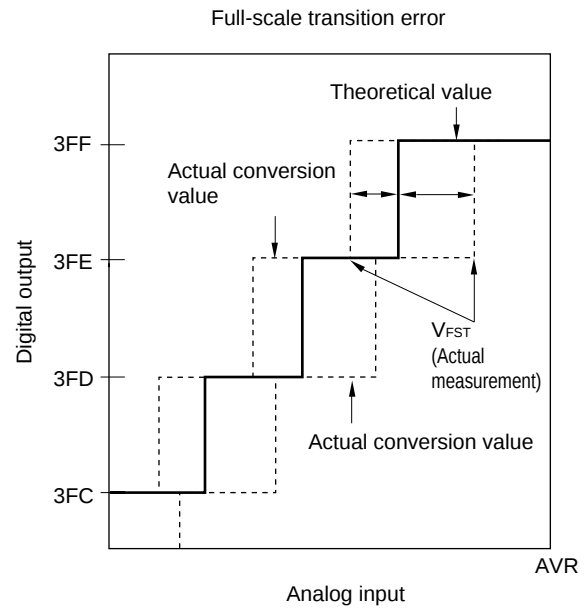
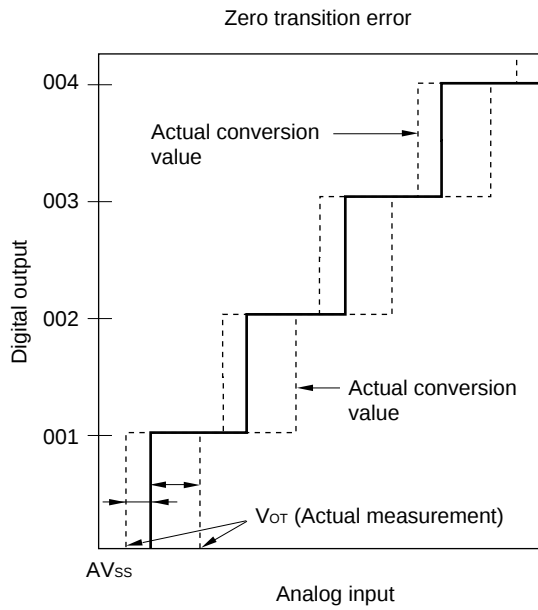
- Resolution  
Analog changes that are identifiable with the A/D converter
- Linearity error  
The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics
- Differential linearity error  
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)  
The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



(Continued)

# MB89630R Series

(Continued)



$$\text{Digital output } N \text{ linearity error} = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Digital output } N \text{ differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

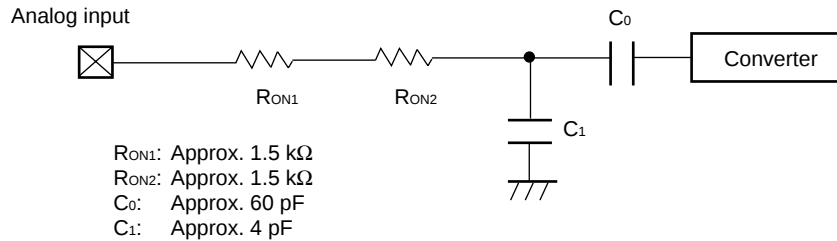
## 7. Notes on Using A/D Converter

### • Input impedance of the analog input pins

The output impedance of the external circuit for the analog input must satisfy the following conditions.

If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6  $\mu$ s at 10MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 k $\Omega$ .

### • Analog input circuit model



Note: The values mentioned here should be used as a guideline.

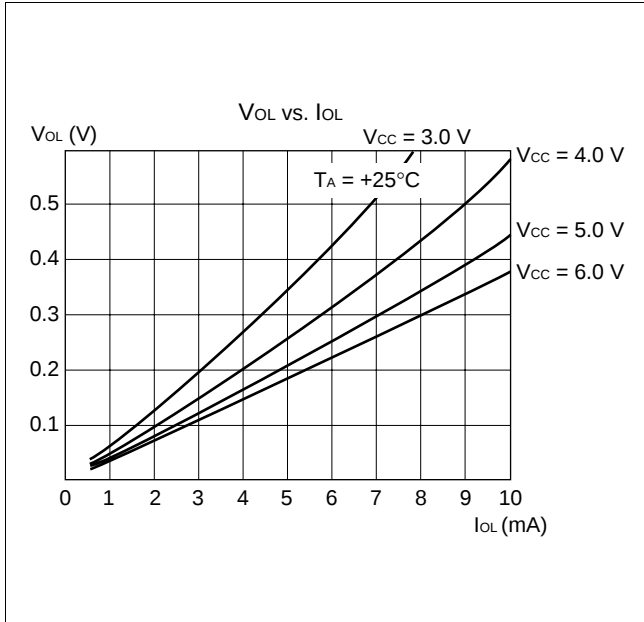
### • Error

The smaller the  $|AVR - AV_{ss}|$ , the greater the error would become relatively.

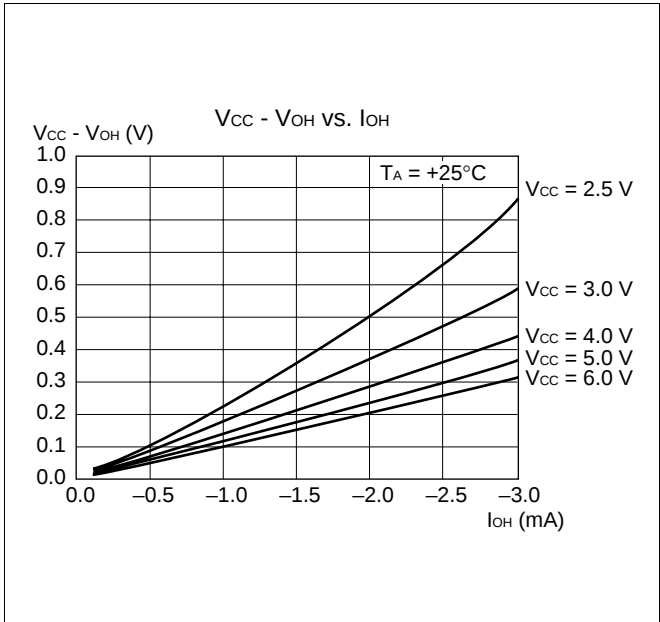
# MB89630R Series

## ■ CHARACTERISTICS EXAMPLE

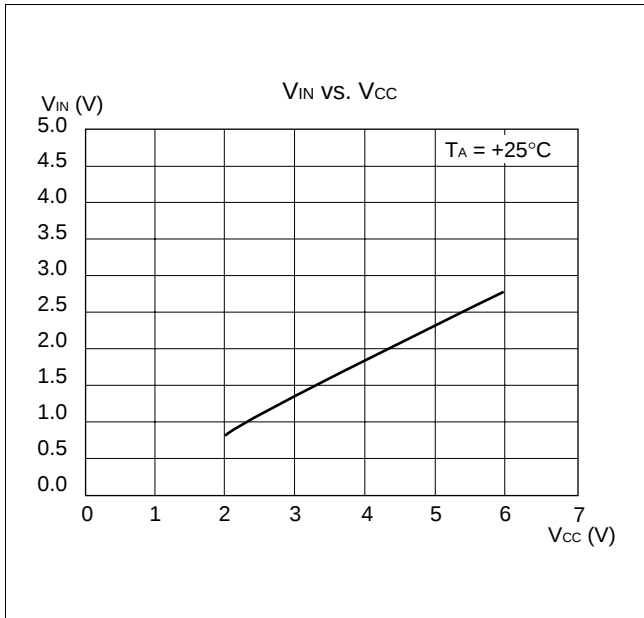
(1) "L" Level Output Voltage



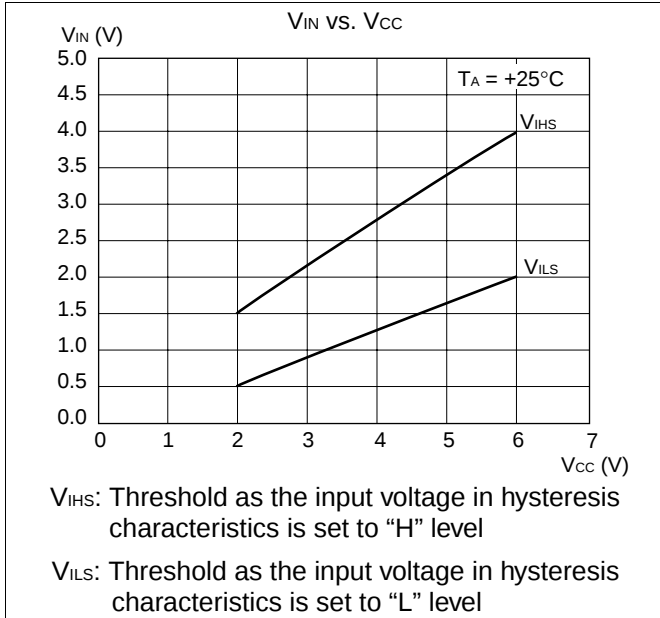
(2) "H" Level Output Voltage



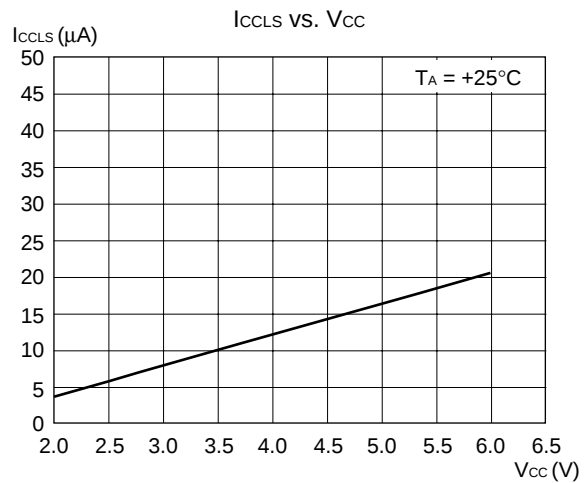
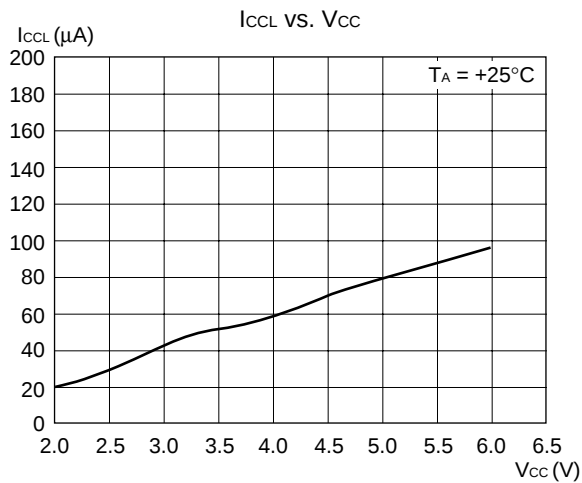
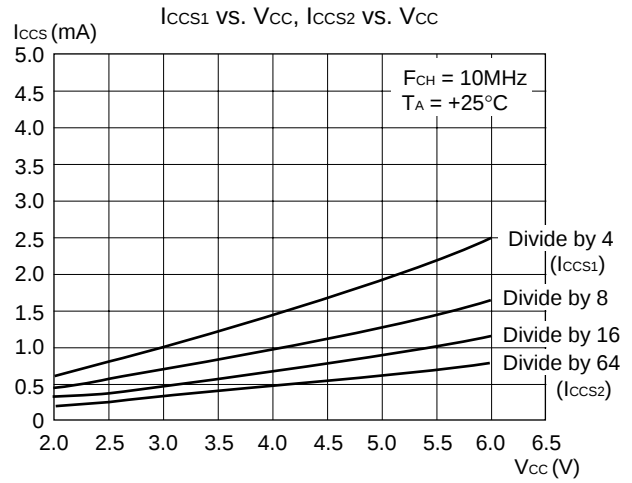
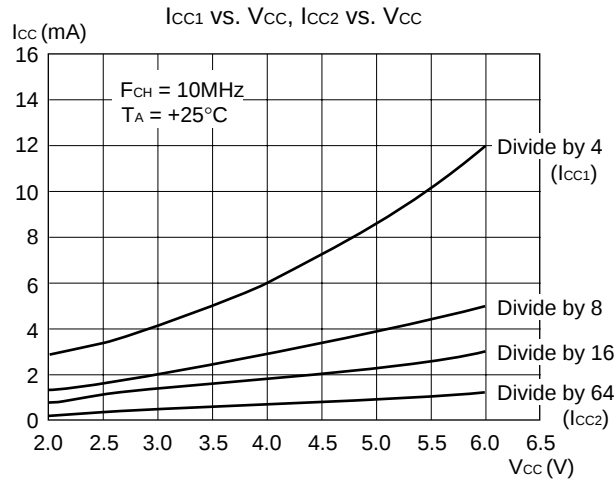
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



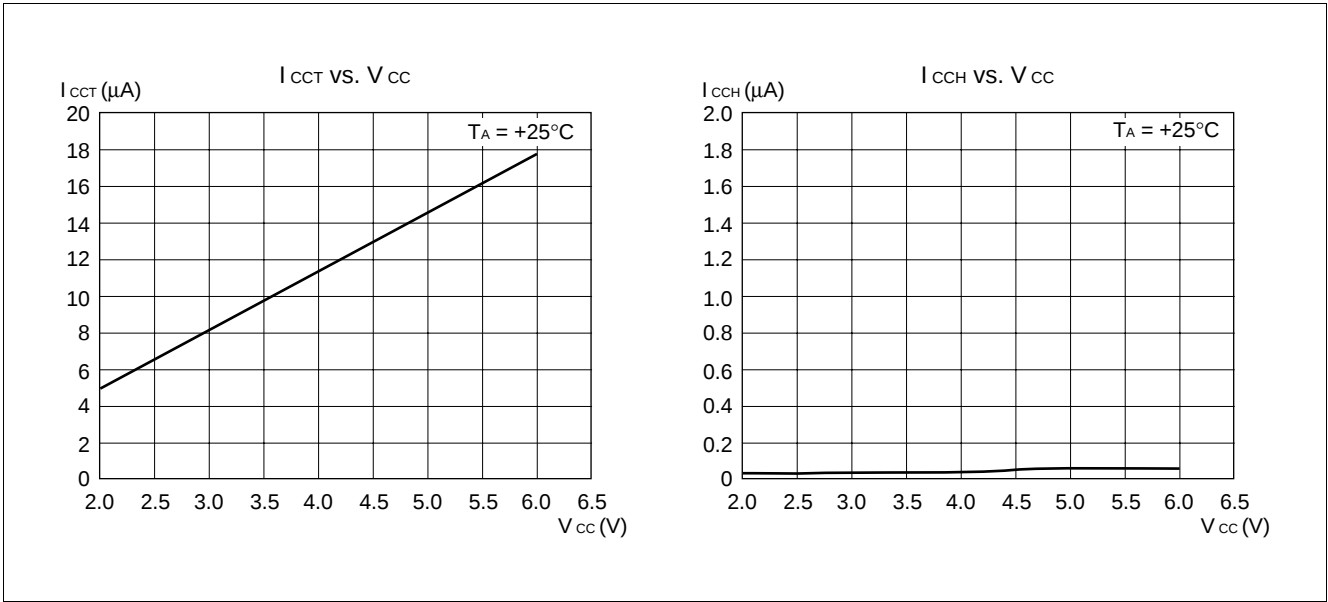
## (5) Power Supply Current (External Clock)



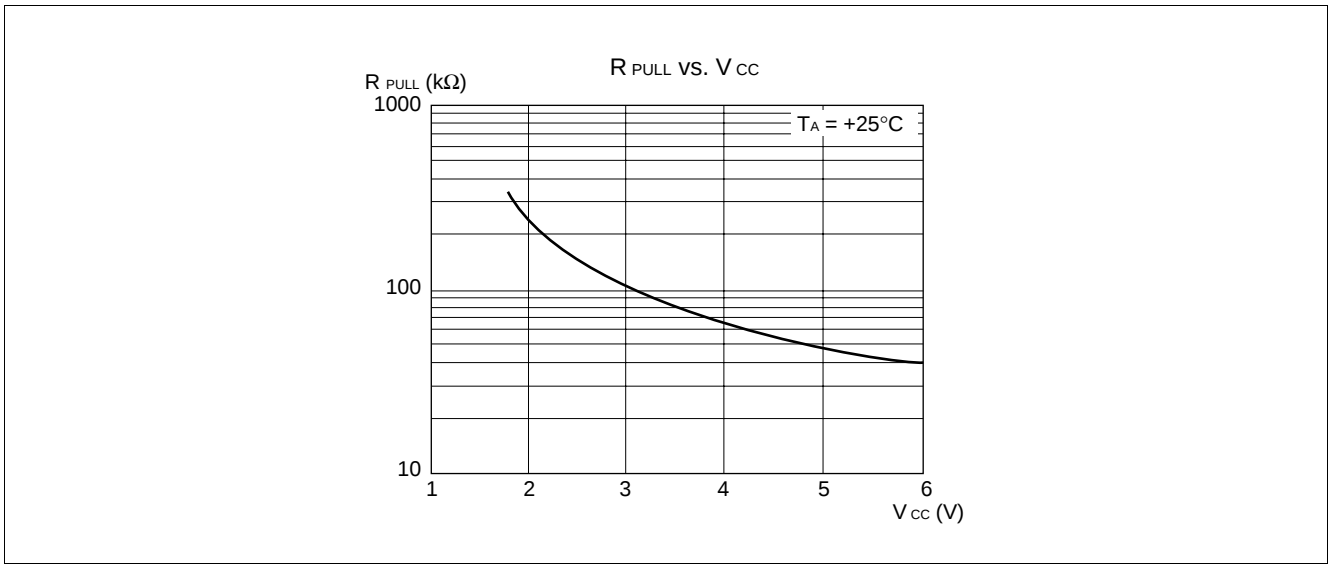
(Continued)

# MB89630R Series

(Continued)



## (6) Pull-up Resistance



## ■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

**Table 1 Instruction Symbols**

| Symbol  | Meaning                                                                                                                                                 |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| dir     | Direct address (8 bits)                                                                                                                                 |
| off     | Offset (8 bits)                                                                                                                                         |
| ext     | Extended address (16 bits)                                                                                                                              |
| #vct    | Vector table number (3 bits)                                                                                                                            |
| #d8     | Immediate data (8 bits)                                                                                                                                 |
| #d16    | Immediate data (16 bits)                                                                                                                                |
| dir: b  | Bit direct address (8:3 bits)                                                                                                                           |
| rel     | Branch relative address (8 bits)                                                                                                                        |
| @       | Register indirect (Example: @A, @IX, @EP)                                                                                                               |
| A       | Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)                                                             |
| AH      | Upper 8 bits of accumulator A (8 bits)                                                                                                                  |
| AL      | Lower 8 bits of accumulator A (8 bits)                                                                                                                  |
| T       | Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)                                                   |
| TH      | Upper 8 bits of temporary accumulator T (8 bits)                                                                                                        |
| TL      | Lower 8 bits of temporary accumulator T (8 bits)                                                                                                        |
| IX      | Index register IX (16 bits)                                                                                                                             |
| EP      | Extra pointer EP (16 bits)                                                                                                                              |
| PC      | Program counter PC (16 bits)                                                                                                                            |
| SP      | Stack pointer SP (16 bits)                                                                                                                              |
| PS      | Program status PS (16 bits)                                                                                                                             |
| dr      | Accumulator A or index register IX (16 bits)                                                                                                            |
| CCR     | Condition code register CCR (8 bits)                                                                                                                    |
| RP      | Register bank pointer RP (5 bits)                                                                                                                       |
| Ri      | General-purpose register Ri (8 bits, i = 0 to 7)                                                                                                        |
| ×       | Indicates that the very × is the immediate data.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.)                       |
| ( × )   | Indicates that the contents of × is the target of accessing.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.)           |
| (( × )) | The address indicated by the contents of × is the target of accessing.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.) |

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “–” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

# MB89630R Series

Table 2 Transfer Instructions (48 instructions)

| Mnemonic         | ~ | # | Operation                                         | TL | TH | AH | NZVC    | OP code  |
|------------------|---|---|---------------------------------------------------|----|----|----|---------|----------|
| MOV dir,A        | 3 | 2 | (dir) ← (A)                                       | —  | —  | —  | — — — — | 45       |
| MOV @IX +off,A   | 4 | 2 | ( (IX) +off ) ← (A)                               | —  | —  | —  | — — — — | 46       |
| MOV ext,A        | 4 | 3 | (ext) ← (A)                                       | —  | —  | —  | — — — — | 61       |
| MOV @EP,A        | 3 | 1 | ( (EP) ) ← (A)                                    | —  | —  | —  | — — — — | 47       |
| MOV Ri,A         | 3 | 1 | (Ri) ← (A)                                        | —  | —  | —  | — — — — | 48 to 4F |
| MOV A,#d8        | 2 | 2 | (A) ← d8                                          | AL | —  | —  | + + — — | 04       |
| MOV A,dir        | 3 | 2 | (A) ← (dir)                                       | AL | —  | —  | + + — — | 05       |
| MOV A,@IX +off   | 4 | 2 | (A) ← ( (IX) +off)                                | AL | —  | —  | + + — — | 06       |
| MOV A,ext        | 4 | 3 | (A) ← (ext)                                       | AL | —  | —  | + + — — | 60       |
| MOV A,@A         | 3 | 1 | (A) ← ( (A) )                                     | AL | —  | —  | + + — — | 92       |
| MOV A,@EP        | 3 | 1 | (A) ← ( (EP) )                                    | AL | —  | —  | + + — — | 07       |
| MOV A,Ri         | 3 | 1 | (A) ← (Ri)                                        | AL | —  | —  | + + — — | 08 to 0F |
| MOV dir,#d8      | 4 | 3 | (dir) ← d8                                        | —  | —  | —  | — — — — | 85       |
| MOV @IX +off,#d8 | 5 | 3 | ( (IX) +off ) ← d8                                | —  | —  | —  | — — — — | 86       |
| MOV @EP,#d8      | 4 | 2 | ( (EP) ) ← d8                                     | —  | —  | —  | — — — — | 87       |
| MOV Ri,#d8       | 4 | 2 | (Ri) ← d8                                         | —  | —  | —  | — — — — | 88 to 8F |
| MOVW dir,A       | 4 | 2 | (dir) ← (AH), (dir + 1) ← (AL)                    | —  | —  | —  | — — — — | D5       |
| MOVW @IX +off,A  | 5 | 2 | ( (IX) +off ) ← (AH),<br>( (IX) +off + 1 ) ← (AL) | —  | —  | —  | — — — — | D6       |
| MOVW ext,A       | 5 | 3 | (ext) ← (AH), (ext + 1) ← (AL)                    | —  | —  | —  | — — — — | D4       |
| MOVW @EP,A       | 4 | 1 | ( (EP) ) ← (AH), ( (EP) + 1 ) ← (AL)              | —  | —  | —  | — — — — | D7       |
| MOVW EP,A        | 2 | 1 | (EP) ← (A)                                        | —  | —  | —  | — — — — | E3       |
| MOVW A,#d16      | 3 | 3 | (A) ← d16                                         | AL | AH | dH | + + — — | E4       |
| MOVW A,dir       | 4 | 2 | (AH) ← (dir), (AL) ← (dir + 1)                    | AL | AH | dH | + + — — | C5       |
| MOVW A,@IX +off  | 5 | 2 | (AH) ← ( (IX) +off ),<br>(AL) ← ( (IX) +off + 1 ) | AL | AH | dH | + + — — | C6       |
| MOVW A,ext       | 5 | 3 | (AH) ← (ext), (AL) ← (ext + 1)                    | AL | AH | dH | + + — — | C4       |
| MOVW A,@A        | 4 | 1 | (AH) ← ( (A) ), (AL) ← ( (A) ) + 1                | AL | AH | dH | + + — — | 93       |
| MOVW A,@EP       | 4 | 1 | (AH) ← ( (EP) ), (AL) ← ( (EP) + 1 )              | AL | AH | dH | + + — — | C7       |
| MOVW A,EP        | 2 | 1 | (A) ← (EP)                                        | —  | —  | dH | — — — — | F3       |
| MOVW EP,#d16     | 3 | 3 | (EP) ← d16                                        | —  | —  | —  | — — — — | E7       |
| MOVW IX,A        | 2 | 1 | (IX) ← (A)                                        | —  | —  | —  | — — — — | E2       |
| MOVW A,IX        | 2 | 1 | (A) ← (IX)                                        | —  | —  | dH | — — — — | F2       |
| MOVW SP,A        | 2 | 1 | (SP) ← (A)                                        | —  | —  | —  | — — — — | E1       |
| MOVW A,SP        | 2 | 1 | (A) ← (SP)                                        | —  | —  | dH | — — — — | F1       |
| MOV @A,T         | 3 | 1 | ( (A) ) ← (T)                                     | —  | —  | —  | — — — — | 82       |
| MOVW @A,T        | 4 | 1 | ( (A) ) ← (TH), ( (A) + 1 ) ← (TL)                | —  | —  | —  | — — — — | 83       |
| MOVW IX,#d16     | 3 | 3 | (IX) ← d16                                        | —  | —  | —  | — — — — | E6       |
| MOVW A,PS        | 2 | 1 | (A) ← (PS)                                        | —  | —  | dH | — — — — | 70       |
| MOVW PS,A        | 2 | 1 | (PS) ← (A)                                        | —  | —  | —  | + + + + | 71       |
| MOVW SP,#d16     | 3 | 3 | (SP) ← d16                                        | —  | —  | —  | — — — — | E5       |
| SWAP             | 2 | 1 | (AH) ↔ (AL)                                       | —  | —  | AL | — — — — | 10       |
| SETB dir: b      | 4 | 2 | (dir): b ← 1                                      | —  | —  | —  | — — — — | A8 to AF |
| CLRB dir: b      | 4 | 2 | (dir): b ← 0                                      | —  | —  | —  | — — — — | A0 to A7 |
| XCH A,T          | 2 | 1 | (AL) ↔ (TL)                                       | AL | —  | —  | — — — — | 42       |
| XCHW A,T         | 3 | 1 | (A) ↔ (T)                                         | AL | AH | dH | — — — — | 43       |
| XCHW A,EP        | 3 | 1 | (A) ↔ (EP)                                        | —  | —  | dH | — — — — | F7       |
| XCHW A,IX        | 3 | 1 | (A) ↔ (IX)                                        | —  | —  | dH | — — — — | F6       |
| XCHW A,SP        | 3 | 1 | (A) ↔ (SP)                                        | —  | —  | dH | — — — — | F5       |
| MOVW A,PC        | 2 | 1 | (A) ← (PC)                                        | —  | —  | dH | — — — — | F0       |

Note: During byte transfer to A, T ← A is restricted to low bytes.

Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F<sup>2</sup>MC-8 family)

**Table 3 Arithmetic Operation Instructions (62 instructions)**

| Mnemonic        | ~  | # | Operation                                        | TL | TH | AH | NZVC | OP code  |
|-----------------|----|---|--------------------------------------------------|----|----|----|------|----------|
| ADDC A,Ri       | 3  | 1 | $(A) \leftarrow (A) + (Ri) + C$                  | —  | —  | —  | ++++ | 28 to 2F |
| ADDC A,#d8      | 2  | 2 | $(A) \leftarrow (A) + d8 + C$                    | —  | —  | —  | ++++ | 24       |
| ADDC A,dir      | 3  | 2 | $(A) \leftarrow (A) + (dir) + C$                 | —  | —  | —  | ++++ | 25       |
| ADDC A,@IX +off | 4  | 2 | $(A) \leftarrow (A) + ((IX) + off) + C$          | —  | —  | —  | ++++ | 26       |
| ADDC A,@EP      | 3  | 1 | $(A) \leftarrow (A) + ((EP)) + C$                | —  | —  | —  | ++++ | 27       |
| ADDCW A         | 3  | 1 | $(A) \leftarrow (A) + (T) + C$                   | —  | —  | dH | ++++ | 23       |
| ADDC A          | 2  | 1 | $(AL) \leftarrow (AL) + (TL) + C$                | —  | —  | —  | ++++ | 22       |
| SUBC A,Ri       | 3  | 1 | $(A) \leftarrow (A) - (Ri) - C$                  | —  | —  | —  | ++++ | 38 to 3F |
| SUBC A,#d8      | 2  | 2 | $(A) \leftarrow (A) - d8 - C$                    | —  | —  | —  | ++++ | 34       |
| SUBC A,dir      | 3  | 2 | $(A) \leftarrow (A) - (dir) - C$                 | —  | —  | —  | ++++ | 35       |
| SUBC A,@IX +off | 4  | 2 | $(A) \leftarrow (A) - ((IX) + off) - C$          | —  | —  | —  | ++++ | 36       |
| SUBC A,@EP      | 3  | 1 | $(A) \leftarrow (A) - ((EP)) - C$                | —  | —  | —  | ++++ | 37       |
| SUBCW A         | 3  | 1 | $(A) \leftarrow (T) - (A) - C$                   | —  | —  | dH | ++++ | 33       |
| SUBC A          | 2  | 1 | $(AL) \leftarrow (TL) - (AL) - C$                | —  | —  | —  | ++++ | 32       |
| INC Ri          | 4  | 1 | $(Ri) \leftarrow (Ri) + 1$                       | —  | —  | —  | +++- | C8 to CF |
| INCW EP         | 3  | 1 | $(EP) \leftarrow (EP) + 1$                       | —  | —  | —  | ---- | C3       |
| INCW IX         | 3  | 1 | $(IX) \leftarrow (IX) + 1$                       | —  | —  | —  | ---- | C2       |
| INCW A          | 3  | 1 | $(A) \leftarrow (A) + 1$                         | —  | —  | dH | ++-- | C0       |
| DEC Ri          | 4  | 1 | $(Ri) \leftarrow (Ri) - 1$                       | —  | —  | —  | +++- | D8 to DF |
| DECW EP         | 3  | 1 | $(EP) \leftarrow (EP) - 1$                       | —  | —  | —  | ---- | D3       |
| DECW IX         | 3  | 1 | $(IX) \leftarrow (IX) - 1$                       | —  | —  | —  | ---- | D2       |
| DECW A          | 3  | 1 | $(A) \leftarrow (A) - 1$                         | —  | —  | dH | ++-- | D0       |
| MULU A          | 19 | 1 | $(A) \leftarrow (AL) \times (TL)$                | —  | —  | dH | ---- | 01       |
| DIVU A          | 21 | 1 | $(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$ | dL | 00 | 00 | ---- | 11       |
| ANDW A          | 3  | 1 | $(A) \leftarrow (A) \wedge (T)$                  | —  | —  | dH | ++R— | 63       |
| ORW A           | 3  | 1 | $(A) \leftarrow (A) \vee (T)$                    | —  | —  | dH | ++R— | 73       |
| XORW A          | 3  | 1 | $(A) \leftarrow (A) \nabla (T)$                  | —  | —  | dH | ++R— | 53       |
| CMP A           | 2  | 1 | $(TL) - (AL)$                                    | —  | —  | —  | ++++ | 12       |
| CMPW A          | 3  | 1 | $(T) - (A)$                                      | —  | —  | —  | ++++ | 13       |
| RORC A          | 2  | 1 | $\rightarrow C \rightarrow A \leftarrow$         | —  | —  | —  | ++-+ | 03       |
| ROLA A          | 2  | 1 | $\leftarrow C \leftarrow A \leftarrow$           | —  | —  | —  | ++-+ | 02       |
| CMP A,#d8       | 2  | 2 | $(A) - d8$                                       | —  | —  | —  | ++++ | 14       |
| CMP A,dir       | 3  | 2 | $(A) - (dir)$                                    | —  | —  | —  | ++++ | 15       |
| CMP A,@EP       | 3  | 1 | $(A) - ((EP))$                                   | —  | —  | —  | ++++ | 17       |
| CMP A,@IX +off  | 4  | 2 | $(A) - ((IX) + off)$                             | —  | —  | —  | ++++ | 16       |
| CMP A,Ri        | 3  | 1 | $(A) - (Ri)$                                     | —  | —  | —  | ++++ | 18 to 1F |
| DAA             | 2  | 1 | Decimal adjust for addition                      | —  | —  | —  | ++++ | 84       |
| DAS             | 2  | 1 | Decimal adjust for subtraction                   | —  | —  | —  | ++++ | 94       |
| XOR A           | 2  | 1 | $(A) \leftarrow (AL) \nabla (TL)$                | —  | —  | —  | ++R— | 52       |
| XOR A,#d8       | 2  | 2 | $(A) \leftarrow (AL) \nabla d8$                  | —  | —  | —  | ++R— | 54       |
| XOR A,dir       | 3  | 2 | $(A) \leftarrow (AL) \nabla (dir)$               | —  | —  | —  | ++R— | 55       |
| XOR A,@EP       | 3  | 1 | $(A) \leftarrow (AL) \nabla ((EP))$              | —  | —  | —  | ++R— | 57       |
| XOR A,@IX +off  | 4  | 2 | $(A) \leftarrow (AL) \nabla ((IX) + off)$        | —  | —  | —  | ++R— | 56       |
| XOR A,Ri        | 3  | 1 | $(A) \leftarrow (AL) \nabla (Ri)$                | —  | —  | —  | ++R— | 58 to 5F |
| AND A           | 2  | 1 | $(A) \leftarrow (AL) \wedge (TL)$                | —  | —  | —  | ++R— | 62       |
| AND A,#d8       | 2  | 2 | $(A) \leftarrow (AL) \wedge d8$                  | —  | —  | —  | ++R— | 64       |
| AND A,dir       | 3  | 2 | $(A) \leftarrow (AL) \wedge (dir)$               | —  | —  | —  | ++R— | 65       |

(Continued)

# MB89630R Series

(Continued)

| Mnemonic         | ~ | # | Operation                                 | TL | TH | AH | NZVC | OP code  |
|------------------|---|---|-------------------------------------------|----|----|----|------|----------|
| AND A,@EP        | 3 | 1 | $(A) \leftarrow (AL) \wedge (EP)$         | —  | —  | —  | ++R— | 67       |
| AND A,@IX +off   | 4 | 2 | $(A) \leftarrow (AL) \wedge ((IX) + off)$ | —  | —  | —  | ++R— | 66       |
| AND A,Ri         | 3 | 1 | $(A) \leftarrow (AL) \wedge (Ri)$         | —  | —  | —  | ++R— | 68 to 6F |
| OR A             | 2 | 1 | $(A) \leftarrow (AL) \vee (TL)$           | —  | —  | —  | ++R— | 72       |
| OR A,#d8         | 2 | 2 | $(A) \leftarrow (AL) \vee d8$             | —  | —  | —  | ++R— | 74       |
| OR A,dir         | 3 | 2 | $(A) \leftarrow (AL) \vee (dir)$          | —  | —  | —  | ++R— | 75       |
| OR A,@EP         | 3 | 1 | $(A) \leftarrow (AL) \vee (EP)$           | —  | —  | —  | ++R— | 77       |
| OR A,@IX +off    | 4 | 2 | $(A) \leftarrow (AL) \vee ((IX) + off)$   | —  | —  | —  | ++R— | 76       |
| OR A,Ri          | 3 | 1 | $(A) \leftarrow (AL) \vee (Ri)$           | —  | —  | —  | ++R— | 78 to 7F |
| CMP dir,#d8      | 5 | 3 | $(dir) - d8$                              | —  | —  | —  | ++++ | 95       |
| CMP @EP,#d8      | 4 | 2 | $((EP)) - d8$                             | —  | —  | —  | ++++ | 97       |
| CMP @IX +off,#d8 | 5 | 3 | $((IX) + off) - d8$                       | —  | —  | —  | ++++ | 96       |
| CMP Ri,#d8       | 4 | 2 | $(Ri) - d8$                               | —  | —  | —  | ++++ | 98 to 9F |
| INCW SP          | 3 | 1 | $(SP) \leftarrow (SP) + 1$                | —  | —  | —  | ---- | C1       |
| DECW SP          | 3 | 1 | $(SP) \leftarrow (SP) - 1$                | —  | —  | —  | ---- | D1       |

**Table 4 Branch Instructions (17 instructions)**

| Mnemonic       | ~ | # | Operation                                       | TL | TH | AH | NZVC    | OP code  |
|----------------|---|---|-------------------------------------------------|----|----|----|---------|----------|
| BZ/BEQ rel     | 3 | 2 | If $Z = 1$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | FD       |
| BNZ/BNE rel    | 3 | 2 | If $Z = 0$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | FC       |
| BC/BLO rel     | 3 | 2 | If $C = 1$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | F9       |
| BNC/BHS rel    | 3 | 2 | If $C = 0$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | F8       |
| BN rel         | 3 | 2 | If $N = 1$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | FB       |
| BP rel         | 3 | 2 | If $N = 0$ then $PC \leftarrow PC + rel$        | —  | —  | —  | ----    | FA       |
| BLT rel        | 3 | 2 | If $V \vee N = 1$ then $PC \leftarrow PC + rel$ | —  | —  | —  | ----    | FF       |
| BGE rel        | 3 | 2 | If $V \vee N = 0$ then $PC \leftarrow PC + rel$ | —  | —  | —  | ----    | FE       |
| BBC dir: b,rel | 5 | 3 | If $(dir: b) = 0$ then $PC \leftarrow PC + rel$ | —  | —  | —  | —+---   | B0 to B7 |
| BBS dir: b,rel | 5 | 3 | If $(dir: b) = 1$ then $PC \leftarrow PC + rel$ | —  | —  | —  | —+---   | B8 to BF |
| JMP @A         | 2 | 1 | $(PC) \leftarrow (A)$                           | —  | —  | —  | ----    | E0       |
| JMP ext        | 3 | 3 | $(PC) \leftarrow ext$                           | —  | —  | —  | ----    | 21       |
| CALLV #vct     | 6 | 1 | Vector call                                     | —  | —  | —  | ----    | E8 to EF |
| CALL ext       | 6 | 3 | Subroutine call                                 | —  | —  | —  | ----    | 31       |
| XCHW A,PC      | 3 | 1 | $(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$  | —  | —  | dH | ----    | F4       |
| RET            | 4 | 1 | Return from subroutine                          | —  | —  | —  | ----    | 20       |
| RETI           | 6 | 1 | Return from interrupt                           | —  | —  | —  | Restore | 30       |

**Table 5 Other Instructions (9 instructions)**

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC  | OP code |
|----------|---|---|-----------|----|----|----|-------|---------|
| PUSHW A  | 4 | 1 |           | —  | —  | —  | ----  | 40      |
| POPW A   | 4 | 1 |           | —  | —  | dH | ----  | 50      |
| PUSHW IX | 4 | 1 |           | —  | —  | —  | ----  | 41      |
| POPW IX  | 4 | 1 |           | —  | —  | —  | ----  | 51      |
| NOP      | 1 | 1 |           | —  | —  | —  | ----  | 00      |
| CLRC     | 1 | 1 |           | —  | —  | —  | ----R | 81      |
| SETC     | 1 | 1 |           | —  | —  | —  | ----S | 91      |
| CLRI     | 1 | 1 |           | —  | —  | —  | ----  | 80      |
| SETI     | 1 | 1 |           | —  | —  | —  | ----  | 90      |

## INSTRUCTION MAP

| L | H | 0              | 1              | 2               | 3               | 4              | 5              | 6              | 7             | 8                | 9                | A              | B                 | C               | D                 | E               | F             |
|---|---|----------------|----------------|-----------------|-----------------|----------------|----------------|----------------|---------------|------------------|------------------|----------------|-------------------|-----------------|-------------------|-----------------|---------------|
| 0 |   | NOP            | SWAP           | RET             | RETI            | PUSHW<br>A     | POPW<br>A      | MOV<br>A,ext   | MOVW<br>A,PS  | CLRI             | SETI             | CLRB<br>dir: 0 | BBC<br>dir: 0,rel | INCW<br>A       | DECW<br>A         | JMP<br>@A       | MOVW<br>A,PC  |
| 1 |   | MULU<br>A      | DIVU<br>A      | JMP<br>addr16   | CALL<br>addr16  | PUSHW<br>IX    | POPW<br>IX     | MOV<br>ext,A   | MOVW<br>PS,A  | CLRC             | SETC             | CLRB<br>dir: 1 | BBC<br>dir: 1,rel | INCW<br>SP      | DECW<br>SP        | MOVW<br>SPA     | MOVW<br>A,SP  |
| 2 |   | ROL            | CMP<br>A       | ADDC<br>A       | SUBC<br>A       | XCH<br>A,T     | XOR<br>A       | AND<br>A       | OR<br>A       | MOV<br>@A,T      | MOV<br>A,@A      | CLRB<br>dir: 2 | BBC<br>dir: 2,rel | INCW<br>IX      | DECW<br>IX        | MOVW<br>IX,A    | MOVW<br>A,IX  |
| 3 |   | ROR            | CMPW<br>A      | ADDCW<br>A      | SUBCW<br>A      | XCHW<br>A,T    | XORW<br>A      | ANDW<br>A      | ORW<br>A      | MOVW<br>@A,T     | MOVW<br>A,@A     | CLRB<br>dir: 3 | BBC<br>dir: 3,rel | INCW<br>EP      | DECW<br>EP        | MOVW<br>EPA     | MOVW<br>A,EP  |
| 4 |   | MOV<br>A,#d8   | CMP<br>A,#d8   | ADDC<br>A,#d8   | SUBC<br>A,#d8   | /              |                | AND<br>A,#d8   | OR<br>A,#d8   | DAA              | DAS              | CLRB<br>dir: 4 | BBC<br>dir: 4,rel | MOVW<br>A,ext   | MOVW<br>ext,A     | MOVW<br>A,#d16  | XCHW<br>A,PC  |
| 5 |   | MOV<br>A,dir   | CMP<br>A,dir   | ADDC<br>A,dir   | SUBC<br>A,dir   |                |                | MOV<br>dir,A   | XOR<br>A,dir  | AND<br>A,dir     | OR<br>A,dir      | MOV<br>dir,#d8 | CMP<br>dir,#d8    | CLRB<br>dir: 5  | BBC<br>dir: 5,rel | MOVW<br>A,dir   | MOVW<br>dir,A |
| 6 |   | MOV<br>A,@IX+d | CMP<br>A,@IX+d | ADDC<br>A,@IX+d | SUBC<br>A,@IX+d | MOV<br>@IX+d,A | XOR<br>A,@IX+d | AND<br>A,@IX+d | OR<br>A,@IX+d | MOV<br>@IX+d,#d8 | CMP<br>@IX+d,#d8 | CLRB<br>dir: 6 | BBC<br>dir: 6,rel | MOVW<br>A,@IX+d | MOVW<br>@IX+d,A   | MOVW<br>IX,#d16 | XCHW<br>A,IX  |
| 7 |   | MOV<br>A,@EP   | CMP<br>A,@EP   | ADDC<br>A,@EP   | SUBC<br>A,@EP   | MOV<br>@EPA    | XOR<br>A,@EP   | AND<br>A,@EP   | OR<br>A,@EP   | MOV<br>@EP,#d8   | CMP<br>@EP,#d8   | CLRB<br>dir: 7 | BBC<br>dir: 7,rel | MOVW<br>A,@EP   | MOVW<br>@EPA      | MOVW<br>EP,#d16 | XCHW<br>A,EP  |
| 8 |   | MOV<br>A,R0    | CMP<br>A,R0    | ADDC<br>A,R0    | SUBC<br>A,R0    | MOV<br>R0,A    | XOR<br>A,R0    | AND<br>A,R0    | OR<br>A,R0    | MOV<br>R0,#d8    | CMP<br>R0,#d8    | SETB<br>dir: 0 | BBS<br>dir: 0,rel | INC<br>R0       | DEC<br>R0         | CALLV<br>#0     | BNC<br>rel    |
| 9 |   | MOV<br>A,R1    | CMP<br>A,R1    | ADDC<br>A,R1    | SUBC<br>A,R1    | MOV<br>R1,A    | XOR<br>A,R1    | AND<br>A,R1    | OR<br>A,R1    | MOV<br>R1,#d8    | CMP<br>R1,#d8    | SETB<br>dir: 1 | BBS<br>dir: 1,rel | INC<br>R1       | DEC<br>R1         | CALLV<br>#1     | BC<br>rel     |
| A |   | MOV<br>A,R2    | CMP<br>A,R2    | ADDC<br>A,R2    | SUBC<br>A,R2    | MOV<br>R2,A    | XOR<br>A,R2    | AND<br>A,R2    | OR<br>A,R2    | MOV<br>R2,#d8    | CMP<br>R2,#d8    | SETB<br>dir: 2 | BBS<br>dir: 2,rel | INC<br>R2       | DEC<br>R2         | CALLV<br>#2     | BP<br>rel     |
| B |   | MOV<br>A,R3    | CMP<br>A,R3    | ADDC<br>A,R3    | SUBC<br>A,R3    | MOV<br>R3,A    | XOR<br>A,R3    | AND<br>A,R3    | OR<br>A,R3    | MOV<br>R3,#d8    | CMP<br>R3,#d8    | SETB<br>dir: 3 | BBS<br>dir: 3,rel | INC<br>R3       | DEC<br>R3         | CALLV<br>#3     | BN<br>rel     |
| C |   | MOV<br>A,R4    | CMP<br>A,R4    | ADDC<br>A,R4    | SUBC<br>A,R4    | MOV<br>R4,A    | XOR<br>A,R4    | AND<br>A,R4    | OR<br>A,R4    | MOV<br>R4,#d8    | CMP<br>R4,#d8    | SETB<br>dir: 4 | BBS<br>dir: 4,rel | INC<br>R4       | DEC<br>R4         | CALLV<br>#4     | BNZ<br>rel    |
| D |   | MOV<br>A,R5    | CMP<br>A,R5    | ADDC<br>A,R5    | SUBC<br>A,R5    | MOV<br>R5,A    | XOR<br>A,R5    | AND<br>A,R5    | OR<br>A,R5    | MOV<br>R5,#d8    | CMP<br>R5,#d8    | SETB<br>dir: 5 | BBS<br>dir: 5,rel | INC<br>R5       | DEC<br>R5         | CALLV<br>#5     | BZ<br>rel     |
| E |   | MOV<br>A,R6    | CMP<br>A,R6    | ADDC<br>A,R6    | SUBC<br>A,R6    | MOV<br>R6,A    | XOR<br>A,R6    | AND<br>A,R6    | OR<br>A,R6    | MOV<br>R6,#d8    | CMP<br>R6,#d8    | SETB<br>dir: 6 | BBS<br>dir: 6,rel | INC<br>R6       | DEC<br>R6         | CALLV<br>#6     | BGE<br>rel    |
| F |   | MOV<br>A,R7    | CMP<br>A,R7    | ADDC<br>A,R7    | SUBC<br>A,R7    | MOV<br>R7,A    | XOR<br>A,R7    | AND<br>A,R7    | OR<br>A,R7    | MOV<br>R7,#d8    | CMP<br>R7,#d8    | SETB<br>dir: 7 | BBS<br>dir: 7,rel | INC<br>R7       | DEC<br>R7         | CALLV<br>#7     | BLT<br>rel    |

# MB89630R Series

## ■ MASK OPTIONS

| No. | Part number                                                                                                                                                                                                                                                                                                                                                                     | MB89635R<br>MB89636R<br>MB89637R | MB89P637<br>MB89W637      | MB89PV630<br>MB89T635R<br>MB89T637R                                                                         |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|---------------------------|-------------------------------------------------------------------------------------------------------------|
|     | Specifying procedure                                                                                                                                                                                                                                                                                                                                                            | Specify when ordering masking    | Set with EPROM programmer | Setting not possible                                                                                        |
| 1   | Pull-up resistors<br><div> <div>P00 to P07, P10 to P17,<br/>P30 to P37, P40 to P43,<br/>P50 to P53, P72 to P74</div> </div>                                                                                                                                                                                                                                                     | Selectable by pin                | Can be set per pin*       | Fixed to “without pull-up resistor”                                                                         |
| 2   | Power-on reset selection<br><div> <div>With power-on reset</div> <div>Without power-on reset</div> </div>                                                                                                                                                                                                                                                                       | Selectable                       | Setting possible          | Fixed to “with power-on reset”                                                                              |
| 3   | Selection of the main clock oscillation stabilization time (at 10 MHz)<br><div> <div>Approx. <math>2^{18}/F_{CH}</math> (Approx. 26.2 ms)</div> <div>Approx. <math>2^{17}/F_{CH}</math> (Approx. 13.1 ms)</div> <div>Approx. <math>2^{14}/F_{CH}</math> (Approx. 1.6 ms)</div> <div>Approx. <math>2^4/F_{CH}</math> (Approx. 0 ms)</div> </div> $F_{CH}$ : Main clock frequency | Selectable                       | Setting possible          | Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)                                                                  |
| 4   | Reset pin output<br><div> <div>Reset output provided</div> <div>No reset output</div> </div>                                                                                                                                                                                                                                                                                    | Selectable                       | Setting possible          | Fixed to “with reset output”                                                                                |
| 5   | Single/dual-clock system option<br><div> <div>Single clock</div> <div>Dual clock</div> </div>                                                                                                                                                                                                                                                                                   | Selectable                       | Setting possible          | MB89PV630-101 Single-clock system<br>MB89T635R-101 Single-clock system<br>MB89T637R-101 Single-clock system |
|     |                                                                                                                                                                                                                                                                                                                                                                                 |                                  |                           | MB89PV630-102 Dual-clock systems<br>MB89T635R-102 Dual-clock systems<br>MB89T637R-102 Dual-clock systems    |

\* : Pull-up resistors cannot be set for P50 to P53.

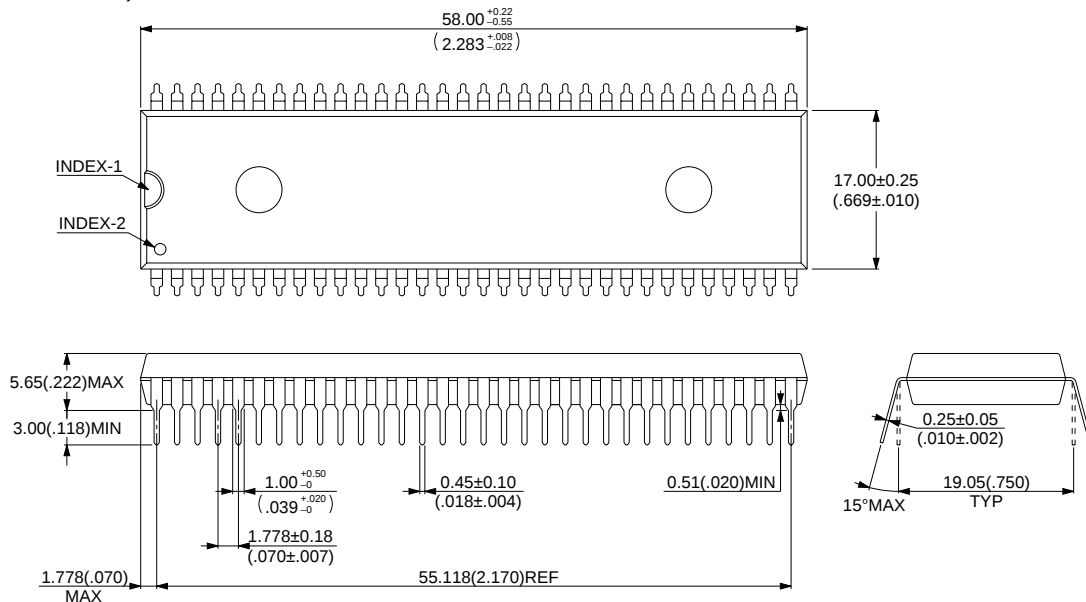
## ■ ORDERING INFORMATION

| Part number                                                                                    | Package                                | Remarks |
|------------------------------------------------------------------------------------------------|----------------------------------------|---------|
| MB89635RP-SH<br>MB89T635RP-SH<br>MB89636RP-SH<br>MB89637RP-SH<br>MB89P637P-SH<br>MB89T637RP-SH | 64-pin Plastic SH-DIP<br>(DIP-64P-M01) |         |
| MB89635RPF<br>MB89T635RPF<br>MB89636RPF<br>MB89637RPF<br>MB89P637PF<br>MB89T637RPF             | 64-pin Plastic QFP<br>(FPT-64P-M06)    |         |
| MB89635RPFM<br>MB89636RPFM<br>MB89637RPFM<br>MB89T635RPFM                                      | 64-pin Plastic QFP<br>(FPT-64P-M09)    |         |
| MB89W637C-SH                                                                                   | 64-pin Ceramic SH-DIP<br>(DIP-64C-A06) |         |
| MB89PV630CF                                                                                    | 64-pin Ceramic MQFP<br>(MQP-64C-P01)   |         |
| MB89PV630C-SH                                                                                  | 64-pin Ceramic MDIP<br>(MDP-64C-P02)   |         |

# MB89630R Series

## ■ PACKAGE DIMENSIONS

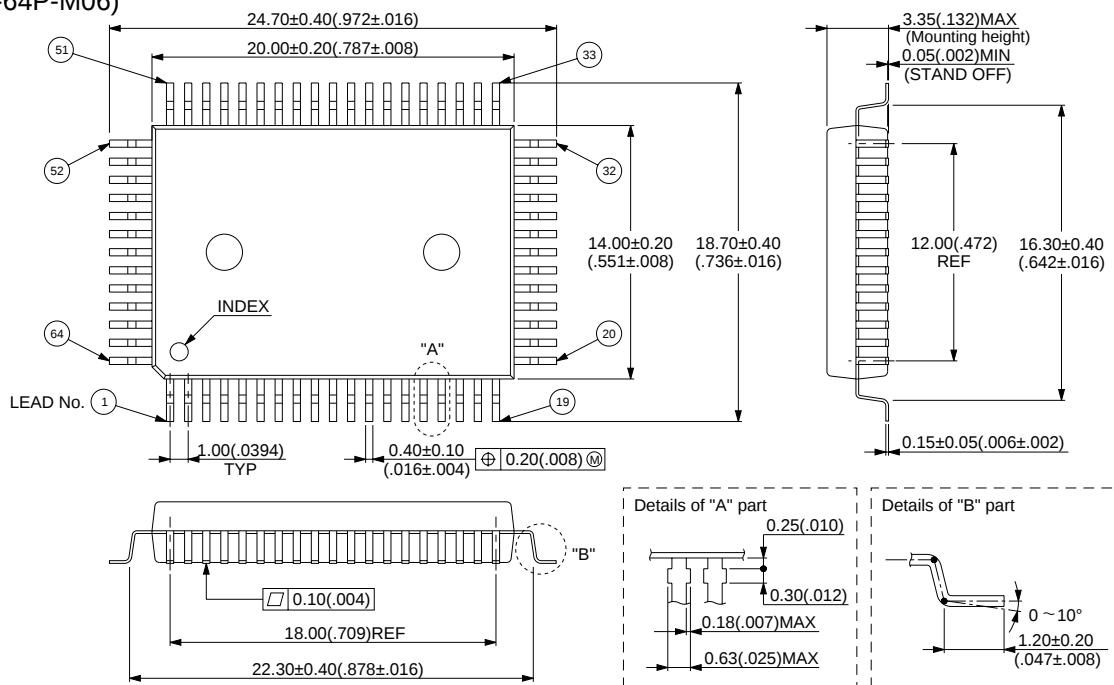
64-pin Plastic SH-DIP  
(DIP-64P-M01)



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Dimensions in mm (inches)

64-pin Plastic QFP  
(FPT-64P-M06)

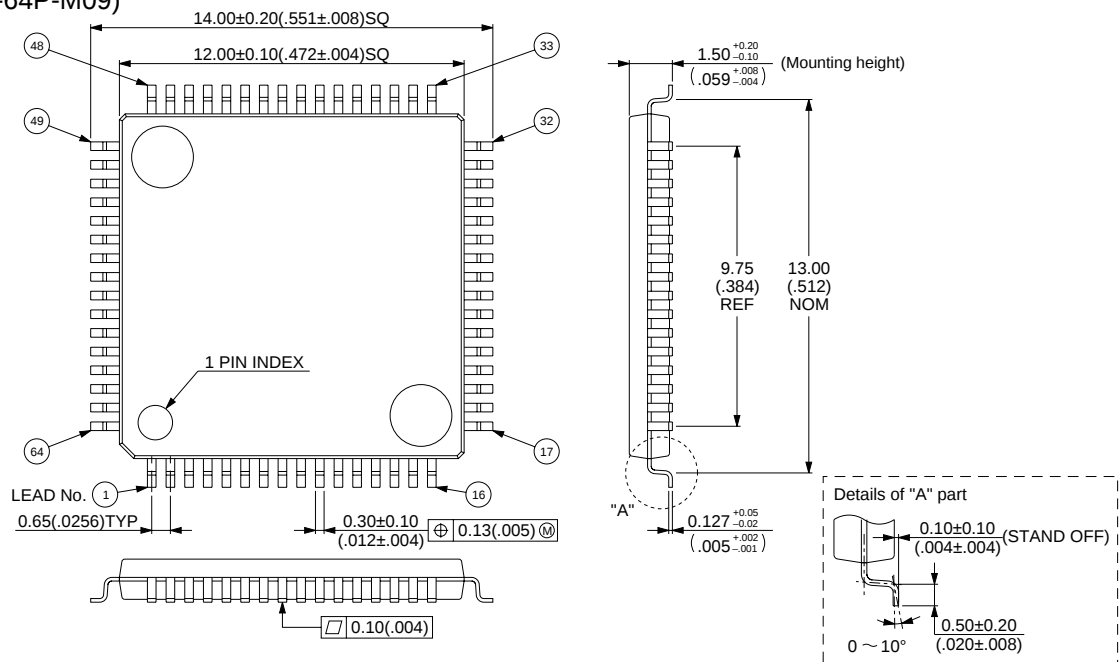


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Dimensions in mm (inches)

# MB89630R Series

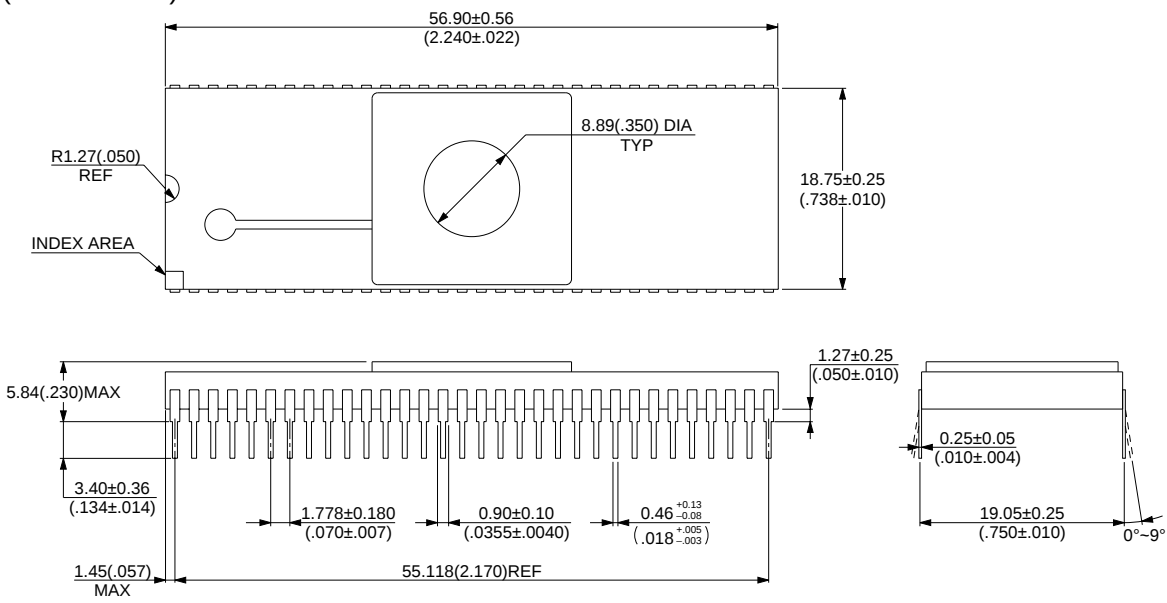
## 64-pin Plastic QFP (FPT-64P-M09)



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Dimensions in mm (inches)

## 64-pin Ceramic SH-DIP (DIP-64C-A06)

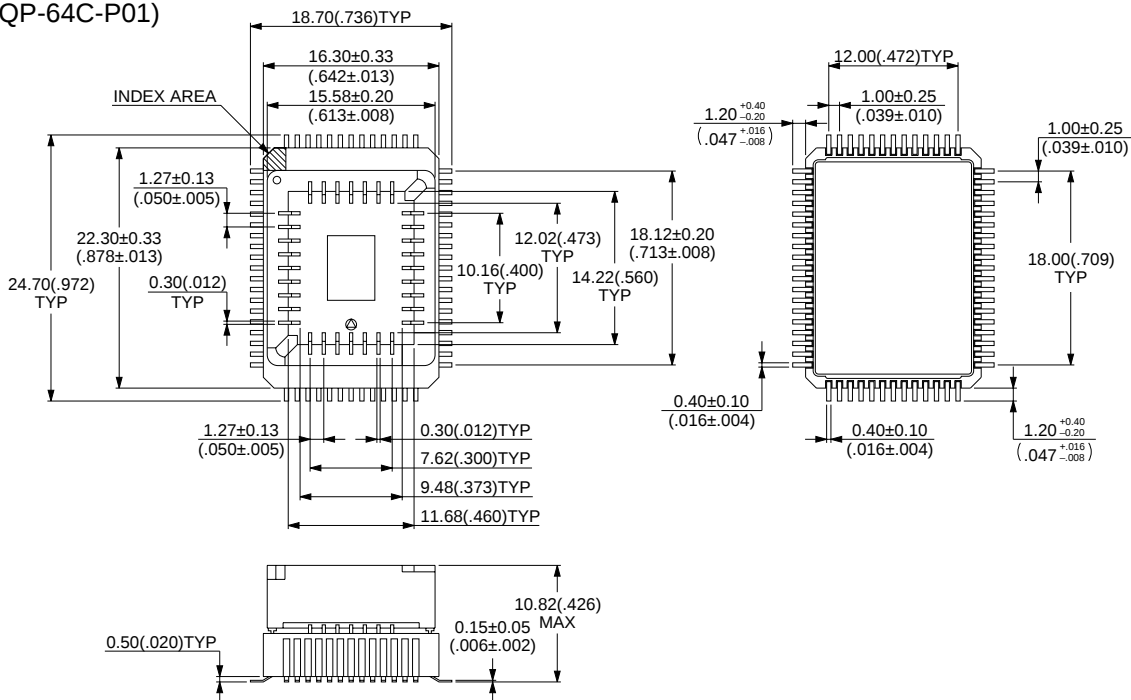


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Dimensions in mm (inches)

# MB89630R Series

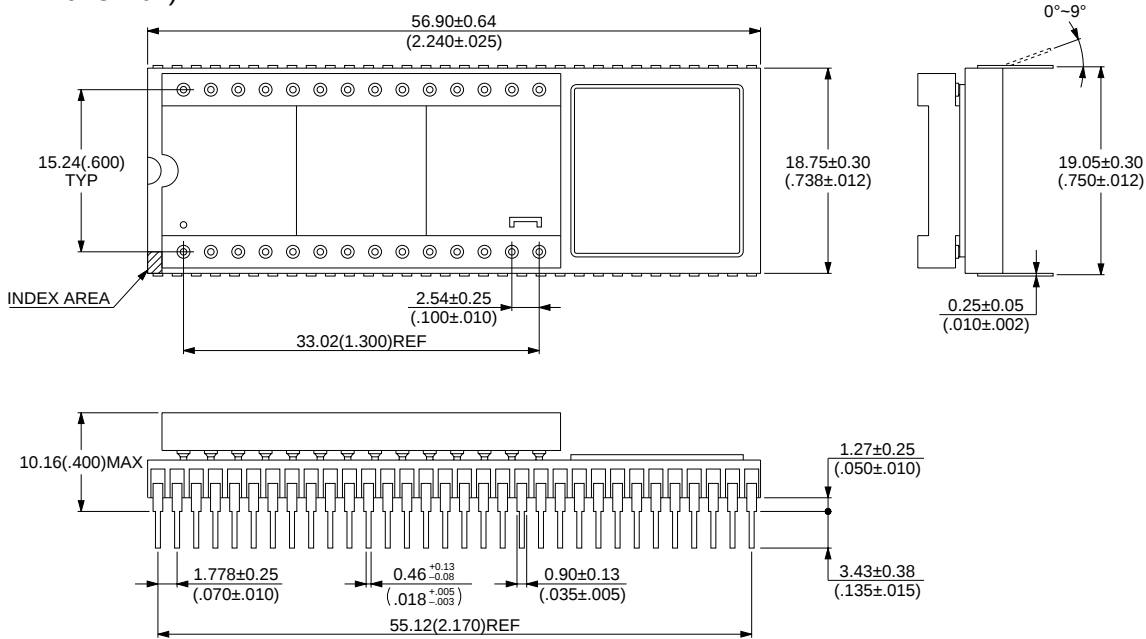
64-pin Ceramic MQFP  
(MQP-64C-P01)



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Dimensions in mm (inches)

64-pin Ceramic MDIP  
(MDP-64C-P02)



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Dimensions in mm (inches)

# MB89630R Series

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