

# IS61NLF12836A/IS61NVF12836A IS61NLF25618A/IS61NVF25618A



## 128K x 36 and 256K x 18 4Mb, FLOW THROUGH 'NO WAIT' STATE BUS SRAM

AUGUST 2011

### FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single Read/Write control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$  pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 119-ball PBGA, and 165-ball PBGA packages
- Power supply:  
NVF:  $V_{\text{DD}} 2.5\text{V} (\pm 5\%)$ ,  $V_{\text{DDQ}} 2.5\text{V} (\pm 5\%)$   
NLF:  $V_{\text{DD}} 3.3\text{V} (\pm 5\%)$ ,  $V_{\text{DDQ}} 3.3\text{V}/2.5\text{V} (\pm 5\%)$
- Industrial temperature available
- Lead-free available

### DESCRIPTION

The 4 Meg 'NLF/NVF' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 128K words by 36 bits and 256K words by 18 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable,  $\overline{\text{CKE}}$  is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when  $\overline{\text{WE}}$  is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

### FAST ACCESS TIME

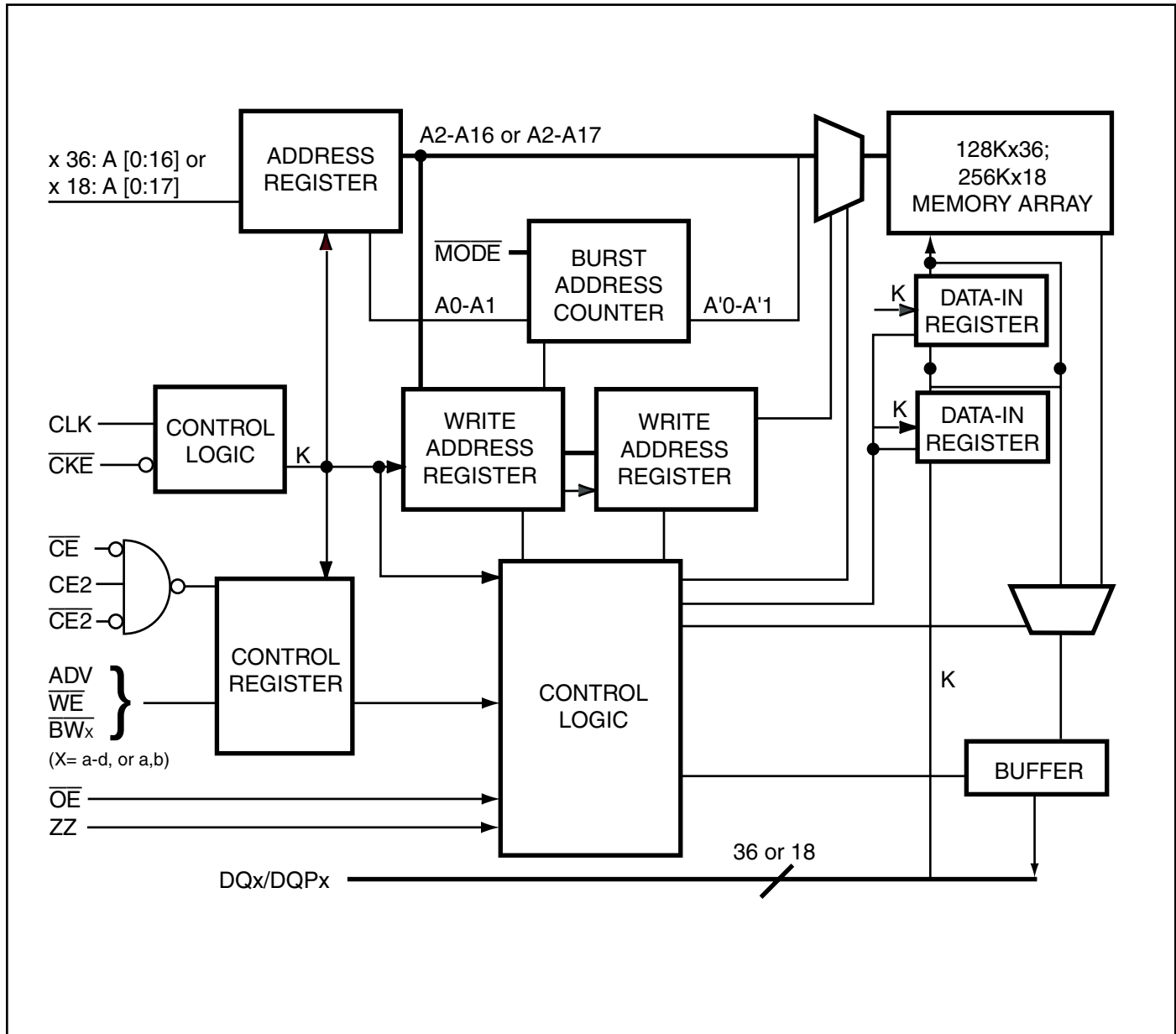
Symbol	Parameter	6.5	7.5	Units
$t_{\text{KQ}}$	Clock Access Time	6.5	7.5	ns
$t_{\text{KC}}$	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

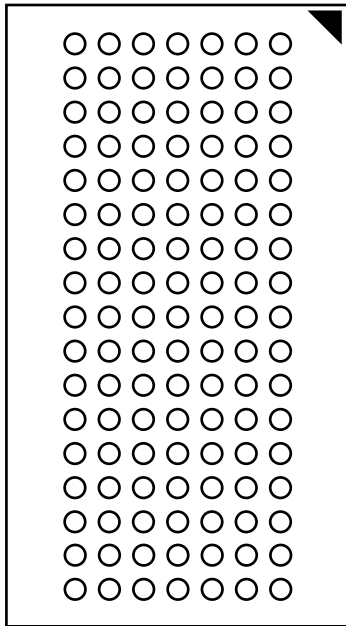
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**BLOCK DIAGRAM**





Bottom View  
119-Ball, 14 mm x 22 mm BGA



Bottom View  
165-Ball, 13 mm x 15mm BGA

**PIN CONFIGURATION — 128K x 36, 165-Ball PBGA (TOP VIEW)**

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{CKE}$	ADV	NC	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPd
P	NC	NC	A	A	NC	A1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A0*	NC	A	A	A	A

**Note:** A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

**PIN DESCRIPTIONS**

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$ , $\overline{CE2}$ , CE2	Synchronous Chip Enable
$\overline{BWx}$ (x=a-d)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode

MODE	Burst Sequence Selection
VDD	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
VDDQ	Isolated output Power Supply 3.3V/2.5V
VSS	Ground

**119-PIN PBGA PACKAGE CONFIGURATION —128K x 36 (TOP VIEW)**

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	A	A	NC	A	A	V <sub>DDQ</sub>
B	NC	CE2	A	ADV	A	$\overline{\text{CE}}2$	NC
C	NC	A	A	V <sub>DD</sub>	A	A	NC
D	DQ <sub>c</sub>	DQP <sub>c</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>b</sub>	DQ <sub>b</sub>
E	DQ <sub>c</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{CE}}$	V <sub>SS</sub>	DQ <sub>b</sub>	DQ <sub>b</sub>
F	V <sub>DDQ</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>b</sub>	V <sub>DDQ</sub>
G	DQ <sub>c</sub>	DQ <sub>c</sub>	$\overline{\text{BW}}_c$	NC	$\overline{\text{BW}}_b$	DQ <sub>b</sub>	DQ <sub>b</sub>
H	DQ <sub>c</sub>	DQ <sub>c</sub>	V <sub>SS</sub>	$\overline{\text{WE}}$	V <sub>SS</sub>	DQ <sub>b</sub>	DQ <sub>b</sub>
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQ <sub>d</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>a</sub>	DQ <sub>a</sub>
L	DQ <sub>d</sub>	DQ <sub>d</sub>	$\overline{\text{BW}}_d$	NC	$\overline{\text{BW}}_a$	DQ <sub>a</sub>	DQ <sub>a</sub>
M	V <sub>DDQ</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	$\overline{\text{CKE}}$	V <sub>SS</sub>	DQ <sub>a</sub>	V <sub>DDQ</sub>
N	DQ <sub>d</sub>	DQ <sub>d</sub>	V <sub>SS</sub>	A <sub>1</sub> *	V <sub>SS</sub>	DQ <sub>a</sub>	DQ <sub>a</sub>
P	DQ <sub>d</sub>	DQP <sub>d</sub>	V <sub>SS</sub>	A <sub>0</sub> *	V <sub>SS</sub>	DQP <sub>a</sub>	DQ <sub>a</sub>
R	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

**Note:** A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

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A	Address Inputs
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ADV	Synchronous Burst Address Advance/Load
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CLK	Synchronous Clock
$\overline{\text{CKE}}$	Clock Enable
$\overline{\text{CE}}$	Synchronous Chip Select
$\overline{\text{CE}}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{\text{BW}}_x$ (x=a-d)	Synchronous Byte Write Inputs

$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V <sub>DD</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connect
DQ <sub>a</sub> -DQ <sub>d</sub>	Data Inputs/Outputs
DQP <sub>a</sub> -Pd	Parity Data I/O
V <sub>DDQ</sub>	Output Power Supply

**165-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)**

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{CKE}$	ADV	NC	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQP <sub>a</sub>
D	NC	DQ <sub>b</sub>	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ <sub>a</sub>
E	NC	DQ <sub>b</sub>	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ <sub>a</sub>
F	NC	DQ <sub>b</sub>	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ <sub>a</sub>
G	NC	DQ <sub>b</sub>	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQ <sub>a</sub>
H	NC	NC	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQ <sub>b</sub>	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ <sub>a</sub>	NC
K	DQ <sub>b</sub>	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ <sub>a</sub>	NC
L	DQ <sub>b</sub>	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ <sub>a</sub>	NC
M	DQ <sub>b</sub>	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQ <sub>a</sub>	NC
N	DQP <sub>b</sub>	NC	VDDQ	Vss	NC	NC	NC	Vss	VDDQ	NC	NC
P	NC	NC	A	A	NC	A <sub>1</sub> *	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A <sub>0</sub> *	NC	A	A	A	A

**Note:** A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

**PIN DESCRIPTIONS**

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$ , $\overline{CE2}$ , CE2	Synchronous Chip Enable
$\overline{BWx}$ (x=a,b)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode

MODE	Burst Sequence Selection
VDD	3.3V/2.5V Power Supply
NC	No Connect
DQ <sub>x</sub>	Data Inputs/Outputs
DQP <sub>x</sub>	Parity Data I/O
VDDQ	Isolated output Power Supply 3.3V/2.5V
Vss	Ground

**119-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)**

	1	2	3	4	5	6	7
A	VDDQ	A	A	NC	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{\text{CE}}2$	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQPa	NC
E	NC	DQb	VSS	$\overline{\text{CE}}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{BW}}b$	NC	NC	NC	DQa
H	DQb	NC	VSS	$\overline{\text{WE}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	NC	NC	$\overline{\text{BW}}a$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{CKE}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1*	VSS	DQa	NC
P	NC	DQPb	VSS	A0*	VSS	NC	DQa
R	NC	A	MODE	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

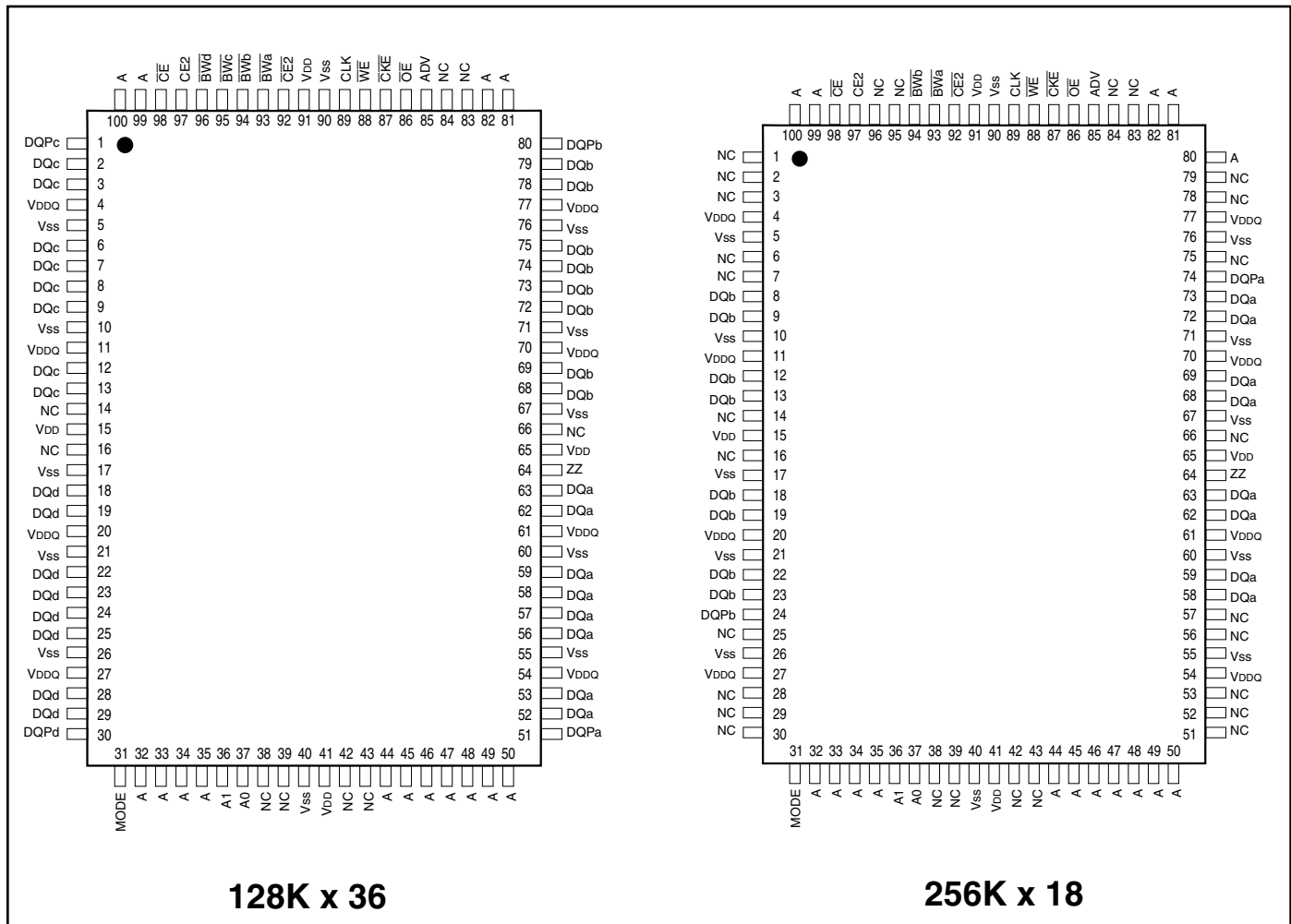
**Note:** A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

**PIN DESCRIPTIONS**

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{\text{WE}}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{\text{CKE}}$	Clock Enable
$\overline{\text{CE}}$	Synchronous Chip Select
$\overline{\text{CE}}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{\text{BW}}x$ (x=a,b)	Synchronous Byte Write Inputs

$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
VDD	Power Supply
VSS	Ground
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Parity Data I/O
VDDQ	Output Power Supply

**PIN CONFIGURATION**  
**100-Pin TQFP**



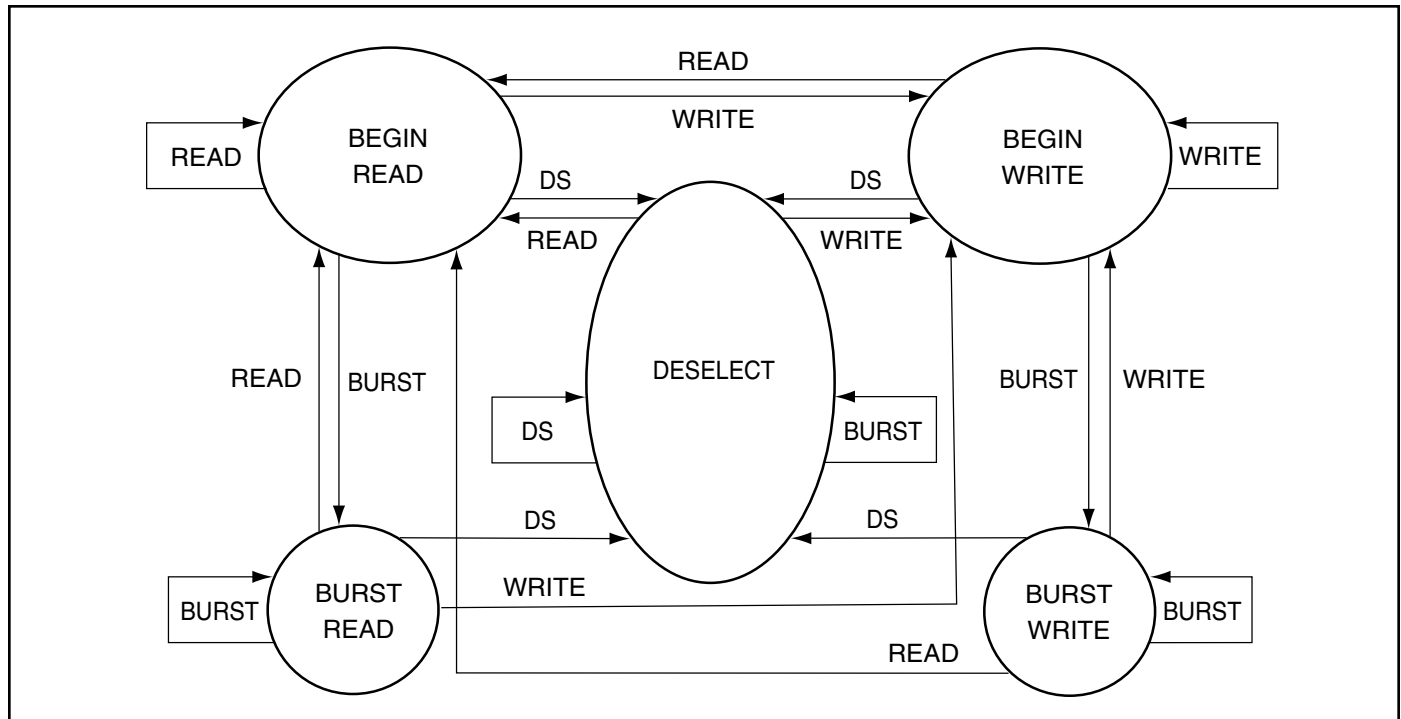
**PIN DESCRIPTIONS**

A0, A1	Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
BW <sub>a</sub> -BW <sub>d</sub>	Synchronous Byte Write Enable
WE	Write Enable
CKE	Clock Enable
Vss	Ground for Core
NC	Not Connected

CE, CE2, CE <sub>2</sub>	Synchronous Chip Enable
OE	Output Enable
DQ <sub>a</sub> -DQ <sub>d</sub>	Synchronous Data Input/Output
DQP <sub>a</sub> -DQP <sub>d</sub>	Parity Data I/O
MODE	Burst Sequence Selection
VDD	+3.3V/2.5V Power Supply
Vss	Ground for output Buffer
VDDQ	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable



## STATE DIAGRAM



## SYNCHRONOUS TRUTH TABLE<sup>(1)</sup>

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

### Notes:

- "X" means don't care.
- The rising edge of clock is symbolized by ↑
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{WE} = L$  means Write operation in Write Truth Table.  
 $\overline{WE} = H$  means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous pins ( $\overline{ZZ}$  and  $\overline{OE}$ ).

**ASYNCHRONOUS TRUTH TABLE<sup>(1)</sup>**

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**Notes:**

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

**WRITE TRUTH TABLE (x18)**

Operation	$\overline{WE}$	$\overline{Bw}a$	$\overline{Bw}b$
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTES	L	L	L
WRITE ABORT/NOP	L	H	H

**Notes:**

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

**WRITE TRUTH TABLE** (x36)

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTES	L	L	L	L	L
WRITE ABORT/NOF	L	H	H	H	H

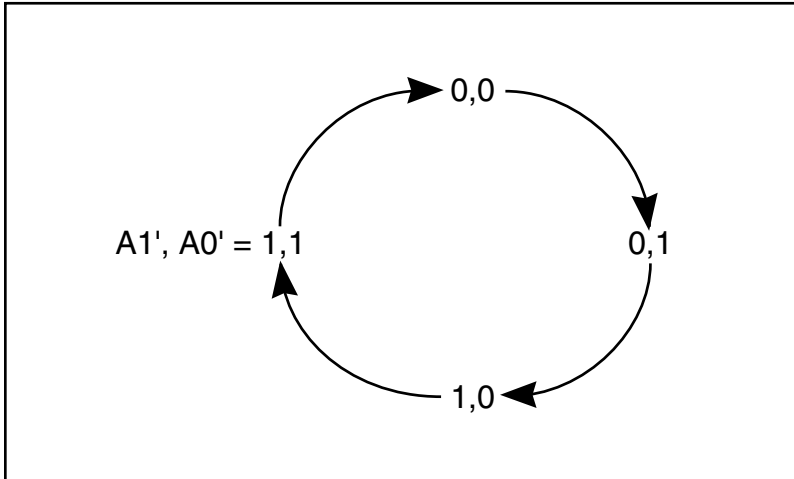
**Notes:**

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

**INTERLEAVED BURST ADDRESS TABLE** (MODE = V<sub>DD</sub> or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**LINEAR BURST ADDRESS TABLE (MODE = V<sub>SS</sub>)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>D</sub>	Power Dissipation	1.6	W
I <sub>OUT</sub>	Output Current (per I/O)	100	mA
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage Relative to V <sub>SS</sub> for I/O Pins	-0.5 to V <sub>DDQ</sub> + 0.3	V
V <sub>IN</sub>	Voltage Relative to V <sub>SS</sub> for for Address and Control Inputs	-0.3 to 4.6	V

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

**OPERATING RANGE (IS61NLFx)**

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

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**OPERATING RANGE (IS61NVFx)**

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0 mA (3.3V) I <sub>OH</sub> = -1.0 mA (2.5V)	2.4	—	2.0	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0 mA (3.3V) I <sub>OL</sub> = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>DD</sub> + 0.3	1.7	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	-0.3	0.7	V
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> <sup>(1)</sup>	-5	5	-5	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> , OE = V <sub>IH</sub>	-5	5	-5	5	μA

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	6.5 MAX		7.5 MAX		Unit
				x18	x36	x18	x36	
I <sub>CC</sub>	AC Operating Supply Current	Device Selected, OE = V <sub>IH</sub> , ZZ ≤ V <sub>IL</sub> ,	Com.	175	175	155	155	mA
		All Inputs ≤ 0.2V or ≥ V <sub>DD</sub> - 0.2V, Cycle Time ≥ t <sub>kc</sub> min.	Ind. typ. <sup>(2)</sup>	180	180	160	160	
I <sub>SB</sub>	Standby Current TTL Input	Device Deselected, V <sub>DD</sub> = Max.,	Com.	90	90	90	90	mA
		All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> , ZZ ≤ V <sub>IL</sub> , f = Max.	Ind.	100	100	100	100	
I <sub>SB1</sub>	Standby Current CMOS Input	Device Deselected, V <sub>DD</sub> = Max.,	Com.	70	70	70	70	mA
		V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V or ≥ V <sub>DD</sub> - 0.2V f = 0	Ind. typ. <sup>(2)</sup>	75	75	75	75	
I <sub>SB2</sub>	Sleep Mode	ZZ > V <sub>IH</sub>	Com.	30	30	30	30	mA
			Ind. typ. <sup>(2)</sup>	35	35	35	35	
				20		20		

**Note:**

- MODE pin has an internal pullup and should be tied to V<sub>DD</sub> or V<sub>SS</sub>. It exhibits ±100 μA maximum leakage current when tied to ≤ V<sub>SS</sub> + 0.2V or ≥ V<sub>DD</sub> - 0.2V.
- Typical values are measured at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C and not 100% tested.

### CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

### 3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

### 3.3V I/O OUTPUT LOAD EQUIVALENT



Figure 1

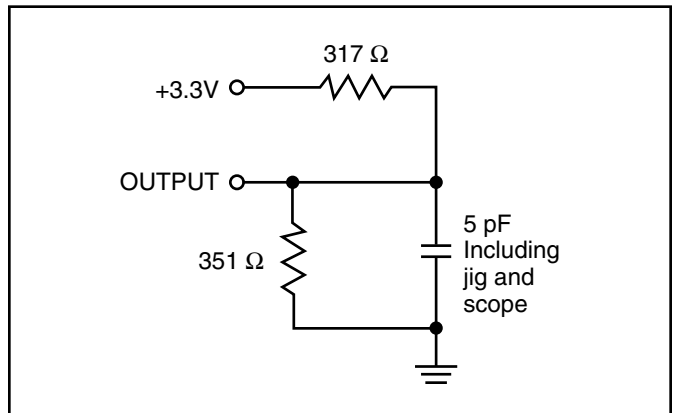


Figure 2

**2.5V I/O AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

**2.5V I/O OUTPUT LOAD EQUIVALENT**

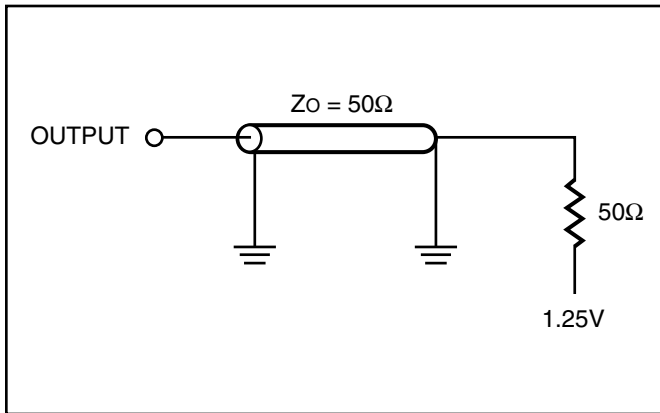


Figure 3

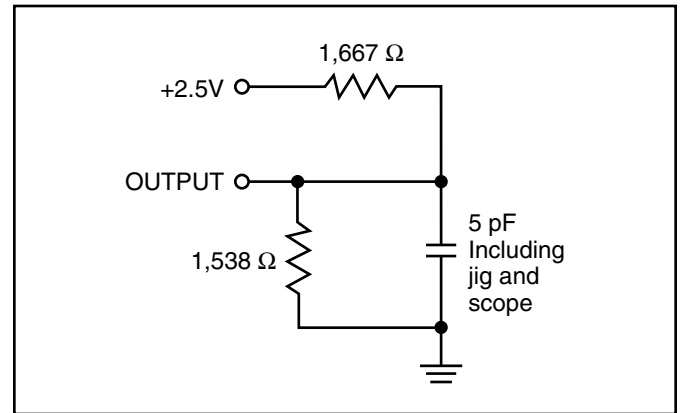


Figure 4

**READ/WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	6.5		7.5		Unit
		Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	133	—	117	MHz
tkc	Cycle Time	7.5	—	8.5	—	ns
tkH	Clock High Time	2.2	—	2.5	—	ns
tkL	Clock Low Time	2.2	—	2.5	—	ns
tkQ	Clock Access Time	—	6.5	—	7.5	ns
tkQX <sup>(2)</sup>	Clock High to Output Invalid	2.5	—	2.5	—	ns
tkQLZ <sup>(2,3)</sup>	Clock High to Output Low-Z	2.5	—	2.5	—	ns
tkQHZ <sup>(2,3)</sup>	Clock High to Output High-Z	—	3.8	—	4.0	ns
toEQ	Output Enable to Output Valid	—	3.2	—	3.4	ns
toELZ <sup>(2,3)</sup>	Output Enable to Output Low-Z	0	—	0	—	ns
toEHZ <sup>(2,3)</sup>	Output Disable to Output High-Z	—	3.5	—	3.5	ns
tAS	Address Setup Time	1.5	—	1.5	—	ns
tWS	Read/Write Setup Time	1.5	—	1.5	—	ns
tCES	Chip Enable Setup Time	1.5	—	1.5	—	ns
tSE	Clock Enable Setup Time	1.5	—	1.5	—	ns
tADVS	Address Advance Setup Time	1.5	—	1.5	—	ns
tDS	Data Setup Time	1.5	—	1.5	—	ns
tAH	Address Hold Time	0.5	—	0.5	—	ns
tHE	Clock Enable Hold Time	0.5	—	0.5	—	ns
tWH	Write Hold Time	0.5	—	0.5	—	ns
tCEH	Chip Enable Hold Time	0.5	—	0.5	—	ns
tADVH	Address Advance Hold Time	0.5	—	0.5	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	ns
tpDS	ZZ High to Power Down	—	2	—	2	cyc
tpUS	ZZ Low to Power Down	—	2	—	2	cyc

**Notes:**

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.



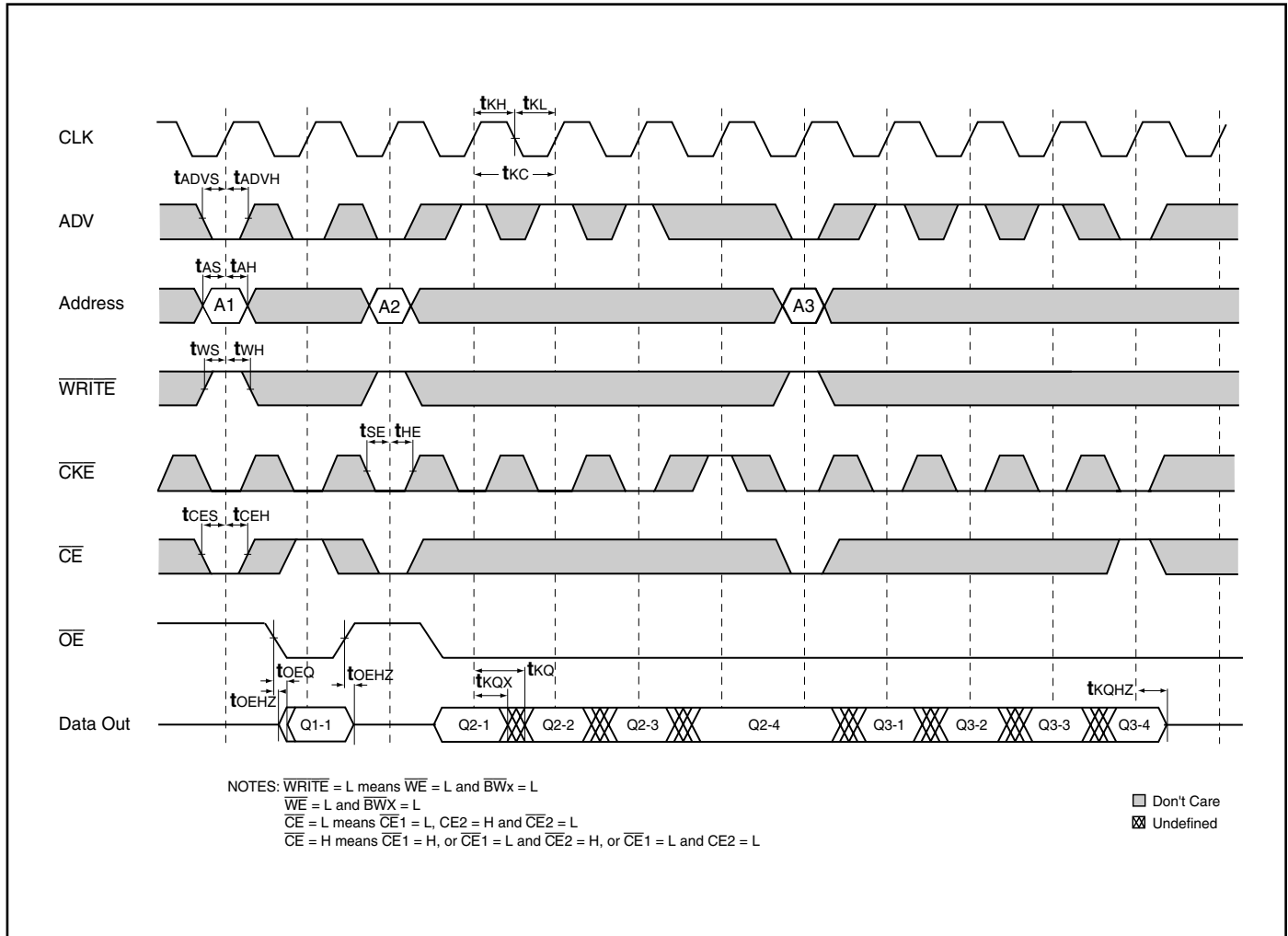
**SLEEP MODE ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Max.	Unit
$I_{SB2}$	Current during SLEEP MODE	$ZZ \geq V_{IH}$		35	mA
$t_{PDS}$	ZZ active to input ignored			2	cycle
$t_{PUS}$	ZZ inactive to input sampled		2		cycle
$t_{ZZI}$	ZZ active to SLEEP current		2		cycle
$t_{RZZI}$	ZZ inactive to exit SLEEP current		0		ns

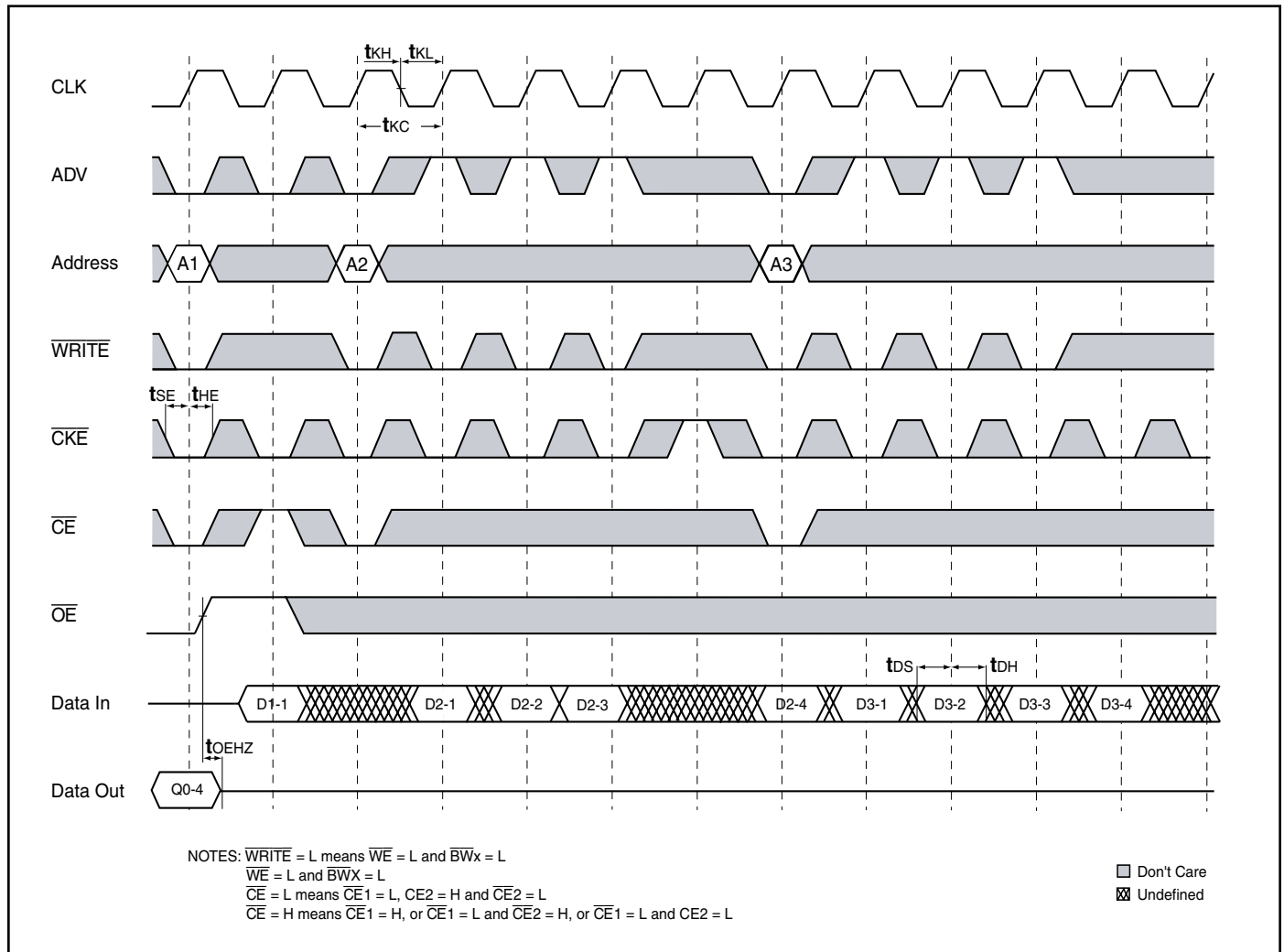
**SLEEP MODE TIMING**



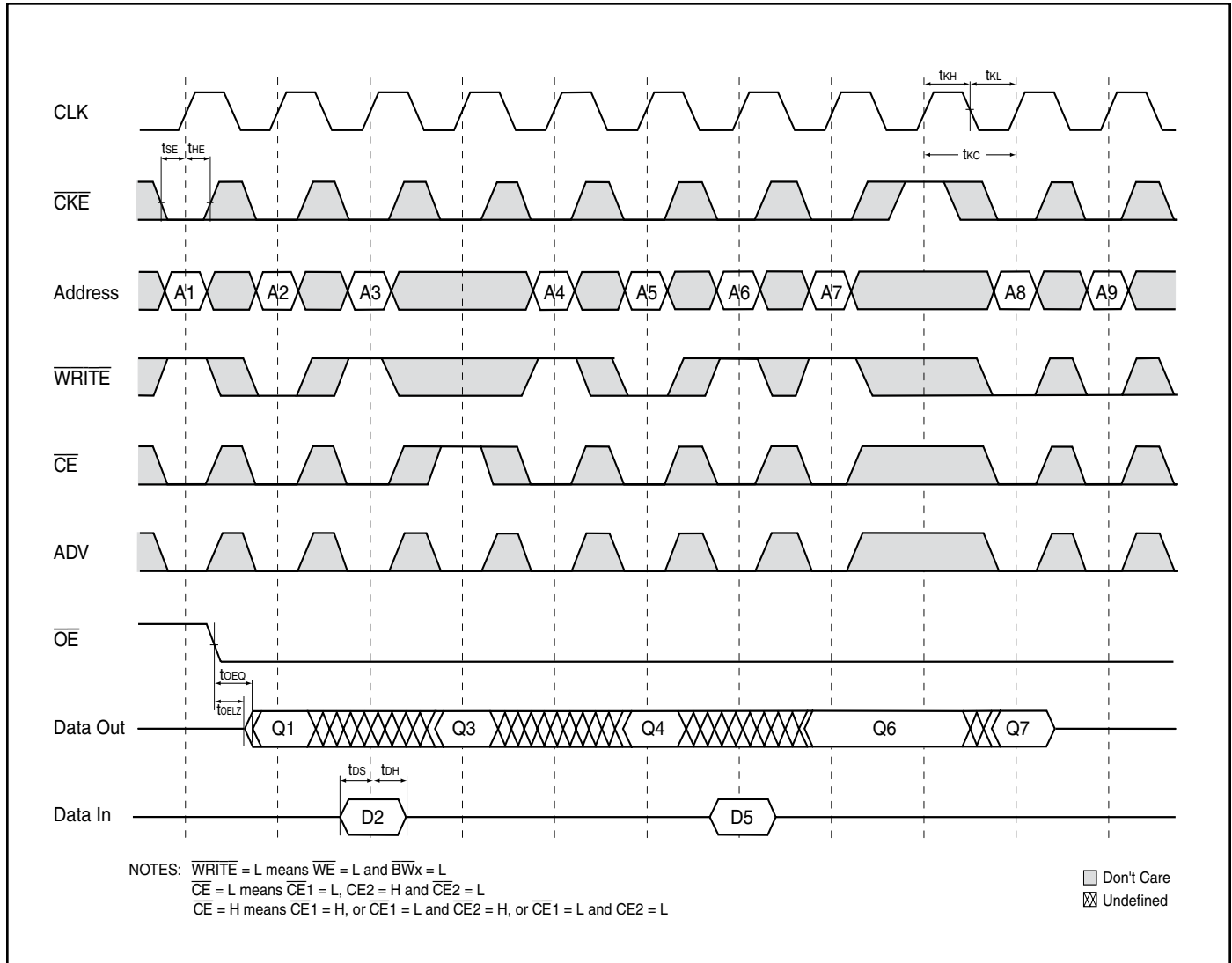
READ CYCLE TIMING



## WRITE CYCLE TIMING



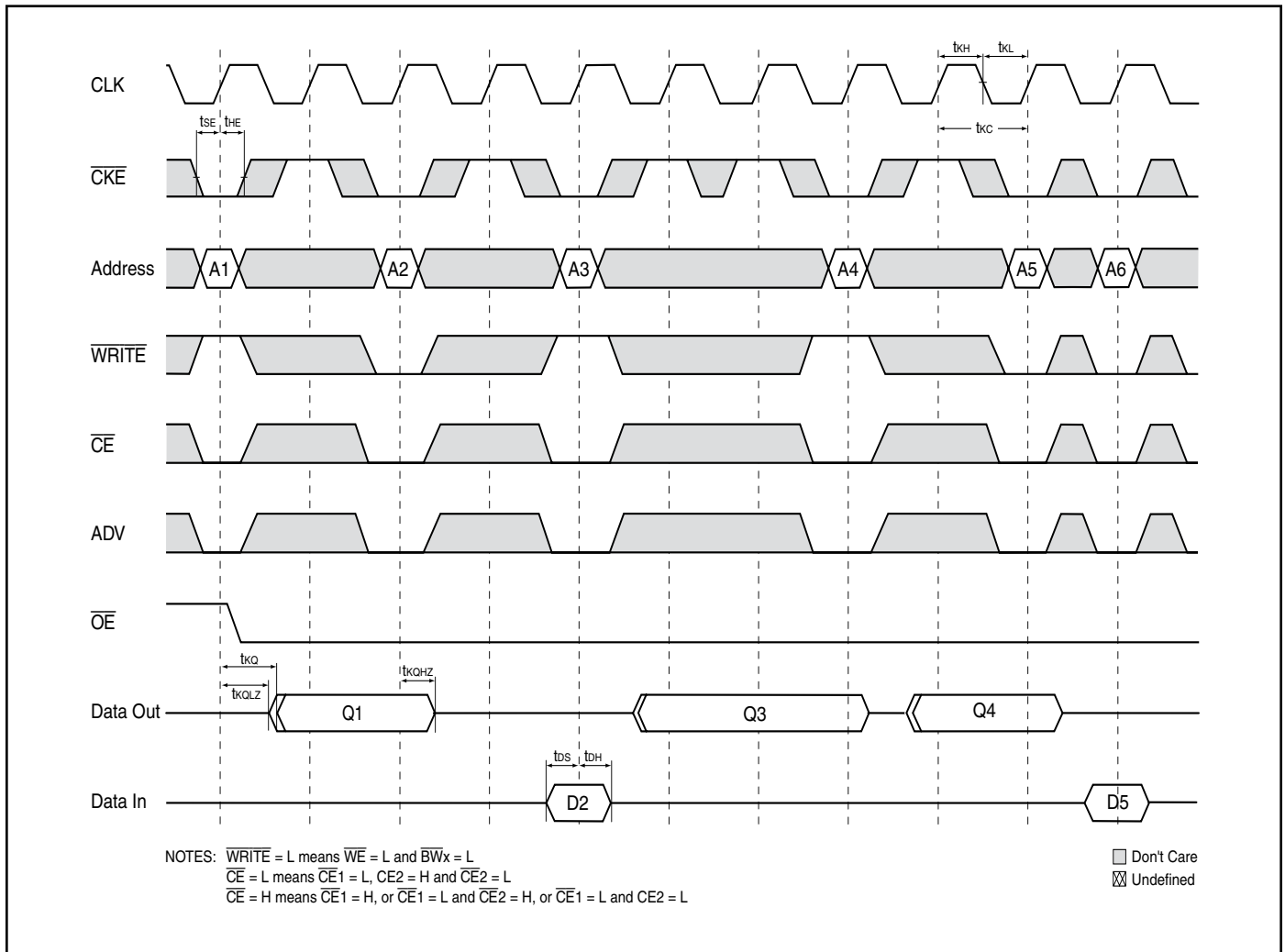
**SINGLE READ/WRITE CYCLE TIMING**



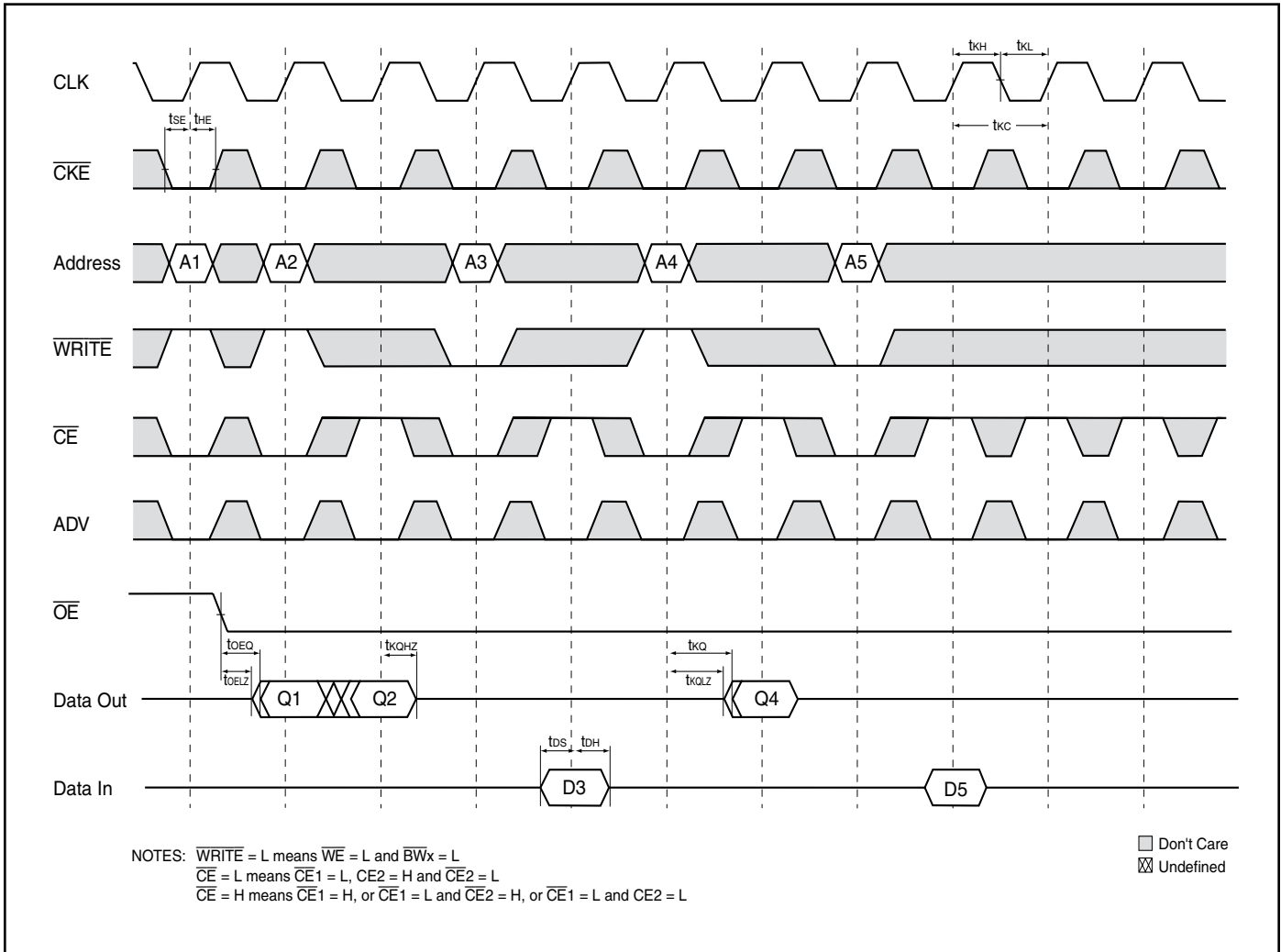
NOTES:  $\overline{WRITE} = L$  means  $\overline{WE} = L$  and  $\overline{BWx} = L$   
 $\overline{CE} = L$  means  $\overline{CE1} = L$ ,  $CE2 = H$  and  $\overline{CE2} = L$   
 $\overline{CE} = H$  means  $\overline{CE1} = H$ , or  $\overline{CE1} = L$  and  $CE2 = H$ , or  $\overline{CE1} = L$  and  $\overline{CE2} = L$

□ Don't Care  
 ⊗ Undefined

**CKE OPERATION TIMING**



**CE OPERATION TIMING**





**IS61NLF12836A/IS61NVF12836A**  
**IS61NLF25618A/IS61NVF25618A**

**ORDERING INFORMATION ( $V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V$ )**  
**Commercial Range: 0°C to +70°C**

Access Time	Order Part Number	Package
<b>128Kx36</b>		
6.5	IS61NLF12836A-6.5TQ	100 TQFP
	IS61NLF12836A-6.5B2	119 PBGA
	IS61NLF12836A-6.5B3	165 PBGA
7.5	IS61NLF12836A-7.5TQ	100 TQFP
	IS61NLF12836A-7.5B2	119 PBGA
	IS61NLF12836A-7.5B3	165 PBGA
<b>256Kx18</b>		
6.5	IS61NLF25618A-6.5TQ	100 TQFP
	IS61NLF25618A-6.5B2	119 PBGA
	IS61NLF25618A-6.5B3	165 PBGA
7.5	IS61NLF25618A-7.5TQ	100 TQFP
	IS61NLF25618A-7.5B2	119 PBGA
	IS61NLF25618A-7.5B3	165 PBGA

**Industrial Range: -40°C to +85°C**

Access Time	Order Part Number	Package
<b>128Kx36</b>		
6.5	IS61NLF12836A-6.5TQI	100 TQFP
	IS61NLF12836A-6.5B2I	119 PBGA
	IS61NLF12836A-6.5B3I	165 PBGA
7.5	IS61NLF12836A-7.5TQI	100 TQFP
	IS61NLF12836A-7.5TQLI	100 TQFP, Lead-free
	IS61NLF12836A-7.5B2I	119 PBGA
	IS61NLF12836A-7.5B3I	165 PBGA
	IS61NLF12836A-7.5B3LI	165 PBGA, Lead-free
<b>256Kx18</b>		
6.5	IS61NLF25618A-6.5TQI	100 TQFP
	IS61NLF25618A-6.5B2I	119 PBGA
	IS61NLF25618A-6.5B3I	165 PBGA
7.5	IS61NLF25618A-7.5TQI	100 TQFP
	IS61NLF25618A-7.5TQLI	100 TQFP, Lead-free
	IS61NLF25618A-7.5B2I	119 PBGA
	IS61NLF25618A-7.5B3I	165 PBGA

**ORDERING INFORMATION (V<sub>DD</sub> = 2.5V/V<sub>DDQ</sub> = 2.5V)**

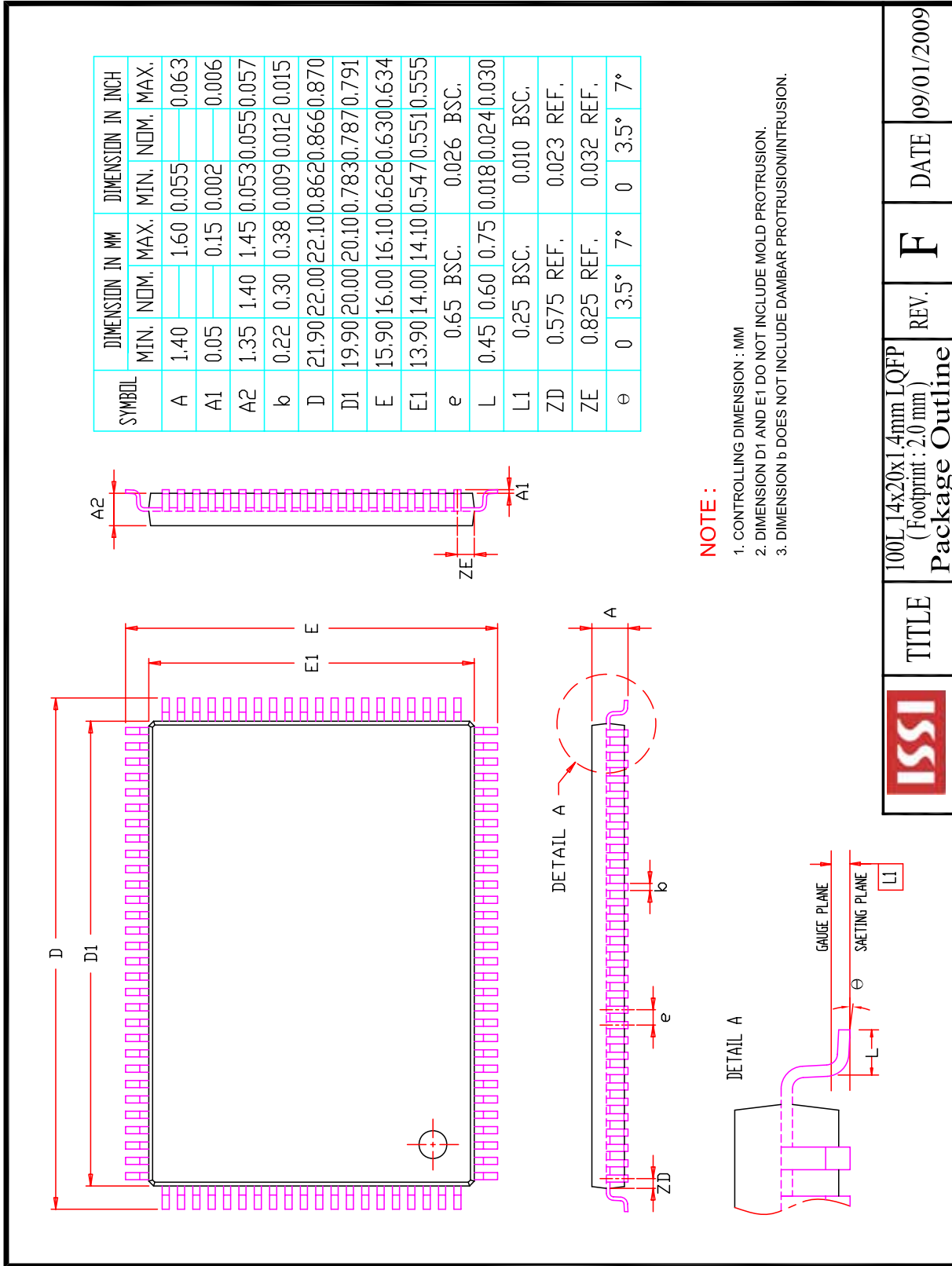
**Commercial Range: 0°C to +70°C**

Access Time	Order Part Number	Package
<b>128Kx36</b>		
6.5	IS61NVF12836A-6.5TQ	100 TQFP
	IS61NVF12836A-6.5B2	119 PBGA
	IS61NVF12836A-6.5B3	165 PBGA
7.5	IS61NVF12836A-7.5TQ	100 TQFP
	IS61NVF12836A-7.5B2	119 PBGA
	IS61NVF12836A-7.5B3	165 PBGA
<b>256Kx18</b>		
6.5	IS61NVF25618A-6.5TQ	100 TQFP
	IS61NVF25618A-6.5B2	119 PBGA
	IS61NVF25618A-6.5B3	165 PBGA
7.5	IS61NVF25618A-7.5TQ	100 TQFP
	IS61NVF25618A-7.5B2	119 PBGA
	IS61NVF25618A-7.5B3	165 PBGA

**Industrial Range: -40°C to +85°C**

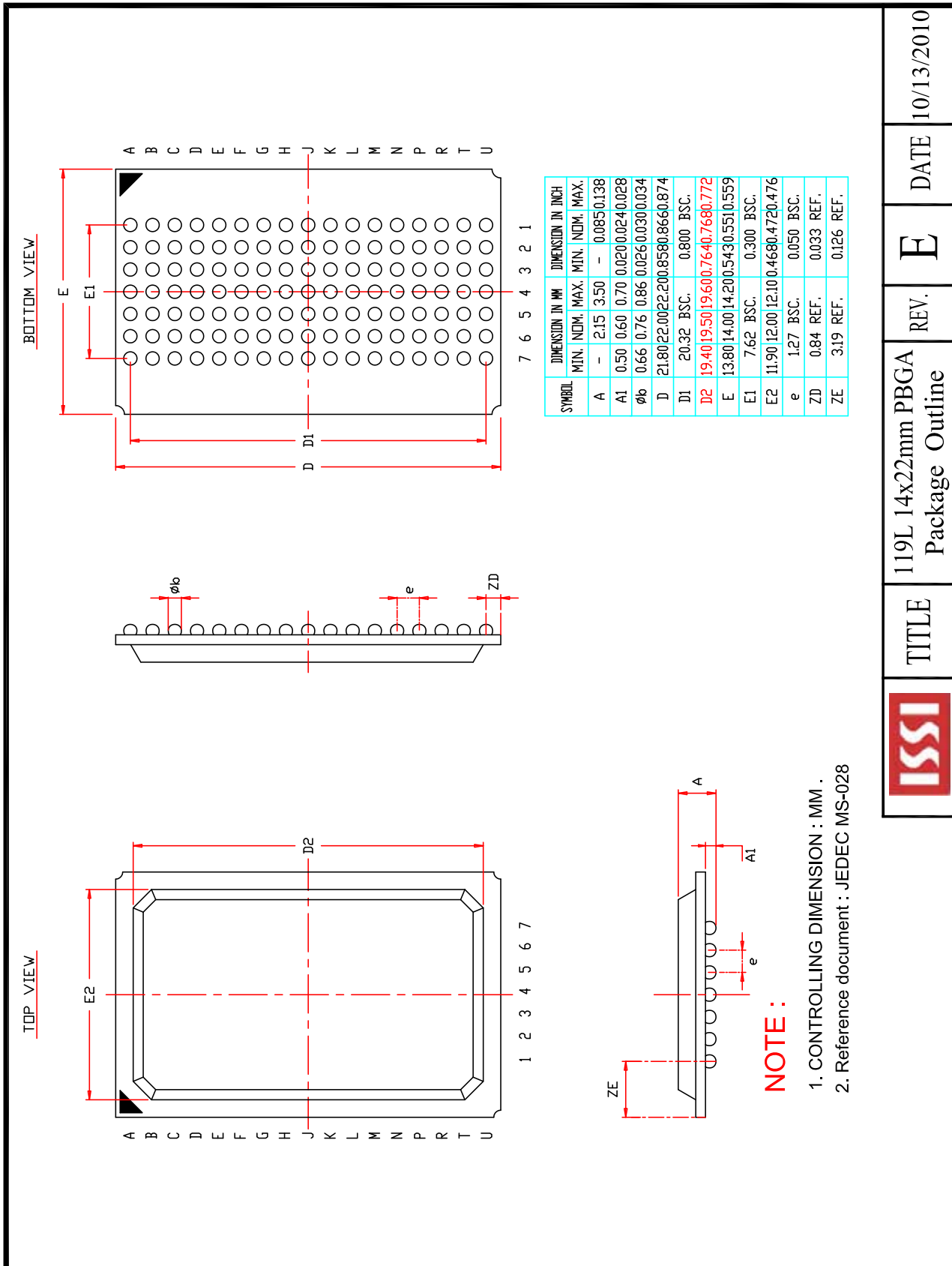
Access Time	Order Part Number	Package
<b>128Kx36</b>		
6.5	IS61NVF12836A-6.5TQI	100 TQFP
	IS61NVF12836A-6.5B2I	119 PBGA
	IS61NVF12836A-6.5B3I	165 PBGA
7.5	IS61NVF12836A-7.5TQI	100 TQFP
	IS61NVF12836A-7.5B2I	119 PBGA
	IS61NVF12836A-7.5B3I	165 PBGA
<b>256Kx18</b>		
6.5	IS61NVF25618A-6.5TQI	100 TQFP
	IS61NVF25618A-6.5B2I	119 PBGA
	IS61NVF25618A-6.5B3I	165 PBGA
7.5	IS61NVF25618A-7.5TQI	100 TQFP
	IS61NVF25618A-7.5B2I	119 PBGA
	IS61NVF25618A-7.5B3I	165 PBGA



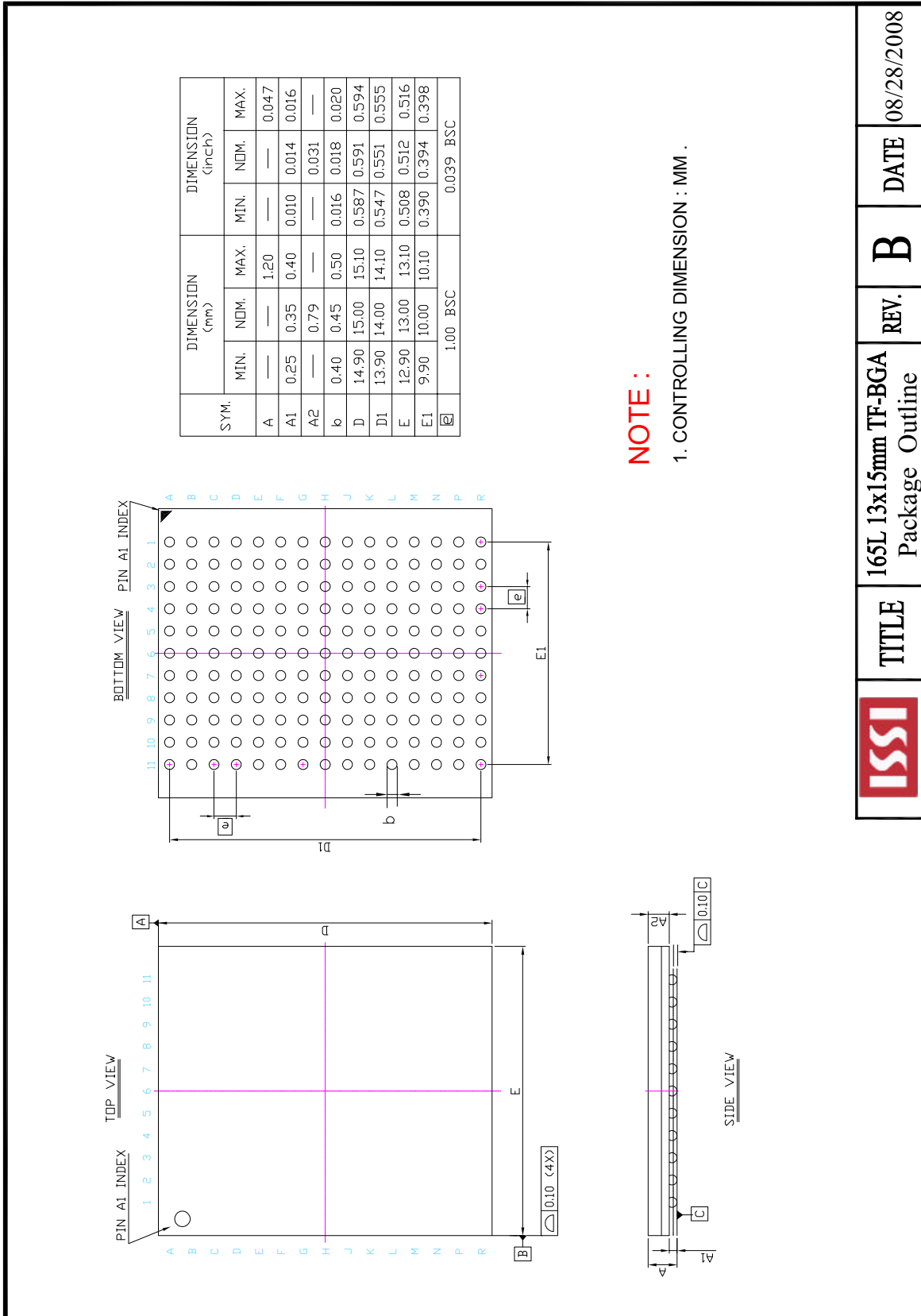


	TITLE	REV.	DATE
	100L 14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline	F	09/01/2009

280-600-011 REV. A



	TITLE	REV.	DATE
	119L 14x22mm PBGA Package Outline	E	10/13/2010



	TITLE	165L 13x15mm TF-BGA Package Outline	REV. B	DATE 08/28/2008
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