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April 1st, 2010
Renesas Electronics Corporation

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1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 32-pin molded-plastic LQFP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/27 Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/26 Group and R8C/27 Group is only the presence or absence of data flash.

Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/26 Group and Table 1.2 outlines the Functions and Specifications for R8C/27 Group.

Table 1.1 Functions and Specifications for R8C/26 Group

| | Item | Specification |
|-------------------------------|------------------------------------|--|
| CPU | Number of fundamental instructions | 89 instructions |
| | Minimum instruction execution time | 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version) |
| | Operating mode | Single-chip |
| | Address space | 1 Mbyte |
| | Memory capacity | Refer to Table 1.3 Product Information for R8C/26 Group |
| Peripheral Functions | Ports | I/O ports: 25 pins, Input port: 3 pins |
| | LED drive ports | I/O ports: 8 pins (N, D version) |
| | Timers | Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.) |
| | Serial interfaces | 2 channels (UART0, UART1) Clock synchronous serial I/O, UART |
| | Clock synchronous serial interface | 1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select |
| | LIN module | Hardware LIN: 1 channel (timer RA, UART0) |
| | A/D converter | 10-bit A/D converter: 1 circuit, 12 channels |
| | Watchdog timer | 15 bits × 1 channel (with prescaler) Start-on-reset selectable |
| | Interrupts | Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels |
| | Clock generation circuits | 3 circuits <ul style="list-style-type: none"> • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz) (N, D version) • Real-time clock (timer RE) (N, D version) |
| | Oscillation-stopped detector | XIN clock oscillation stop detection function |
| | Voltage detection circuit | On-chip |
| | Power-on reset circuit | On-chip |
| Electrical Characteristics | Supply voltage | VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version) |
| | Current consumption (N, D version) | Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Flash Memory | Programming and erasure voltage | VCC = 2.7 to 5.5 V |
| | Programming and erasure endurance | 100 times |
| Operating Ambient Temperature | | -20 to 85°C (N version) |
| | | -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾ |
| Package | | 32-pin molded-plastic LQFP |

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D, K version if D, K version functions are to be used.

Table 1.2 Functions and Specifications for R8C/27 Group

| | Item | Specification |
|------------------------------------|------------------------------------|--|
| CPU | Number of fundamental instructions | 89 instructions |
| | Minimum instruction execution time | 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version) 62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version) |
| | Operating mode | Single-chip |
| | Address space | 1 Mbyte |
| | Memory capacity | Refer to Table 1.4 Product Information of R8C/27 Group |
| Peripheral Functions | Ports | I/O ports: 25 pins, Input port: 3 pins |
| | LED drive ports | I/O ports: 8 pins (N, D version) |
| | Timers | Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RC: 16 bits × 1 channel (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.) |
| | Serial interfaces | 2 channels (UART0, UART1) Clock synchronous serial I/O, UART |
| | Clock synchronous serial interface | 1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select |
| | LIN module | Hardware LIN: 1 channel (timer RA, UART0) |
| | A/D converter | 10-bit A/D converter: 1 circuit, 12 channels |
| | Watchdog timer | 15 bits × 1 channel (with prescaler) Start-on-reset selectable |
| | Interrupts | Internal: 15 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels |
| | Clock generation circuits | 3 circuits <ul style="list-style-type: none"> XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function XCIN clock generation circuit (32 kHz) (N, D version) Real-time clock (timer RE) (N, D version) |
| | Oscillation-stopped detector | XIN clock oscillation stop detection function |
| | Voltage detection circuit | On-chip |
| | Power-on reset circuit | On-chip |
| | Electrical Characteristics | Supply voltage |
| Current consumption (N, D version) | | Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Flash Memory | Programming and erasure voltage | VCC = 2.7 to 5.5 V |
| | Programming and erasure endurance | 10,000 times (data flash) 1,000 times (program ROM) |
| Operating Ambient Temperature | | -20 to 85°C (N version) -40 to 85°C (D, J version) ⁽²⁾ , -40 to 125°C (K version) ⁽²⁾ |
| | Package | 32-pin molded-plastic LQFP |

NOTES:

- I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- Specify the D, K version if D, K version functions are to be used.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

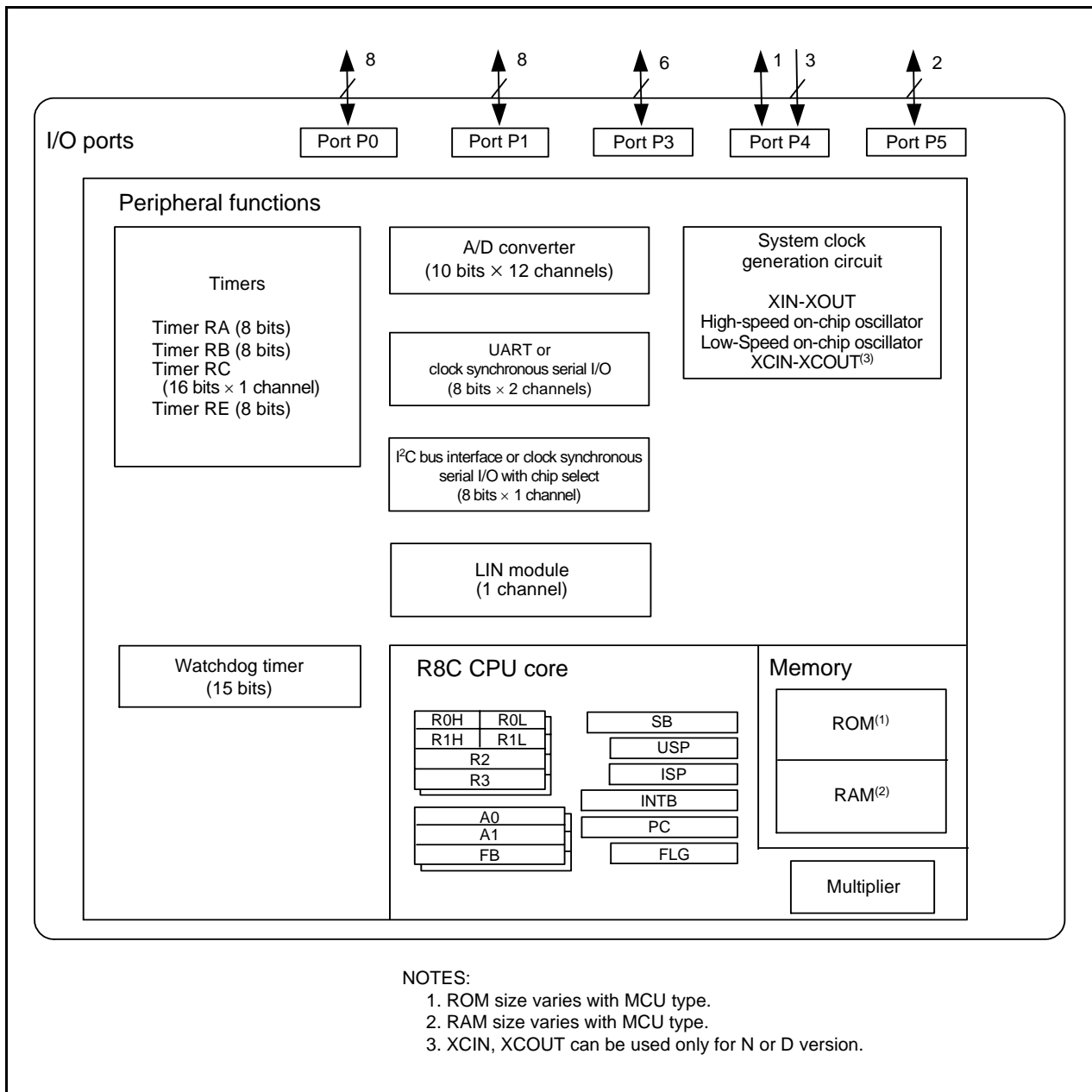


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/26 Group and Table 1.4 lists the Product Information for R8C/27 Group.

Table 1.3 Product Information for R8C/26 Group

Current of Sep. 2008

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks | |
|-----------------|--------------|--------------|--------------|-----------|--|
| R5F21262SNFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | N version | |
| R5F21264SNFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | | |
| R5F21265SNFP | 24 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21266SNFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21262SDFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | D version | |
| R5F21264SDFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | | |
| R5F21265SDFP | 24 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21266SDFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21264JFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | J version | |
| R5F21266JFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21264KFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | K version | |
| R5F21266KFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21262SNXXXFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | N version | Factory programming product ⁽¹⁾ |
| R5F21264SNXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | | |
| R5F21265SNXXXFP | 24 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21266SNXXXFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21262SDXXXFP | 8 Kbytes | 512 bytes | PLQP0032GB-A | D version | |
| R5F21264SDXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | | |
| R5F21265SDXXXFP | 24 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21266SDXXXFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21264JXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | J version | |
| R5F21266JXXXFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21264KXXXFP | 16 Kbytes | 1 Kbyte | PLQP0032GB-A | K version | |
| R5F21266KXXXFP | 32 Kbytes | 1.5 Kbytes | PLQP0032GB-A | | |

NOTE:

1. The user ROM is programmed before shipment.

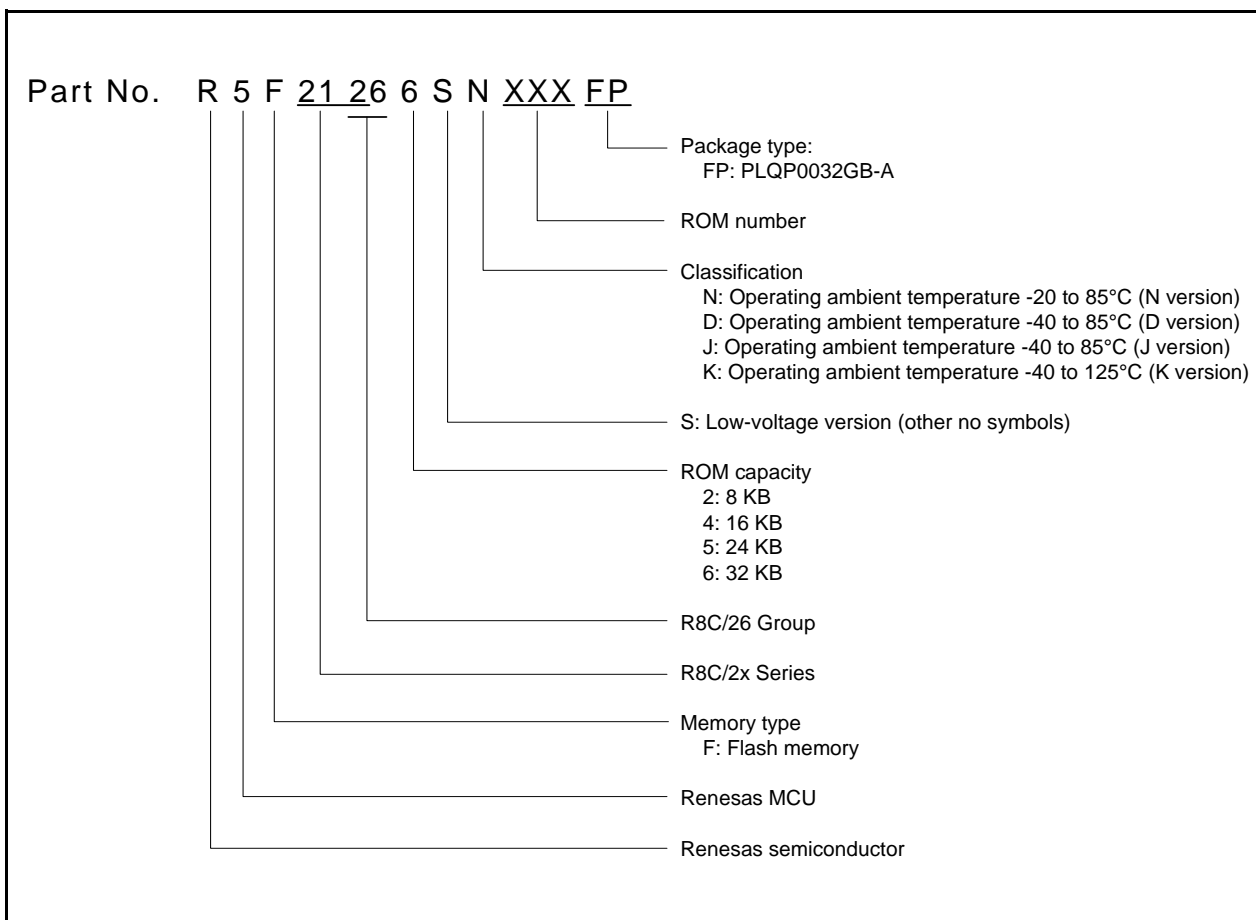


Figure 1.2 Part Number, Memory Size, and Package of R8C/26 Group

Table 1.4 Product Information for R8C/27 Group

Current of Sep. 2008

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks | |
|-----------------|--------------|-------------|--------------|--------------|-----------|--|
| | Program ROM | Data flash | | | | |
| R5F21272SNFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | N version | |
| R5F21274SNFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | | |
| R5F21275SNFP | 24 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21276SNFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21272SDFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | D version | |
| R5F21274SDFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | | |
| R5F21275SDFP | 24 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21276SDFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21274JFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | J version | |
| R5F21276JFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21274KFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | K version | |
| R5F21276KFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21272SNXXXFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | N version | Factory programming product ⁽¹⁾ |
| R5F21274SNXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | | |
| R5F21275SNXXXFP | 24 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21276SNXXXFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21272SDXXXFP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLQP0032GB-A | D version | |
| R5F21274SDXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | | |
| R5F21275SDXXXFP | 24 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21276SDXXXFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21274JXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | J version | |
| R5F21276JXXXFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |
| R5F21274KXXXFP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLQP0032GB-A | K version | |
| R5F21276KXXXFP | 32 Kbytes | 1 Kbyte × 2 | 1.5 Kbytes | PLQP0032GB-A | | |

NOTE:

1. The user ROM is programmed before shipment.

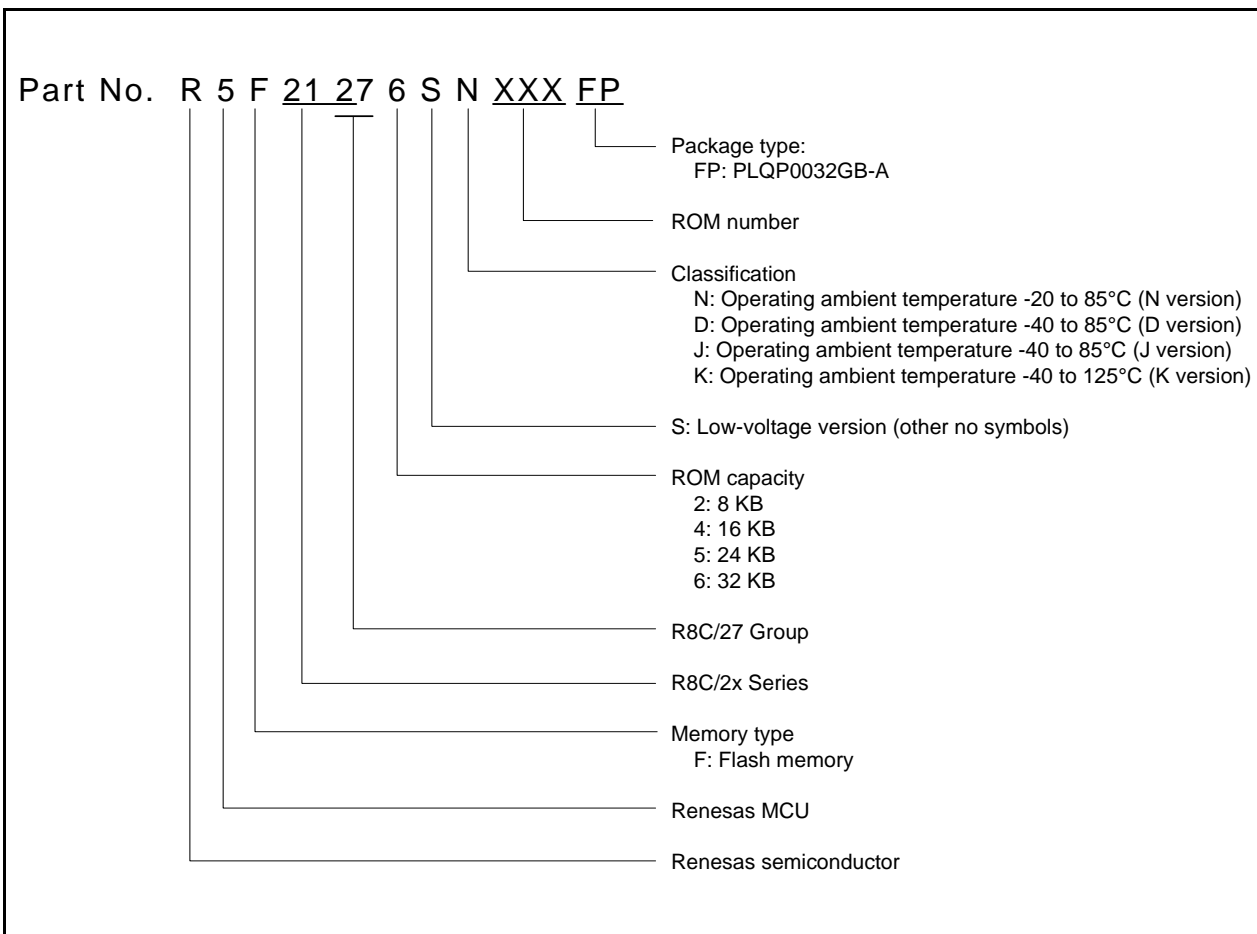


Figure 1.3 Part Number, Memory Size, and Package of R8C/27 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

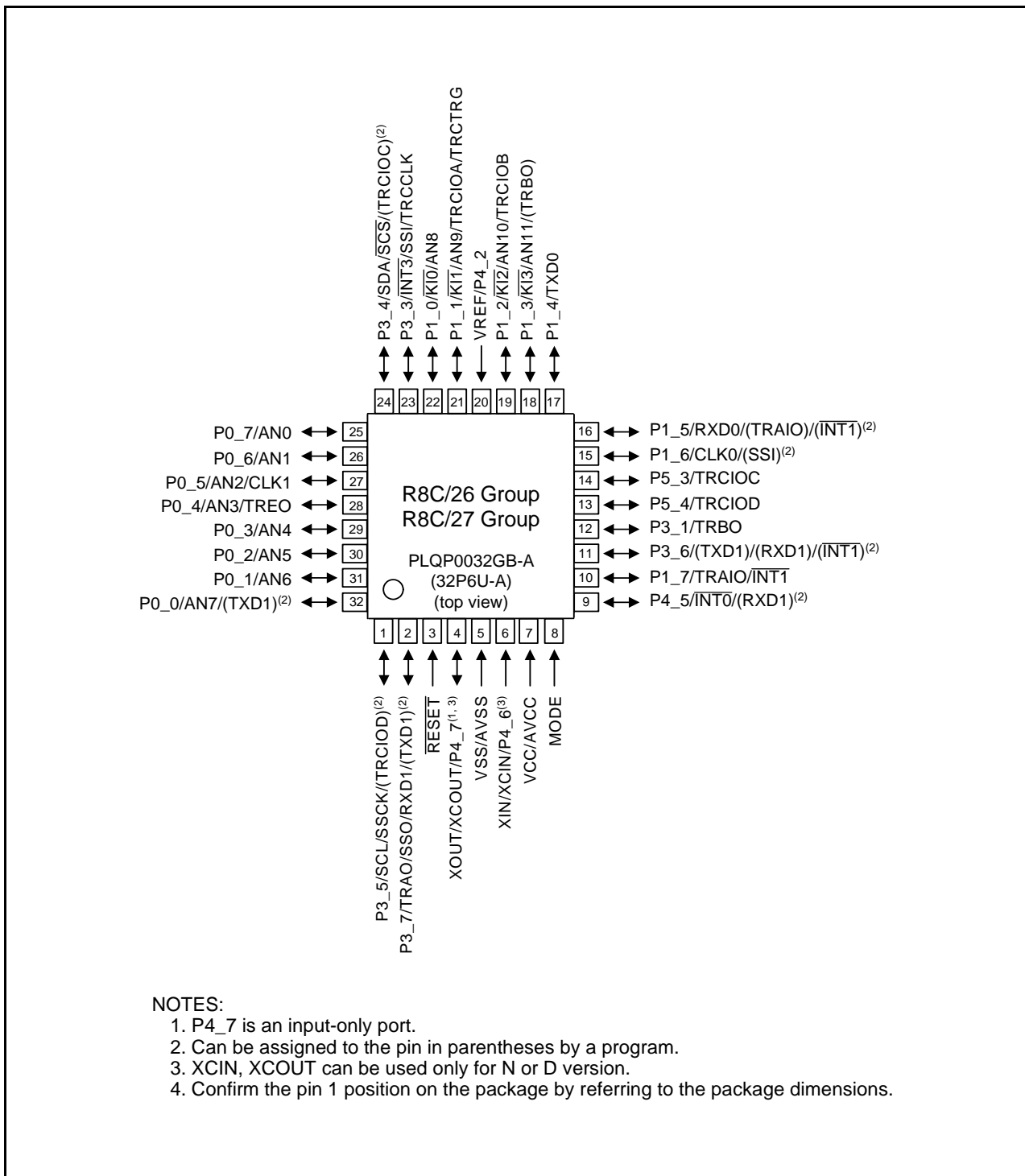


Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

| Type | Symbol | I/O Type | Description |
|---|--|----------|--|
| Power supply input | VCC, VSS | I | Apply 2.2 to 5.5 V (J, K version are 2.7 to 5.5 V) to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input "L" on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output | XOUT | O | |
| XCIN clock input (N, D version) | XCIN | I | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins. To use an external clock, input it to the XCIN pin and leave the XCOU pin open. |
| XCIN clock output (N, D version) | XCOU | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRA0 | O | Timer RA output pin |
| | TRAIO | I/O | Timer RA I/O pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RC | TRCLK | I | External clock input pin |
| | TRCTR | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIO, TRCIOD | I/O | Sharing output-compare output / input-capture input / PWM / PWM2 output pins |
| Timer RE | TREO | O | Timer RE output pin |
| Serial interface | CLK0, CLK1 | I/O | Clock I/O pin |
| | RXD0, RXD1 | I | Receive data input pin |
| | TXD0, TXD1 | O | Transmit data output pin |
| I ² C bus interface | SCL | I/O | Clock I/O pin |
| | SDA | I/O | Data I/O pin |
| Clock synchronous serial I/O with chip select | SSI | I/O | Data I/O pin |
| | $\overline{\text{SCS}}$ | I/O | Chip-select signal I/O pin |
| | SSCK | I/O | Clock I/O pin |
| | SSO | I/O | Data I/O pin |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter |
| A/D converter | AN0 to AN11 | I | Analog input pins to A/D converter |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P3_1, P3_3 to P3_7, P4_5, P5_3, P5_4 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_7 also function as LED drive ports (N, D version). |
| Input port | P4_2, P4_6, P4_7 | I | Input-only ports |

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | |
|------------|---------------------------|------|---|-------------------------|-------------------------------------|---|--------------------------------|---------------|
| | | | Interrupt | Timer | Serial Interface | Clock Synchronous Serial I/O with Chip Select | I ² C bus Interface | A/D Converter |
| 1 | | P3_5 | | (TRCIOD) ⁽¹⁾ | | SSCK | SCL | |
| 2 | | P3_7 | | TRAO | RXD1/ (TXD1) ^(1, 3) | SSO | | |
| 3 | RESET | | | | | | | |
| 4 | XOUT/XCOUT ⁽²⁾ | P4_7 | | | | | | |
| 5 | VSS/AVSS | | | | | | | |
| 6 | XIN/XCIN ⁽²⁾ | P4_6 | | | | | | |
| 7 | VCC/AVCC | | | | | | | |
| 8 | MODE | | | | | | | |
| 9 | | P4_5 | $\overline{\text{INT0}}$ | | (RXD1) ^(1, 3) | | | |
| 10 | | P1_7 | $\overline{\text{INT1}}$ | TRAIO | | | | |
| 11 | | P3_6 | $\overline{(\text{INT1})}^{(1)}$ | | (TXD1)/ (RXD1) ^(1, 3) | | | |
| 12 | | P3_1 | | TRBO | | | | |
| 13 | | P5_4 | | TRCIOD | | | | |
| 14 | | P5_3 | | TRCIOC | | | | |
| 15 | | P1_6 | | | CLK0 | (SSI) ⁽¹⁾ | | |
| 16 | | P1_5 | $\overline{(\text{INT1})}^{(1)}$ | (TRAIO) ⁽¹⁾ | RXD0 | | | |
| 17 | | P1_4 | | | TXD0 | | | |
| 18 | | P1_3 | $\overline{\text{KI3}}$ | (TRBO) | | | | AN11 |
| 19 | | P1_2 | $\overline{\text{KI2}}$ | TRCIOB | | | | AN10 |
| 20 | VRFF | P4_2 | | | | | | |
| 21 | | P1_1 | $\overline{\text{KI1}}$ | TRCIOA/ TRCTRG | | | | AN9 |
| 22 | | P1_0 | $\overline{\text{KI0}}$ | | | | | AN8 |
| 23 | | P3_3 | $\overline{\text{INT3}}$ | TRCCLK | | SSI | | |
| 24 | | P3_4 | | (TRCIOC) ⁽¹⁾ | | $\overline{\text{SCS}}$ | SDA | |
| 25 | | P0_7 | | | | | | AN0 |
| 26 | | P0_6 | | | | | | AN1 |
| 27 | | P0_5 | | | CLK1 | | | AN2 |
| 28 | | P0_4 | | TREO | | | | AN3 |
| 29 | | P0_3 | | | | | | AN4 |
| 30 | | P0_2 | | | | | | AN5 |
| 31 | | P0_1 | | | | | | AN6 |
| 32 | | P0_0 | | | (TXD1) ^(1, 3) | | | AN7 |

NOTES:

1. This can be assigned to the pin in parentheses by a program.
2. XCIN, XCOU can be used only for N or D version.
3. For the combination of using pins TXD1 and RXD1, refer to **Figure 15.7 Registers PINSR1 and PMR** of Hardware Manual (REJ09B0278).

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

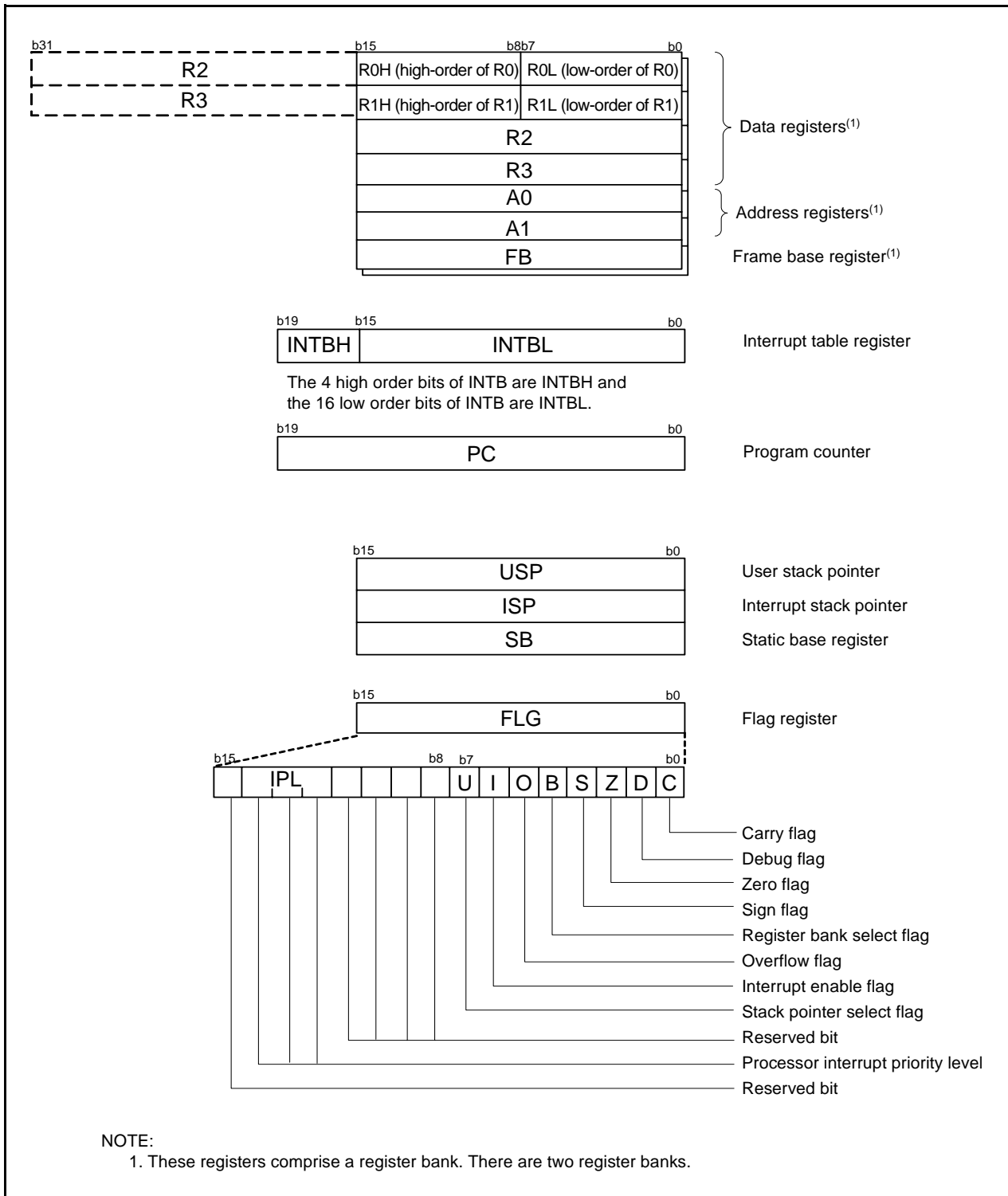


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/26 Group

Figure 3.1 is a Memory Map of R8C/26 Group. The R8C/26 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

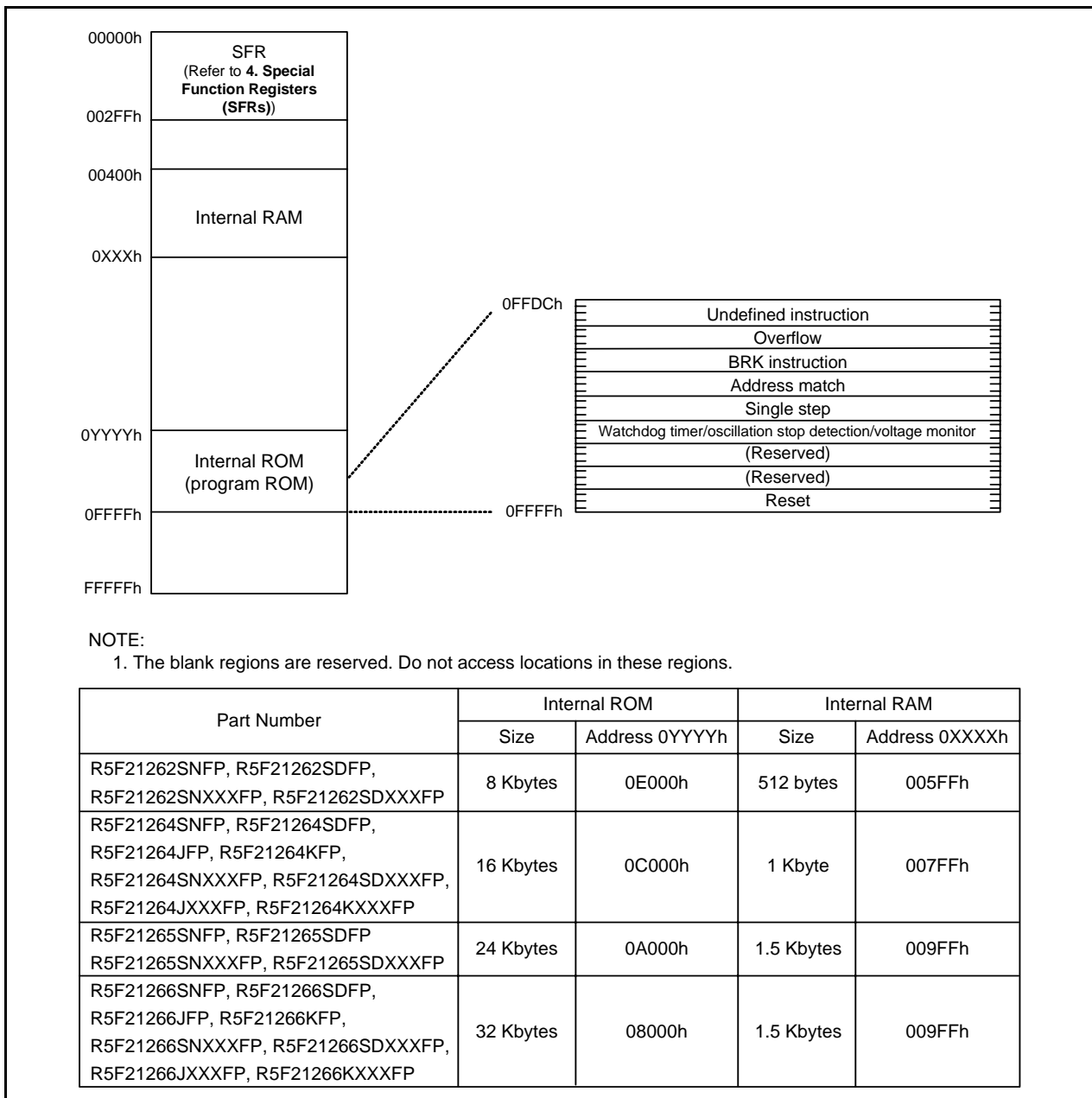


Figure 3.1 Memory Map of R8C/26 Group

3.2 R8C/27 Group

Figure 3.2 is a Memory Map of R8C/27 Group. The R8C/27 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

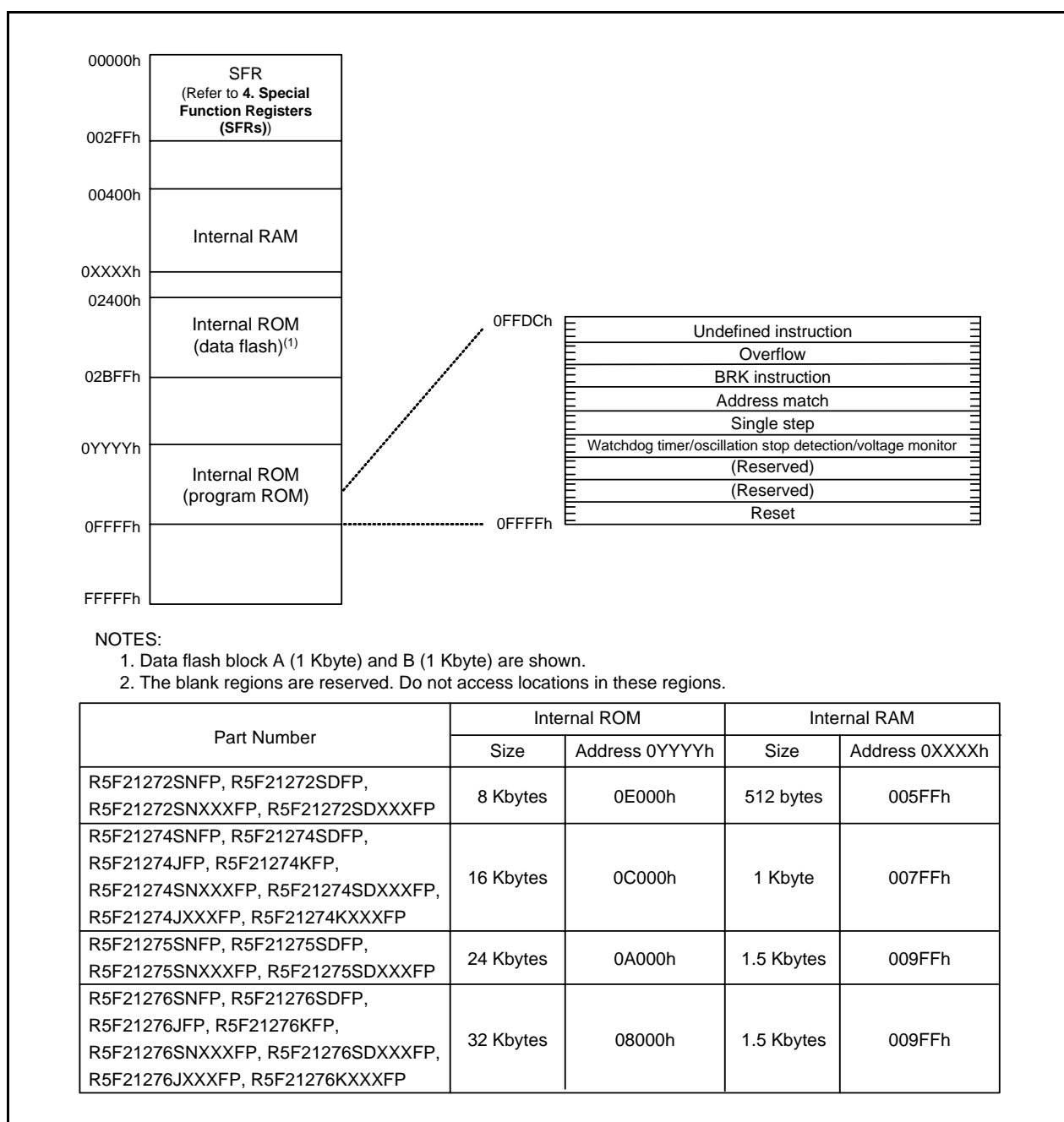


Figure 3.2 Memory Map of R8C/27 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|---------------------------------|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | | | |
| 0009h | | | |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00X11111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | 00h |
| 0013h | Address Match Interrupt Enable Register | AIER | 00h |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | 00h |
| 0017h | | | 00h |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h 10000000b ⁽²⁾ |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | | | |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag | CPSRF | 00h |
| 0029h | High-Speed On-Chip Oscillator Control Register 4 ⁽³⁾ | FRA4 | When shipping |
| 002Ah | | | |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 ⁽³⁾ | FRA6 | When shipping |
| 002Ch | High-Speed On-Chip Oscillator Control Register 7 ⁽³⁾ | FRA7 | When shipping |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)(1)

| Address | Register | Symbol | After reset |
|---------|--|-------------|--|
| 0030h | | | |
| 0031h | Voltage Detection Register 1 (2) | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2 (2) | VCA2 | • N, D version 00h(3) 00100000b(4) • J, K version 00h(7) 01000000b(8) |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register (5) | VW1C | • N, D version 00001000b • J, K version 0000X000b(7) 0100X001b(8) |
| 0037h | Voltage Monitor 2 Circuit Control Register (5) | VW2C | 00h |
| 0038h | Voltage Monitor 0 Circuit Control Register (6) | VW0C | 0000X000b(3) 0100X001b(4) |
| 0039h | | | |
| 003Fh | | | |
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | | | |
| 0049h | | | |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | | | |
| 004Ch | | | |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | SSU/IIC bus Interrupt Control Register(9) | SSUIC/IICIC | XXXXX000b |
| 0050h | | | |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | | | |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | | | |
| 005Ch | | | |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | | | |
| 0060h | | | |
| 006Fh | | | |
| 0070h | | | |
| 007Fh | | | |

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- The LVD0ON bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
(J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
(J, K version) These regions are reserved. Do not access locations in these regions.
- The LVD1ON bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 1 reset, or the LVD1ON bit in the OFS register is set to 0 and hardware reset.
- Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|---------------|-----------------|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 00A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 00AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 00ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 00AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 00AFh | | | XXh |
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | SS Control Register H / IIC bus Control Register 1 ⁽²⁾ | SSCRH / ICCR1 | 00h |
| 00B9h | SS Control Register L / IIC bus Control Register 2 ⁽²⁾ | SSCRL / ICCR2 | 01111101b |
| 00BAh | SS Mode Register / IIC bus Mode Register ⁽²⁾ | SSMR / ICMR | 00011000b |
| 00BBh | SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾ | SSER / ICIER | 00h |
| 00BCh | SS Status Register / IIC bus Status Register ⁽²⁾ | SSSR / ICSR | 00h / 0000X000b |
| 00BDh | SS Mode Register 2 / Slave Address Register ⁽²⁾ | SSMR2 / SAR | 00h |
| 00BEh | SS Transmit Data Register / IIC bus Transmit Data Register ⁽²⁾ | SSTDR / ICDRT | FFh |
| 00BFh | SS Receive Data Register / IIC bus Receive Data Register ⁽²⁾ | SSRDR / ICDRR | FFh |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|--|--------|-------------|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | XXh |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | 00h |
| 00E1h | Port P1 Register | P1 | 00h |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | | | |
| 00E5h | Port P3 Register | P3 | 00h |
| 00E6h | | | |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | 00h |
| 00E9h | Port P5 Register | P5 | 00h |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | | | |
| 00EDh | | | |
| 00EEh | | | |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | Pin Select Register 1 | PINSR1 | 00h |
| 00F6h | Pin Select Register 2 | PINSR2 | 00h |
| 00F7h | Pin Select Register 3 | PINSR3 | 00h |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | 00h |
| 00FEh | Port P1 Drive Capacity Control Register ⁽²⁾ | P1DRR | 00h |
| 00FFh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|---------|-------------|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | | | |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRES | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Second Data Register / Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Minute Data Register / Compare Data Register | TREMIN | 00h |
| 011Ah | Timer RE Hour Data Register ⁽²⁾ | TREHR | 00h |
| 011Bh | Timer RE Day of Week Data Register ⁽²⁾ | TREWK | 00h |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Count Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | | | |
| 0138h | | | |
| 0139h | | | |
| 013Ah | | | |
| 013Bh | | | |
| 013Ch | | | |
| 013Dh | | | |
| 013Eh | | | |
| 013Fh | | | |

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0140h | | | |
| 0141h | | | |
| 0142h | | | |
| 0143h | | | |
| 0144h | | | |
| 0145h | | | |
| 0146h | | | |
| 0147h | | | |
| 0148h | | | |
| 0149h | | | |
| 014Ah | | | |
| 014Bh | | | |
| 014Ch | | | |
| 014Dh | | | |
| 014Eh | | | |
| 014Fh | | | |
| 0150h | | | |
| 0151h | | | |
| 0152h | | | |
| 0153h | | | |
| 0154h | | | |
| 0155h | | | |
| 0156h | | | |
| 0157h | | | |
| 0158h | | | |
| 0159h | | | |
| 015Ah | | | |
| 015Bh | | | |
| 015Ch | | | |
| 015Dh | | | |
| 015Eh | | | |
| 015Fh | | | |
| 0160h | | | |
| 0161h | | | |
| 0162h | | | |
| 0163h | | | |
| 0164h | | | |
| 0165h | | | |
| 0166h | | | |
| 0167h | | | |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |
| 0170h | | | |
| 0171h | | | |
| 0172h | | | |
| 0173h | | | |
| 0174h | | | |
| 0175h | | | |
| 0176h | | | |
| 0177h | | | |
| 0178h | | | |
| 0179h | | | |
| 017Ah | | | |
| 017Bh | | | |
| 017Ch | | | |
| 017Dh | | | |
| 017Eh | | | |
| 017Fh | | | |

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

| Address | Register | Symbol | After reset |
|---------|---------------------------------|--------|-------------|
| 0180h | | | |
| 0181h | | | |
| 0182h | | | |
| 0183h | | | |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | | | |
| 0189h | | | |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

| | | | |
|-------|---------------------------------|-----|----------|
| FFFFh | Option Function Select Register | OFS | (Note 2) |
|-------|---------------------------------|-----|----------|

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

5.1 N, D Version

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|-----------------------------------|-------------------------------|-------------------------|--|------|
| V _{CC} /AV _{CC} | Supply voltage | | -0.3 to 6.5 | V |
| V _I | Input voltage | | -0.3 to V _{CC} + 0.3 | V |
| V _O | Output voltage | | -0.3 to V _{CC} + 0.3 | V |
| P _d | Power dissipation | T _{opr} = 25°C | 500 | mW |
| T _{opr} | Operating ambient temperature | | -20 to 85 (N version) / -40 to 85 (D version) | °C |
| T _{stg} | Storage temperature | | -65 to 150 | °C |

Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit | |
|--|--|---|--|---------------------|------|---------------------|------|-----|
| | | | | Min. | Typ. | Max. | | |
| V _{CC} /AV _{CC} | Supply voltage | | | 2.2 | – | 5.5 | V | |
| V _{SS} /AV _{SS} | Supply voltage | | | – | 0 | – | V | |
| V _{IH} | Input “H” voltage | | | 0.8 V _{CC} | – | V _{CC} | V | |
| V _{IL} | Input “L” voltage | | | 0 | – | 0.2 V _{CC} | V | |
| I _{OH} (sum) | Peak sum output “H” current | Sum of all pins I _{OH} (peak) | | – | – | -160 | mA | |
| I _{OH} (sum) | Average sum output “H” current | Sum of all pins I _{OH} (avg) | | – | – | -80 | mA | |
| I _{OH} (peak) | Peak output “H” current | Except P1_0 to P1_7 | | – | – | -10 | mA | |
| | | P1_0 to P1_7 | | – | – | -40 | mA | |
| I _{OH} (avg) | Average output “H” current | Except P1_0 to P1_7 | | – | – | -5 | mA | |
| | | P1_0 to P1_7 | | – | – | -20 | mA | |
| I _{OL} (sum) | Peak sum output “L” currents | Sum of all pins I _{OL} (peak) | | – | – | 160 | mA | |
| I _{OL} (sum) | Average sum output “L” currents | Sum of all pins I _{OL} (avg) | | – | – | 80 | mA | |
| I _{OL} (peak) | Peak output “L” currents | Except P1_0 to P1_7 | | – | – | 10 | mA | |
| | | P1_0 to P1_7 | | – | – | 40 | mA | |
| I _{OL} (avg) | Average output “L” current | Except P1_0 to P1_7 | | – | – | 5 | mA | |
| | | P1_0 to P1_7 | | – | – | 20 | mA | |
| f(XIN) | XIN clock input oscillation frequency | | 3.0 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 20 | MHz | |
| | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz | |
| | | | 2.2 V ≤ V _{CC} < 2.7 V | 0 | – | 5 | MHz | |
| f(XCIN) | XCIN clock input oscillation frequency | | 2.2 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 70 | kHz | |
| – | System clock | OCD2 = 0 XIN clock selected | 3.0 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 20 | MHz | |
| | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz | |
| | | | 2.2 V ≤ V _{CC} < 2.7 V | 0 | – | 5 | MHz | |
| | | OCD2 = 1 On-chip oscillator clock selected | FRA01 = 0 Low-speed on-chip oscillator clock selected | – | 125 | – | – | kHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V _{CC} ≤ 5.5 V | – | – | – | 20 | MHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V _{CC} ≤ 5.5 V | – | – | – | 10 | MHz |
| FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V _{CC} ≤ 5.5 V | – | – | – | 5 | MHz | | | |

NOTES:

- V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------------|-------------------------------------|-------------------------|---|----------|------|-----------|---------------|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref} = AV_{CC}$ | – | – | 10 | Bits |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 3 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 2 | LSB |
| | | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 5 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 2 | LSB |
| | | 10-bit mode | $\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$ | – | – | ± 5 | LSB |
| | | 8-bit mode | $\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$ | – | – | ± 2 | LSB |
| R_{ladder} | Resistor ladder | | $V_{ref} = AV_{CC}$ | 10 | – | 40 | $k\Omega$ |
| t_{conv} | Conversion time | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 3.3 | – | – | μs |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 2.8 | – | – | μs |
| V_{ref} | Reference voltage | | | 2.2 | – | AV_{CC} | V |
| V_{IA} | Analog input voltage ⁽²⁾ | | | 0 | – | AV_{CC} | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$ | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$ | 1 | – | 10 | MHz |
| | | Without sample and hold | $V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ | 0.25 | – | 5 | MHz |
| | | With sample and hold | $V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ | 1 | – | 5 | MHz |

NOTES:

1. $AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

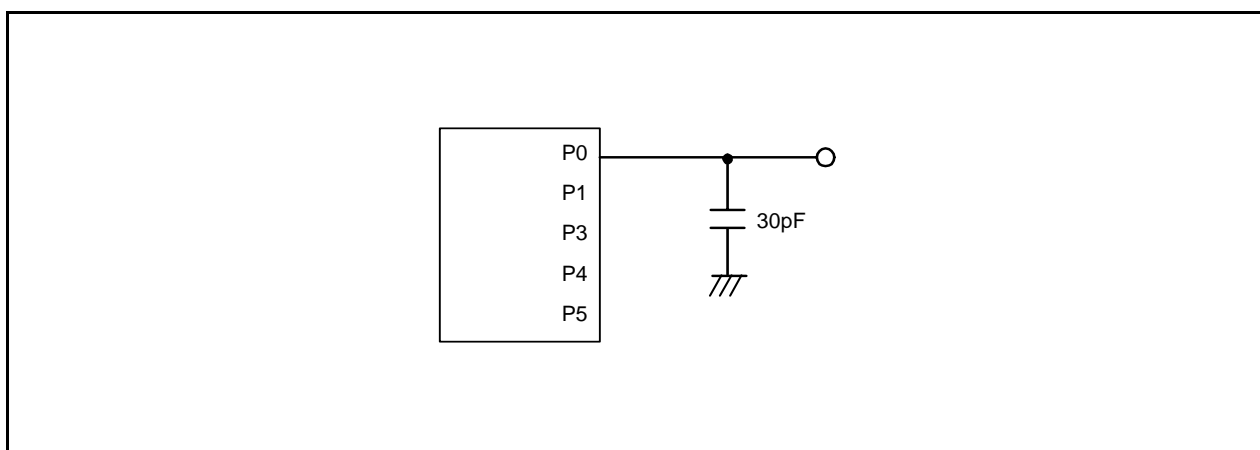
**Figure 5.1 Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|----------------------------|----------------------|------|------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | R8C/26 Group | 100 ⁽³⁾ | – | – | times |
| | | R8C/27 Group | 1,000 ⁽³⁾ | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97 + CPU clock x 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3 + CPU clock x 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time ⁽⁷⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|----------------------------|-----------------------|------|------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | | 10,000 ⁽³⁾ | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | μs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | μs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97 + CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3 + CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | -20 ⁽⁸⁾ | – | 85 | °C |
| – | Data hold time ⁽⁹⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

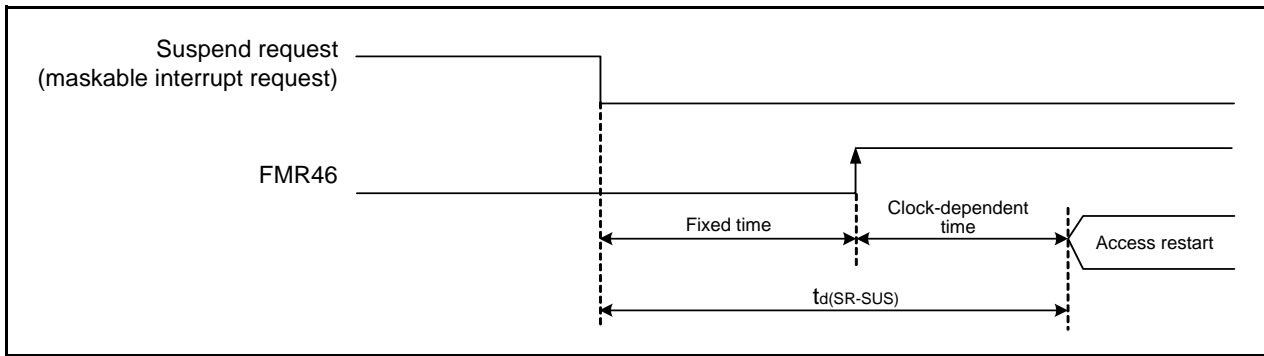


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det0} | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, V _{CC} = 5.0 V | – | 0.9 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽²⁾ | | – | – | 300 | μs |
| V _{ccmin} | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage detection level ⁽⁴⁾ | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time ⁽²⁾ | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | – | – | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time ⁽²⁾ | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | – | – | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|----------|------|-------------------|---------|
| | | | Min. | Typ. | Max. | |
| V _{por1} | Power-on reset valid voltage ⁽⁴⁾ | | – | – | 0.1 | V |
| V _{por2} | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | V _{det0} | V |
| tr _{th} | External power V _{CC} rise gradient ⁽²⁾ | | 20 | – | – | mV/msec |

NOTES:

1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

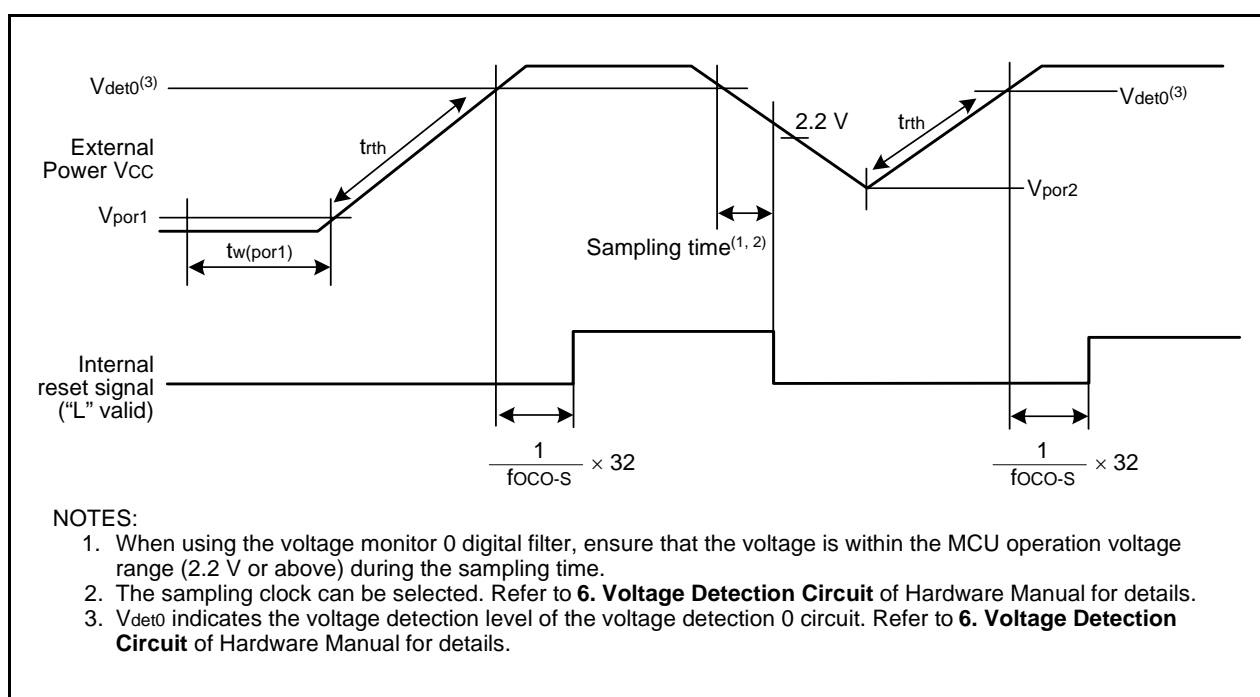
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|--|------|--------------------|------|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾ | 39.2 | 40 | 40.8 | MHz |
| | | V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.8 | 40 | 41.2 | MHz |
| | | V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.4 | 40 | 41.6 | MHz |
| | | V _{CC} = 2.7 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38 | 40 | 42 | MHz |
| | | V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 37.6 | 40 | 42.4 | MHz |
| | | V _{CC} = 2.2 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾ | 35.2 | 40 | 44.8 | MHz |
| | | V _{CC} = 2.2 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾ | 34 | 40 | 46 | MHz |
| | | V _{CC} = 5.0 V ± 10% -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.8 | 40 | 40.8 | MHz |
| | | V _{CC} = 5.0 V ± 10% -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.4 | 40 | 40.8 | MHz |
| | | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register ⁽⁴⁾ | V _{CC} = 5.0 V, T _{opr} = 25°C | – | 36.864 | – |
| V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C | -3% | | – | 3% | % | |
| – | Value in FRA1 register after reset | | 08h ⁽³⁾ | – | F7h ⁽³⁾ | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | – | 400 | – | μA |

NOTES:

- V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- These standard values show when the FRA1 register value after reset is assumed.
- These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | – | 15 | – | μA |

NOTE:

- V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------|---|-----------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _d (P-R) | Time for internal power supply stabilization during power-on ⁽²⁾ | | 1 | – | 2000 | μs |
| t _d (R-S) | STOP exit time ⁽³⁾ | | – | – | 150 | μs |

NOTES:

- The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
- Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------|------------------------------------|--------|---------------------|------------|------|---------------|---------------------|
| | | | | Min. | Typ. | Max. | |
| tsucyc | SSCK clock cycle time | | | 4 | – | – | tcyc ⁽²⁾ |
| tHI | SSCK clock "H" width | | | 0.4 | – | 0.6 | tsucyc |
| tLO | SSCK clock "L" width | | | 0.4 | – | 0.6 | tsucyc |
| tRISE | SSCK clock rising time | Master | | – | – | 1 | tcyc ⁽²⁾ |
| | | Slave | | – | – | 1 | μs |
| tFALL | SSCK clock falling time | Master | | – | – | 1 | tcyc ⁽²⁾ |
| | | Slave | | – | – | 1 | μs |
| tsu | SSO, SSI data input setup time | | | 100 | – | – | ns |
| tH | SSO, SSI data input hold time | | | 1 | – | – | tcyc ⁽²⁾ |
| tLEAD | $\overline{\text{SCS}}$ setup time | Slave | | 1tcyc + 50 | – | – | ns |
| tLAG | $\overline{\text{SCS}}$ hold time | Slave | | 1tcyc + 50 | – | – | ns |
| tOD | SSO, SSI data output delay time | | | – | – | 1 | tcyc ⁽²⁾ |
| tSA | SSI slave access time | | 2.7 V ≤ Vcc ≤ 5.5 V | – | – | 1.5tcyc + 100 | ns |
| | | | 2.2 V ≤ Vcc < 2.7 V | – | – | 1.5tcyc + 200 | ns |
| tOR | SSI slave out open time | | 2.7 V ≤ Vcc ≤ 5.5 V | – | – | 1.5tcyc + 100 | ns |
| | | | 2.2 V ≤ Vcc < 2.7 V | – | – | 1.5tcyc + 200 | ns |

NOTES:

1. Vcc = 2.2 to 5.5 V, Vss = 0 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

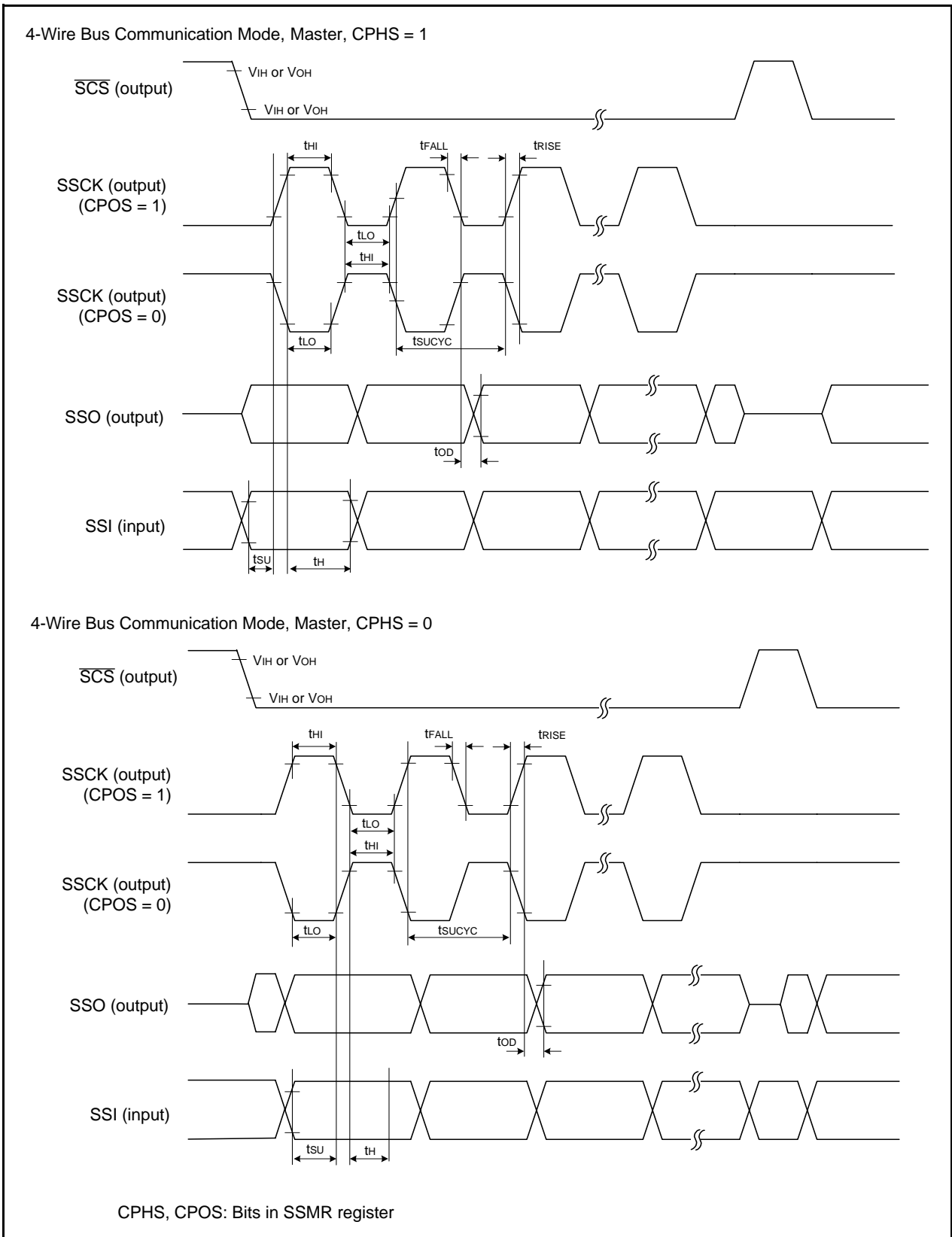


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

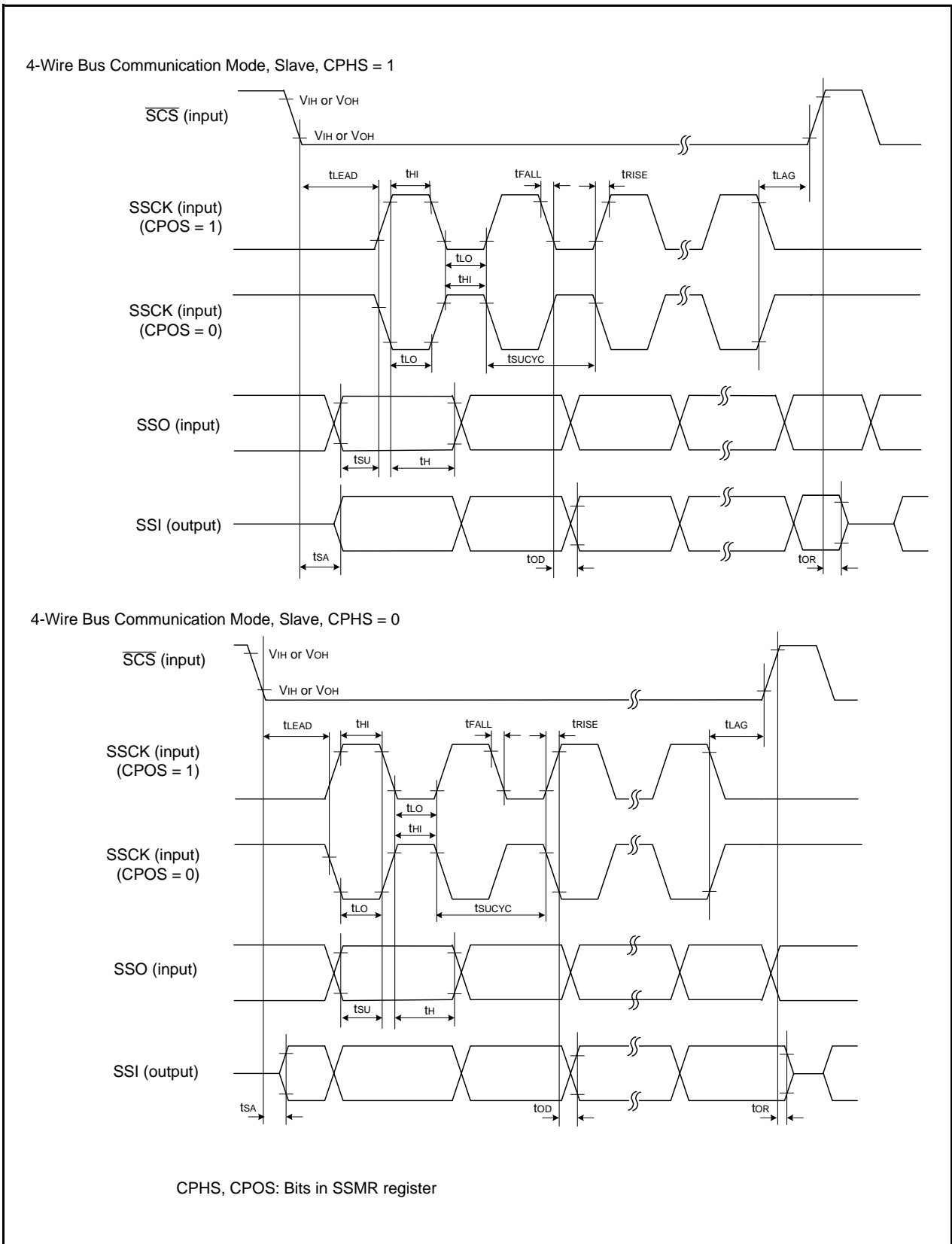


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

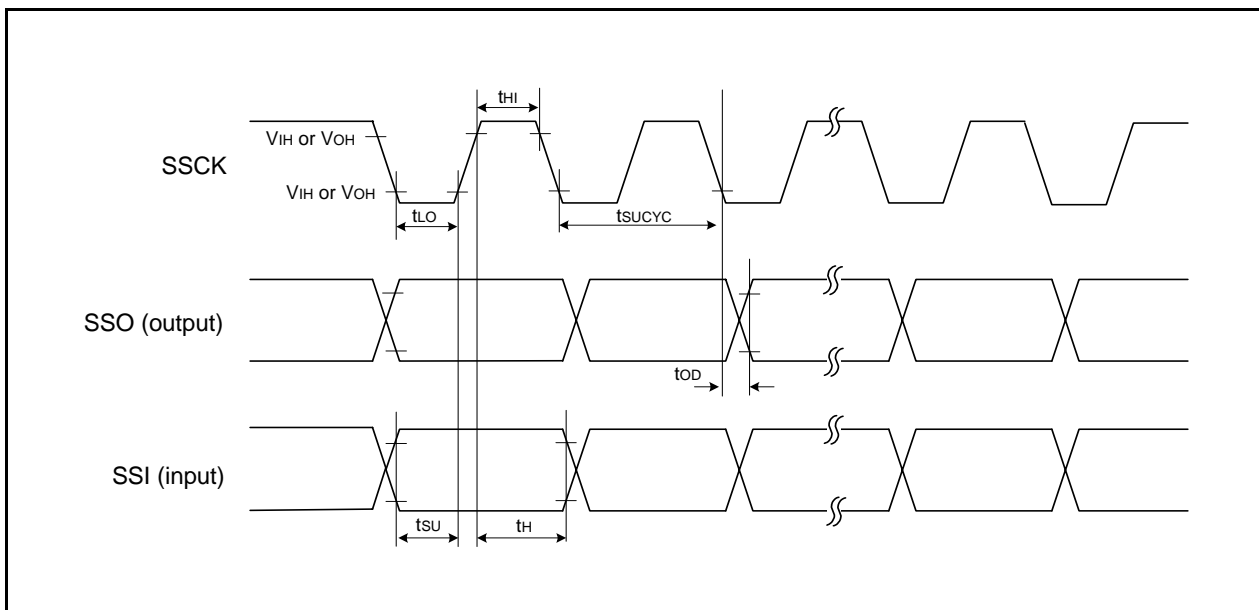


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.14 Timing Requirements of I²C bus Interface⁽¹⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|---|------|----------------------------------|------|
| | | | Min. | Typ. | Max. | |
| t _{SCL} | SCL input cycle time | | 12t _{CYC} + 600 ⁽²⁾ | – | – | ns |
| t _{SCLH} | SCL input “H” width | | 3t _{CYC} + 300 ⁽²⁾ | – | – | ns |
| t _{SCLL} | SCL input “L” width | | 5t _{CYC} + 500 ⁽²⁾ | – | – | ns |
| t _{sf} | SCL, SDA input fall time | | – | – | 300 | ns |
| t _{SP} | SCL, SDA input spike pulse rejection time | | – | – | 1t _{CYC} ⁽²⁾ | ns |
| t _{BUF} | SDA input bus-free time | | 5t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STAH} | Start condition input hold time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STAS} | Retransmit start condition input setup time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STOP} | Stop condition input setup time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{SDAS} | Data input setup time | | 1t _{CYC} + 20 ⁽²⁾ | – | – | ns |
| t _{SDAH} | Data input hold time | | 0 | – | – | ns |

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

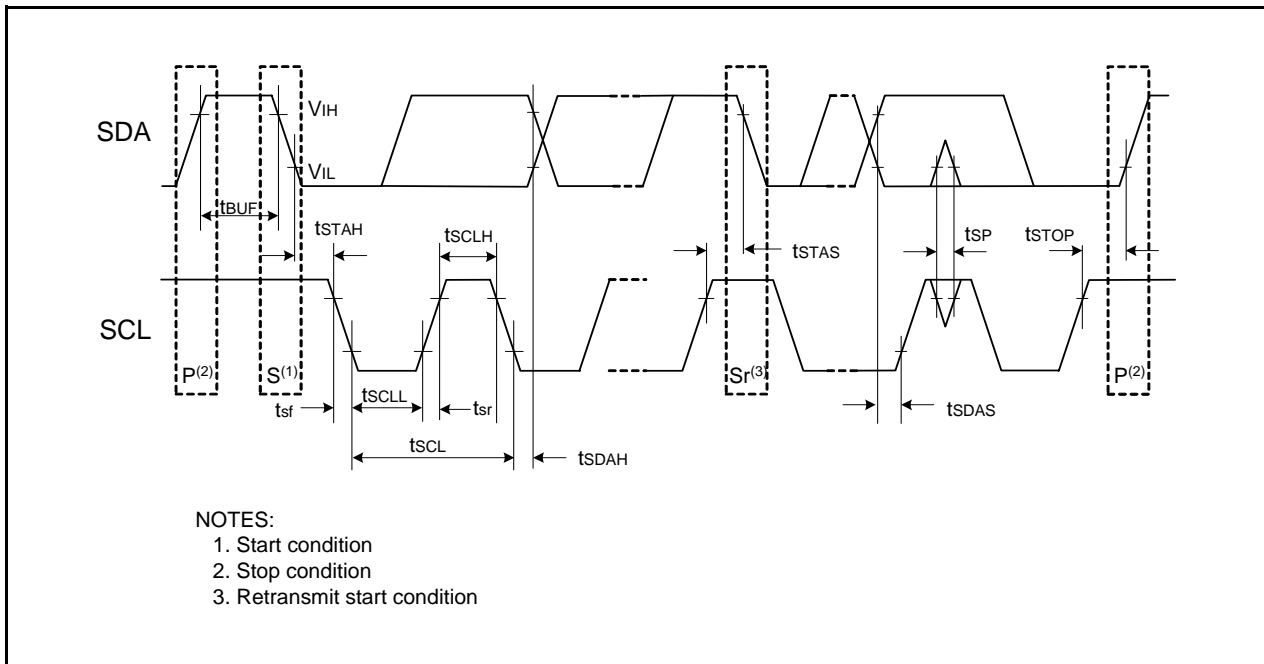
**Figure 5.7 I/O Timing of I²C bus Interface**

Table 5.15 Electrical Characteristics (1) [V_{CC} = 5 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|---|---------------------------|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except P1_0 to P1_7, XOUT | I _{OH} = -5 mA | | V _{CC} - 2.0 | - | V _{CC} | V |
| | | | I _{OH} = -200 μA | | V _{CC} - 0.5 | - | V _{CC} | V |
| | P1_0 to P1_7 | | Drive capacity HIGH | I _{OH} = -20 mA | V _{CC} - 2.0 | - | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -5 mA | V _{CC} - 2.0 | - | V _{CC} | V |
| | XOUT | | Drive capacity HIGH | I _{OH} = -1 mA | V _{CC} - 2.0 | - | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -500 μA | V _{CC} - 2.0 | - | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except P1_0 to P1_7, XOUT | I _{OL} = 5 mA | | - | - | 2.0 | V |
| | | | I _{OL} = 200 μA | | - | - | 0.45 | V |
| | P1_0 to P1_7 | | Drive capacity HIGH | I _{OL} = 20 mA | - | - | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} = 5 mA | - | - | 2.0 | V |
| | XOUT | | Drive capacity HIGH | I _{OL} = 1 mA | - | - | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} = 500 μA | - | - | 2.0 | V |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT3, K10, K11, K12, K13, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | - | V |
| | | RESET | | | 0.1 | 1.0 | - | V |
| I _{IH} | Input "H" current | V _I = 5 V, V _{CC} = 5 V | | - | - | 5.0 | μA | |
| I _{IL} | Input "L" current | V _I = 0 V, V _{CC} = 5 V | | - | - | -5.0 | μA | |
| R _{PULLUP} | Pull-up resistance | V _I = 0 V, V _{CC} = 5 V | | 30 | 50 | 167 | kΩ | |
| R _{IXIN} | Feedback resistance | XIN | | | - | 1.0 | - | MΩ |
| R _{IXCIN} | Feedback resistance | XCIN | | | - | 18 | - | MΩ |
| V _{RAM} | RAM hold voltage | During stop mode | | 1.8 | - | - | V | |

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

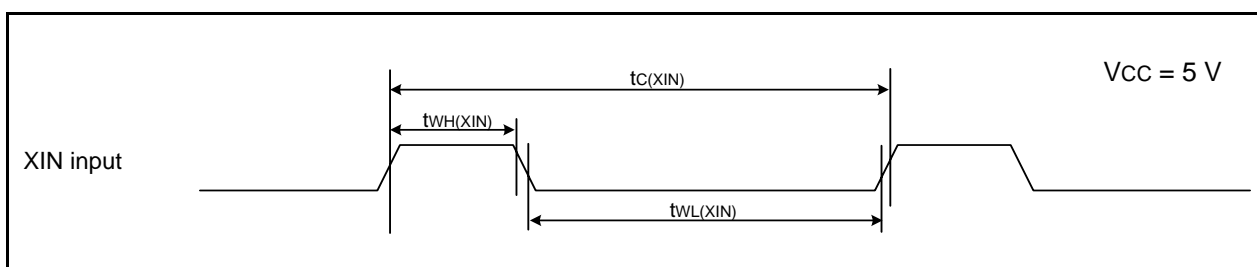
| Symbol | Parameter | Condition | Standard | | | Unit | |
|--------|--|---|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 10 | 17 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 9 | 15 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 6 | – | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 5 | – | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 10 | 15 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 4 | – | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5.5 | 10 | mA |
| | | | XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 130 | 300 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 30 | – | μA |

**Table 5.17 Electrical Characteristics (3) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|-----------|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS} | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 75 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 60 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 4.0 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 2.2 | – | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.8 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.2 | – | μA |
| | | | | | | | |

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.18 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 25 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH(XCIN)}$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL(XCIN)}$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAI0 Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 40 | – | ns |

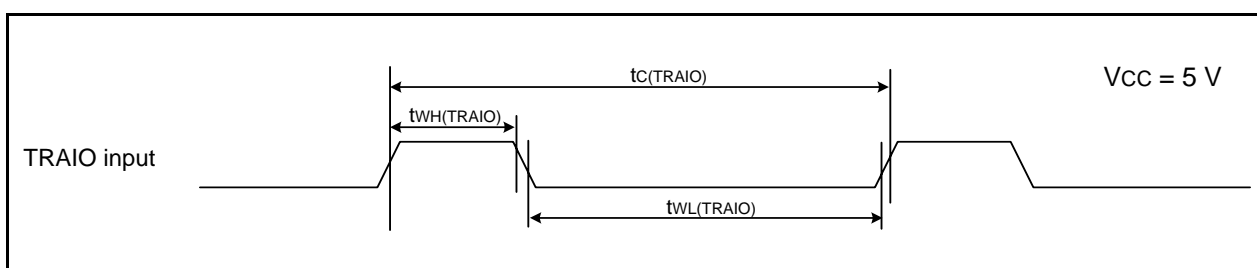
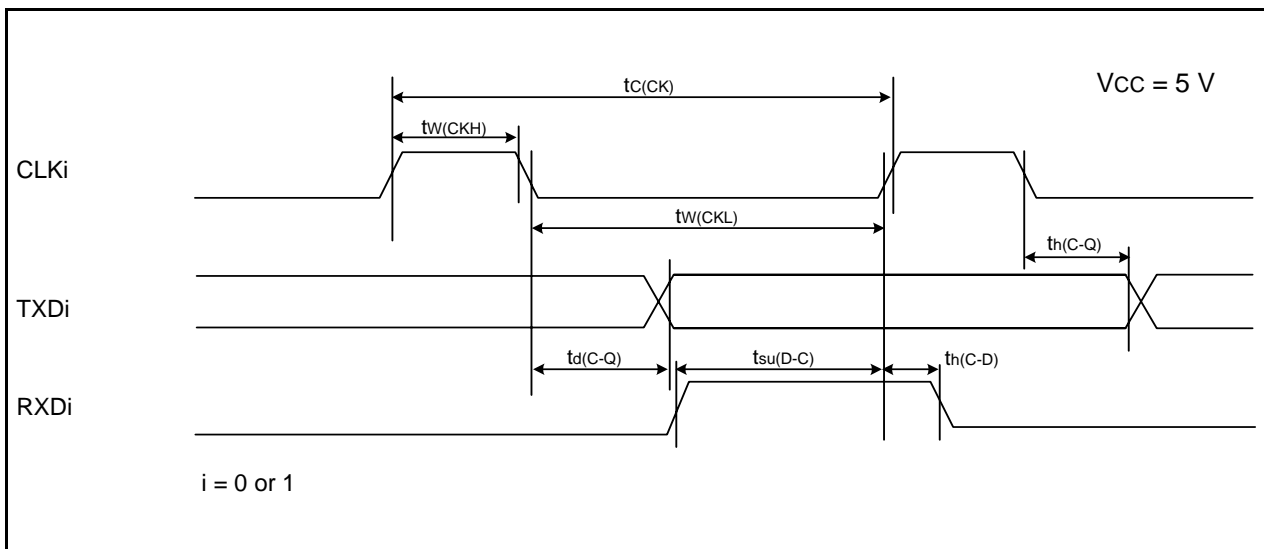
**Figure 5.9 TRAI0 Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.20 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{w(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.21 External Interrupt \overline{INTi} (i = 0, 1, 3) Input**

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 250 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 250 ⁽²⁾ | – | ns |

NOTES:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

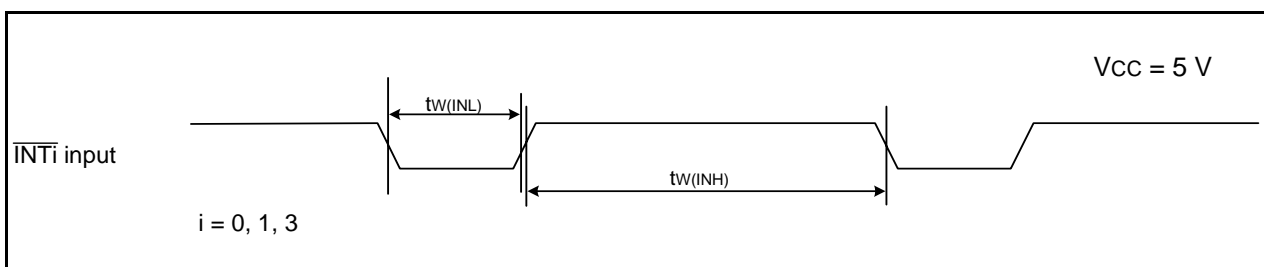
**Figure 5.11 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 5 V**

Table 5.22 Electrical Characteristics (3) [V_{CC} = 3 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|---|-------------------------|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except P1_0 to P1_7, XOUT | I _{OH} = -1 mA | | V _{CC} - 0.5 | – | V _{CC} | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I _{OH} = -5 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | XOUT | Drive capacity HIGH | I _{OH} = -0.1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50 μA | V _{CC} - 0.5 | – | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except P1_0 to P1_7, XOUT | I _{OL} = 1 mA | | – | – | 0.5 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I _{OL} = 5 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50 μA | – | – | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.1 | 0.3 | – | V |
| | | RESET | | | 0.1 | 0.4 | – | V |
| I _{IH} | Input "H" current | V _I = 3 V, V _{CC} = 3 V | | – | – | 4.0 | μA | |
| I _{IL} | Input "L" current | V _I = 0 V, V _{CC} = 3 V | | – | – | -4.0 | μA | |
| R _{PULLUP} | Pull-up resistance | V _I = 0 V, V _{CC} = 3 V | | 66 | 160 | 500 | kΩ | |
| R _{FXIN} | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | | – | 18 | – | MΩ |
| V _{RAM} | RAM hold voltage | During stop mode | | 1.8 | – | – | V | |

NOTE:

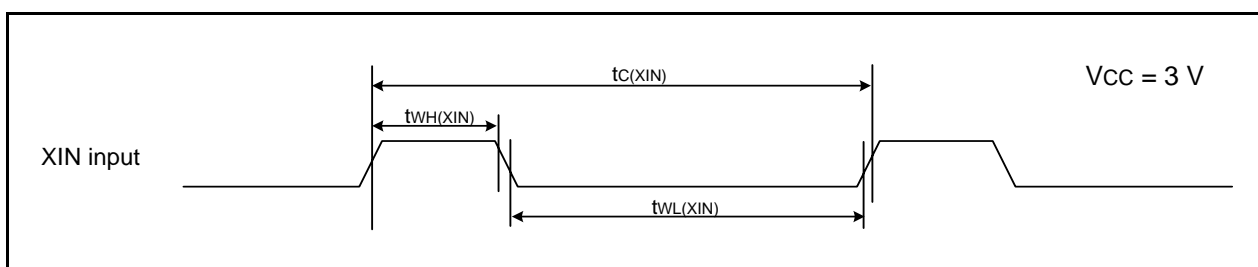
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.23 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|---|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5 | 9 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 130 | 300 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 30 | – | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 70 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 55 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 3.8 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 2.0 | – | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.24 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 40 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH(XCIN)}$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL(XCIN)}$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.25 TRAI0 Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 120 | – | ns |

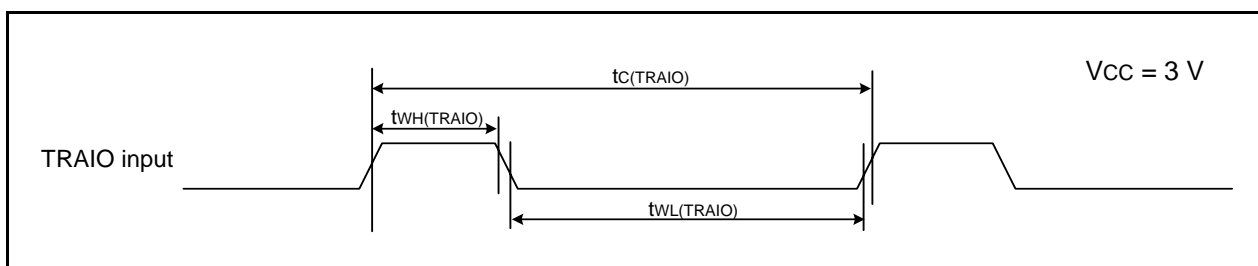
**Figure 5.13 TRAI0 Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.26 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{w(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_h(C-Q)$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_h(C-D)$ | RXDi input hold time | 90 | – | ns |

$i = 0$ or 1

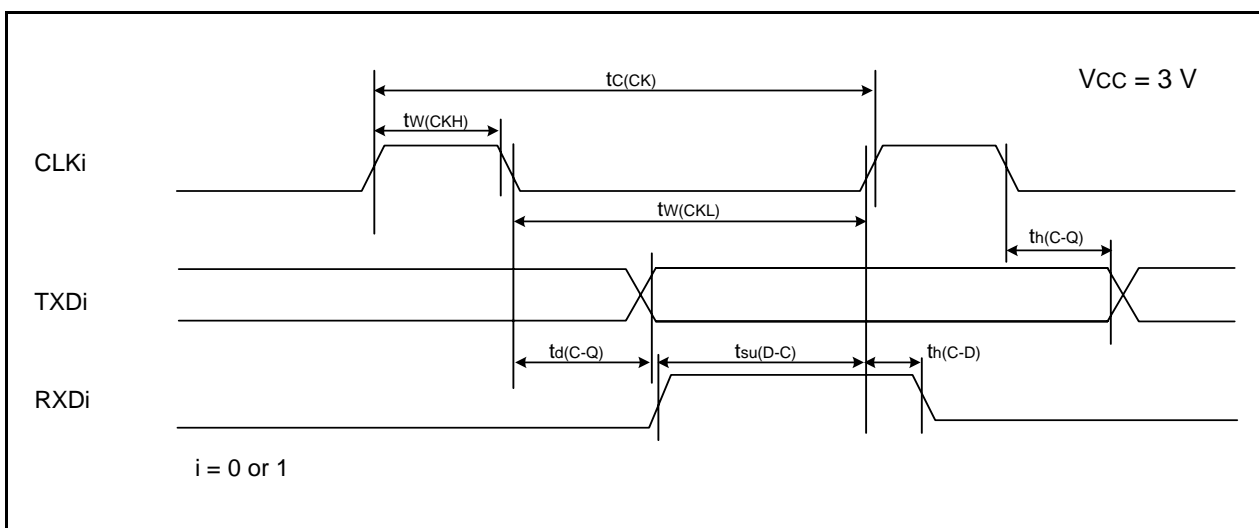


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.27 External Interrupt \overline{INTi} ($i = 0, 1, 3$) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 380 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 380 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

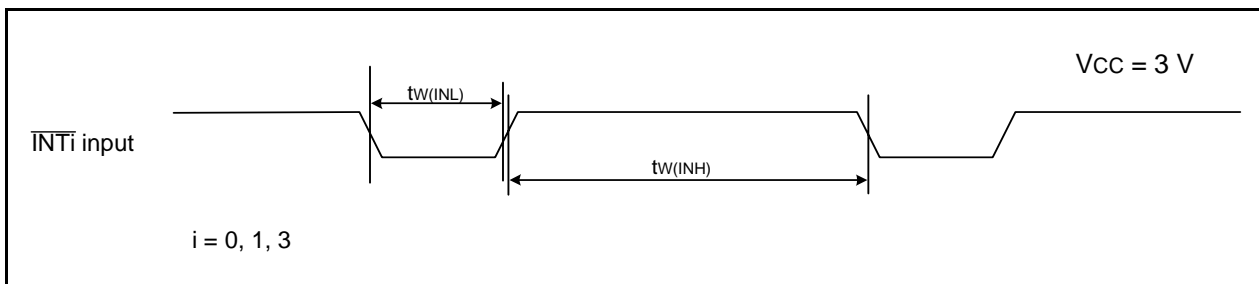


Figure 5.15 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V

Table 5.28 Electrical Characteristics (5) [V_{CC} = 2.2 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|---|-------------------------|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except P1_0 to P1_7, XOUT | I _{OH} = -1 mA | | V _{CC} - 0.5 | – | V _{CC} | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I _{OH} = -2 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | XOUT | Drive capacity HIGH | I _{OH} = -0.1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50 μA | V _{CC} - 0.5 | – | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except P1_0 to P1_7, XOUT | I _{OL} = 1 mA | | – | – | 0.5 | V |
| | | P1_0 to P1_7 | Drive capacity HIGH | I _{OL} = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50 μA | – | – | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.05 | 0.3 | – | V |
| | | RESET | | | 0.05 | 0.15 | – | V |
| I _{IH} | Input "H" current | V _I = 2.2 V | | – | – | 4.0 | μA | |
| I _{IL} | Input "L" current | V _I = 0 V | | – | – | -4.0 | μA | |
| R _{PULLUP} | Pull-up resistance | V _I = 0 V | | 100 | 200 | 600 | kΩ | |
| R _{FXIN} | Feedback resistance | XIN | | | – | 5 | – | MΩ |
| R _{FXCIN} | Feedback resistance | XCIN | | | – | 35 | – | MΩ |
| V _{RAM} | RAM hold voltage | During stop mode | | 1.8 | – | – | V | |

NOTE:

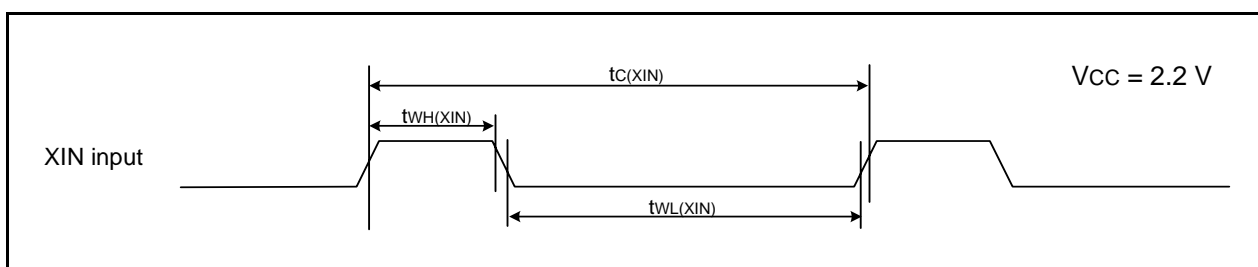
- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Table 5.29 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|---|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 3.5 | – | mA |
| | | | XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 1.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 3.5 | – | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 100 | 230 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 100 | 230 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 25 | – | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 22 | 60 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 20 | 55 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 3.0 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 1.8 | – | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.30 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 200 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 90 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH(XCIN)}$ | XCIN input "H" width | 7 | – | μs |
| $t_{WL(XCIN)}$ | XCIN input "L" width | 7 | – | μs |

**Figure 5.16 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.31 TRAI0 Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 200 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 200 | – | ns |

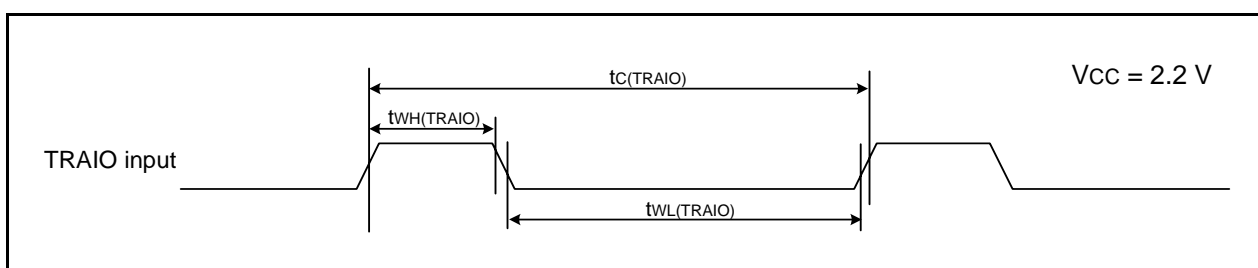
**Figure 5.17 TRAI0 Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.32 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 400 | – | ns |
| $t_{w(CKL)}$ | CLKi input “L” width | 400 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

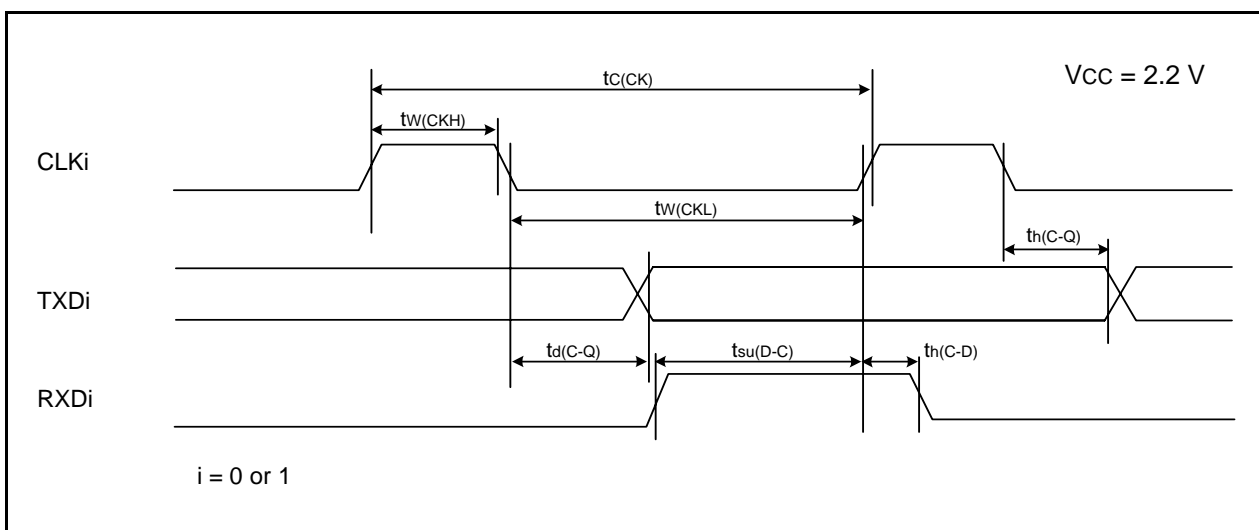


Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.33 External Interrupt \overline{INTi} (i = 0, 1, 3) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 1000 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 1000 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

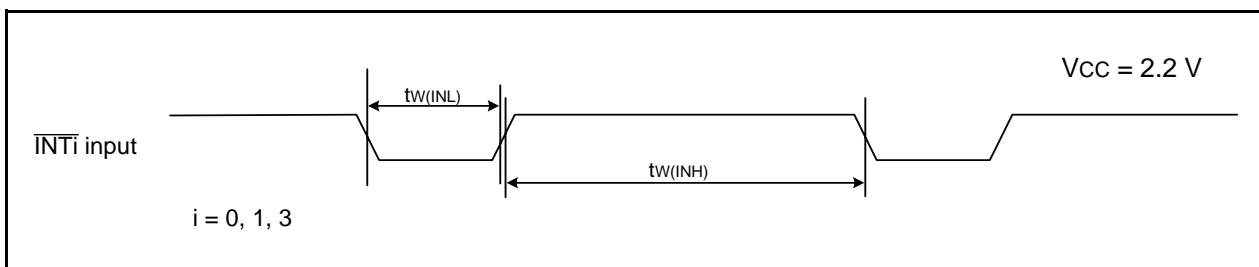


Figure 5.19 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 2.2 V

5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|-----------------------------------|-------------------------------|-----------------------------------|---|------|
| V _{CC} /AV _{CC} | Supply voltage | | -0.3 to 6.5 | V |
| V _I | Input voltage | | -0.3 to V _{CC} + 0.3 | V |
| V _O | Output voltage | | -0.3 to V _{CC} + 0.3 | V |
| P _d | Power dissipation | -40 °C ≤ T _{opr} ≤ 85 °C | 300 | mW |
| | | 85 °C ≤ T _{opr} ≤ 125 °C | 125 | mW |
| T _{opr} | Operating ambient temperature | | -40 to 85 (J version) / -40 to 125 (K version) | °C |
| T _{stg} | Storage temperature | | -65 to 150 | °C |

Table 5.35 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit | |
|-----------------------------------|---------------------------------------|---|--|---------------------|------|---------------------|------|-----|
| | | | | Min. | Typ. | Max. | | |
| V _{CC} /AV _{CC} | Supply voltage | | | 2.7 | – | 5.5 | V | |
| V _{SS} /AV _{SS} | Supply voltage | | | – | 0 | – | V | |
| V _{IH} | Input “H” voltage | | | 0.8 V _{CC} | – | V _{CC} | V | |
| V _{IL} | Input “L” voltage | | | 0 | – | 0.2 V _{CC} | V | |
| I _{OH(sum)} | Peak sum output “H” current | Sum of all pins I _{OH(peak)} | | – | – | -60 | mA | |
| I _{OH(peak)} | Peak output “H” current | | | – | – | -10 | mA | |
| I _{OH(avg)} | Average output “H” current | | | – | – | -5 | mA | |
| I _{OL(sum)} | Peak sum output “L” currents | Sum of all pins I _{OL(peak)} | | – | – | 60 | mA | |
| I _{OL(peak)} | Peak output “L” currents | | | – | – | 10 | mA | |
| I _{OL(avg)} | Average output “L” current | | | – | – | 5 | mA | |
| f _(XIN) | XIN clock input oscillation frequency | | 3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version) | 0 | – | 20 | MHz | |
| | | | 3.0 V ≤ V _{CC} ≤ 5.5 V (K version) | 0 | – | 16 | MHz | |
| | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz | |
| – | System clock | OCD2 = 0 XIN clock selected | 3.0 V ≤ V _{CC} ≤ 5.5 V (other than K version) | 0 | – | 20 | MHz | |
| | | | 3.0 V ≤ V _{CC} ≤ 5.5 V (K version) | 0 | – | 16 | MHz | |
| | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz | |
| | | OCD2 = 1 On-chip oscillator clock selected | FRA01 = 0 Low-speed on-chip oscillator clock selected | – | 125 | – | – | kHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version) | – | – | – | 20 | MHz |
| | | | FRA01 = 1 High-speed on-chip oscillator clock selected | – | – | – | 10 | MHz |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

Table 5.36 A/D Converter Characteristics

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------------|-------------------------------------|-------------------------|---|----------|------|-----------|---------------|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref} = AV_{CC}$ | – | – | 10 | Bits |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 3 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 2 | LSB |
| | | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 5 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 2 | LSB |
| R_{ladder} | Resistor ladder | | $V_{ref} = AV_{CC}$ | 10 | – | 40 | $k\Omega$ |
| t_{conv} | Conversion time | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 3.3 | – | – | μs |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 2.8 | – | – | μs |
| V_{ref} | Reference voltage | | | 2.7 | – | AV_{CC} | V |
| V_{IA} | Analog input voltage ⁽²⁾ | | | 0 | – | AV_{CC} | V |
| – | A/D operating clock frequency | Without sample and hold | | 0.25 | – | 10 | MHz |
| | | With sample and hold | | 1 | – | 10 | MHz |

NOTES:

- $AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -40$ to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

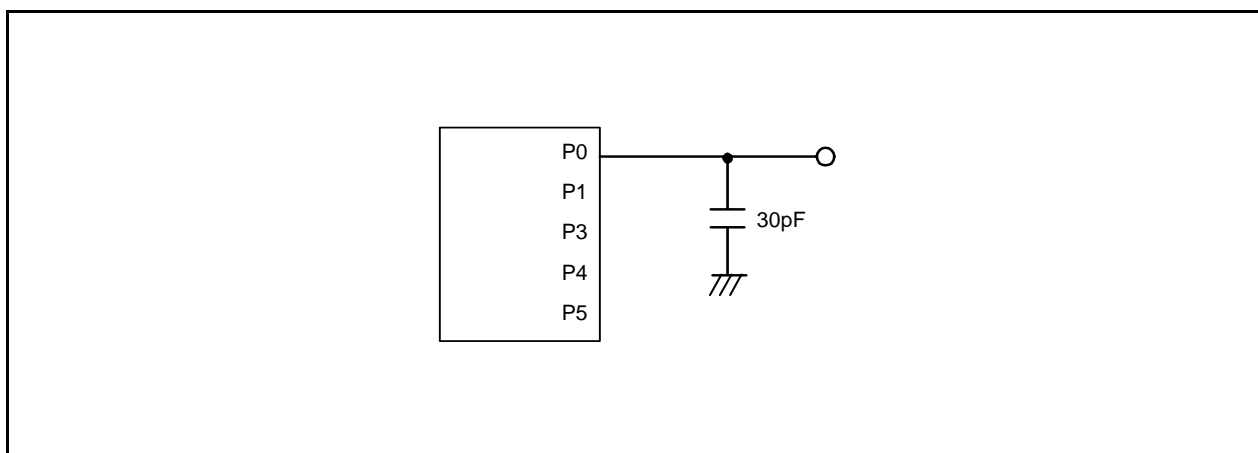
**Figure 5.20 Ports P0, P1, and P3 to P5 Timing Measurement Circuit**

Table 5.37 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|----------------------------|----------------------|------|------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | R8C/26 Group | 100 ⁽³⁾ | – | – | times |
| | | R8C/27 Group | 1,000 ⁽³⁾ | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97 + CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3 + CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time ⁽⁷⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.38 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|----------------------------|-----------------------|------|------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | | 10,000 ⁽³⁾ | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | μs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | μs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97 + CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3 + CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | -40 | – | 85 ⁽⁸⁾ | °C |
| – | Data hold time ⁽⁹⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 125°C for K version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

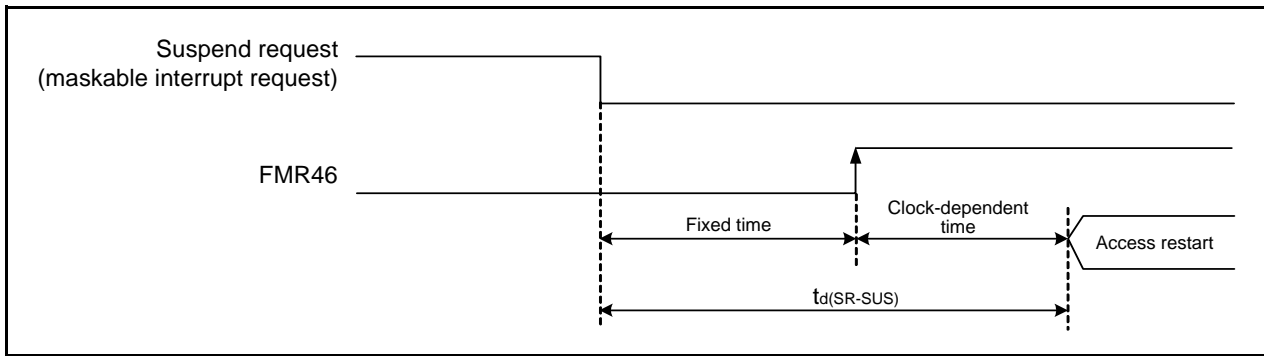


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage detection level ^(2, 4) | | 2.70 | 2.85 | 3.0 | V |
| t _d (V _{det1} -A) | Voltage monitor 1 reset generation time ⁽⁵⁾ | | – | 40 | 200 | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _d (E-A) | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | – | – | 100 | μs |
| V _{ccmin} | MCU operating voltage minimum value | | 2.70 | – | – | V |

NOTES:

- The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
- Hold V_{det2} > V_{det1}.
- Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- This parameter shows the voltage detection level when the power supply drops.
The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
- Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to t_d(V_{det1}-A). When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage detection level ⁽²⁾ | | 3.3 | 3.6 | 3.9 | V |
| t _d (V _{det2} -A) | Voltage monitor 2 reset/interrupt request generation time ^(3, 5) | | – | 40 | 200 | μs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _d (E-A) | Waiting time until voltage detection circuit operation starts ⁽⁴⁾ | | – | – | 100 | μs |

NOTES:

- The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version).
- Hold V_{det2} > V_{det1}.
- Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes V_{det2}.
- Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
- When using the digital filter, its sampling time is added to t_d(V_{det2}-A). When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.41 Power-on Reset Circuit, Voltage Monitor 1 Reset Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-------------------------|-------------------|------|-------------------|---------|
| | | | Min. | Typ. | Max. | |
| V _{por1} | Power-on reset valid voltage ⁽⁴⁾ | | – | – | 0.1 | V |
| V _{por2} | Power-on reset or voltage monitor 1 reset valid voltage | | 0 | – | V _{det1} | V |
| tr _{th} | External power V _{cc} rise gradient | V _{cc} ≤ 3.6 V | 20 ⁽²⁾ | – | – | mV/msec |
| | | V _{cc} > 3.6 V | 20 ⁽²⁾ | – | 2,000 | mV/msec |

NOTES:

1. The measurement condition is T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{cc} rise gradient) does not apply if V_{por2} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{cc} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30 s or more if -20°C ≤ T_{opr} ≤ 125°C, maintain t_{w(por1)} for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.

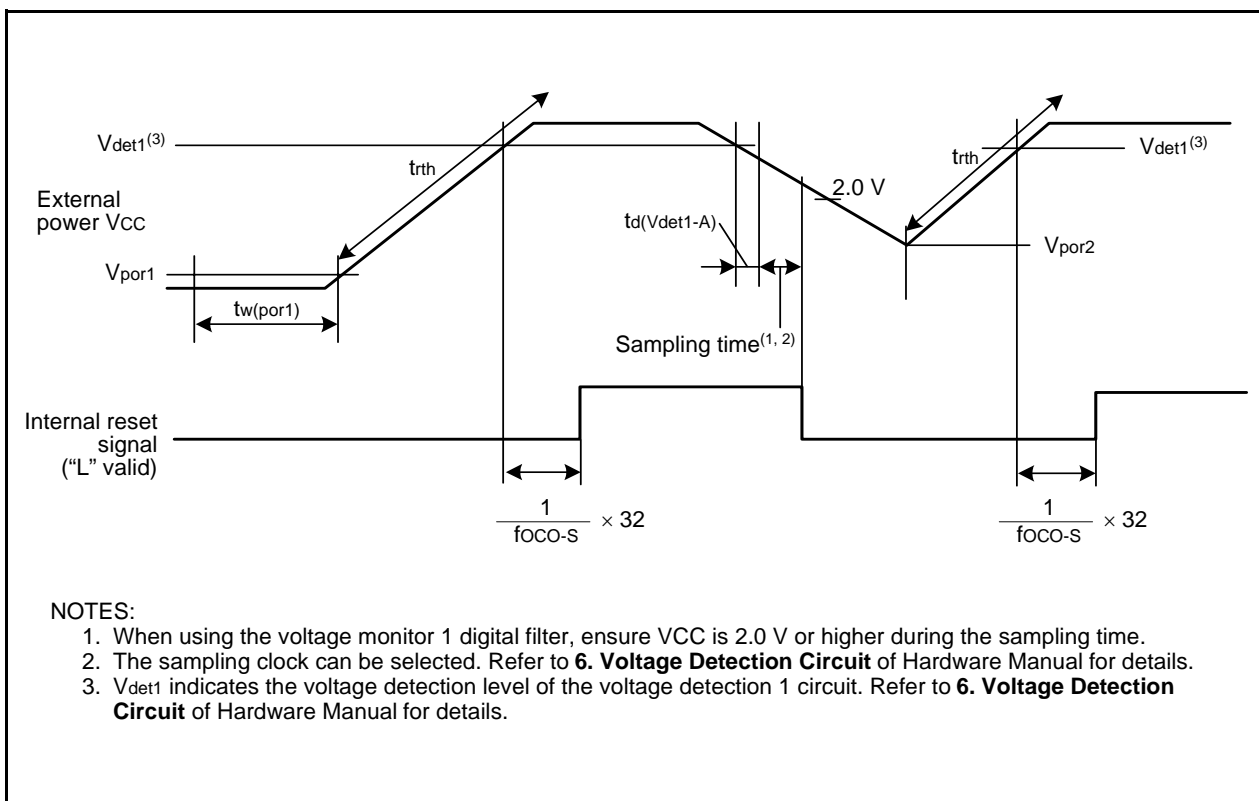


Figure 5.22 Reset Circuit Electrical Characteristics

Table 5.42 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature · supply voltage dependence | V _{CC} = 4.75 to 5.25 V 0°C ≤ T _{opr} ≤ 60°C ⁽²⁾ | 39.2 | 40 | 40.8 | MHz |
| | | V _{CC} = 3.0 to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.8 | 40 | 41.2 | MHz |
| | | V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 38.4 | 40 | 41.6 | MHz |
| | | V _{CC} = 3.0 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾ | 38 | 40 | 42 | MHz |
| | | V _{CC} = 2.7 to 5.5 V -40°C ≤ T _{opr} ≤ 125°C ⁽²⁾ | 37.6 | 40 | 42.4 | MHz |
| – | Value in FRA1 register after reset | | 08h | – | F7h | – |
| – | Oscillation frequency adjustment unit of high-speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | – | +0.3 | – | MHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | – | 400 | – | μA |

NOTES:

- V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- These standard values show when the FRA1 register value after reset is assumed.

Table 5.43 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 40 | 125 | 250 | kHz |
| – | Oscillation stability time | | – | 10 | 100 | μs |
| – | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | – | 15 | – | μA |

NOTE:

- V_{CC} = 2.7 to 5.5 V, T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

Table 5.44 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------|---|-----------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _d (P-R) | Time for internal power supply stabilization during power-on ⁽²⁾ | | 1 | – | 2000 | μs |
| t _d (R-S) | STOP exit time ⁽³⁾ | | – | – | 150 | μs |

NOTES:

- The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25°C.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
- Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.45 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------|------------------------------------|--------|------------|------------|------|---------------|---------|
| | | | | Min. | Typ. | Max. | |
| tsucyc | SSCK clock cycle time | | | 4 | – | – | tcyc(2) |
| tHI | SSCK clock "H" width | | | 0.4 | – | 0.6 | tsucyc |
| tLO | SSCK clock "L" width | | | 0.4 | – | 0.6 | tsucyc |
| tRISE | SSCK clock rising time | Master | | – | – | 1 | tcyc(2) |
| | | Slave | | – | – | 1 | μs |
| tFALL | SSCK clock falling time | Master | | – | – | 1 | tcyc(2) |
| | | Slave | | – | – | 1 | μs |
| tsu | SSO, SSI data input setup time | | | 100 | – | – | ns |
| tH | SSO, SSI data input hold time | | | 1 | – | – | tcyc(2) |
| tLEAD | $\overline{\text{SCS}}$ setup time | Slave | | 1tcyc + 50 | – | – | ns |
| tLAG | $\overline{\text{SCS}}$ hold time | Slave | | 1tcyc + 50 | – | – | ns |
| tOD | SSO, SSI data output delay time | | | – | – | 1 | tcyc(2) |
| tSA | SSI slave access time | | | – | – | 1.5tcyc + 100 | ns |
| tOR | SSI slave out open time | | | – | – | 1.5tcyc + 100 | ns |

NOTES:

1. $V_{CC} = 2.7$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -40$ to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1tcyc = 1/f_1(\text{s})$

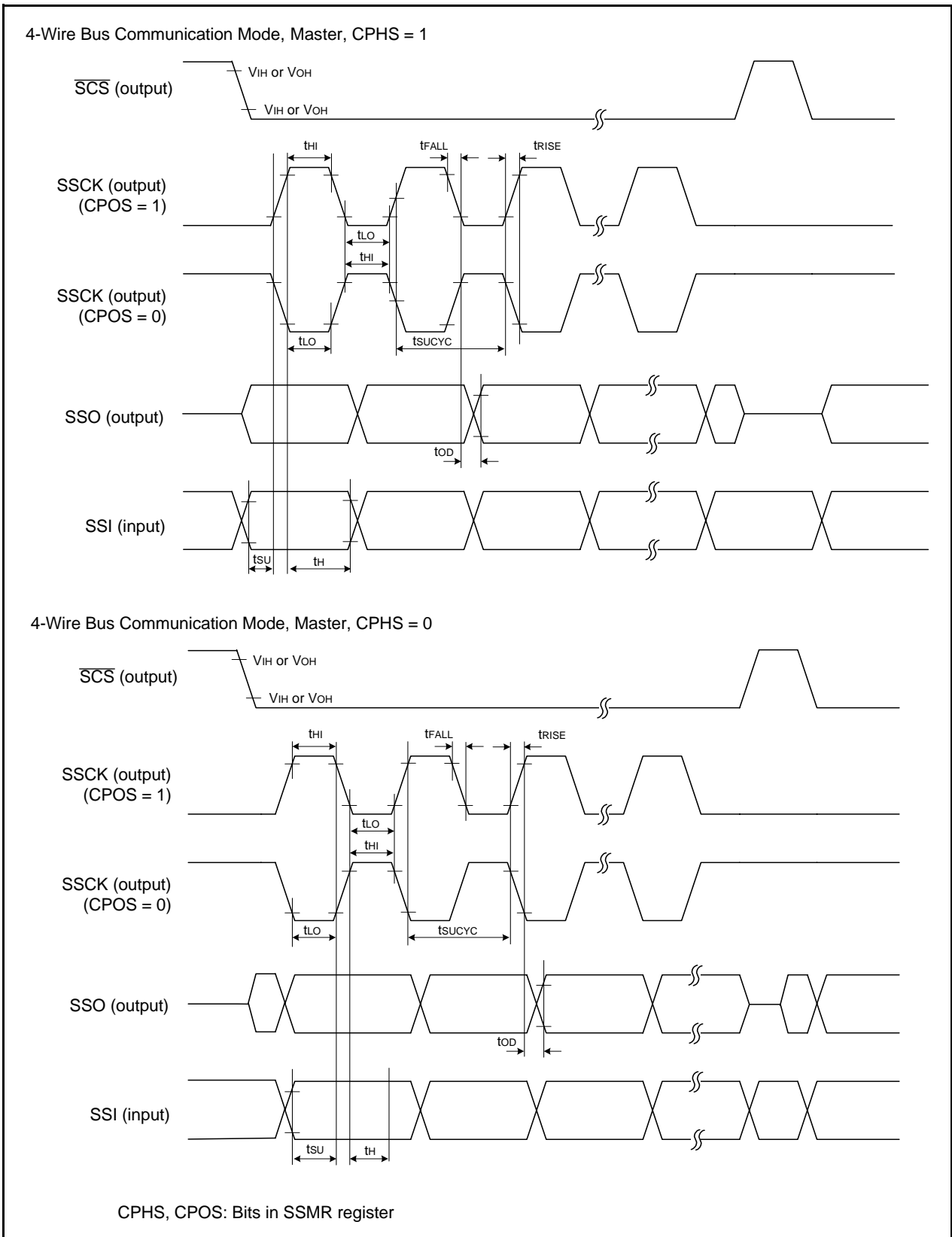


Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

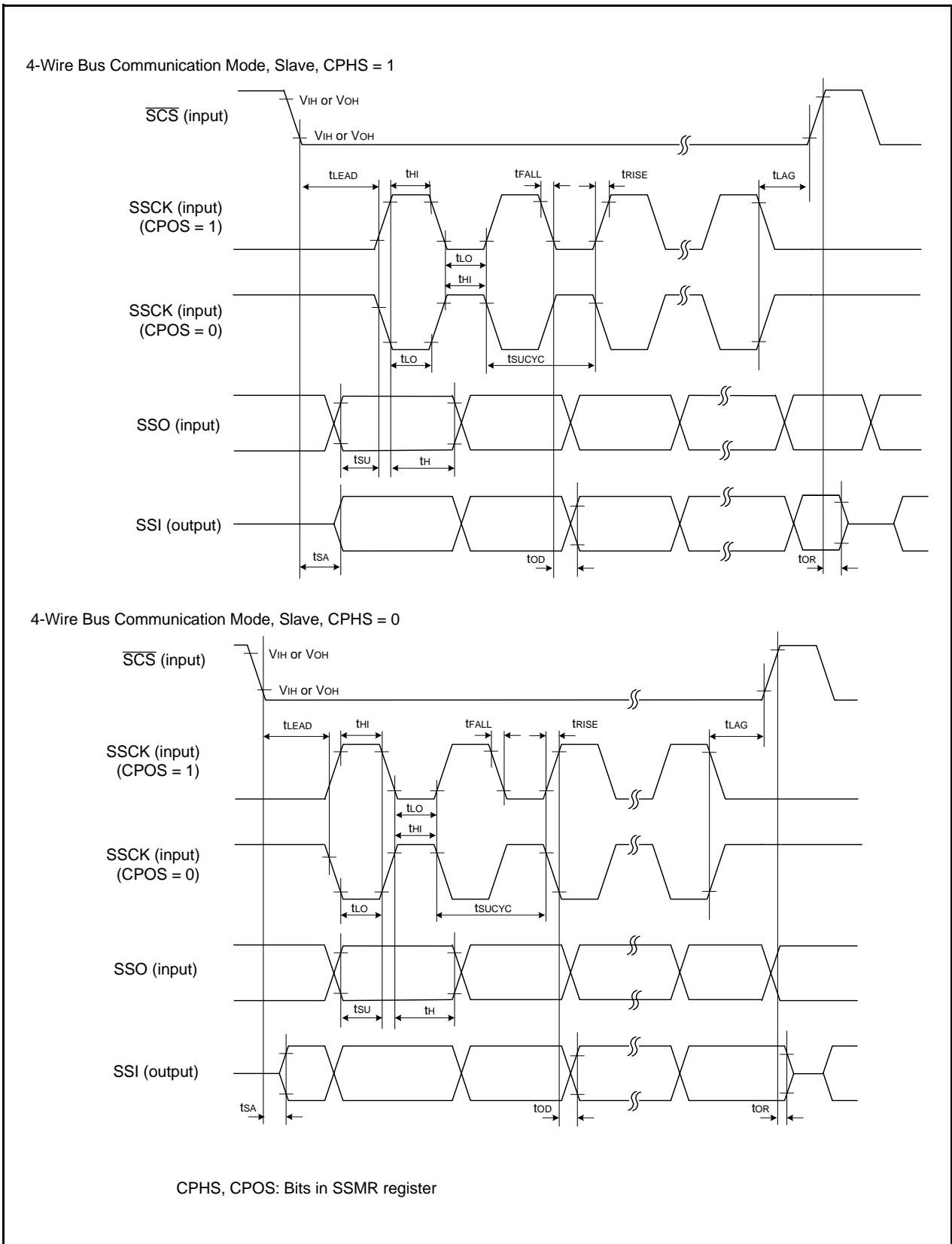


Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

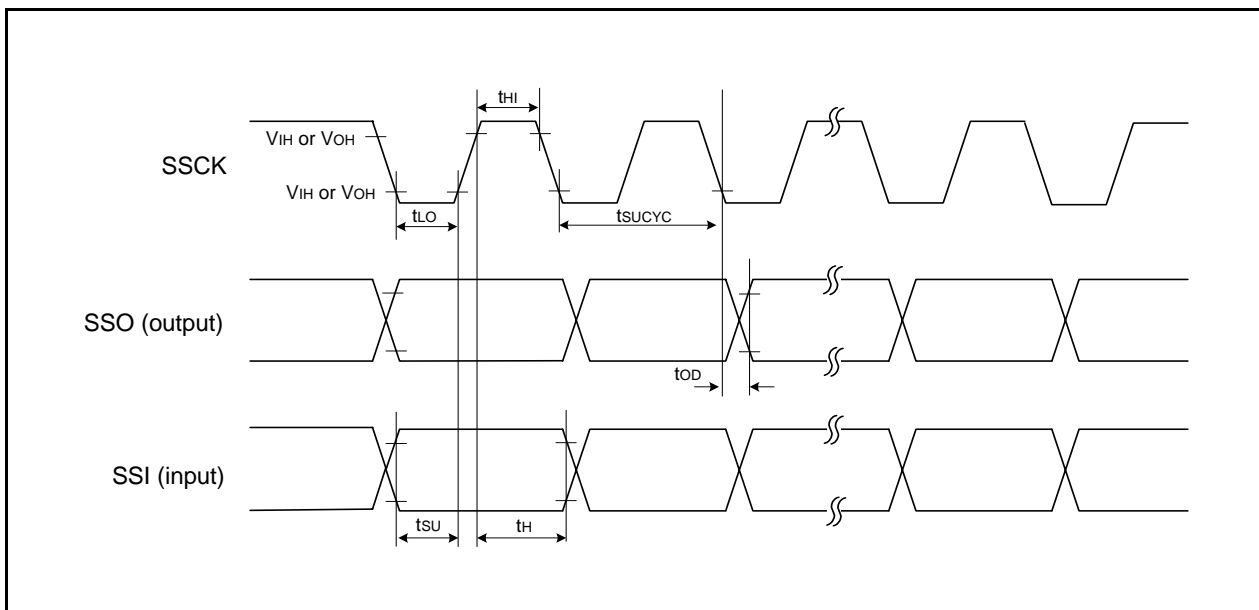


Figure 5.25 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.46 Timing Requirements of I²C bus Interface(1)

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|---|------|----------------------------------|------|
| | | | Min. | Typ. | Max. | |
| t _{SCL} | SCL input cycle time | | 12t _{CYC} + 600 ⁽²⁾ | – | – | ns |
| t _{SCLH} | SCL input “H” width | | 3t _{CYC} + 300 ⁽²⁾ | – | – | ns |
| t _{SCLL} | SCL input “L” width | | 5t _{CYC} + 500 ⁽²⁾ | – | – | ns |
| t _{sf} | SCL, SDA input fall time | | – | – | 300 | ns |
| t _{SP} | SCL, SDA input spike pulse rejection time | | – | – | 1t _{CYC} ⁽²⁾ | ns |
| t _{BUF} | SDA input bus-free time | | 5t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STAH} | Start condition input hold time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STAS} | Retransmit start condition input setup time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{STOP} | Stop condition input setup time | | 3t _{CYC} ⁽²⁾ | – | – | ns |
| t _{SDAS} | Data input setup time | | 1t _{CYC} + 20 ⁽²⁾ | – | – | ns |
| t _{SDAH} | Data input hold time | | 0 | – | – | ns |

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

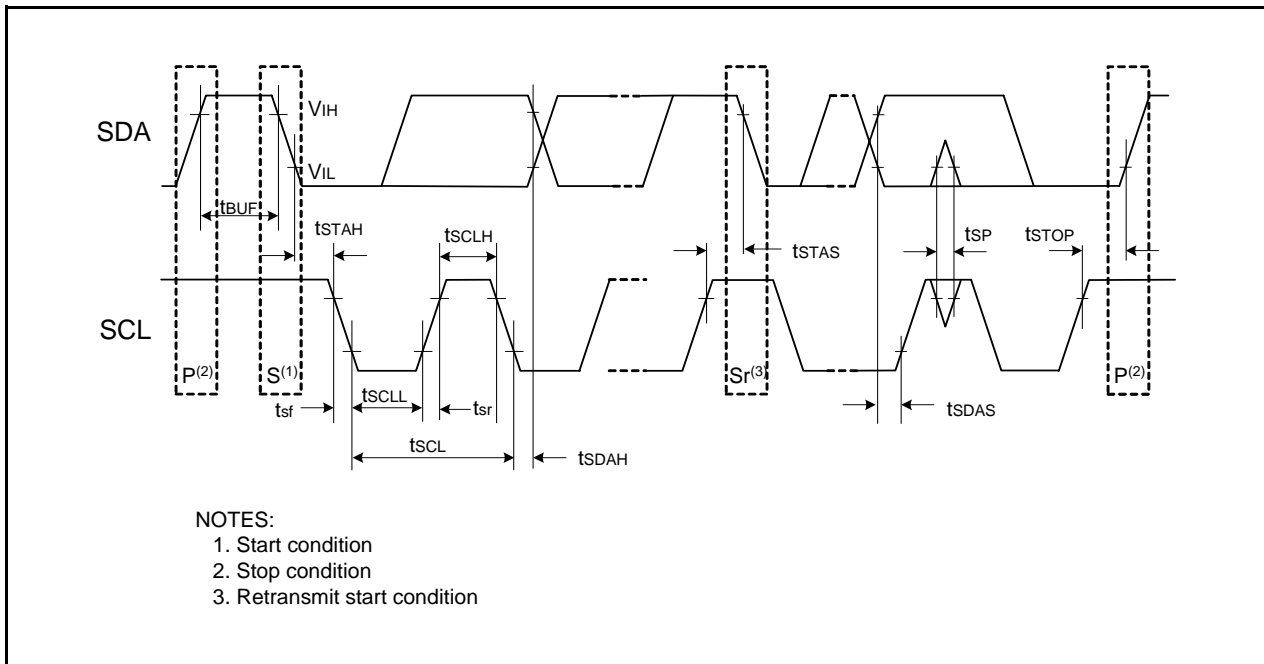
**Figure 5.26 I/O Timing of I²C bus Interface**

Table 5.47 Electrical Characteristics (1) [V_{CC} = 5 V]

| Symbol | Parameter | | Condition | Standard | | | Unit | |
|----------------------------------|---------------------|---|--|---------------------------|-----------------------|------|-----------------|----|
| | | | | Min. | Typ. | Max. | | |
| V _{OH} | Output "H" voltage | Except XOUT | I _{OH} = -5 mA | | V _{CC} - 2.0 | – | V _{CC} | V |
| | | | I _{OH} = -200 μA | | V _{CC} - 0.3 | – | V _{CC} | V |
| | XOUT | | Drive capacity HIGH | I _{OH} = -1 mA | V _{CC} - 2.0 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -500 μA | V _{CC} - 2.0 | – | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except XOUT | I _{OL} = 5 mA | | – | – | 2.0 | V |
| | | | I _{OL} = 200 μA | | – | – | 0.45 | V |
| | XOUT | | Drive capacity HIGH | I _{OL} = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} = 500 μA | – | – | 2.0 | V |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT3, K10, K11, K12, K13, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | – | V |
| | | RESET | | | 0.1 | 1.0 | – | V |
| I _{IH} | Input "H" current | | V _I = 5 V, V _{CC} = 5V | | – | – | 5.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 5V | | – | – | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 5V | | 30 | 50 | 167 | kΩ |
| R _{fXIN} | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | | 2.0 | – | – | V |

NOTE:

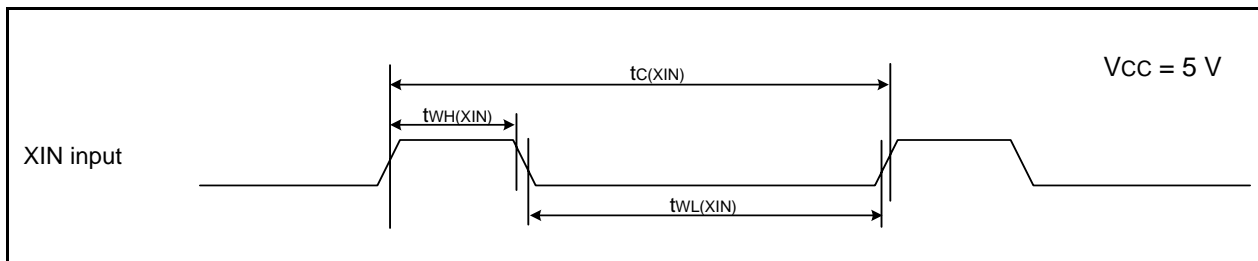
- V_{CC} = 4.2 to 5.5 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.48 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|---|---|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 10 | 17 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 9 | 15 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 6 | – | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 5 | – | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.5 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division | – | 10 | 15 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 4 | – | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5.5 | 10 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 75 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 60 | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.8 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.2 | – | μA |
| | | | XIN clock off, T _{opr} = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 4.0 | – | μA |

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.49 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 25 | – | ns |

**Figure 5.27 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.50 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 40 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 40 | – | ns |

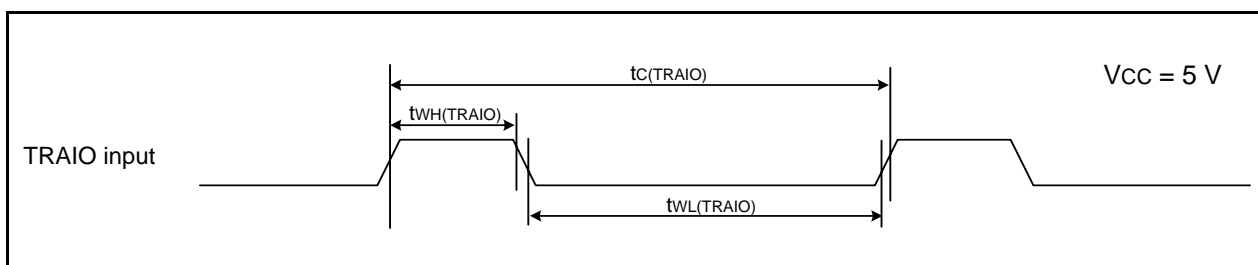
**Figure 5.28 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.51 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{w(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

$i = 0$ or 1

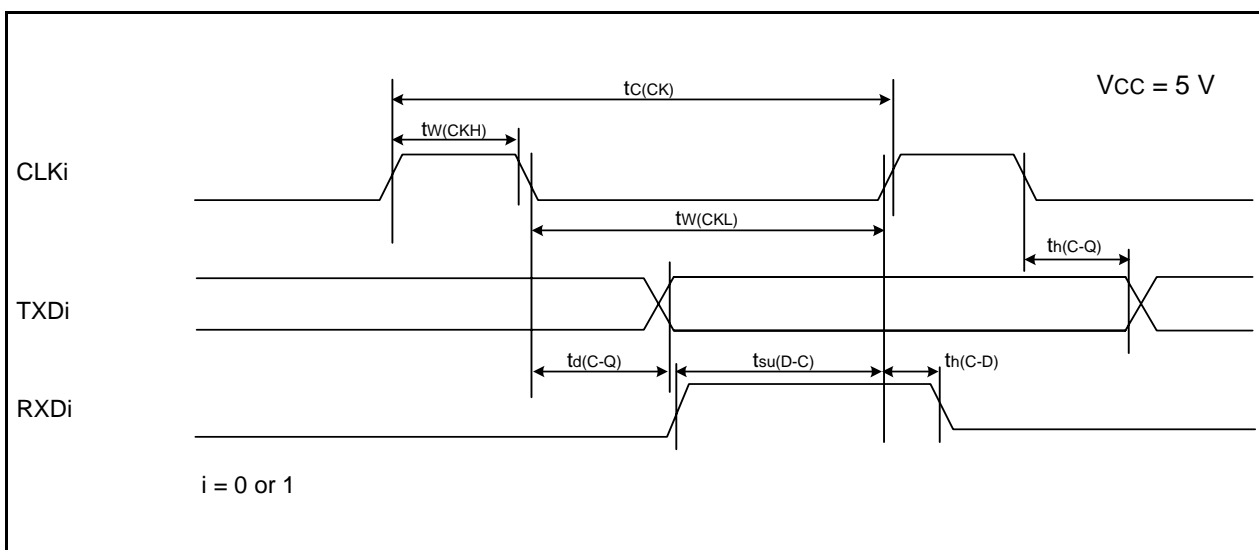


Figure 5.29 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.52 External Interrupt \overline{INTi} ($i = 0, 1, 3$) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 250 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 250 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

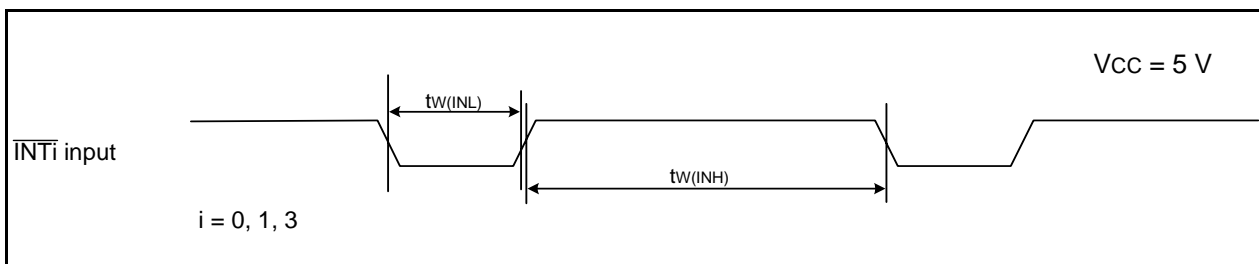


Figure 5.30 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 5 V

Table 5.53 Electrical Characteristics (3) [V_{CC} = 3 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|--|--|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except XOUT | I _{OH} = -1 mA | | V _{CC} - 0.5 | – | V _{CC} | V |
| | | XOUT | Drive capacity HIGH | I _{OH} = -0.1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50 μA | V _{CC} - 0.5 | – | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except XOUT | I _{OL} = 1 mA | | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50 μA | – | – | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}},$ $\text{K10}, \text{K11}, \text{K12}, \text{K13},$ $\text{TRAIO}, \text{RXD0}, \text{RXD1},$ $\text{CLK0}, \text{CLK1},$ $\text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$ | | | 0.1 | 0.3 | – | V |
| | | $\overline{\text{RESET}}$ | | | 0.1 | 0.4 | – | V |
| I _{IH} | Input "H" current | | V _I = 3 V, V _{CC} = 3V | | – | – | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V, V _{CC} = 3V | | – | – | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V, V _{CC} = 3V | | 66 | 160 | 500 | kΩ |
| R _{fXIN} | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | | 2.0 | – | – | V |

NOTE:

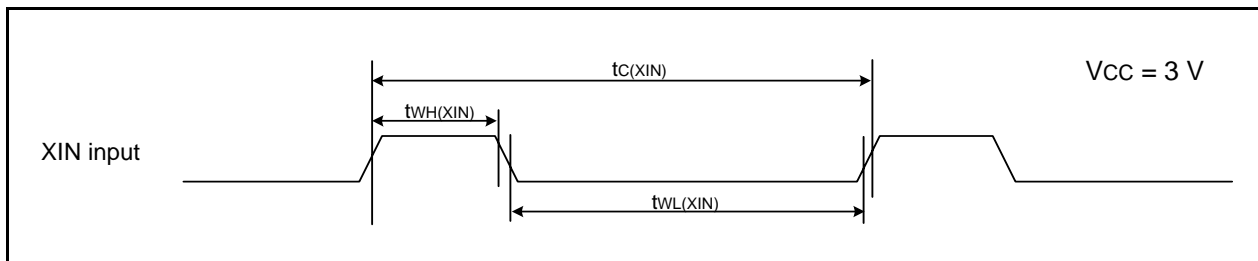
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.54 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)**

| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|---|---|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 6 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5 | 9 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 130 | 300 | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 25 | 70 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 23 | 55 | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.1 | – | μA |
| | | | XIN clock off, T _{opr} = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 3.8 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.55 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input "H" width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input "L" width | 40 | – | ns |

**Figure 5.31 XIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.56 TRAI0 Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width | 120 | – | ns |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width | 120 | – | ns |

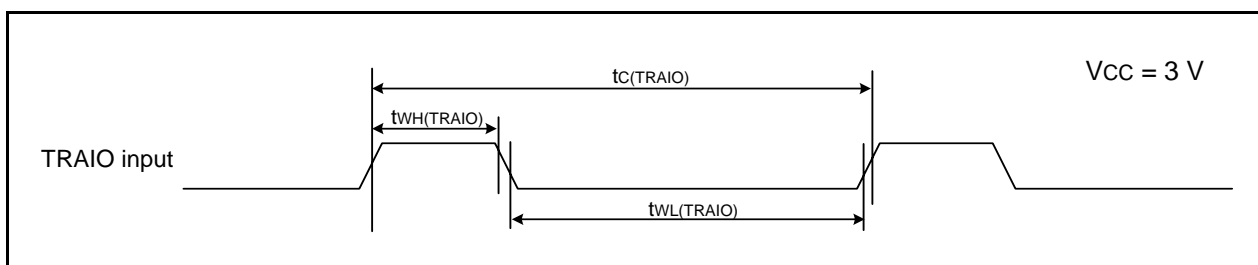
**Figure 5.32 TRAI0 Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.57 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{w(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

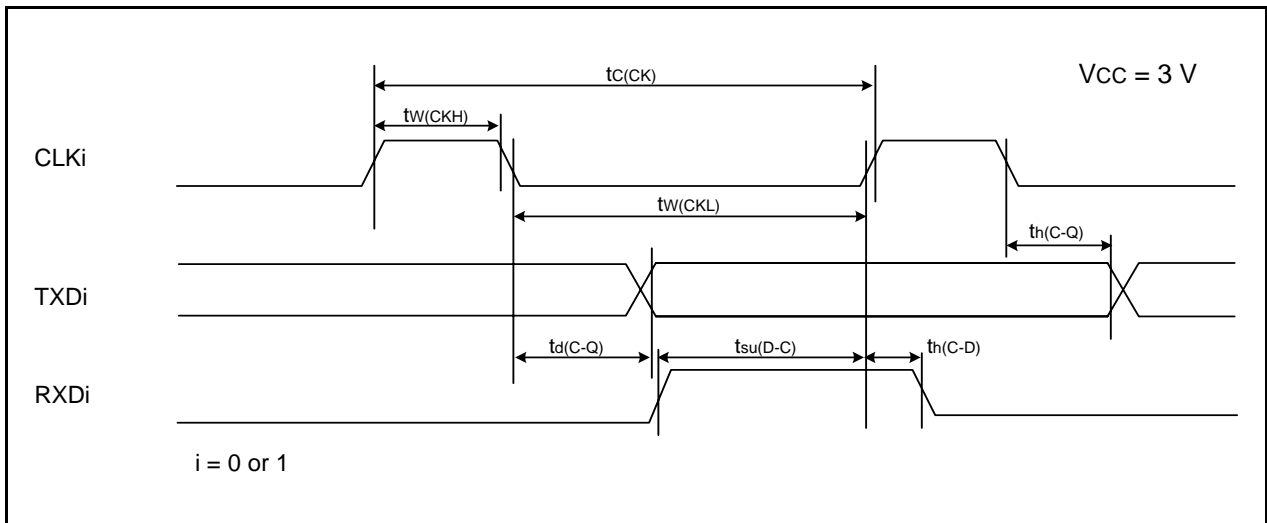


Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.58 External Interrupt \overline{INTi} (i = 0, 1, 3) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | \overline{INTi} input “H” width | 380 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | \overline{INTi} input “L” width | 380 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

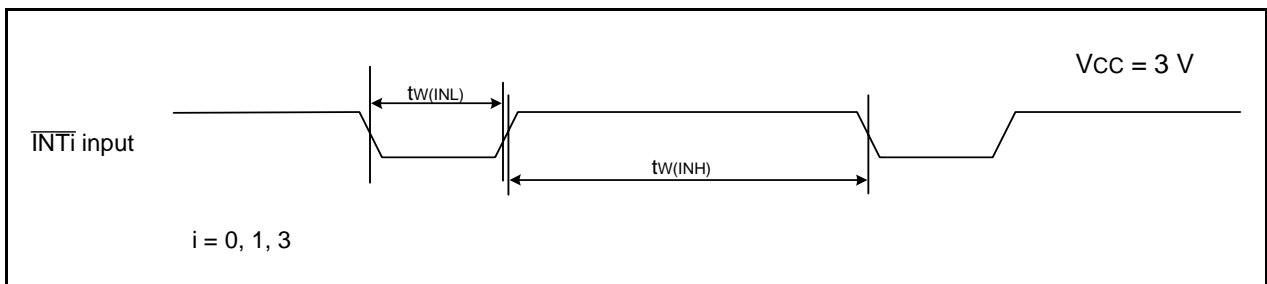
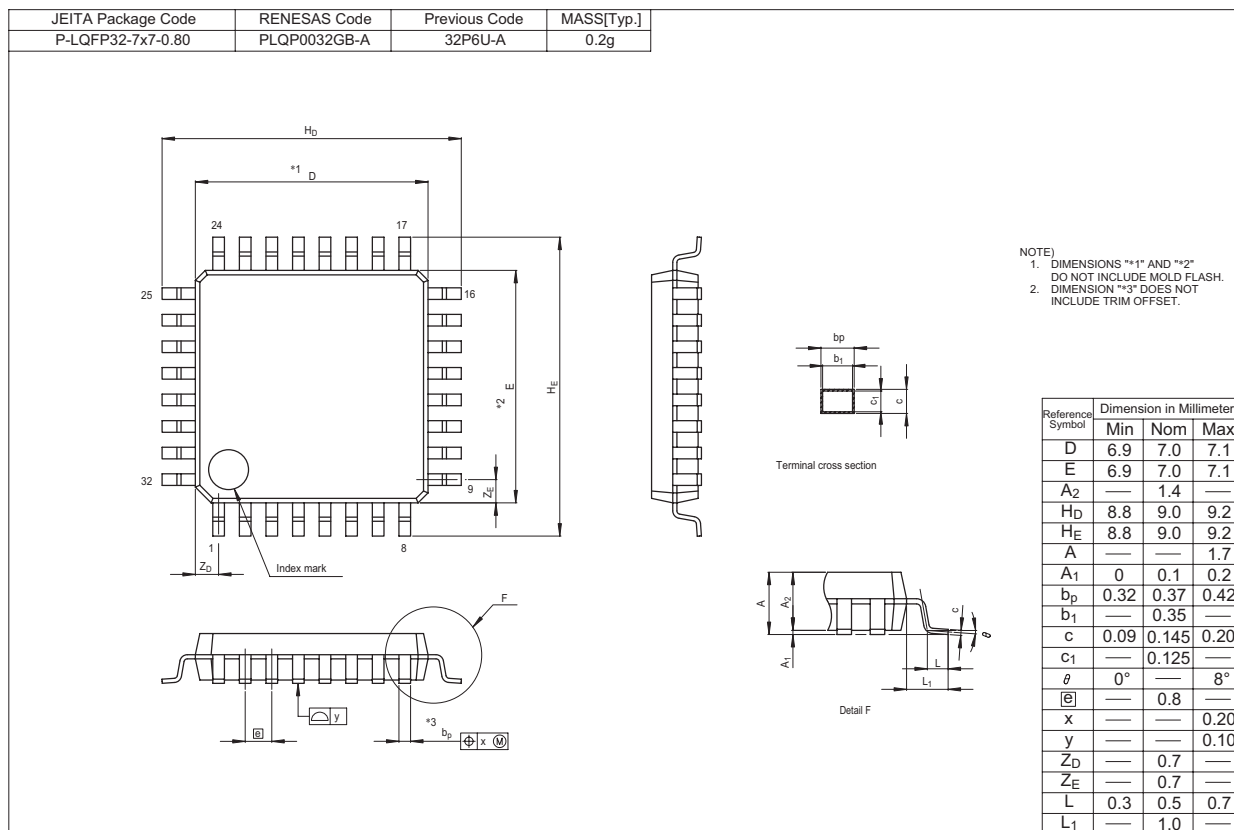


Figure 5.34 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

| Rev. | Date | Description | |
|------|--|-------------|---|
| | | Page | Summary |
| 0.10 | Nov 14, 2005 | – | First edition issued |
| 0.20 | Feb 06, 2006 | 2, 3 | Table 1.1 Functions and Specifications for R8C/26Group and Table 1.2 Functions and Specifications for R8C/27 Group; Minimum instruction execution time and Supply voltage revised |
| | | 9 | Table 1.6 Pin Name Information by Pin Number; “XOUT” → “XOUT/XCOUT” and “XIN” → “XIN/XCIN” revised |
| | | 18 | Table 4.4 SFR Information (4); 00FEh: “DRR” → “P1DRR” revised |
| | | 19 | Table 4.5 SFR Information (5); -0119h: “Timer RE Minute Data Register / Compare Register” → “Timer RE Minute Data Register / Compare Data Register” -011Ah: “Timer RE Time Data Register” → “Timer RE Hour Data Register” -011Bh: “Timer RE Day Data Register” → “Timer RE Day of Week Data Register” revised |
| | | 22 to 45 | 5. Electrical Characteristics added |
| 1.00 | Nov 08, 2006 | All pages | “Preliminary” deleted |
| | | 2 | Table 1.1 revised |
| | | 3 | Table 1.2 revised |
| | | 4 | Figure 1.1 revised |
| | | 5 | Table 1.3 revised |
| | | 6 | Table 1.4 revised |
| | | 7 | Figure 1.4 revised |
| | | 9 | Table 1.6 revised |
| | | 15 | Table 4.1; • 001Ch: “00h” → “00h, 10000000b” revised • 000Fh: “000XXXXXb” → “00X11111b” revised • 0029h: “High-Speed On-Chip Oscillator Control Register 4, FRA4, When shipping” added • 002Bh: “High-Speed On-Chip Oscillator Control Register 6, FRA6, When shipping” added • 0032h: “00h, 01000000b” → “00h, 00100000b” revised • 0038h: “00001000b, 01001001b” → “0000X000b, 0100X001b” revised • NOTE3 and 4 revised; NOTE6 added |
| | | 18 | Table 4.4; • 00E0h, 00E1h, 00E5h, 00E8h, 00E9h: “XXh” → “00h” revised • 00FDh: “XX00000000b” → “00h” revised |
| | | 22 | Table 5.2 revised |
| | | 23 | Figure 5.1 title revised |
| | | 24 | Table 5.4 revised |
| 25 | Table 5.5 revised | | |
| 26 | Figure 5.2 title revised and Table 5.7 NOTE4 added | | |

REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

| Rev. | Date | Description | |
|----------|------------------------|-------------|--|
| | | Page | Summary |
| 1.00 | Nov 08, 2006 | 27 | Table 5.9, Figure 5.3 revised and Table 5.10 deleted |
| | | 28 | Table 5.10, Table 5.11 revised |
| | | 34 | Table 5.15 revised |
| | | 35 | Table 5.16 revised |
| | | 36 | Table 5.17 revised |
| | | 39 | Table 5.22 revised |
| | | 40 | Table 5.23 revised |
| | | 44 | Table 5.29 revised |
| | | 47 | Package Dimensions; "Diagrams showing the latest...website." added |
| 1.10 | Nov 29, 2006 | All pages | "J, K version" added |
| | | 1 | 1 "J and K versions are under development...notice." added 1.1 revised |
| | | 2 | Table 1.1 revised |
| | | 3 | Table 1.2 revised |
| | | 4 | Figure 1.1 NOTE3 added |
| | | 5 | Table 1.3, Figure 1.2 revised |
| | | 6 | Table 1.4, Figure 1.3 revised |
| | | 7 | Figure 1.4 NOTE3 added |
| | | 8 | Table 1.5 revised |
| | | 9 | Table 1.6 NOTE2 added |
| | | 13 | Figure 3.1 revised |
| | | 14 | Figure 3.2 revised |
| | | 15 | Table 4.1; "0000h to 003Fh" → "0000h to 002Fh" revised • NOTE3 added |
| | | 16 | Table 4.2; "0040h to 007Fh" → "0030h to 007Fh" revised • 0032h, 0036h: "After reset" is revised • 0038h: NOTE revised • NOTES 2, 5, 6 revised and NOTE 7, 8 added |
| | | 19 | Table 4.5 NOTE2 added |
| 28 | Table 5.10 revised | | |
| 48 to 66 | 5.2 J, K Version added | | |
| 1.20 | Jan 17, 2007 | 18 | Table 4.4 NOTE2 added |
| 1.30 | May 25, 2007 | 2 | Table 1.1 revised |
| | | 3 | Table 1.2 revised |
| | | 5 | Table 1.3 revised |
| | | 6 | Figure 1.2 revised |
| | | 7 | Table 1.4 revised |
| | | 8 | Figure 1.3 revised |
| | | 9 | Figure 1.4 NOTE4 added |
| | | 15 | Figure 3.1 part number revised |

REVISION HISTORY

R8C/26 Group, R8C/27 Group Datasheet

| Rev. | Date | Description | |
|-------|---------------------------------|-------------|--|
| | | Page | Summary |
| 1.30 | May 25, 2007 | 16 | Figure 3.2 part number revised |
| | | 30 | Table 5.10 revised |
| | | 53 | Table 5.39 NOTE4 added |
| | | 55 | Table 5.42 revised |
| 1.40a | Jun 14, 2007 | 5, 7 | Table 1.3 and Table 1.4 revised |
| 2.00 | Mar 01, 2008 | 1, 49 | 1.1, 5.2 "J and K versions are ..." deleted |
| | | 5, 7 | Table 1.3, Table 1.4 revised |
| | | 11 | Table 1.6 NOTE3 added |
| | | 15, 16 | Figure 3.1, Figure 3.2; "Expanded area" deleted |
| | | 17 | Table 4.1 "002Ch" added |
| | | 18 | Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b" |
| | | 24, 49 | Table 5.2, Table 5.35; NOTE2 revised |
| 30 | Table 5.10 revised, NOTE4 added | | |
| 2.10 | Sep 26, 2008 | – | "RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E |
| | | 26, 51 | Table 5.4, Table 5.37 NOTE2, NOTE4 revised |
| | | 27, 52 | Table 5.5, Table 5.38 NOTE2, NOTE5 revised |
| | | 53 | Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added |
| | | 54 | Table 5.40 revised Table 5.41 revised Figure 5.22 revised |
| | | | |

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