



## **A8032 Series**

***Preliminary***

***8 Bit Microcontroller***

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### **Document Title**

**8 Bit Microcontroller**

### **Revision History**

| <b><u>Rev. No.</u></b> | <b><u>History</u></b> | <b><u>Issue Date</u></b> | <b><u>Remark</u></b> |
|------------------------|-----------------------|--------------------------|----------------------|
| 0.0                    | Initial issue         | November 27, 1998        |                      |



# A8032 Series

## Preliminary

## 8 Bit Microcontroller

### Features

- 8-bit CMOS microcontroller
- Fully static design with power saving idle mode and power down mode
- Low standby current at full supply voltage
- Versions for 12/24/40MHz operating frequency
- On chip 256B RAM
- Four 8-bit bidirectional ports
- 64K bytes external data memory space

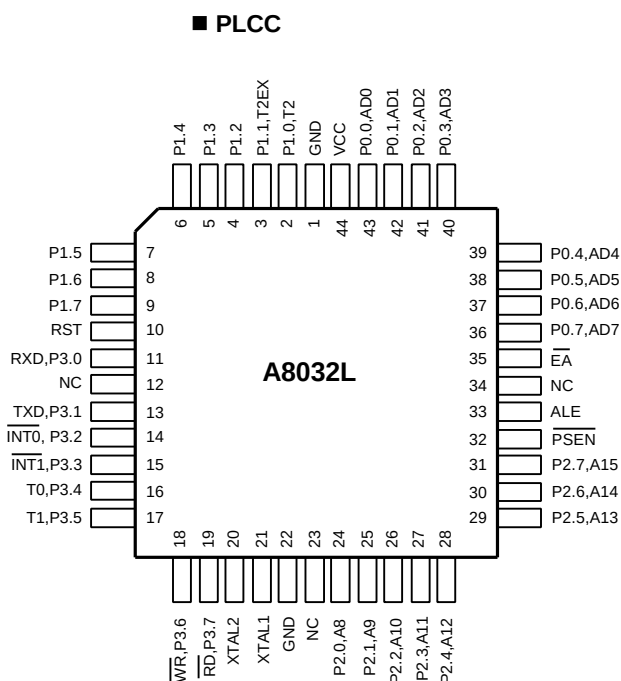
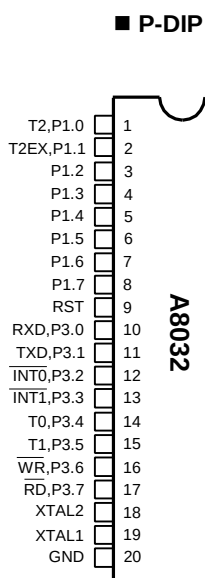
- Three 16-bit Timers/Counters (Timer 2 with up/down counter feature)
- One full duplex serial port
- Boolean processor
- Six interrupt sources, two priority levels
- Available in 40-pin P-DIP and 44-pin PLCC packages

### General Description

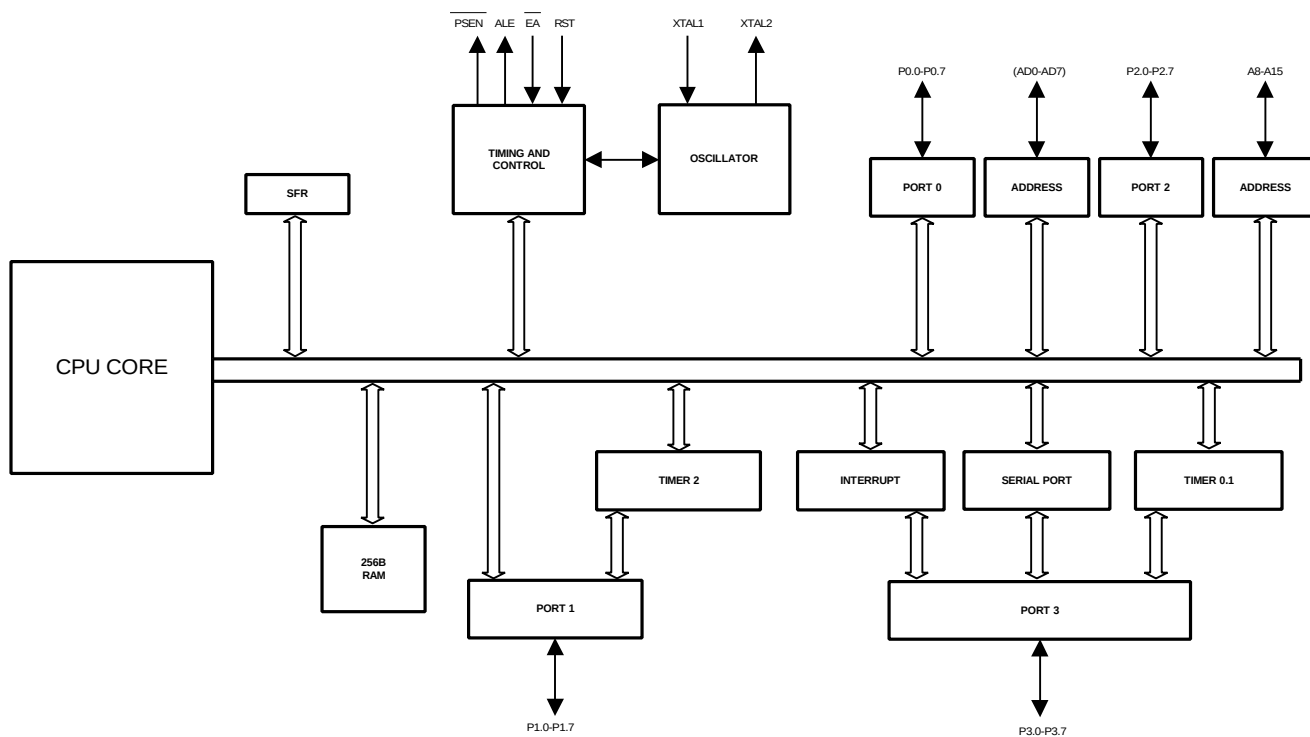
The AMIC A8032 is a high-performance 8-bit microcontroller. It is compatible with the industry standard 80C52 microcontroller series.

The A8032 contains a 256B RAM, four 8-bit bidirectional parallel ports, three 16-bit timer/counters, a serial port and six interrupt sources with two priority levels. The A8032 has supports 64KB external data memory.

### Pin Configurations



## Block Diagram



**Pin Description**

| Pin No. | Symbol                   | I/O                                    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|--------------------------|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 - 8   | P1.0 - P1.7              | I/O<br>I/O<br>I                        | Port1. Port1 is a bidirectional I/O port with internal pull-ups. Pin P1.0 and P1.1 also provide alternate functions as follows:<br>P1.0    T2        Timer/Counter2 external input/clock out<br>P1.1    T2EX     Timer/Counter2 capture/reload input                                                                                                                                                                                                                                                                                                               |
| 9       | RST                      | I                                      | Reset input, active high. It must be kept high for at least two machine cycles to be recognized by the processor                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 10 - 17 | P3.0 - P3.7              | I/O<br>I<br>O<br>I<br>I<br>I<br>O<br>O | Port3. Port3 is a bidirectional I/O port with internal pull-ups. Port3 pins also serve alternate functions as follows:<br>P3.0 $\overline{\text{RXD}}$ Serial receive port<br>P3.1 $\overline{\text{TXD}}$ Serial transmit port<br>P3.2 $\overline{\text{INT0}}$ External interrupt 0<br>P3.3 $\overline{\text{INT1}}$ External interrupt 1<br>P3.4    T0        Timer/Counter 0 input<br>P3.5    T1        Timer/Counter 1 input<br>P3.6 $\overline{\text{WR}}$ External data memory write strobe<br>P3.7 $\overline{\text{RD}}$ External data memory read strobe |
| 18      | XTAL2                    | O                                      | Crystal2. This is the output of crystal oscillator. It is the inversion of XTAL1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19      | XTAL1                    | I                                      | Crystal1. This is the input of crystal oscillator. It can be driven by an external clock                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 20      | GND                      | I                                      | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 21 - 28 | P2.0 - P2.7              | I/O                                    | Port2. Port2 is a bidirectional I/O port with internal pull-ups. Port2 is also the multiplexed upper-order address bus during accesses to external data memory                                                                                                                                                                                                                                                                                                                                                                                                     |
| 29      | $\overline{\text{PSEN}}$ | O                                      | Program Store Enable, active low. The read strobe to external program memory. $\overline{\text{PSEN}}$ is activated in each machine cycle when fetching external program memory                                                                                                                                                                                                                                                                                                                                                                                    |
| 30      | ALE                      | O                                      | Address latch enable, active high. ALE is used to enable the address latch that separates the data on Port 0                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 31      | $\overline{\text{EA}}$   | I                                      | External Access enable, active low. It is held low to enable the device to fetch code from external program memory                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 32 - 39 | P0.7 - P0.0              | I/O                                    | Port0. Port0 is an open drain, bidirectional I/O port. Port0 is also the multiplexed low-order address bus during accesses to external data memory                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 40      | VCC                      | I                                      | Power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## Functional Description

The A8032 is a high speed 8-bit microcontroller. The architecture consists of a core controller, four general purposes I/O ports, 256 bytes RAM internal register and a serial port. This microcontroller supports 111 opcodes and executes instructions in a 6-clock bus cycle. It can reference both a 64K program address space and a 64K data storage space.

## Timer/Counter 0, 1 and 2

Timer 0,1 and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0. TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TMOD and TCON registers support control function for Timer 0 and Timer 1. The T2CON register provides control function for Timer 2. When operating reload/capture mode, RCAP2H and RCAP2L will be used.

## Interrupt

The A8032 provides 6 interrupt modes. These consist of 2 external interrupts, 3 internal interrupts and a serial port interrupt.

The enable/disable interrupt is controlled by IE register in SFR.

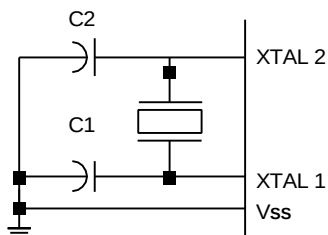
The priority of interrupts is controlled by IP register in SFR.

## Serial Port Transfer

The A8032 provides a full duplex serial transfer function. This function is controlled by SCON register in SFR. And the data is stored in SBUF register during transmitting and receiving.

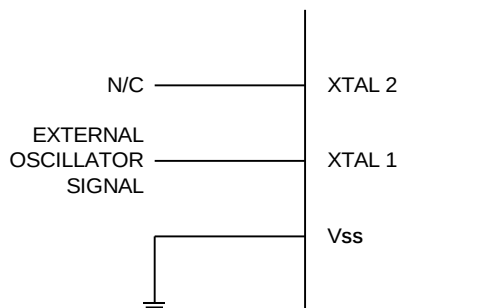
## Oscillator Characteristics

The oscillator connections are shown as Figure 1. And Figure 2. When quartz crystal is used, C1 and C2 are 30pF shown in Figure 1. When external clock is used, the internal clock will be gotten through a divide-by-two flip-flop. When starting up, the input loading for XTAL1 pin is 100pF. This is due to interaction between the amplifier and its feedback capacitance interaction. After the external signal meets the  $V_{IL}$  and  $V_{IH}$  specification the capacitance will not exceed 20pF.



$C1, C2 = 30\text{pF} \pm 10\text{pF}$  for Crystals

**Figure 1. Oscillator Connections**



**Figure 2. External Clock Drive configuration**

## RESET

The external reset signal must be held high for at least two machine cycles during the oscillator running. After reset, the ports are held high, SP register to 07H, all of the other SFR registers except SBUF to 00H, and SBUF is not reset.

**Recommended DC Operating Conditions** ( $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

| Symbol     | Parameter          | Min. | Typ. | Max.    | Unit |
|------------|--------------------|------|------|---------|------|
| VCC        | Supply Voltage     | 4.5  | 5.0  | 5.5     | V    |
| GND        | Ground             | 0    | 0    | 0       | V    |
| $V_{IH}^*$ | Input High Voltage | 2.4  | -    | VCC+0.2 | V    |
| $V_{IL}$   | Input Low Voltage  | 0    | -    | 0.8     | V    |

\* XTAL1 is a CMOS input. RESET is a Schmit trigger input.  
The min. of  $V_{IH}$  is 3.5 Volts for these two pins.

**Absolute Maximum Ratings\***

VCC to GND . . . . .  $-0.3\text{V}$  to  $+7.0\text{V}$   
 IN, IN/OUT Volt to GND . . . . .  $-0.5\text{V}$  to VCC +  $0.5\text{V}$   
 Operating Temperature,  $T_{opr}$  . . . . .  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 Storage Temperature,  $T_{stg}$  . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Power Dissipation<sup>1\*</sup>,  $P_r$  . . . . . 1W  
 Soldering Temperature & Time . . . . .  $260^{\circ}\text{C}$ , 10sec

1\* : Operating frequency is 40MHz

**\*Comments**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** ( $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , VCC =  $5\text{V} \pm 10\%$ )

| Symbol       | Parameter                                                        | Min. | Max. | Unit          | Conditions                                                      |
|--------------|------------------------------------------------------------------|------|------|---------------|-----------------------------------------------------------------|
| $ I_{L1} ^1$ | Input Leakage Current                                            | -    | 10   | $\mu\text{A}$ | $V_{IN} = \text{GND to VCC}$                                    |
| $ I_{LO} $   | Output Leakage Current                                           | -    | 10   | $\mu\text{A}$ | $V_{IO} = \text{GND to VCC}$                                    |
| $I_{CC}$     | Operating Current                                                | -    | 50   | mA            | foper = 40MHz<br>External oscillator is on XTAL1 pin<br>No load |
| $V_{OL1}$    | Output Low Voltage<br>(PORT1, PORT2 and PORT3)                   | -    | 0.45 | V             | $I_{OL} = 2\text{mA}$                                           |
| $V_{OL2}$    | Output Low Voltage<br>(ALE, $\overline{\text{PSEN}}$ and PORT0)  | -    | 0.45 | V             | $I_{OL} = 4\text{mA}$                                           |
| $V_{OH1}$    | Output High Voltage<br>(PORT1, PORT2 and PORT3)                  | 2.4  | -    | V             | $I_{OH} = -100\mu\text{A}$                                      |
| $V_{OH2}$    | Output High Voltage<br>(ALE, $\overline{\text{PSEN}}$ and PORT0) | 2.4  | -    | V             | $I_{OH} = -400\mu\text{A}$                                      |
| $C_1$        | Input Pin Capacitance                                            | -    | 10   | pF            | 1MHz, $25^{\circ}\text{C}$                                      |

1. For RESET pin, the  $|I_{L1}|$  max. is  $300\mu\text{A}$ , since it has an internal pull-low of approx.  $30\text{K}\Omega$  resistor.

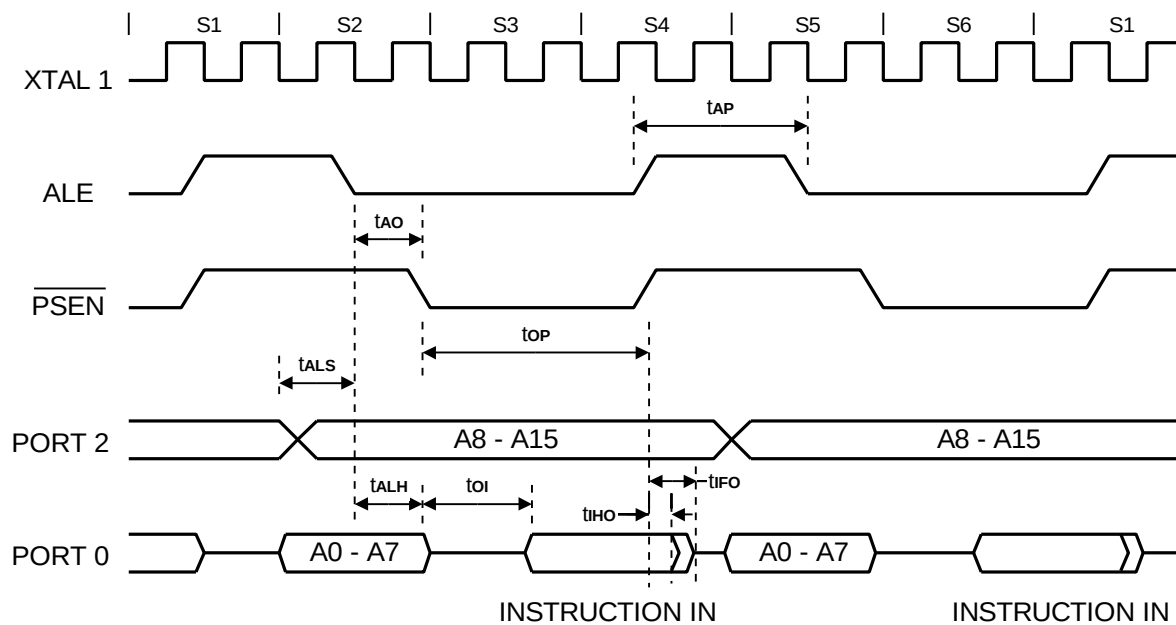
**AC Characteristics** ( $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )

| Symbol                      | Parameter                                            | Min.             | Max.             | Unit |
|-----------------------------|------------------------------------------------------|------------------|------------------|------|
| <b>Program Memory Cycle</b> |                                                      |                  |                  |      |
| $t_{AP}$                    | ALE Pulse Width                                      | $2t_{ck} - 20^1$ | -                | ns   |
| $t_{ALS}$                   | Address Valid to ALE Low                             | $1t_{ck}$        | -                | ns   |
| $t_{ALH}$                   | Address Hold from ALE Low                            | $1t_{ck}$        | -                | ns   |
| $t_{op}$                    | $\overline{PSEN}$ Pulse Width                        | $3t_{ck} - 20^1$ | -                | ns   |
| $t_{AO}$                    | ALE Low to $\overline{PSEN}$ Low                     | $1t_{ck}$        | -                | ns   |
| $t_{oi}^2$                  | $\overline{PSEN}$ Low to Valid Instruction in        | -                | $2t_{ck}$        | ns   |
| $t_{iDO}$                   | Input Instruction Hold after $\overline{PSEN}$ High  | -                | $1t_{ck}$        | ns   |
| $t_{iFO}$                   | Input Instruction Float after $\overline{PSEN}$ High | -                | $1t_{ck}$        | ns   |
| <b>External Clock</b>       |                                                      |                  |                  |      |
| $f_{OPER}$                  | Clock Frequency                                      | 0                | 40               | MHz  |
| $t_{CK}^3$                  | Clock Period                                         | 25               | -                | ns   |
| $t_{CKH}^4$                 | Clock High Time                                      | 10               | -                | ns   |
| $t_{CKL}^4$                 | Clock Low Time                                       | 10               | -                | ns   |
| <b>Data Memory Cycle</b>    |                                                      |                  |                  |      |
| $t_{PR}$                    | $\overline{RD}$ Pulse Width                          | $6t_{ck} - 20^1$ | -                | ns   |
| $t_{PD}$                    | $\overline{RD}$ Low to Valid Data in                 | -                | $4t_{ck}$        | ns   |
| $t_{DHR}$                   | Data Hold from $\overline{RD}$ High                  | 0                | $2t_{ck}$        | ns   |
| $t_{DFR}$                   | Data Float from $\overline{RD}$ High                 | 0                | $2t_{ck}$        | ns   |
| $t_{AR}$                    | ALE Low to $\overline{RD}$ Low                       | $3t_{ck}$        | $3t_{ck} + 20^1$ | ns   |
| $t_{WP}$                    | $\overline{WR}$ Pulse Width                          | $6t_{ck} - 20^1$ | -                | ns   |
| $t_{DS}$                    | Valid Data to $\overline{WR}$ Low                    | $1t_{ck}$        | -                | ns   |
| $t_{DHW}$                   | Data Hold from $\overline{WR}$ High                  | $1t_{ck}$        | -                | ns   |
| $t_{AW}$                    | ALE Low to $\overline{WR}$ Low                       | $3t_{ck}$        | $3t_{ck} + 20^1$ | ns   |
| <b>Serial Port Cycle</b>    |                                                      |                  |                  |      |
| $t_{SCK}$                   | Serial Port Clock                                    | $12t_{ck}$       | -                | ns   |
| $t_{KI}$                    | Clock Rising Edge to Valid Input Data                | -                | $11t_{ck}$       | ns   |
| $t_{KH}$                    | Input Data to Serial Clock Rising Clock Hold Time    | 0                | -                | ns   |
| $t_{OKS}$                   | Output Data to Serial Clock Rising Edge Setup Time   | $11t_{ck}$       | -                | ns   |
| $t_{OKH}$                   | Output Data to Serial Clock Rising Edge Hold Time    | $1t_{ck}$        | -                | ns   |

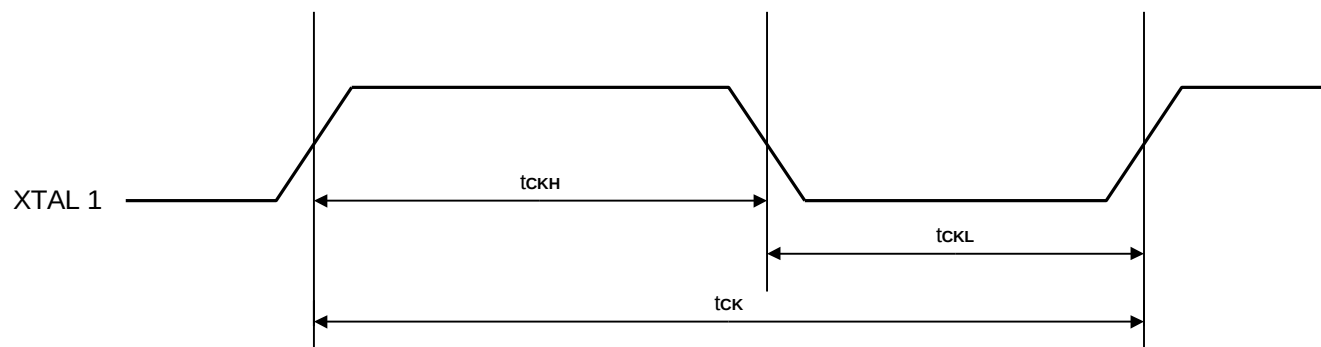
1. This 20 ns is due to buffer driving delay and wire loading.
2. Instruction cycle time is  $12 t_{ck}$ .
3.  $t_{ck} = 1 / f_{oper}$
4. There are no duty cycle requirements on the XTAL1 input.

## Timing Waveforms

### Program Memory Cycle



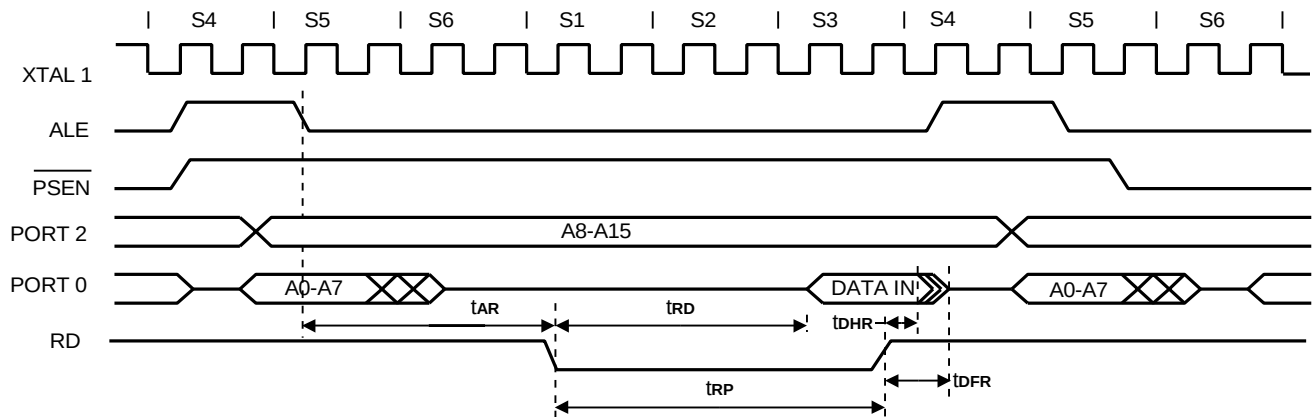
### Clock Input Waveform



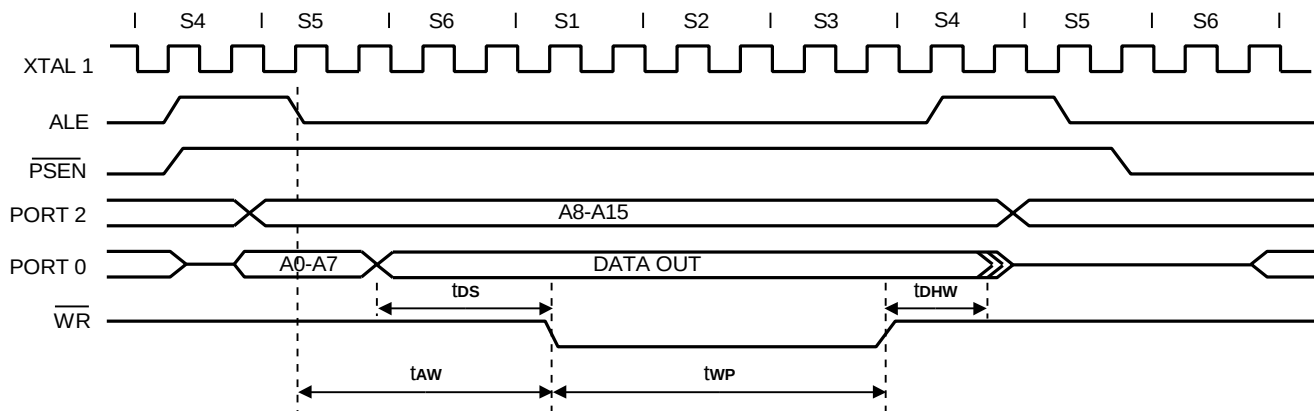


## Timing Waveforms (continued)

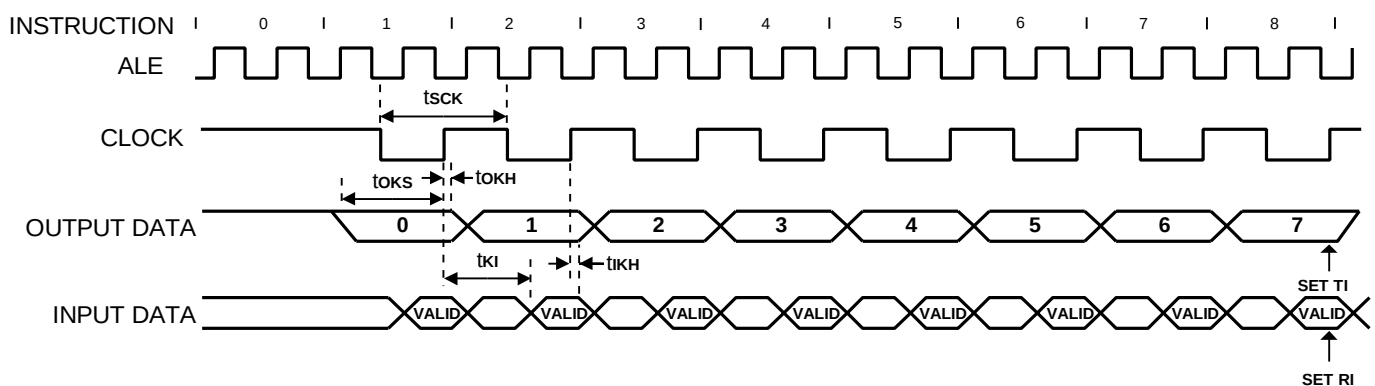
### Data Memory Read Cycle



### Data Memory Write Cycle



### Serial Port Timing – Shift Register Mode

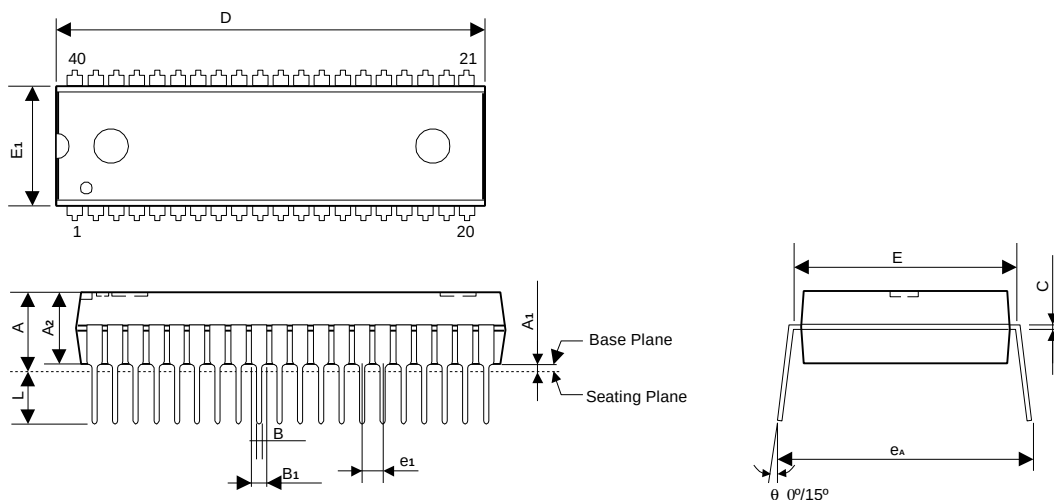


**Ordering Information**

| Part No.  | RAM      | FREQ (MHz) | Package   |
|-----------|----------|------------|-----------|
| A8032-12  | 256 Byte | 12         | 40L P-DIP |
| A8032L-12 | 256 Byte | 12         | 44L PLCC  |
| A8032-24  | 256 Byte | 24         | 40L P-DIP |
| A8032L-24 | 256 Byte | 24         | 44L PLCC  |
| A8032-40  | 256 Byte | 40         | 40L P-DIP |
| A8032L-40 | 256 Byte | 40         | 44L PLCC  |

**Package Information**
**P-DIP 40L Outline Dimensions**

unit: inches/mm



| Symbol | Dimensions in inches |       |       | Dimensions in mm |        |        |
|--------|----------------------|-------|-------|------------------|--------|--------|
|        | Min                  | Nom   | Max   | Min              | Nom    | Max    |
| A      | -                    | -     | 0.210 | -                | -      | 5.344  |
| A1     | 0.015                | -     | -     | 0.381            | -      | -      |
| A2     | 0.150                | 0.155 | 0.160 | 3.810            | 3.937  | 4.064  |
| B      | 0.018 TYP            |       |       | 0.457 TYP        |        |        |
| B1     | 0.050 TYP            |       |       | 1.270 TYP        |        |        |
| C      | -                    | 0.010 | -     | -                | 0.254  | -      |
| D      | 2.049                | 2.054 | 2.059 | 52.045           | 52.172 | 52.299 |
| E      | 0.590                | 0.600 | 0.610 | 14.986           | 15.240 | 15.494 |
| E1     | 0.542                | 0.547 | 0.552 | 13.767           | 13.894 | 14.021 |
| e1     | 0.100 TYP            |       |       | 2.540 TYP        |        |        |
| L      | 0.120                | 0.130 | 0.140 | 3.048            | 3.302  | 3.556  |
| eA     | 0.622                | 0.642 | 0.662 | 15.799           | 16.307 | 16.815 |

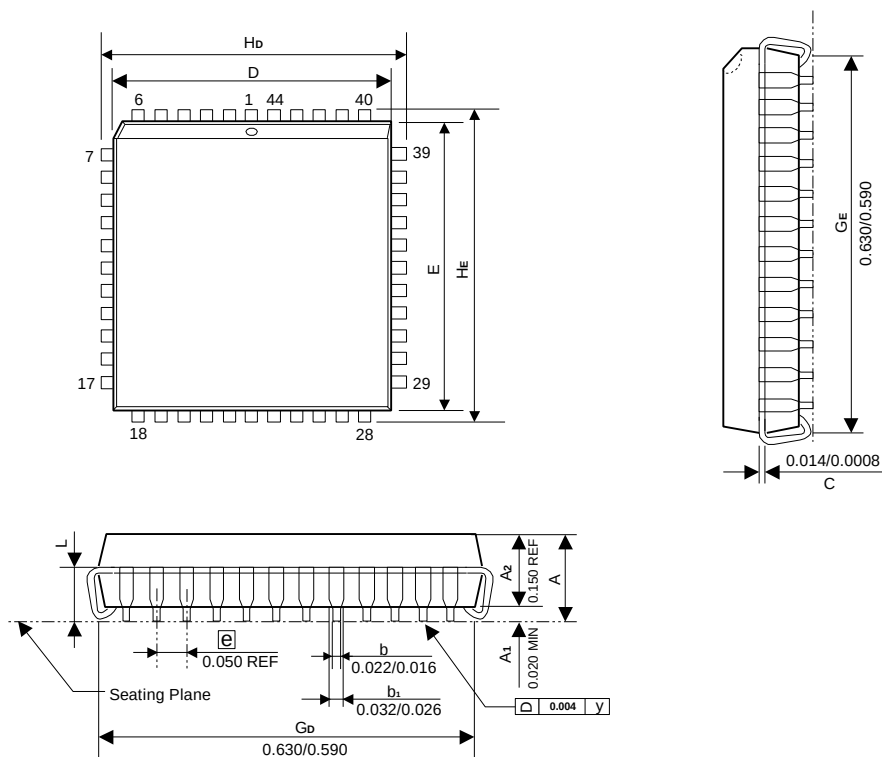
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.

## Package Information

### PLCC 44L Outline Dimension

unit: inches/mm



| Symbol         | Dimensions in inches |       |       | Dimensions in mm |       |       |
|----------------|----------------------|-------|-------|------------------|-------|-------|
|                | Min                  | Nom   | Max   | Min              | Nom   | Max   |
| A              | -                    | -     | 0.185 | -                | -     | 4.70  |
| D              | 0.648                | 0.653 | 0.658 | 16.46            | 16.59 | 16.71 |
| E              | 0.648                | 0.653 | 0.658 | 16.46            | 16.59 | 16.71 |
| H <sub>D</sub> | 0.680                | 0.690 | 0.700 | 17.27            | 17.53 | 17.78 |
| H <sub>E</sub> | 0.680                | 0.690 | 0.700 | 17.27            | 17.53 | 17.78 |
| L              | 0.090                | 0.100 | 0.110 | 2.29             | 2.54  | 2.79  |
| θ              | 0°                   | -     | 10°   | 0°               | -     | 10°   |

#### Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G<sub>D</sub> & G<sub>E</sub> are for PC Board surface mount pad pitch design reference only.

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