

NVTFS5116PL

Power MOSFET

–60 V, –14 A, 52 mΩ, Single P–Channel

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NV Prefix for Automotive and Other Applications Requiring AEC–Q101 Qualified Site and Change Controls
- These are Pb–Free Devices

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	–60	V
Gate–to–Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	$T_{mb} = 25^\circ\text{C}$	I_D –14 A
		$T_{mb} = 100^\circ\text{C}$	–10
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	Steady State	$T_{mb} = 25^\circ\text{C}$	P_D 21 W
		$T_{mb} = 100^\circ\text{C}$	10
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D –6 A
		$T_A = 100^\circ\text{C}$	–4
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.2 W
		$T_A = 100^\circ\text{C}$	1.6
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} –126	A
Operating Junction and Storage Temperature	T_J, T_{stg}	–55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	–17	A
Single Pulse Drain–to–Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 30 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	45	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction–to–Mounting Board (top) – Steady State (Note 2 and 3)	$R_{\Psi J-mb}$	7.2	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – Steady State (Note 3)	$R_{\theta JA}$	47	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface–mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

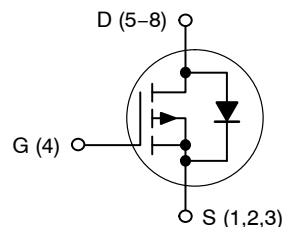


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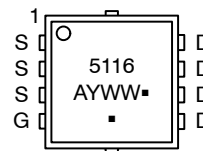
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
–60 V	52 mΩ @ –10 V	–14 A
	72 mΩ @ –4.5 V	

P–Channel MOSFET



WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



5116 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NVTFS5116PLTAG	WDFN8 (Pb–Free)	1500/Tape & Reel
NVTFS5116PLTWG	WDFN8 (Pb–Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVTF5116PL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		-1.0	μA
			T _J = 125°C		-10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1		-3	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -7 A		37	52	mΩ
		V _{GS} = -4.5 V, I _D = -7 A		51	72	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = -5 A		11		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -25 V		1258		pF
Output Capacitance	C _{oss}			127		
Reverse Transfer Capacitance	C _{rss}			84		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -48 V, I _D = -7 A		14		nC
Threshold Gate Charge	Q _{G(TH)}			1		
Gate-to-Source Charge	Q _{GS}			4		
Gate-to-Drain Charge	Q _{GD}			8		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -48 V, I _D = -7 A		25		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DS} = -48 V, I _D = -7 A		14		ns
Rise Time	t _r			68		
Turn-Off Delay Time	t _{d(off)}			24		
Fall Time	t _f			36		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -7 A	T _J = 25°C		-0.79	-1.20	V
			T _J = 125°C		-0.64		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -7 A			21		ns
Charge Time	t _a				16		
Discharge Time	t _b				5		
Reverse Recovery Charge	Q _{RR}				24		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

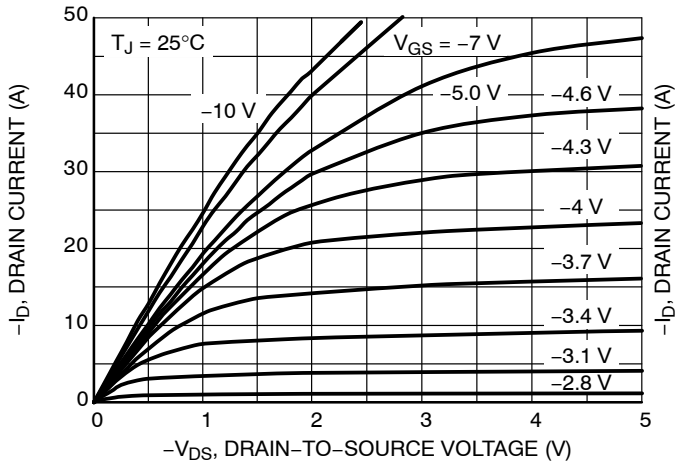


Figure 1. On-Region Characteristics

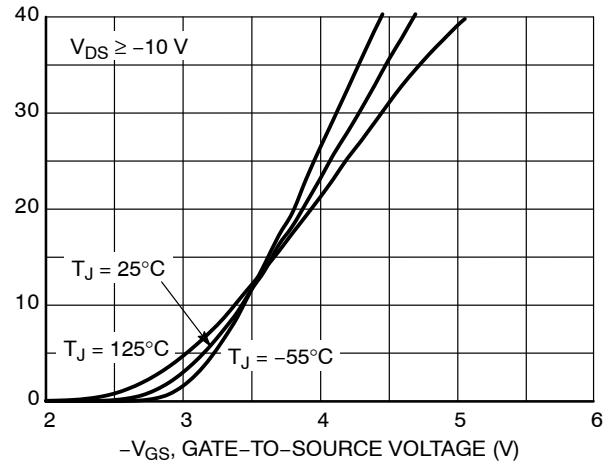


Figure 2. Transfer Characteristics

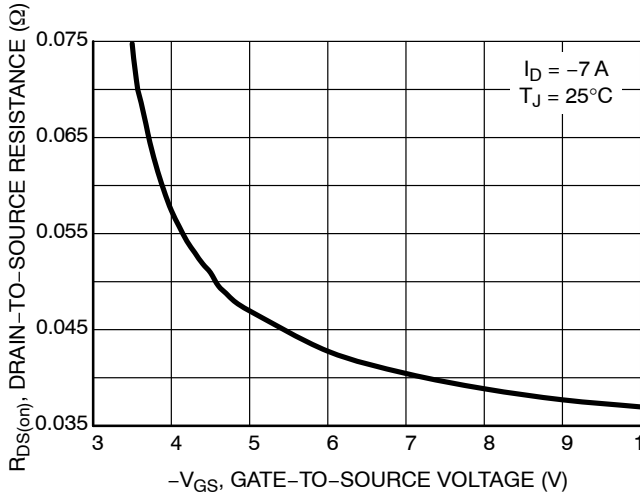


Figure 3. On-Resistance vs. Gate-to-Source Voltage

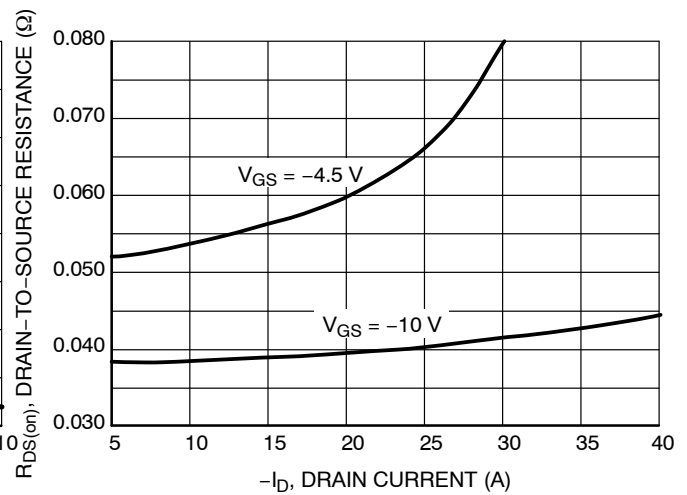


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

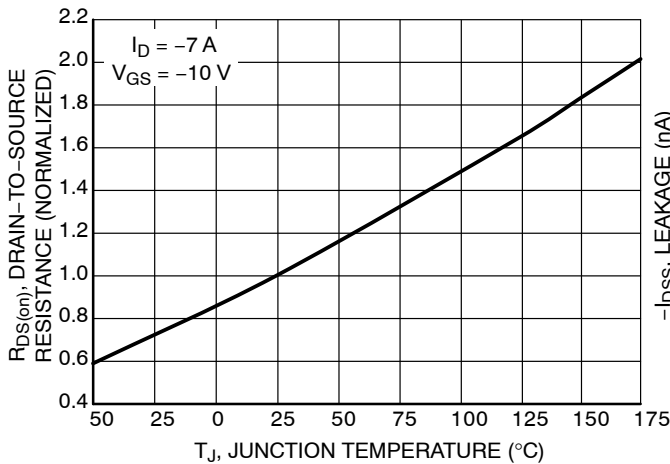


Figure 5. On-Resistance Variation with Temperature

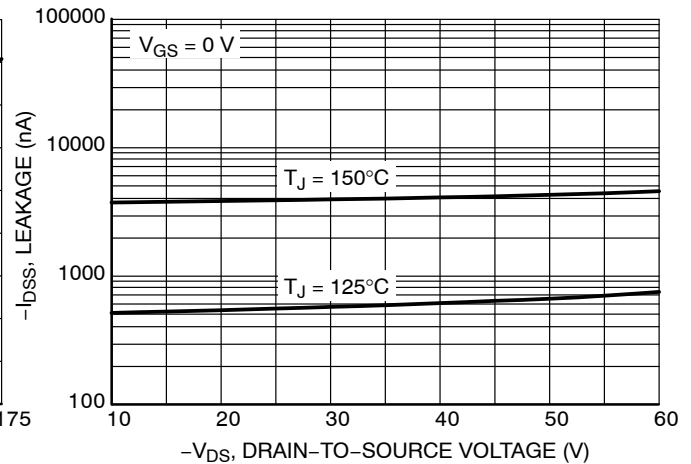


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

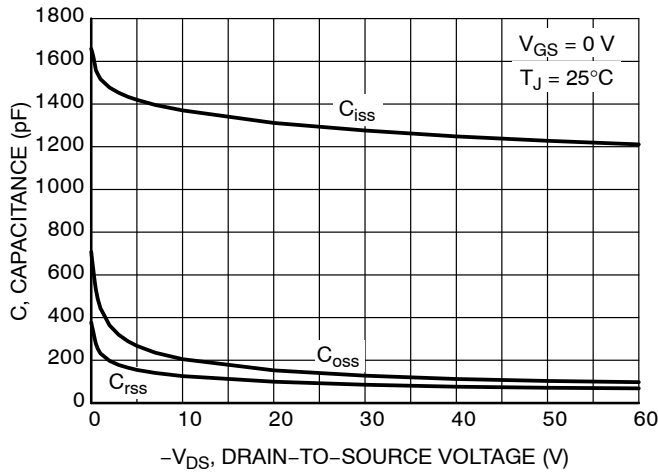


Figure 7. Capacitance Variation

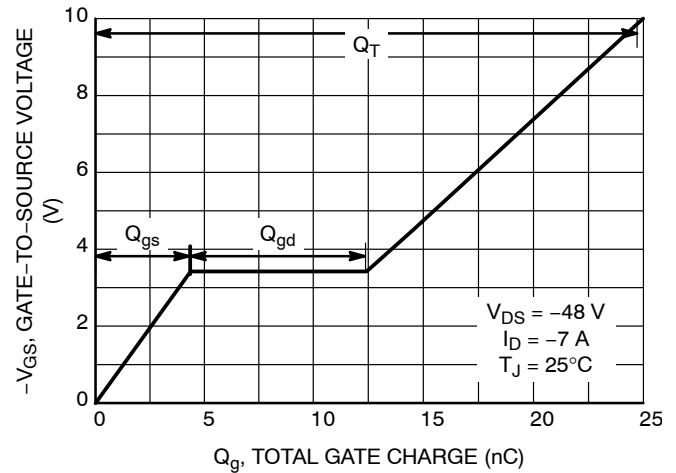


Figure 8. Gate-to-Source Voltage vs. Total Charge

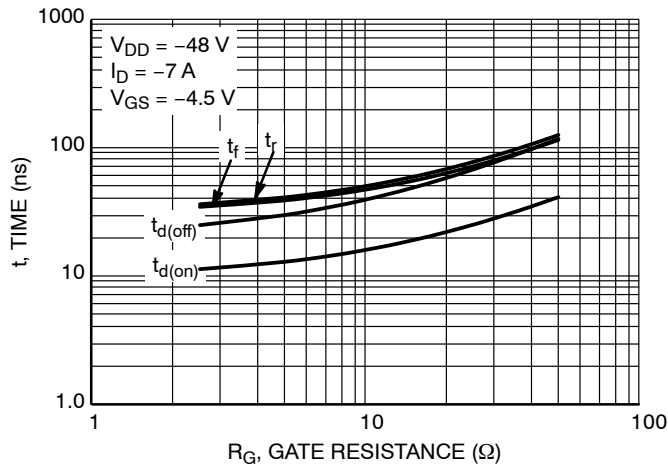


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

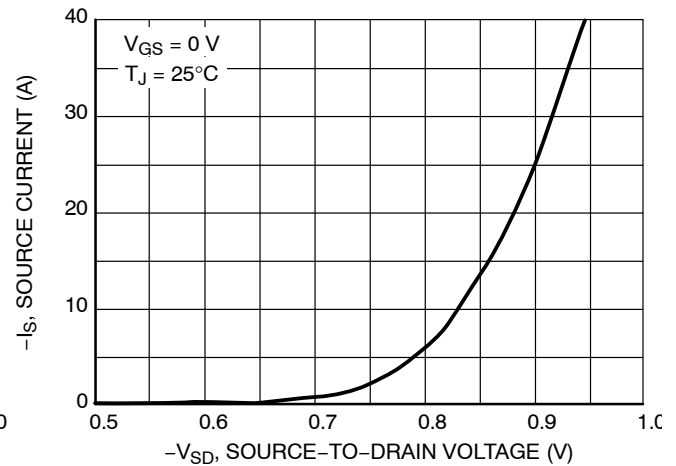


Figure 10. Diode Forward Voltage vs. Current

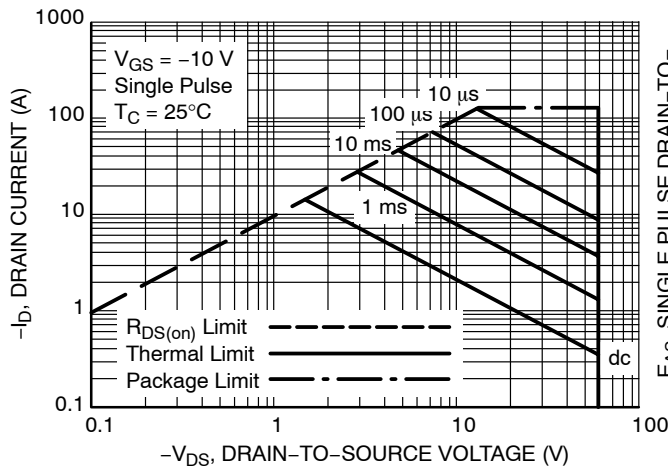


Figure 11. Maximum Rated Forward Biased Safe Operating Area

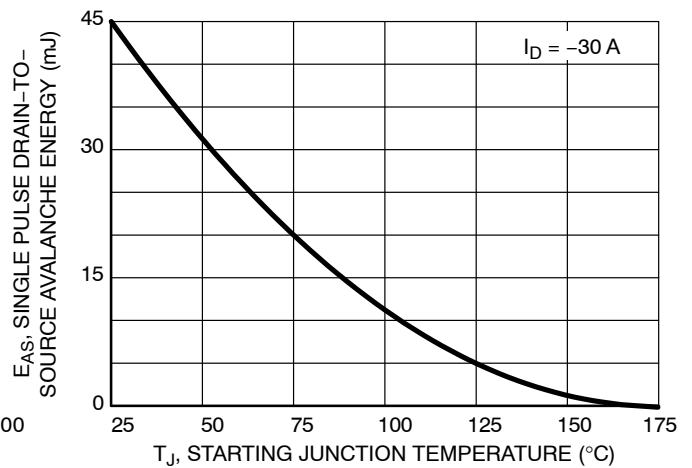


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NVTFS5116PL

TYPICAL CHARACTERISTICS

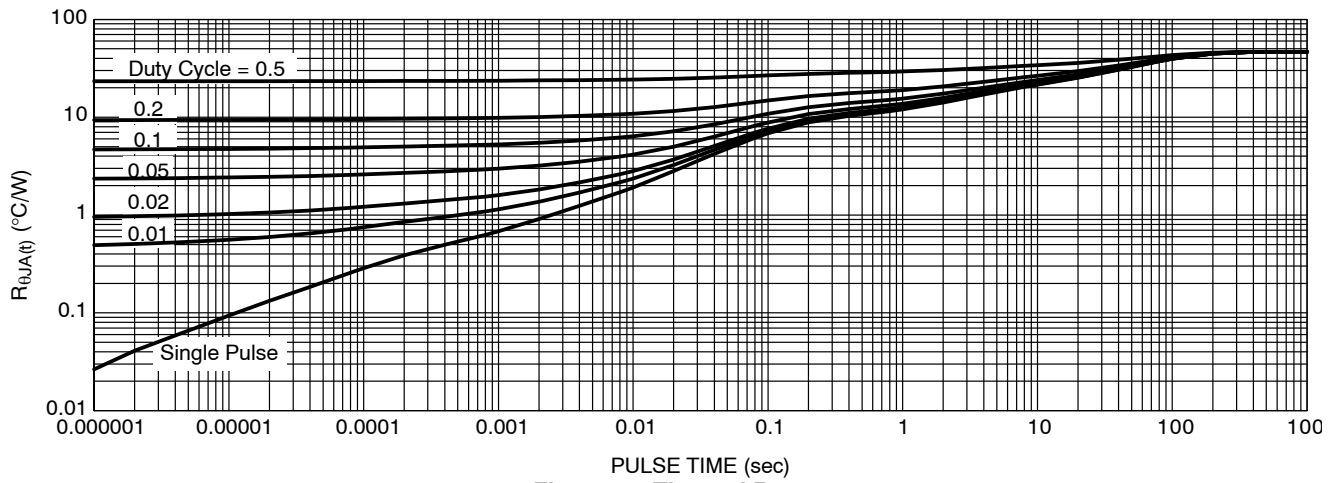
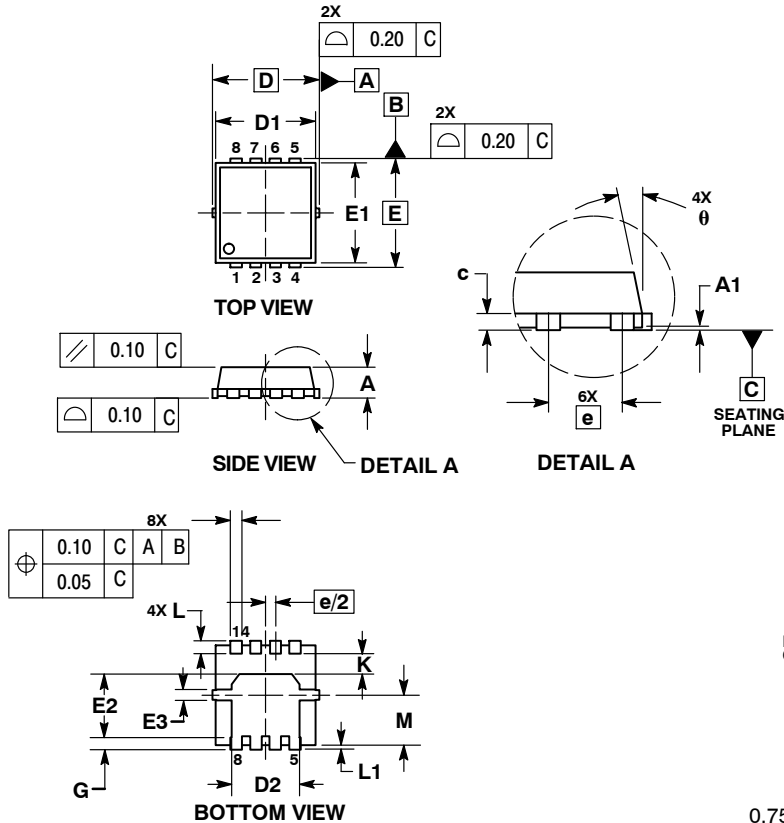


Figure 13. Thermal Response

PACKAGE DIMENSIONS

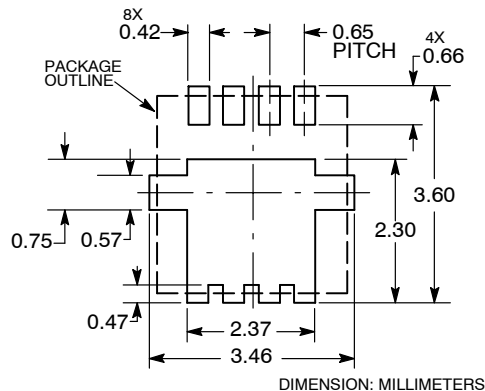
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.64	---	---	0.025	---	---
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Телефон: 8 (812) 309-75-97 (многоканальный)

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А