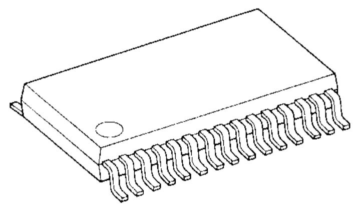
TOSHIBA CDMOS Integrated Circuit Silicon Monolithic

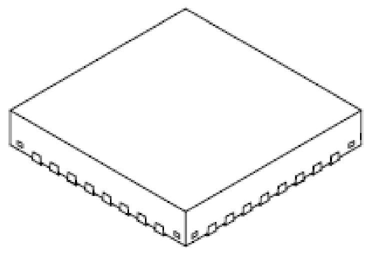
TC78B041FNG/TC78B042FTG

Sine-wave PWM Drive
Three-phase Full Wave Brushless Motor Controller

TC78B041FNG and TC78B042FTG are developed for three-phase brushless DC fan motors.
The TC78B041FNG adopts SSOP30 type package.
The TC78B042FTG adopts QFN32 type package, adding RESX and VREF2 pins.



SSOP30-P-300-0.65
Weight: 0.18 g (typ.)

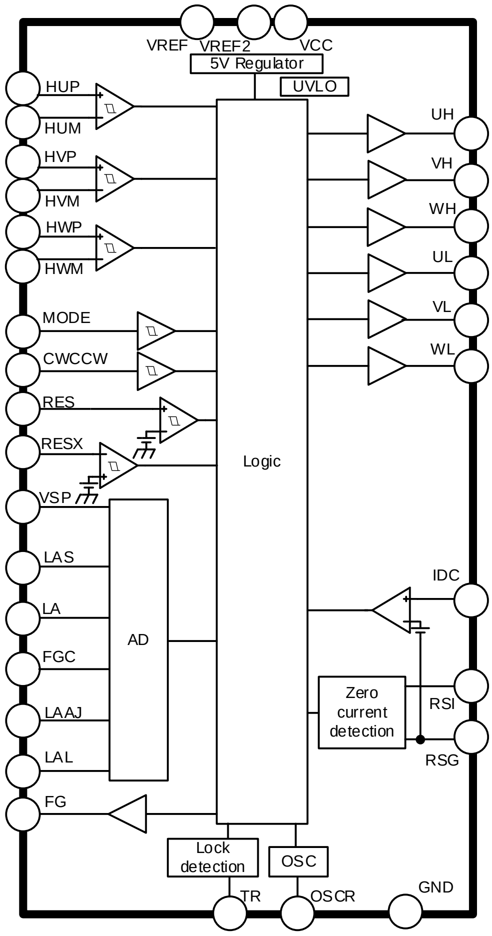


P-VQFN32-0505-0.50-005
Weight: 0.06 g (typ.)

Features

- Sine-wave PWM control
- Automatic lead angle control (InPAC: Intelligent Phase Control)
- Lead angle control with external input
- Hall sensor input/Hall IC input
- Forward rotation/Reverse rotation switch
- Number of pulses of rotation pulse signal output is selectable.
- Output current can be limited.
- Built-in regulator circuit (VREF= 5 V (typ.), 35 mA (max))
- Operating supply voltage range: VCC = 6 V to 16.5 V
- Built-in motor lock detection

Block diagram

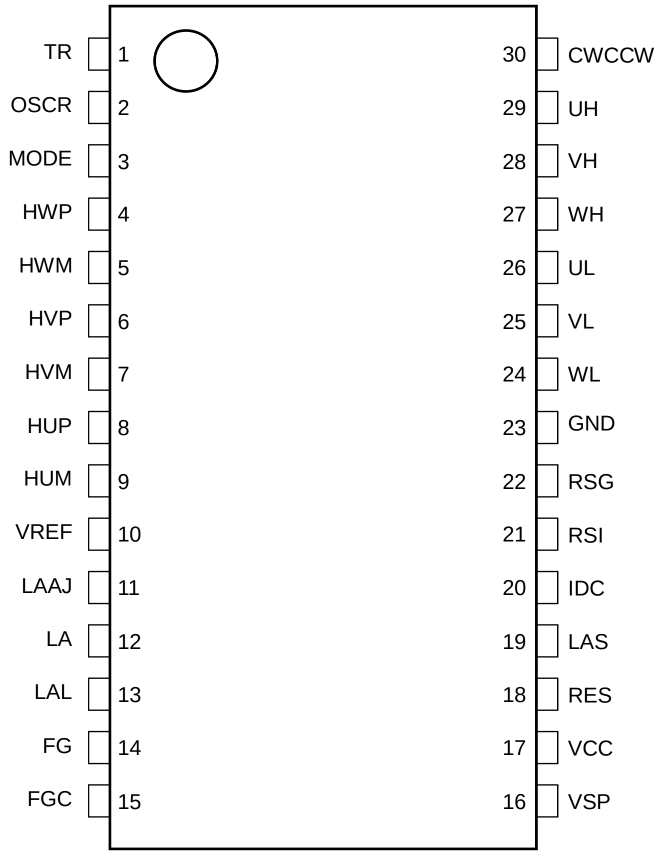


Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Note: RESX pin and VREF2 pin are only for the TC78B042FTG.

Pin assignment: TC78B041FNG (SSOP30)

<Top View>

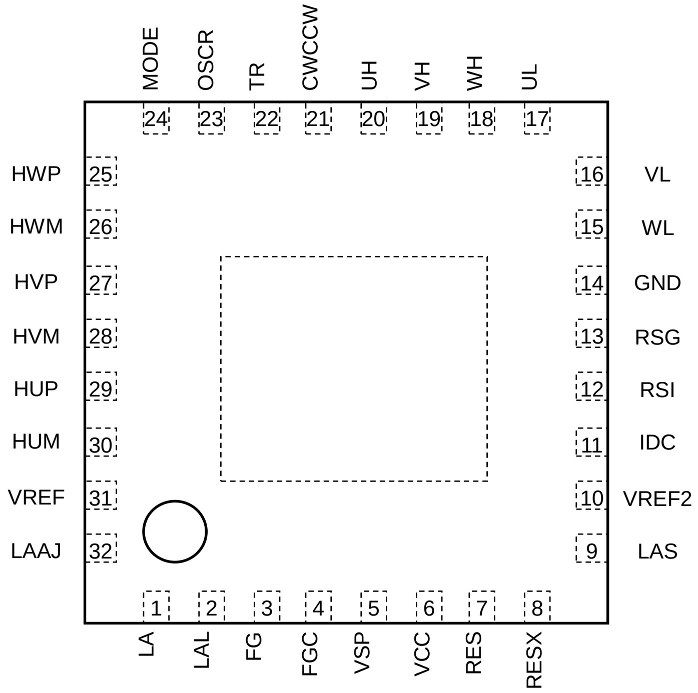


Pin description: TC78B041FNG (SSOP30)

Pin No.	Pin symbol	Description
1	TR	Setting motor lock detection
2	OSCR	Setting internal oscillation frequency
3	MODE	Input pin for selecting VSP setting
4	HWP	W-phase hall-signal input (+)
5	HWM	W-phase hall-signal input (-)
6	HVP	V-phase hall-signal input (+)
7	HVM	V-phase hall-signal input (-)
8	HUP	U-phase hall-signal input (+)
9	HUM	U-phase hall-signal input (-)
10	VREF	5V-reference voltage output pin
11	LAAJ	Input pin for adjusting auto lead angle
12	LA	Input pin for setting lead angle
13	LAL	Input pin for setting VSP lead angle limit
14	FG	Output pin for rotation pulse
15	FGC	Input pin for selecting FG pin setting
16	VSP	Input pin for rotation speed control voltage
17	VCC	Power supply voltage pin
18	RES	Input pin for error detection (positive)
19	LAS	Input pin for selection: Sine-wave generation, Lead angle function
20	IDC	Input pin for limiting output current
21	RSI	Input pin for detecting auto lead angle
22	RSG	Reference pin for detecting auto lead angle
23	GND	Ground pin
24	WL	W-phase output pin (low-side commutation signal)
25	VL	V-phase output pin (low-side commutation signal)
26	UL	U-phase output pin (low-side commutation signal)
27	WH	W-phase output pin (high-side commutation signal)
28	VH	V-phase output pin (high-side commutation signal)
29	UH	U-phase output pin (high-side commutation signal)
30	CWCCW	Input pin for controlling forward/reverse rotation

Pin assignment: TC78B042FTG (QFN32)

<Top View>



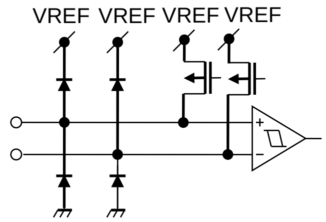
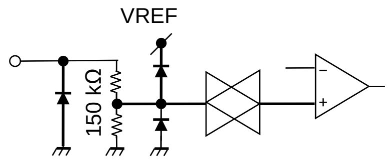
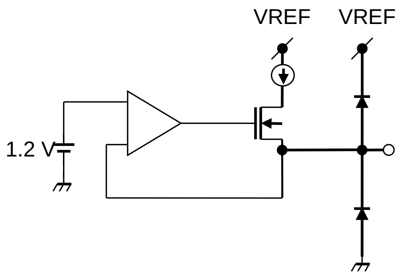
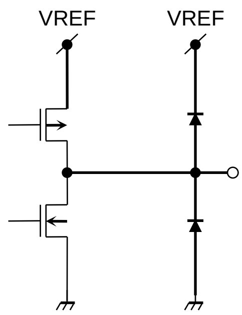
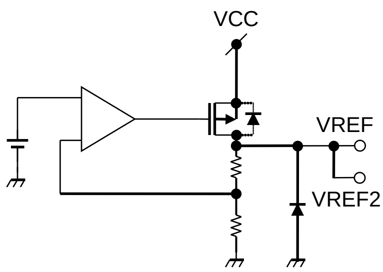
The exposed metal portion of the back side (E-PAD: size 3.3 mm×3.3 mm) should be connected to GND because it is connected to the back of the internal chip electrically.

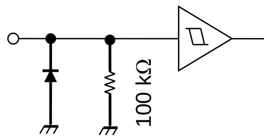
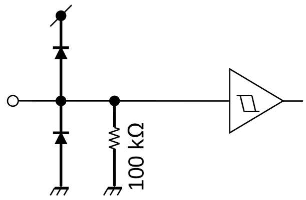
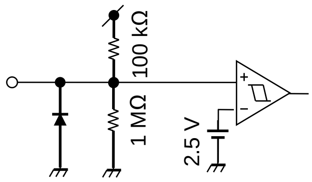
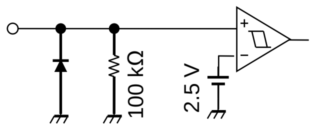
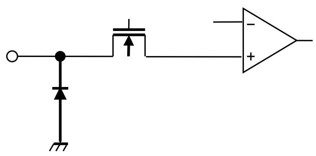
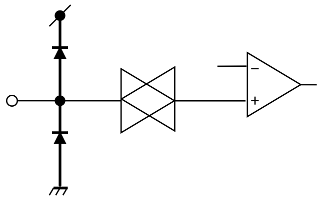
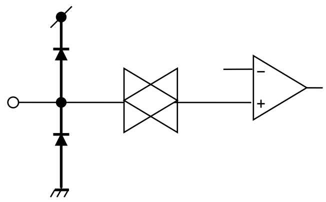
Pin description: TC78B042FTG (QFN32)

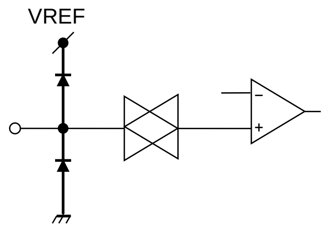
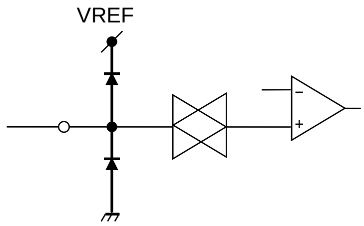
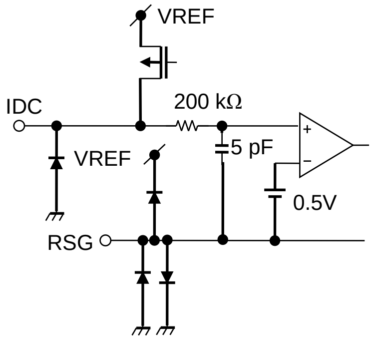
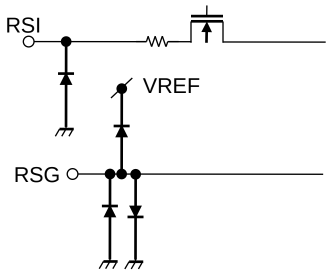
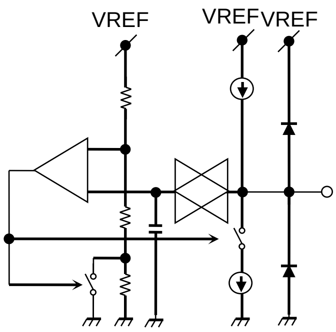
Pin No.	Pin symbol	Description
1	LA	Input pin for setting lead angle
2	LAL	Input pin for setting VSP lead angle limit
3	FG	Output pin for rotation pulse
4	FGC	Input pin for selecting FG pin setting
5	VSP	Input pin for rotation speed control voltage
6	VCC	Power supply voltage pin
7	RES	Input pin for error detection (positive)
8	RESX	Input pin for error detection (negative)
9	LAS	Input pin for selection: Sine-wave generation, Lead angle function
10	VREF2	5V-reference voltage output pin 2
11	IDC	Input pin for limiting output current
12	RSI	Input pin for detecting auto lead angle
13	RSG	Reference pin for detecting auto lead angle
14	GND	Ground pin
15	WL	W-phase output pin (low-side commutation signal)
16	VL	V-phase output pin (low-side commutation signal)
17	UL	U-phase output pin (low-side commutation signal)
18	WH	W-phase output pin (high-side commutation signal)
19	VH	V-phase output pin (high-side commutation signal)
20	UH	U-phase output pin (high-side commutation signal)
21	CWCCW	Input pin for controlling forward/reverse rotation
22	TR	Setting motor lock detection
23	OSCR	Setting internal oscillation frequency
24	MODE	Input pin for selecting VSP setting
25	HWP	W-phase hall-signal input (+)
26	HWM	W-phase hall-signal input (-)
27	HVP	V-phase hall-signal input (+)
28	HVM	V-phase hall-signal input (-)
29	HUP	U-phase hall-signal input (+)
30	HUM	U-phase hall-signal input (-)
31	VREF	5V-reference voltage output pin
32	LAAJ	Input pin for adjusting auto lead angle

I/O Equivalent circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin description	Pin symbol	I/O signal	I/O internal circuit
Hall signal input	HUP HUM HVP HVM HWP HWM	Digital filter 18/fosc = 2 μs (typ.)	
Speed control voltage input	VSP	Analog voltage input Input range: 0 V to 10 V	
Internal oscillation frequency setting	OSCR	Connecting to resistor for setting internal oscillation frequency When R = 22 kΩ, fosc = 9.22 MHz (typ.)	
Commutation signal output Rotation pulse output	UH VH WH UL VL WL FG	Push-pull output (± 2 mA (max))	
5V-reference voltage output 5V-reference voltage output 2	VREF VREF2 (Note)	VREF: 5 V (typ.) (35 mA (max)) VREF2: 5 V (typ.) (3 mA (max))	

Pin description	Pin symbol	I/O signal	I/O internal circuit
Forward/Reverse control input	CWCCW	Digital filter 18/fosc = 2 μs (typ.) H: Reverse (CCW) L/Open: Forward (CW)	
VSP setting select input	MODE	Digital filter 18/fosc = 2μs (typ.) H: VSP input (B mode) L/Open: VSP input (A mode)	
Error detection positive input	RES	Digital filter 18/fosc=2μs (typ.) H/Open: Operation L: Stop (commutation signal output: Low))	
Error detection negative input	RESX (Note)	Digital filter 18/fosc = 2 μs (typ.) H: Stop (commutation signal output: Low) L/OPEN: Operation	
Select input for FG pin setting	FGC	10-level select input Be sure to input voltage in using.	
Lead angle setting input	LA	32-level select input Be sure to input voltage in using.	
Select input: sine-wave generation and lead angle function	LAS	4-level select input Be sure to input voltage in using.	

Pin description	Pin symbol	I/O signal	I/O internal circuit
VSP lead angle limiting input	LAL	16-level select input Be sure to input voltage in using.	
Automatic lead angle adjusting input	LAAJ	64-level select input Be sure to input voltage in using.	
Output current limiting input	IDC	Digital filter 18/fosc = 2 μs (typ.)	
Automatic lead angle detecting input Automatic lead angle detecting for reference	RSI RSG	When using auto lead angle function, connect shunt resistor between RSI and RSG. When auto lead angle function is not used, connect RSI and RSG to GND.	
Motor lock detection setting	TR	Connecting capacitor for motor lock detection	

Note: RESX pin and VREF2 pin are only for the TC78B042FTG.

Absolute maximum ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Power supply voltage	MVCC	18	V	VCC
Input voltage	MVIN1	- 0.3 to 18	V	VSP
	MVIN2	- 0.3 to VREF+ 0.3	V	HUP, HVP, HWP, HUM, HVM, HWM, TR, OSCR, FGC, LA, LAS, LAL, MODE, LAAJ, RES
	MVIN3	- 0.3 to 6	V	RESX, CWCCW
	MVIN4	VREF+ 0.3	V	IDC, RSI
Output voltage	MVout1	6	V	VREF, VREF2
	MVout2	- 0.3 to VREF+ 0.3	V	FG, UH, VH, WH, UL, VL, WL
Output current	MIOUT	2	mA	FG, UH, VH, WH, UL,VL, WL
VREF output current	MI_{refout}	35	mA	VREF (VREF+VREF2)(Note) (VREF2 output current is also included.)
VREF2 output current	$MI_{refout}2$	3	mA	VREF2 (Note)
Power dissipation	P_D1	1.87	W	TC78B041FNG (SSOP30) When mounted on JEDEC 4-layer board
	P_D2	4.25	W	TC78B042FTG (QFN32) When mounted on JEDEC 4-layer board
Operating temperature	T_{opr}	- 40 to 115	°C	Operating temperature range is determined according to the characteristics of power dissipation. The maximum junction temperature should not exceed Tj (max) (150°C).
Storage temperature	T_{opr}	- 55 to 150	°C	—

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

Do not exceed any of these ratings. Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

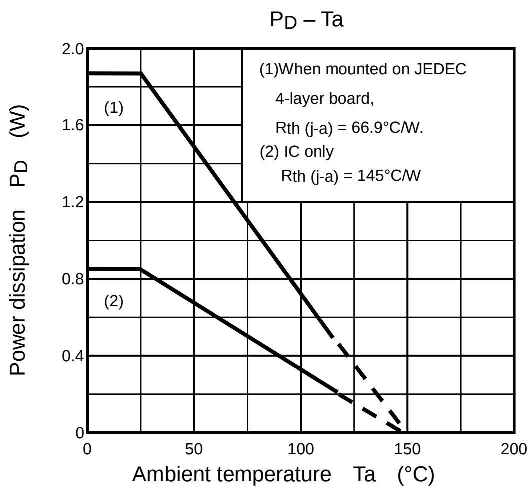
Please use the IC within the specified operating ranges.

Note: VREF2 pin is only for the TC78B042FTG.

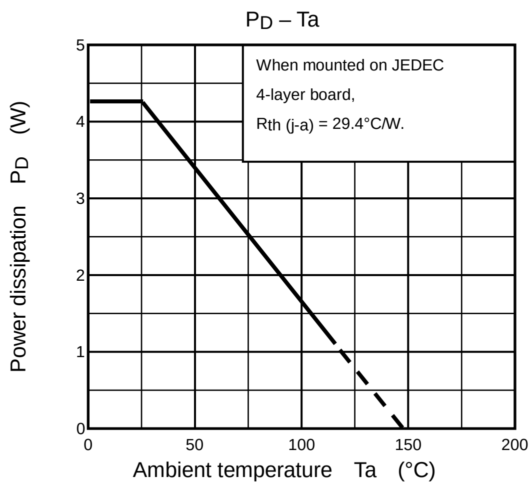
Operating ranges (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Power supply voltage	VCCopr	6	15	16.5	V	VCC
Oscillation frequency	fOSCopr	6.8	9.22	15.5	MHz	—
Speed control voltage input	VSPopr	0	—	7.3	V	VSP: Normal control
	VSPoprT	8.2	—	10	V	VSP: Test mode

Power dissipation (for reference only)



TC78B041FNG (SSOP30)



TC78B042FTG (QFN32)

Electrical characteristics (Unless otherwise specified, Ta = 25°C and VCC = 15 V)

Characteristics		Symbol		Test Condition	Min	Typ.	Max	Unit
Supply current		ICC		VREF = OPEN	2	5	8	mA
Input current		IIN1		VIN = 5 V:CWCCW, MODE, RESX	25	50	100	μA
		IIN2		VIN = 0 V:FGC, LA, LAS, LAL, LAAJ	-1	0	1	
		IIN3		VIN = 5 V:VSP	17	33	70	
		IIN4		VIN = 0 V:RES	-100	-50	-25	
		IIN5		VIN = 5 V:RES	-2	5	10	
Input voltage		VIN1	H	CWCCW, MODE	2	—	—	V
			L	CWCCW, MODE	0	—	0.8	
			Hys	CWCCW, MODE (Reference value)	—	±0.1	—	
		VIN2	HVTH	RES, RESX	—	2.6	2.7	V
			LVTH	RES, RESX	2.3	2.4	—	
			Hys	RES, RESX (Reference value)	—	±0.1	—	
		VSPA	T	PWM Max, ON duty → Test mode	7.3	7.75	8.2	V
			H	Motor operation → PWM Max, ON duty	5.1	5.4	5.7	
			M	Refresh → Output Duty operation start	1.8	2.1	2.4	
			L	Commutation OFF → Refresh	0.7	1.0	1.3	
		VSPB	T	PWM Max, ON duty → Test mode	7.3	7.75	8.2	V
			H	Motor operation → PWM Max, ON duty	4.7	5	5.3	
			M	Refresh → Output Duty operation start	0.1	0.2	0.3	
AD input voltage STEP width		VAD4		LAS (Reference value)	1.125	1.25	1.325	V
		VAD16		LAL, FGC (Reference value)	0.281	0.313	0.331	V
		VAD32		LA (Reference value)	0.141	0.156	0.166	V
		VAD64		LAAJ (Reference value)	0.070	0.078	0.083	V
Hall sensor inputs	Input sensitivity	VS		Differential inputs	40	—	—	mVpp
	Common-mode input voltage	VW		—	0.2	—	3.5	V
	Input hysteresis	VHhys		(Reference value)	±1.5	±7.5	±13.5	mV
Hall IC input		VHIN	H	HUP, HVP, HWP: HUM, HVM, HWM = VREF/2	VREF - 1	—	VREF	V
			L		0	—	0.8	
Input delay time		Thallr		HUP, HVP, HWP = Hall IC input, HUM, HVM, HWM = VREF/2, OSCR = 22 kΩ UH, VH, WH, UL, VL, WL, FG: Rising (Reference value)	—	4	—	μs
		Thalf		HUP, HVP, HWP = Hall IC input, HUM, HVM, HWM = VREF/2, OSCR = 22 kΩ UH, VH, WH, UL, VL, WL, FG: Falling (Reference value)	—	2	—	μs
Output voltage		VOUTH		IOUT = -2 mA: UH, VH, WH, UL, VL, WL, FG	VREF - 0.78	VREF - 0.3	—	V
		VOUTL		IOUT = 2 mA: UH, VH, WH, UL, VL, WL, FG	—	0.3	0.78	
		VREFA		VREF = 0 mA: VREF, (VREF2 = OPEN) (Note1)	4.7	5.0	5.3	
		VREFB		VREF = -15 mA: VREF, (VREF2 = OPEN) (Note1)	4.7	5.0	5.3	
		VREFC		VREF = -35 mA: VREF, (VREF2 = OPEN) (Note1)	4.5	5.0	5.3	
		VREF2A		VREF2 = 0 mA: VREF2, (VREF = OPEN) (Note1)	4.7	5.0	5.3	
		VREF2B		VREF2 = -3 mA: VREF2, (VREF = -12 mA) (Note1)	4.7	5.0	5.3	
		VREF2C		VREF2 = -3 mA: VREF2, (VREF = -32 mA) (Note1)	4.5	5.0	5.3	
Output leakage current		ILH		VOUT = 0 V: UH, VH, WH, UL, VL, WL, FG	—	0	1	μA
		ILL		VOUT = 5 V: UH, VH, WH, UL, VL, WL, FG	—	0	1	

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output OFF time (Dead time)	VOFF(18)	OSCR = 22 kΩ IOUT = 2 mA (Reference value)	1.7	2	2.3	μs
	VOFF(20)	OSCR = 20 kΩ IOUT = 2 mA (Reference value)	1.5	1.79	2.07	μs
Oscillation frequency	fosc(18)	OSCR = 22 kΩ (Reference value)	8.29	9.22	10.14	MHz
	fosc(20)	OSCR = 20 kΩ (Reference value)	9.06	10.06	11.08	MHz
PWM oscillation frequency (Carrier frequency)	FC(18)	OSCR = 22 kΩ (Reference value)	16.2	18	19.8	kHz
	FC(20)	OSCR = 20 kΩ (Reference value)	17.7	19.6	21.7	kHz
Maximum conduction duty width (Sine wave)	TON180MAX	(Reference value)	(Note2)	96.3	(Note2)	%
Maximum conduction duty width (120° commutation)	TON120MAX	(Reference value)	(Note2)	85	(Note2)	%
Minimum conduction duty width	TONMIN	(Reference value)	—	0.2	—	%
Output current limiting voltage	VIDC	IDC	0.48	0.5	0.52	V
Input delay of current detection	TIDC	IDC OSCR = 22 kΩ (Reference value)	—	3.2	—	μs
VCC monitor	VCC(H)	Output turn-on threshold	5.0	5.5	5.9	V
	VCC(L)	Output turn-off threshold	4.5	5	5.5	
	VCC(H)	Input voltage hysteresis (Reference value)	—	0.5	—	
VREF monitor	VREF(H)	Output turn-on threshold	3.7	4	4.3	V
	VREF(L)	Output turn-off threshold	3.4	3.7	4	
	VREF(H)	Input voltage hysteresis (Reference value)	—	0.3	—	
Motor lock detection	TONTR	TR = 0.01 μF Operation period (Reference value)	3.7	5	7.4	s
	TOFFTR	TR = 0.01 μF Output disabled period (Reference value)	22.2	30	44.4	s
	FTR	TR = 0.01 μF frequency	68	100	132	Hz
	ICTR	Charge current (Reference value)	2	3	4	μA
	IDTR	Discharge current (Reference value)	-4	-3	-2	μA
	VHTR	High-side threshold (Reference value)	2.7	3	3.3	V
	VLTR	Low-side threshold (Reference value)	1.35	1.5	1.65	V
Current detection accuracy of auto lead angle	VRS	(Reference value)	-1	0	1	mV

Reference value: Design values. No shipping inspection.
Note1: VREF2 pin is only for the TC78B042FTG.
Note2: Since the output Duty is controlled by the logic circuit, the maximum and minimum values of the maximum conduct duty width are the same with typical values, and these values are design values. However, the values may be different from the typical values due to a delay of the load capacity, etc.

Functional description

1. Basic operation

At startup, the motor is driven with 120° commutation. When the hall signal indicates a rotation speed (f) of 1 Hz or more, the motor rotates by estimating the rotor position. (Note)

0 (Startup) ≤ f < 1 Hz: Square-wave drive (120° commutation)
1Hz ≤ f: Sine-wave PWM drive (180° commutation)

Note: When oscillation frequency (fosc) is 9.22 MHz, the switching period from the hall signal to the following one is about 0.167 s. Then, the frequency for one cycle is about 1 Hz ((6×1536000)/fosc).
When f is 1 Hz or more, the motor is driven according to the command of the LA pin.
When f is less than 1Hz or the motor rotation direction is reverse (according to the timing chart), the motor is driven with 120° commutation (lead angle is 0°).

2. Reference clock and carrier frequency setting

Reference clock (oscillation frequency: fosc) is determined by the resistance (R) of the OSCR pin. It configures PWM frequency (carrier frequency). The calculating formula is shown below. When the resistance (R) of the OSCR pin is 22 kΩ, oscillation frequency is 9.22 MHz (typ.) and carrier frequency is 18 kHz (typ.).

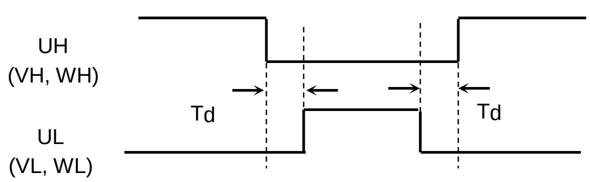
Carrier frequency: F_C = fosc /512 (Hz)

OSCR pin resistor value ［kΩ］	Reference clock fosc[MHz] (typ.)	PWM frequency (carrier frequency) Fc［kHz］ (typ.)
27	7.62	14.9
24	8.5	16.6
22	9.22	18
20	10.06	19.6
18	11.08	21.6
16	12.33	24.1
15	13.07	25.5

3. Dead time insertion (cross conduction protection)

To prevent a short-circuit between external low-side and high-side power devices during sine-wave PWM drive, a dead time is digitally inserted. (The dead time is also implemented at the full duty cycle during square-wave drive.)

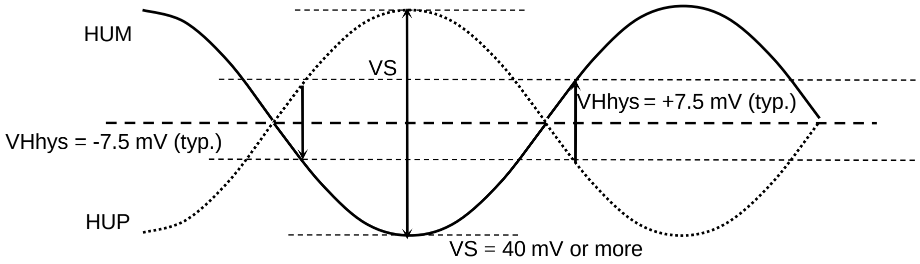
T_d = 18/fosc
Td ≈ 2 μs when fosc ≈ 9.22 MHz, where fosc is reference clock frequency (Oscillation frequency).



4. Hall signal

<Hall sensor input>

Common-mode input voltage range: VW = 0.2 V to 3.5 V
Input hysteresis: VHhys = 7.5 mV (typ.)



<Hall IC input>

Usage setting example 1: HUP, HVP, HWP =GND to VREF: HUM, HVM, HWM=VREF/ 2
Usage setting example 2: HUP, HVP, HWP =VREF/ 2: HUM, HVM, HWM=GND to VREF

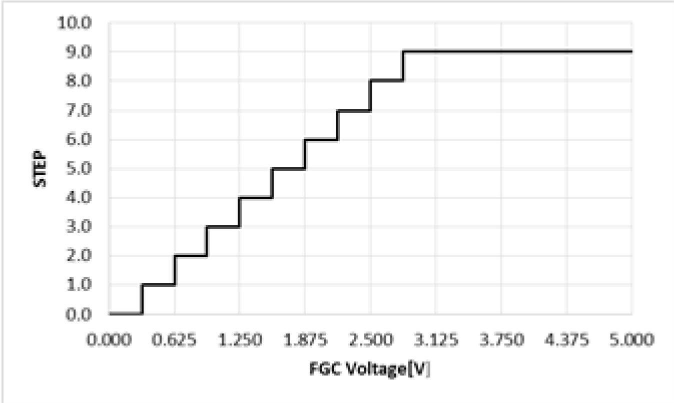
5. Rotation pulse output

The IC outputs rotating pulse based on the hall signal. FGC pin can switch number of pulses. One pulse per electrical angle is generated from the hall signal of U phase. 3 pulses per electrical angle are generated by combining each rising and falling edge of U, V, and W phases.

2.4 or 2 or 0.8 pulses per electrical angle are generated by rotating the motor with 1.5 electrical angle under the condition that the frequency of the hall signal (U phase) is about 0.68 Hz or higher (condition: fosc = 9.22 MHz). They are not generated when f is less than 0.68 Hz. Since the pulses are not generated synchronous with hall signal switching edge, each phase of hall signal cannot be judged by FG signal.

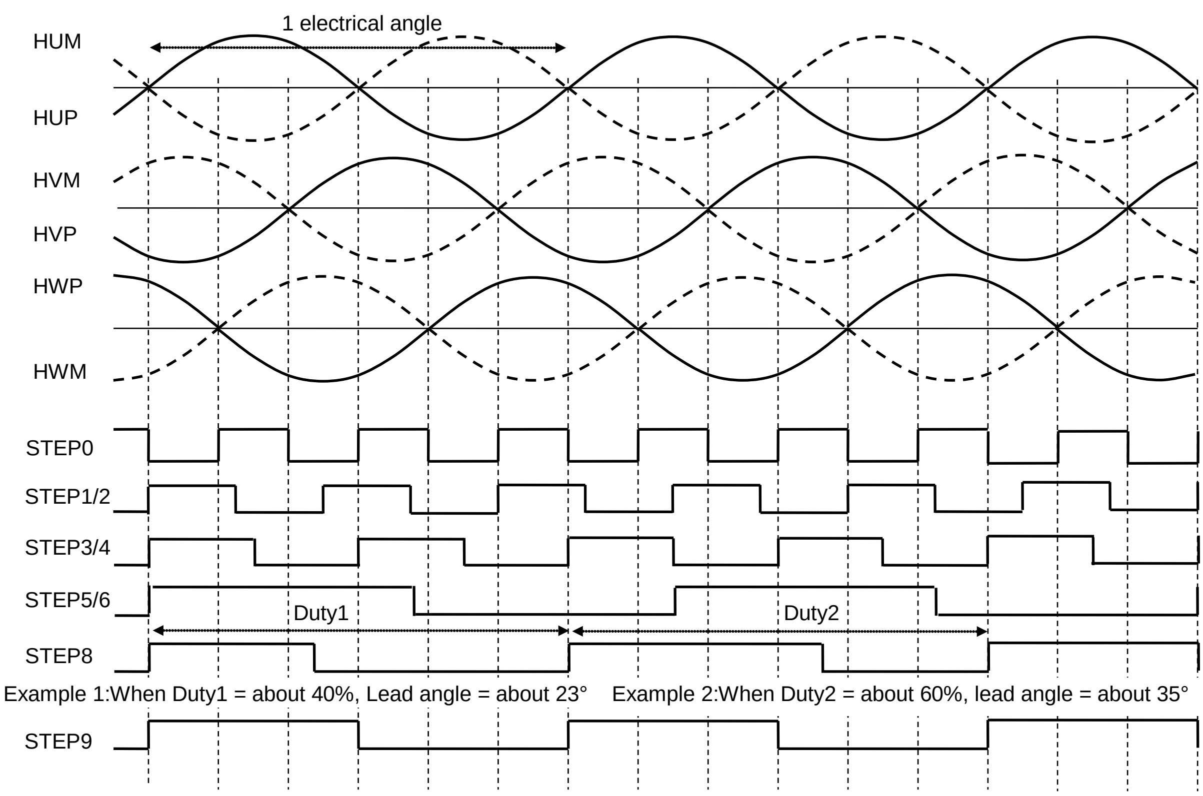
In STEP8, output timing of commutation signal is enabled. Approximate lead angle can be calculated as follows; Lead angle (°) = (0.6×Duty (%))−0.94.

STEP	FGC[V] (Note)	FG
0	0.00	3 pulses/electrical angle
1	0.31	2.4 pulses/electrical angle
2	0.63	
3	0.94	2 pulses/electrical angle
4	1.25	
5	1.56	0.8 pulses/electrical angle
6	1.88	
7	2.19	Test mode 1
8	2.50	Test mode 2: Lead angle timing
9	2.81	1 pulse/electrical angle



Note: The threshold voltage of the FGC pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

<Timing chart of FG signal>



Note: Above timing chart is an example and simplified for explanatory purposes. The 2.4, 2, and 0.8 pulses or electrical angle may not be synchronized with hall signals.

6. Setting rotation speed control

By changing the input voltage of VSP pin, duty of the commutation signal output is changed and the motor rotation speed can be controlled.
Input mode of VSP pin can be selected between A and B by using MODE pin.

MODE pin	Input type of VSP pin
High	B mode
Low/OPEN	A mode

<VSP pin input: A mode, MODE pin: Low/Open>

(1) Voltage command input: $V_{SP} \leq 1.0$ V
The commutation signal outputs are disabled (i.e., gate block protection is activated).

(2) Voltage command input: 1.0 V < $V_{SP} \leq 2.1$ V (Refresh)
The low-side commutation signal is turned on for a constant period (carrier period). ON duty: about 8% (40/fosc)

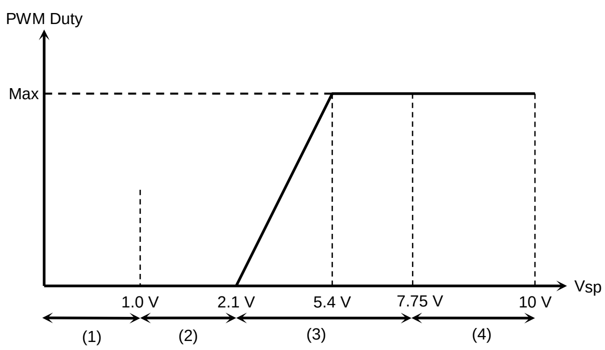
(3) Voltage command input: 2.1 V < $V_{SP} \leq$ 7.75 V
Output ON duty is changed by setting 256-resolution. When V_{SP} is 5.4 V (typ.) or more, output ON duty keeps the maximum value.
During square-wave drive, the low-side commutation signal is turned on forcedly for a constant period (carrier period). ON duty: about 8% (40/fosc)

In stop mode (Rotation frequency < 1 Hz when fosc=9.22 MHz), the commutation signal is output after V_{SP} exceeds 2.1 V and the refresh mode is activated for 1.5 ms (condition: fosc=9.22 MHz). In rotation mode (Rotation frequency ≥ 1 Hz when fosc=9.22 MHz), the commutation signal is output immediately after V_{SP} exceeds 2.1 V.

Note: In startup, low-side commutation signal should be turned on (1.0 V < $V_{SP} \leq 2.1$ V) for a certain period to charge the high-side gate power supply.

(4) Voltage command input: 7.75 V < $V_{SP} \leq$ 10 V (test mode for motor shipping)
In sine-wave drive mode, the motor rotates with lead angle of zero.
Output ON duty keeps the maximum value.

Note: In the test mode for motor shipment, even if the setting of the sine wave generation method is the sine-wave 360° reset with the LAS pin, the setting is the sine-wave 60° reset



Note: The threshold voltage in each state of the VSP pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

<VSP pin input: B mode, MODE pin: High>

(1) Voltage command input: $V_{SP} \le 0.2$ V (Refresh)

The low-side commutation signal is turned on for a constant period (carrier period). ON duty: about 8% (40/fosc)

(2) Voltage command input: $0.2\text{ V} < V_{SP} \le 7.75$ V

Output ON duty is changed by setting 256-resolution. When V_{SP} is 5 V (typ.) or more, output ON duty keeps the maximum value.

During square-wave drive, the low-side commutation signal is turned on forcedly for a constant period (carrier period). ON duty: about 8% (40/fosc)

In stop mode (Rotation frequency < 1 Hz when fosc=9.22 MHz), the commutation signal is output after V_{SP} exceeds 0.2 V and the refresh mode is activated for 1.5 ms (condition: fosc=9.22 MHz). In rotation mode (Rotation frequency ≥ 1 Hz when fosc=9.22 MHz), the commutation signal is output immediately after V_{SP} exceeds 0.2 V.

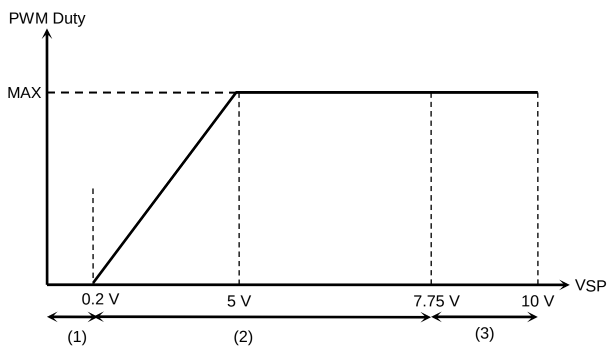
Note: In startup, low-side commutation signal should be turned on ($0.2\text{ V} < V_{SP}$) for a certain period to charge the high-side gate power supply.

(3) Voltage command input: $7.75\text{ V} < V_{SP} \le 10$ V (test mode for motor shipping)

In sine-wave drive mode, the motor rotates with lead angle of zero.

Output ON duty keeps the maximum value.

Note: In the test mode for motor shipment, even if the setting of the sine wave generation method is the sine-wave 360° reset with the LAS pin, the setting is the sine-wave 60° reset.



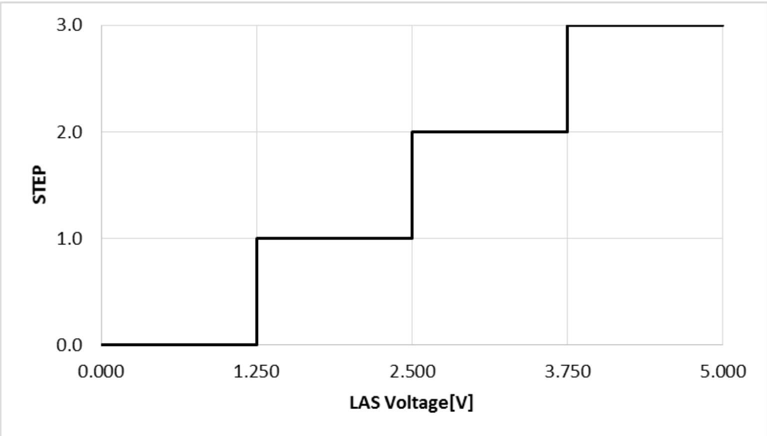
Note: The threshold voltage in each state of the VSP pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

7. Setting lead angle function and sine-wave generation

LAS pin can set sine-wave generation and lead angle function. Details are shown below.

STEP	LAS voltage [V] (Note)	Sine-wave generation	Lead angle function	LA pin setting
0	0	Sine-wave (60°) reset	Automatic (InPAC: Intelligent Phase Control)	Lead angle upper limit setting of the current limiting lead angle 0° to 58° / 32 steps
1	1.25	Sine-wave (360°) reset	Automatic (InPAC: Intelligent Phase Control)	Lead angle upper limit setting of the current limiting lead angle 0° to 58° / 32 steps
2	2.5	Sine-wave (360°) reset	External input	Set phase of commutation signal output: 0° to 58° / 32 steps
3	3.75	Sine-wave (60°) reset	External input	Set phase of commutation signal output: 0° to 58° / 32 steps

Note: The threshold voltage of the LAS pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

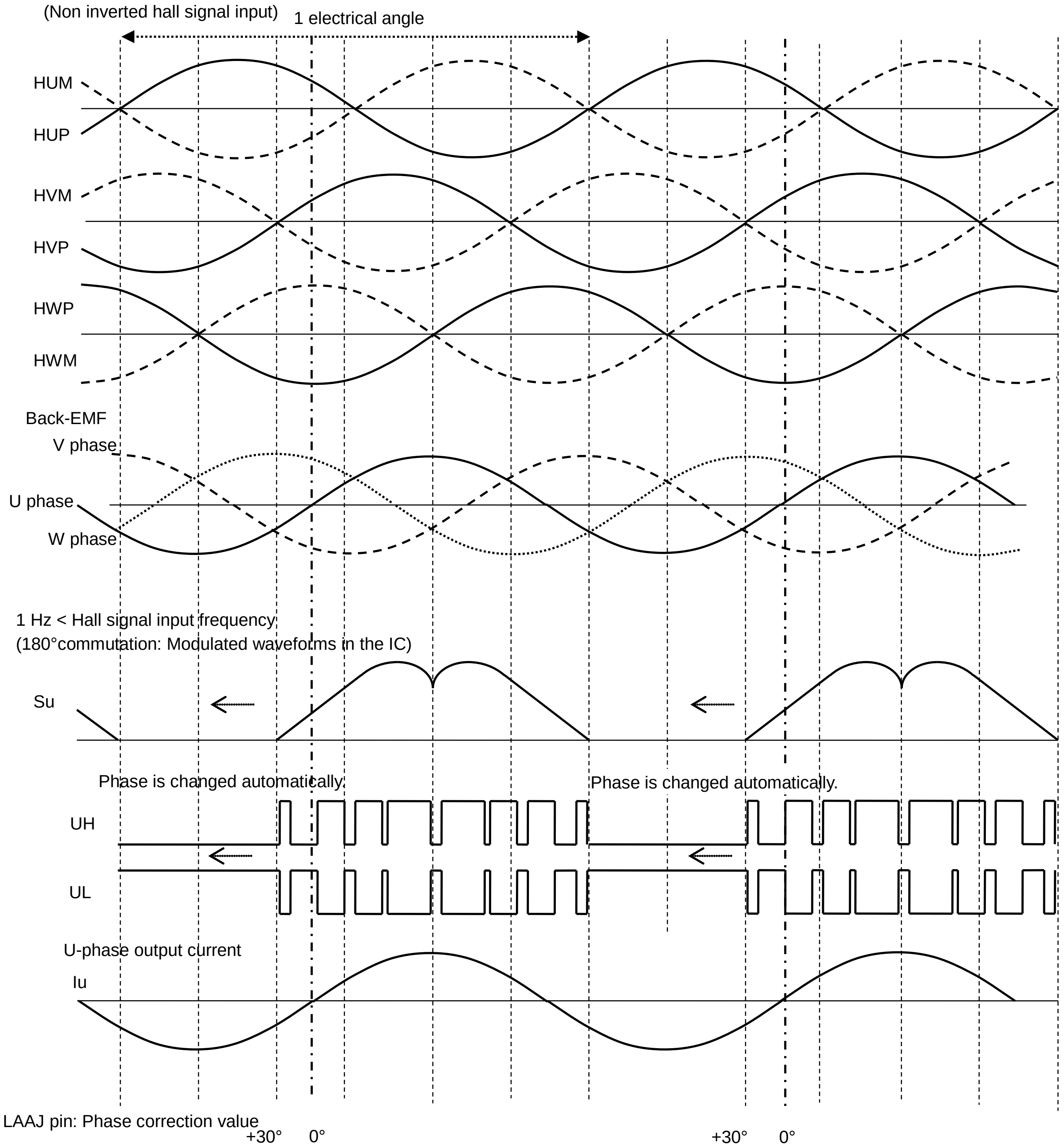


<Lead angle function>

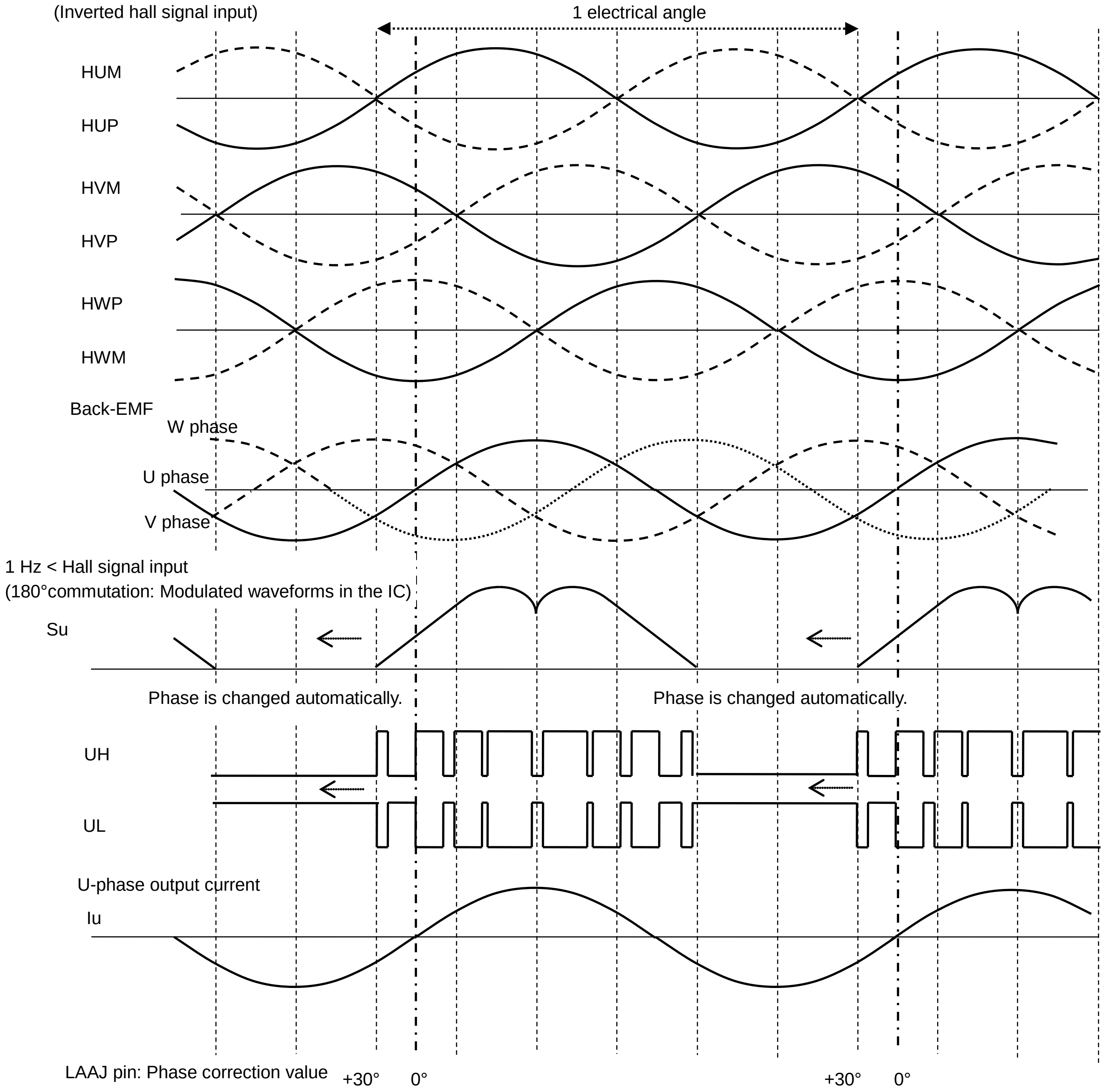
(1) Automatic lead angle control function (InPAC: Intelligent Phase Control)

The auto lead angle control function corrects based on the input signal of hall signal so that zero-cross point of U-phase output current is 0° position in the following timing chart. It detects an output current at the position of 0° in the timing chart, and the phase is judged once per one electrical angle, whether the lead angle or delay angle. When the result judged 4 times continuously is matched, it changes the phase (range: 0° to 58°) of a commutation signal output for each step (0.94°), and corrects the zero crossing position of output current. If the result is not matched, the phase of commutation signal does not change.
Additionally, the auto lead angle control function corrects the zero-cross point of U-phase output current to 0° position of the timing chart when the phase relation between U phase hole signal and U phase Back-EMF is the following timing chart. Therefore, motor driving efficiency is optimized when zero-cross point of U-phase Back-EMF and U-phase output current are corresponded. However, in case that the fixing position of the hall sensor (i.e. hall IC) is slipped off, the zero-cross point of the output current can be corrected by controlling LA voltage. Since zero-cross point of the output current is detected by RSI and RSG pins through shunt resistor, connection of RSI pin and RSG pin via the shunt resistor is required to apply auto lead angle function.
Moreover, rotation speed (i.e. one electrical angular frequency of hall signal) that enables normal auto lead angle control has a limit (Finpac). The limit value (Finpac) is determined according to PWM frequency (carrier frequency) and phase correction value. It can be calculated by the formula of 'Finpac=PWM frequency×{(30+phase)/540}'. When the rotation speed exceeds this limit value, auto lead angle function may not work.
Example: In case of PWM frequency = 16.2 kHz, phase (LAAJ pin function) = 0° setting, Finpac = 900 Hz.

<Timing chart of auto lead angle (CWCCW=Low)>



<Timing chart of auto lead angle (CWCCW=High)>



<Lead angle upper limit value setting of current limiting lead angle of LA pin during auto lead angle control setting (InPAC)>

In the auto lead angle setting (InPAC), when the current limiting (IDC pin function) works at the zero-cross detecting point of output current and does not judge the auto lead angle (InPAC) phase, the current limiting lead angle (IDC lead angle) advances the lead angle. The LA pin is set to the upper limit value of current limiting lead angle (IDC lead angle).

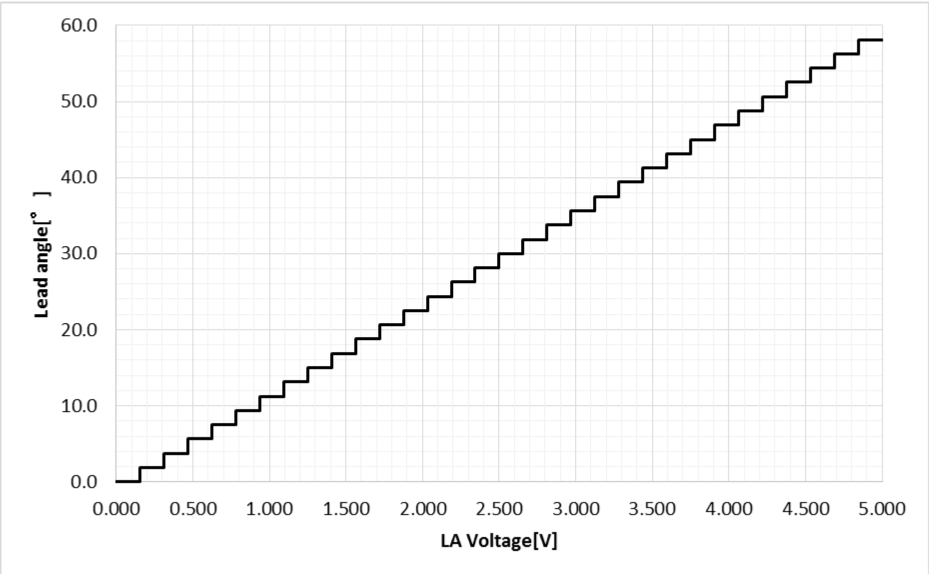
In the auto lead angle setting (InPAC), when the current limiting (IDC pin function) works at zero-cross detecting point of output current, the phase judgement cannot be performed and the auto lead angle control (InPAC) cannot work. However, in this case, the lead angle can be advanced by the current limiting lead angle function (IDC lead angle). Whenever the state where the auto lead angle (InPAC) cannot perform a phase judgement by the current limiting counts 4 times, the lead angle of 1 step (0.94°) is advanced. The lead angle counts by the auto lead angle control (InPAC) are reset when the auto lead angle control (InPAC) does not perform the phase judgement by current limiting.

The LA pin can set the upper limit value of current limiting lead angle not to advance too much the lead angle by this current limiting lead angle function.

The upper limit setting of the LA pin lead angle is only for the setting of this current limiting lead angle function (IDC lead angle), so that normal auto lead function setting (InPAC) cannot be set this limit value arbitrary. The upper limit value is 58.1°.

STEP	LA voltage [V] (Note)	Lead angle [°]	STEP	LA voltage [V] (Note)	Lead angle [°]
0	0.00	0.0	16	2.50	30.0
1	0.16	1.9	17	2.66	31.9
2	0.31	3.8	18	2.81	33.8
3	0.47	5.6	19	2.97	35.6
4	0.63	7.5	20	3.13	37.5
5	0.78	9.4	21	3.28	39.4
6	0.94	11.3	22	3.44	41.3
7	1.09	13.1	23	3.59	43.1
8	1.25	15.0	24	3.75	45.0
9	1.41	16.9	25	3.91	46.9
10	1.56	18.8	26	4.06	48.8
11	1.72	20.6	27	4.22	50.6
12	1.88	22.5	28	4.38	52.5
13	2.03	24.4	29	4.53	54.4
14	2.19	26.3	30	4.69	56.3
15	2.34	28.1	31	4.84	58.1

Note: The threshold voltage of the LA pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

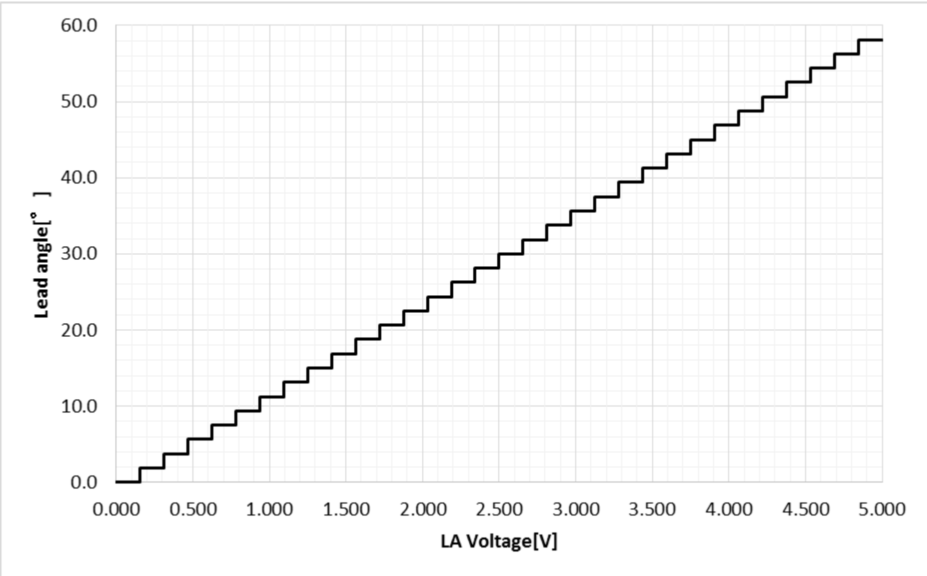


(2) Lead angle set by external input

Lead angle of commutation signal output against hall signal can be fixed by LA input voltage.

STEP	LA voltage [V] (Note)	Lead angle [°]	STEP	LA voltage [V] (Note)	Lead angle [°]
0	0.00	0.0	16	2.50	30.0
1	0.16	1.9	17	2.66	31.9
2	0.31	3.8	18	2.81	33.8
3	0.47	5.6	19	2.97	35.6
4	0.63	7.5	20	3.13	37.5
5	0.78	9.4	21	3.28	39.4
6	0.94	11.3	22	3.44	41.3
7	1.09	13.1	23	3.59	43.1
8	1.25	15.0	24	3.75	45.0
9	1.41	16.9	25	3.91	46.9
10	1.56	18.8	26	4.06	48.8
11	1.72	20.6	27	4.22	50.6
12	1.88	22.5	28	4.38	52.5
13	2.03	24.4	29	4.53	54.4
14	2.19	26.3	30	4.69	56.3
15	2.34	28.1	31	4.84	58.1

Note: The threshold voltage of the LA pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.

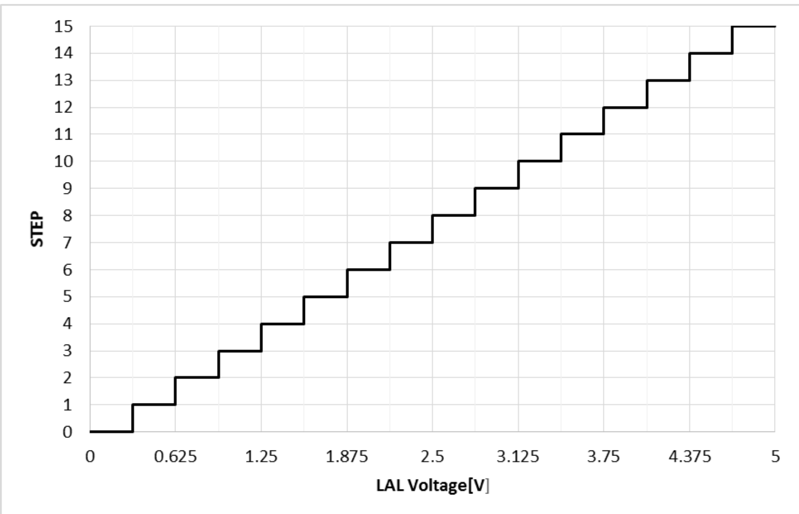


Lead angle limit function (LAL pin setting)

When VSP input voltage is too low to provide enough output current, zero-cross point of output current cannot be detected accurately and auto lead angle function may not work properly because this function is activated by detecting zero-cross point of the output current. In this case, lead angle limit function is applied. In the auto lead angle function setting, when the input voltage (input Duty) of the VSP pin in the following LAL pin setting is less than the setting value, the auto lead angle limiting function is fixed angle of the LAL pin setting without working. As the fixed lead angle value is an initial value, a sine wave of the lead angle value also starts from this fixed lead angle value when changing from a rectangle wave to a sine wave. When the VSP pin voltage exceeds the configured voltage, the auto lead angle control function works and changes from the fixed lead angle to a suitable lead angle by 1 step (0.94°). Moreover, in external input setting, auto lead angle function using LAL pin is not enabled.

<table>
<tr><th rowspan="2">STEP</th><th rowspan="2">LAL voltage [V] (Note)</th><th rowspan="2">Fixed lead angle [°] (Initial value)</th><th colspan="2">VSP voltage [V] / A mode (Note) (VSP input: conversed to duty)</th><th colspan="2">VSP voltage [V] / B mode (Note) (VSP input: conversed to duty)</th></tr>
<tr><th>Hysteresis VSP increase side</th><th>Hysteresis VSP decrease side</th><th>Hysteresis VSP increase side</th><th>Hysteresis VSP decrease side</th></tr>
<tr><td>0</td><td>0.00</td><td>No limit (0°)</td><td>—</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>1</td><td>0.31</td><td>5.6</td><td rowspan="2">2.49 V or less (12% or less)</td><td rowspan="2">2.43 V or less (10% or less)</td><td rowspan="2">0.77 V or less (12% or less)</td><td rowspan="2">0.68 V or less (10% or less)</td></tr>
<tr><td>2</td><td>0.63</td><td>0</td></tr>
<tr><td>3</td><td>0.94</td><td>11.3</td><td rowspan="3">2.66 V or less (17% or less)</td><td rowspan="3">2.60 V or less (15% or less)</td><td rowspan="3">1.01 V or less (17% or less)</td><td rowspan="3">0.92 V or less (15% or less)</td></tr>
<tr><td>4</td><td>1.25</td><td>5.6</td></tr>
<tr><td>5</td><td>1.56</td><td>0</td></tr>
<tr><td>6</td><td>1.88</td><td>12.2</td><td rowspan="3">2.83 V or less (22% or less)</td><td rowspan="3">2.76 V or less (20% or less)</td><td rowspan="3">1.27 V or less (22% or less)</td><td rowspan="3">1.17 V or less (20% or less)</td></tr>
<tr><td>7</td><td>2.19</td><td>6.6</td></tr>
<tr><td>8</td><td>2.50</td><td>0</td></tr>
<tr><td>9</td><td>2.81</td><td>13.1</td><td rowspan="3">2.99 V or less (27% or less)</td><td rowspan="3">2.93 V or less (25% or less)</td><td rowspan="3">1.51 V or less (27% or less)</td><td rowspan="3">1.41 V or less (25% or less)</td></tr>
<tr><td>10</td><td>3.13</td><td>7.5</td></tr>
<tr><td>11</td><td>3.44</td><td>0</td></tr>
<tr><td>12</td><td>3.75</td><td>18.8</td><td rowspan="4">3.15 V or less (32% or less)</td><td rowspan="4">3.09 V or less (30% or less)</td><td rowspan="4">1.74 V or less (32% or less)</td><td rowspan="4">1.64 V or less (30% or less)</td></tr>
<tr><td>13</td><td>4.06</td><td>13.1</td></tr>
<tr><td>14</td><td>4.38</td><td>7.5</td></tr>
<tr><td>15</td><td>4.69</td><td>0</td></tr>
</table>

Note: The threshold voltage of the LAL pin and VSP pin is typical values. The values are configured based on VREF pin voltage, so that they fluctuate with VREF pin voltage.

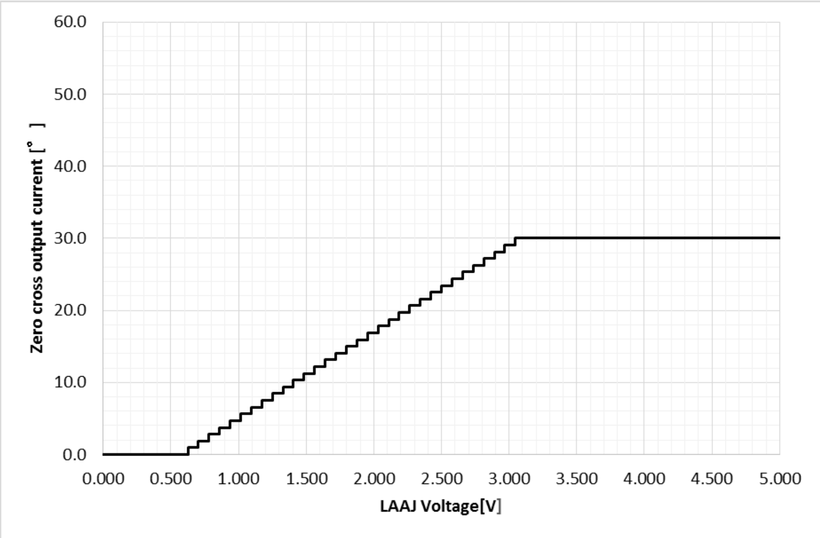


Automatic lead angle correction (LAAJ pin setting)

LAAJ pin can correct zero-cross point of output current during auto lead angle control as well as LA pin. Configuration is shown below.

STEP	LAAJ [V]	Phase [°]	STEP	LAAJ [V]	Phase [°]	STEP	LAAJ [V]	Phase [°]	STEP	LAAJ [V]	Phase [°]
0	0.00	0.0	16	1.25	8.4	32	2.50	23.4	48	3.75	30.0
1	0.08	0.0	17	1.33	9.4	33	2.58	24.4	49	3.83	30.0
2	0.16	0.0	18	1.41	10.3	34	2.66	25.3	50	3.91	30.0
3	0.23	0.0	19	1.48	11.3	35	2.73	26.3	51	3.98	30.0
4	0.31	0.0	20	1.56	12.2	36	2.81	27.2	52	4.06	30.0
5	0.39	0.0	21	1.64	13.1	37	2.89	28.1	53	4.14	30.0
6	0.47	0.0	22	1.72	14.1	38	2.97	29.1	54	4.22	30.0
7	0.55	0.0	23	1.80	15.0	39	3.05	30.0	55	4.30	30.0
8	0.63	0.9	24	1.88	15.9	40	3.13	30.0	56	4.38	30.0
9	0.70	1.9	25	1.95	16.9	41	3.20	30.0	57	4.45	30.0
10	0.78	2.8	26	2.03	17.8	42	3.28	30.0	58	4.53	30.0
11	0.86	3.8	27	2.11	18.8	43	3.36	30.0	59	4.61	30.0
12	0.94	4.7	28	2.19	19.7	44	3.44	30.0	60	4.69	30.0
13	1.02	5.6	29	2.27	20.6	45	3.52	30.0	61	4.77	30.0
14	1.09	6.6	30	2.34	21.6	46	3.59	30.0	62	4.84	30.0
15	1.17	7.5	31	2.42	22.5	47	3.67	30.0	63	4.92	30.0

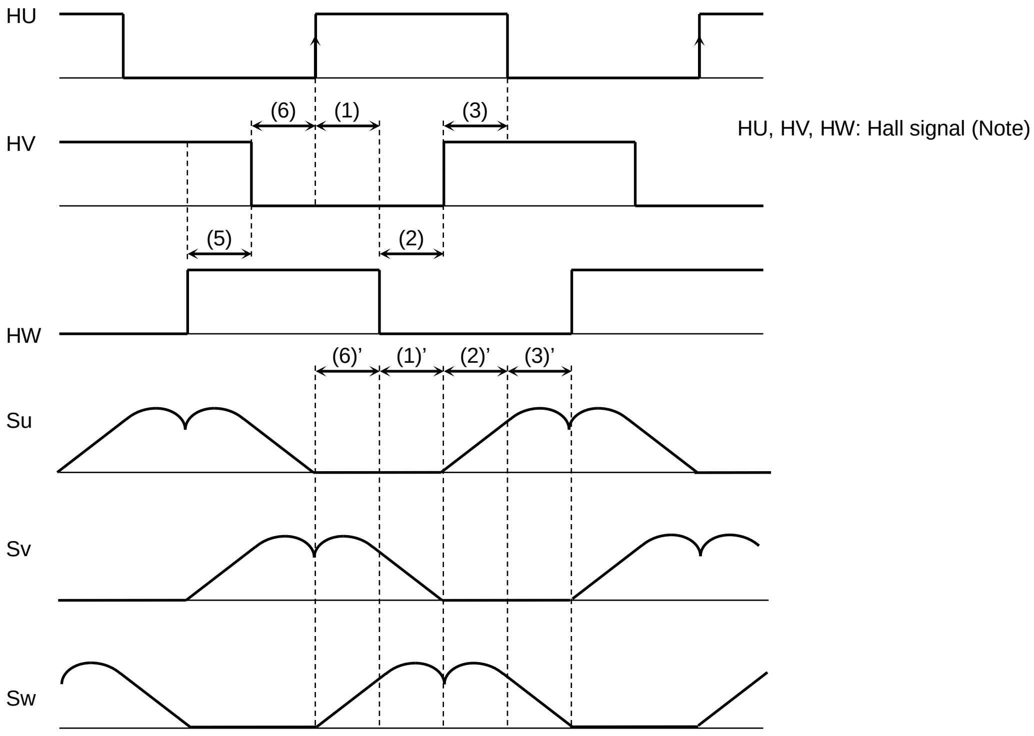
Note: The threshold voltage of the LAAJ pin is a typical value. The value is configured based on VREF pin voltage, so that it fluctuates with VREF pin voltage.



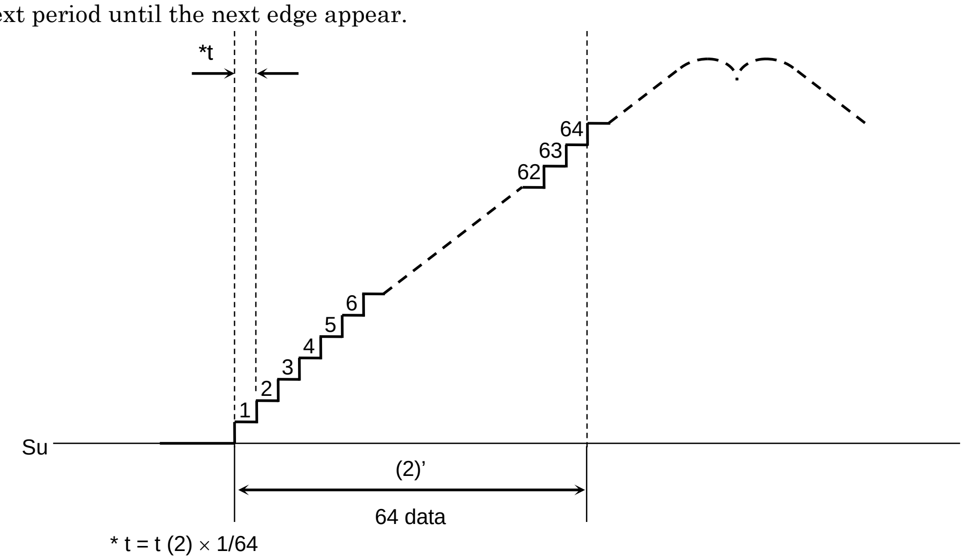
<Sine-wave generation>

(1) Reset of sine-wave (60°)

Hall signals generated from hall sensors are modulated, and a sinusoidal PWM waveform is created by comparing the modulated waveform to a triangular waveform.
The counter measures the period from a rising edge (falling edge) of each hall signal to its next falling edge (rising edge) (corresponding to the electrical angle of 60°). This period is then used as 60° phase data for the next modulation. A total of 64 ticks comprise 60° phase data. The time width of a tick equals 1/64th the time width of the immediately preceding 60° phase.



In the above diagram, the modulated waveforms have an interval (1)' that is equal to the time width between a rising edge of HU to a falling edge of HW (1) of the previous cycle. In the same way, the modulated waveforms have an interval (2)' that is equal to the time width between a falling edge of HW to a rising edge of HV (2) of the previous cycle. If next edge does not appear before 64 ticks end, next 64 ticks become equal to the next period until the next edge appear.

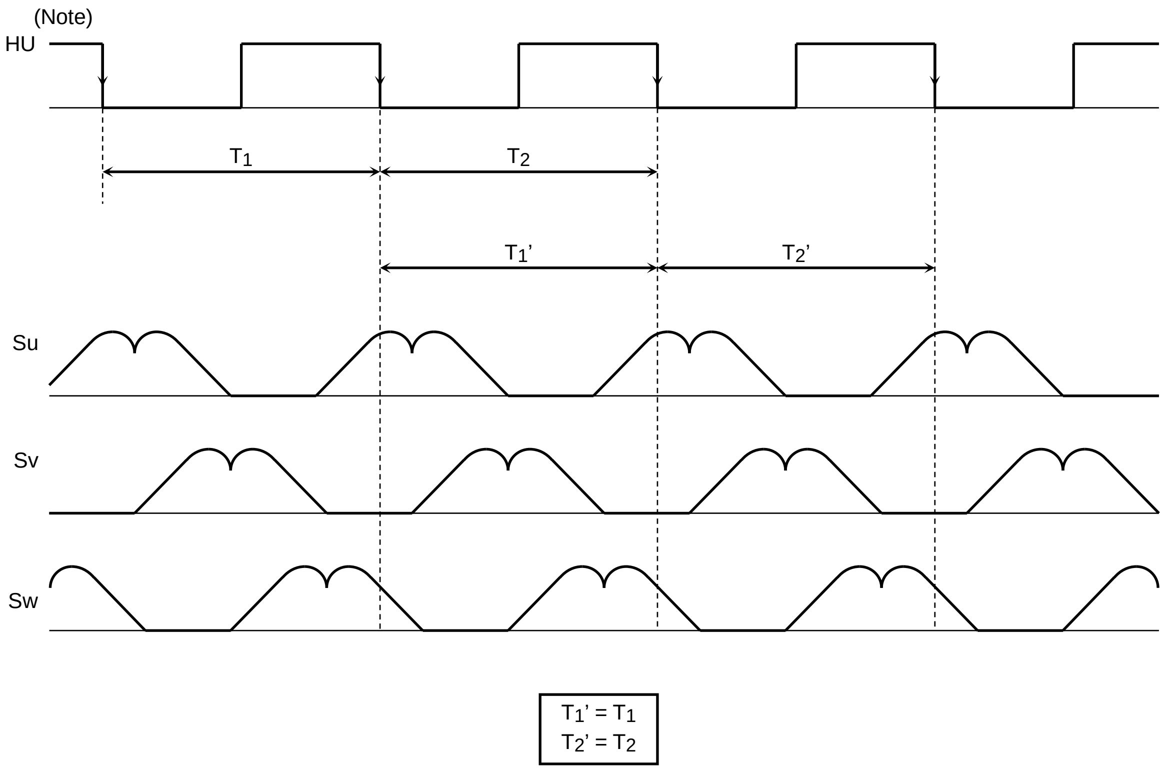


Phase matching between the hall signal and the modulated waveform is carried out for every zero-cross point of the hall signal. Modulation is reset on each rising edge and falling edge of the hall signal for every 60 electrical degrees. Therefore, when the hall sensor is displaced or the motor is accelerating or decelerating, the modulated waveform becomes discontinuous upon each reset.

Note: Square waveforms are used in the above diagram for the sake of simplicity.

(2) Reset of sine-wave (360°)

Hall signals generated from hall sensors are modulated, and a sinusoidal PWM waveform is created by comparing the modulated waveform to a triangular waveform.
The counter measures the period from a falling edge of HU to its next falling edge (corresponding to the electrical angle of 360°). This period is then used as 360° phase data for the next modulation.
A total of 384 ticks comprise 360° phase data. The time width of a tick equals 1/384th the time width of the immediately preceding 360° phase.



In the above diagram, the modulated waveforms have an interval (T_1') that is equal to the time width between a falling edge of HU to the next falling edge of HU (T_1) of the previous cycle. If next edge does not appear before T_1' data ends, next T_1' data becomes equal to the next period until the next edge appear.

Modulation is reset on each falling edge of the hall signal for every 360 electrical degrees. Therefore, when the motor is accelerating or decelerating, the modulated waveform becomes discontinuous upon each reset.

Note: Square waveforms are used in the above diagram for the sake of simplicity.

8. Error detections

(1) Overcurrent protection (IDC pin)

In sine-wave drive, if the IDC pin voltage exceeds the internal reference voltage (0.5 V (typ.)), the commutation signals are forced to output low level. The current limitation is released for each carrier frequency.

Note: In auto lead angle setting (InPAC), when the current limiting (IDC pin function) operates at zero-cross detection point of the output current, the angle leads by the current limiting function. Refer to the description of LA pin setting.

In square-wave drive, if the IDC pin voltage exceeds the internal reference voltage (0.5 V (typ.)), the upper phase signals (UH, VH, and WH) are forced to output low level. Lower phase signals (UL, VL, and WL) are output according to the hall signals as shown in the timing chart. The current limitation is released for each carrier frequency.

(2) Error detection positive input (RES pin)

When low level is input to RES pin, the commutation outputs are disabled. When high level is input to RES pin, the detection function is disabled after every carrier frequency and the commutation resumes.
In stop mode (Rotation frequency < 1 Hz when fosc=9.22 MHz)), commutation resumes after V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V) and the refresh function operates for 1.5 ms (condition: fosc=9.22 MHz).
In rotational mode (Rotation frequency ≥ 1 Hz when fosc=9.22 MHz), commutation resumes after V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V).
The internal counter is operating and FG signal is output during reset.

(3) Error detection negative input (RESX pin)

When high level is input to RESX pin, the commutation outputs are disabled. When low level is input to RESX pin, the detection function is disabled after every carrier frequency and the commutation resumes.
In stop mode (Rotation frequency < 1 Hz when fosc=9.22 MHz)), commutation resumes after V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V) and the refresh function operates for 1.5 ms (condition: fosc=9.22 MHz).
In rotational mode (Rotation frequency ≥ 1 Hz when fosc=9.22 MHz), commutation resumes after V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V).
The internal counter is operating and FG signal is output during reset.

(4) Abnormal hall signal protection

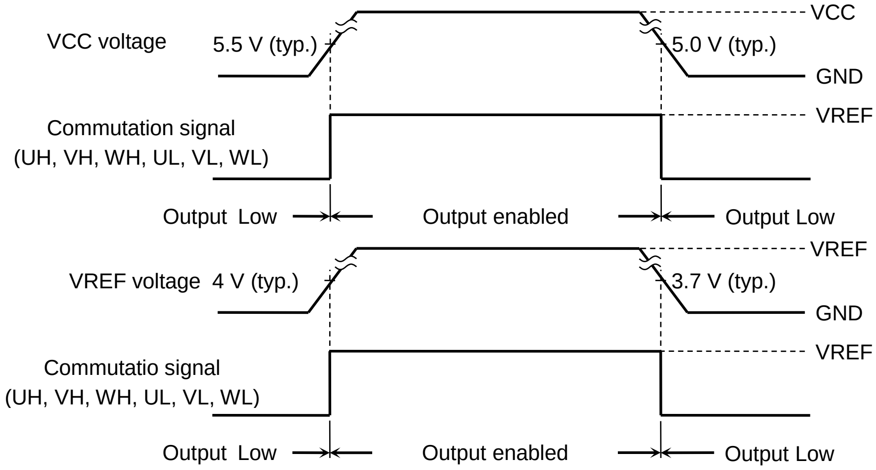
When hall signals (internal hall amplifier outputs) are all high or all low levels, the commutation signals output low level (i.e., gate block protection). When these signals are set to any other combination, the commutation resumes.
When all of hall inputs (HUP, HUM, HVP, HVM, HWP, and HWM) are set open, the commutation signals output low level (i.e., gate block protection). When these signals are set to any other combination, the commutation resumes.
Hall signals (internal hall amplifier outputs) in sine-wave PWM drive have lath type construction.
So, in case the hall signal is output differently from the logic of an expected value, a prior state is held.
Therefore, malfunction may not occur if a slight noise and chattering generate.

(5) Under voltage lockout (VCC monitor and VREF monitor)

While the operating voltage is outside the rated range during power-on or power-off, the commutation outputs are set low level to prevent external power devices from damage due to short-circuits.

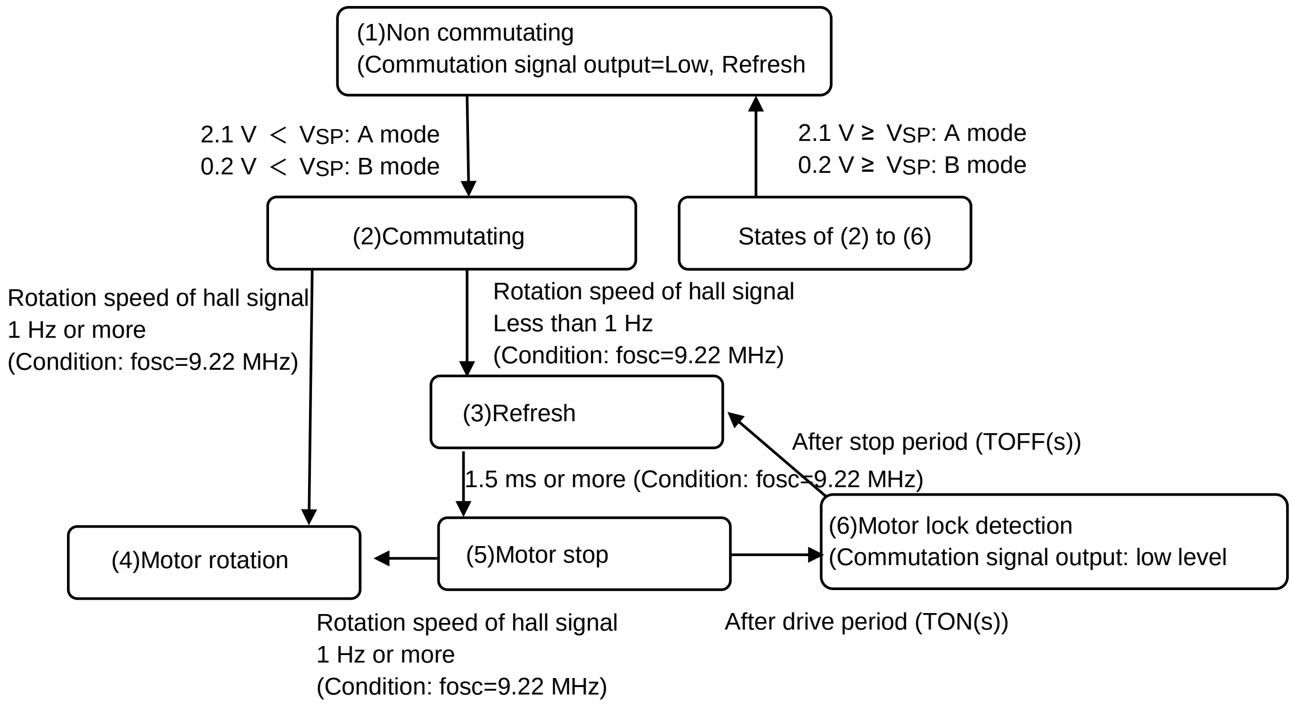
When V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V), refresh function is activated for 1.5 ms (condition: fosc=9.22 MHz) and the commutation resumes.

However, since sequence of returning power supply corresponds to the power-on sequence, the circuit turns into unstable and the operation cannot be guaranteed.



9. Motor lock detection

Motor lock detection function disables the commutation signals when the motor does not rotate although V_{SP} exceeds a certain value (A mode: 2.1 V, B mode: 0.2 V) and continues to stop after the drive period (TON (s)) has passed.
Motor lock detection repeats intermitted operation consisted of drive mode and stop mode. The ratio of drive period: stop period (TOFF(s)) is 1 : 6.
In drive period (TON(s)), when two hall input signal edges are input in the switching order and the time is less than 0.167s (condition: fosc=9.22 MHz), the motor is in a rotation state and the lock detection state is released.
When V_{SP} of a certain value or less (A mode: 2.1 V, B mode: 0.2 V) is applied, reset is carried out and the motor lock detection is released.
After stop period (TOFF(s)), refresh function is activated for 1.5 ms (condition: fosc=9.22 MHz). Then, commutation resumes.



<Setting method>

Period of drive mode and stop mode (commutation output = low level) can be configured by an external capacitor (TRC1) of TR pin. They can be calculated as follows;

Drive period (TON(s)) = TRC1 × (VHTR - VLTR) × 2 / I × 500 counts

Stop period (TOFF(s)) = TRC1 × (VHTR - VLTR) × 2 / I × 3000 counts

Example: When TRC1 is 0.01 μF, I(ICTR,IDTR) = 3 μA (typ.), VHTR = 3 V (typ.), and VLTR = 1.5 V (typ.). Then TON(s) = 5 s (typ.) and TOFF(s) = 30 s (typ.).

< Use range of TR pin external capacitor and characteristics of motor detection lock>

Item	Symbol	Min	Typ.	Max	Unit	Remarks
TR pin external capacitor value	TRC1	470 p	0.01 µ	—	F	Open detection may operate if the capacitor is set less than the minimum value.
Motor lock detection frequency	FTR	—	100	2.1 k	Hz	—
Motor lock detecition enable priod	TON	0.23	5	—	s	—
Motor lock detecition disable period	TOFF	1.4	30	—	s	—

Note1: When TR pin is open, the motor lock detection state is held (commutation signal = low level) by open detection.

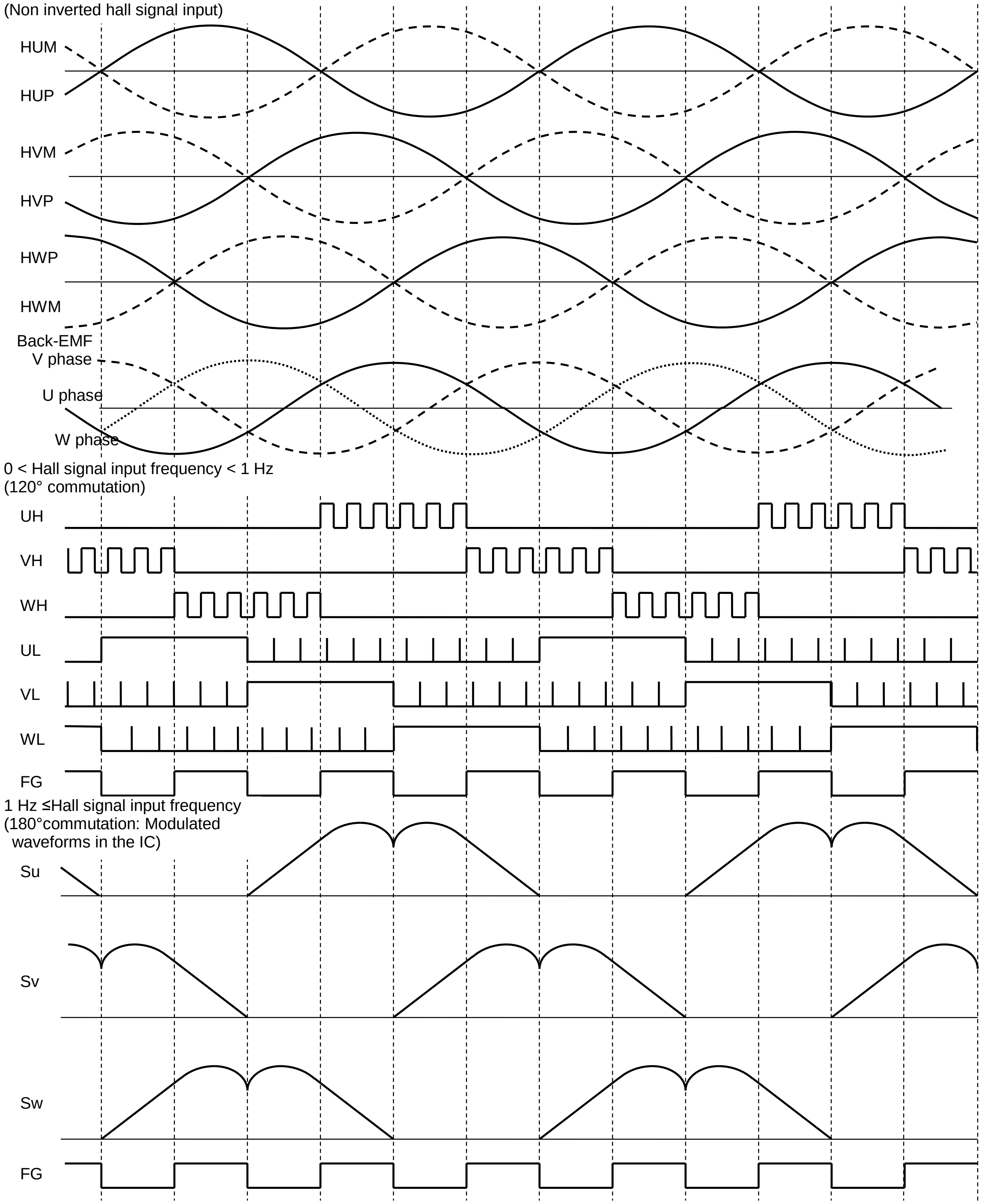
Note2: When TR pin is connected to GND, the motor lock detection is disabled.

10. Forward/Reverse rotation

Motor rotation direction can be switched by using CWCCW pin. Timing chart is shown as follows;

CWCCW	Hall signal input	Drive method	Timing chart
High (Reverse rotation)	Forward direction	120° commutation	(4)
	Reverse direction	Sin-wave drive	(3)
Low/Open (Forward rotation)	Forward direction	Sin-wave drive	(1)
	Reverse direction	120° commutation	(2)

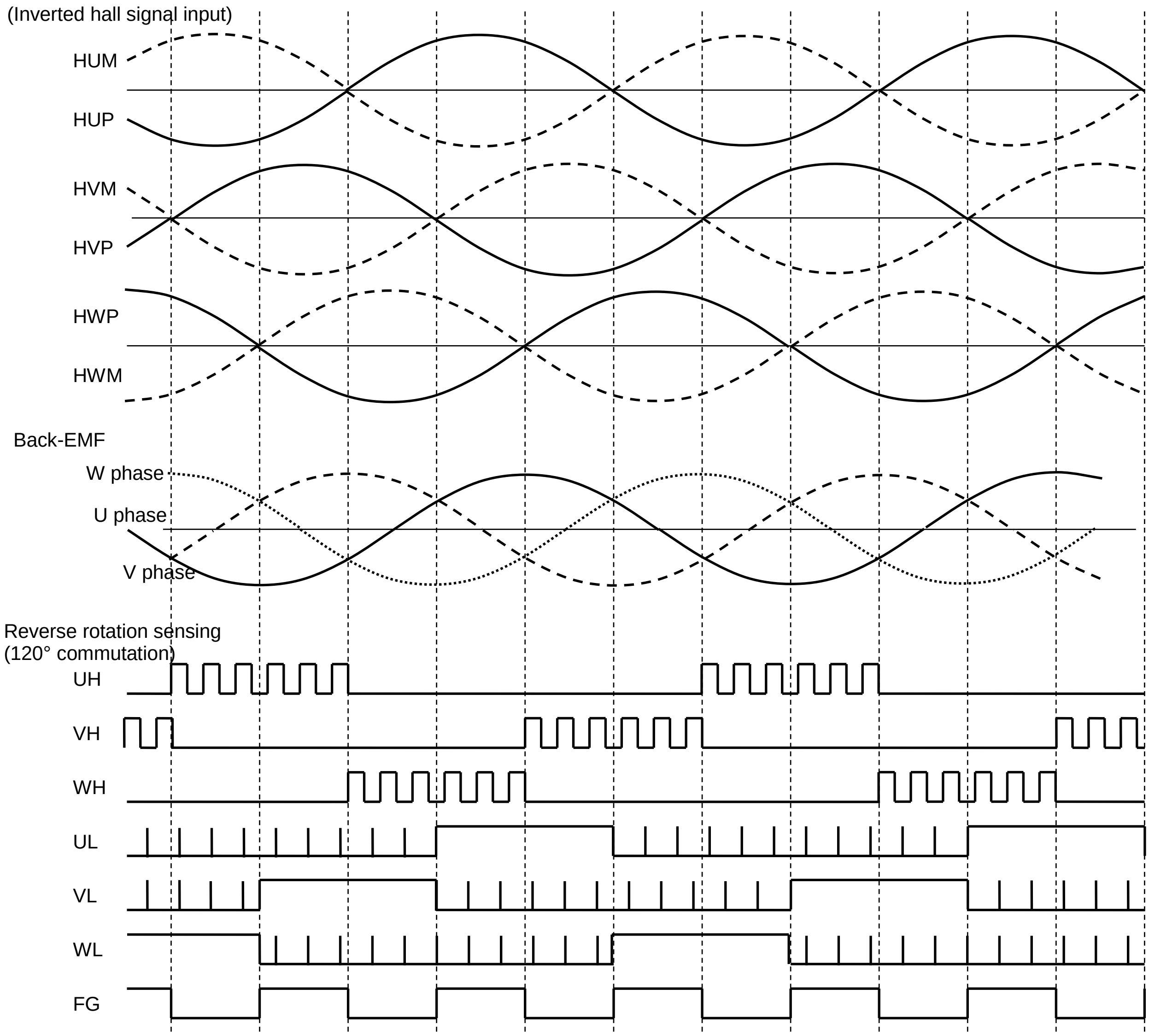
(1) Sine-wave drive timing chart: Forward rotation, Non inverted hall signal input, Lead angle=0° (CWCCW = Low, FGC = GND)



Note: When the Hall signal input frequency is 1 Hz or more (Condition: fosc = 9.22 MHz), lead angle control is activated.

The above timing chart is simplified to illustrate the function and behavior of the device.

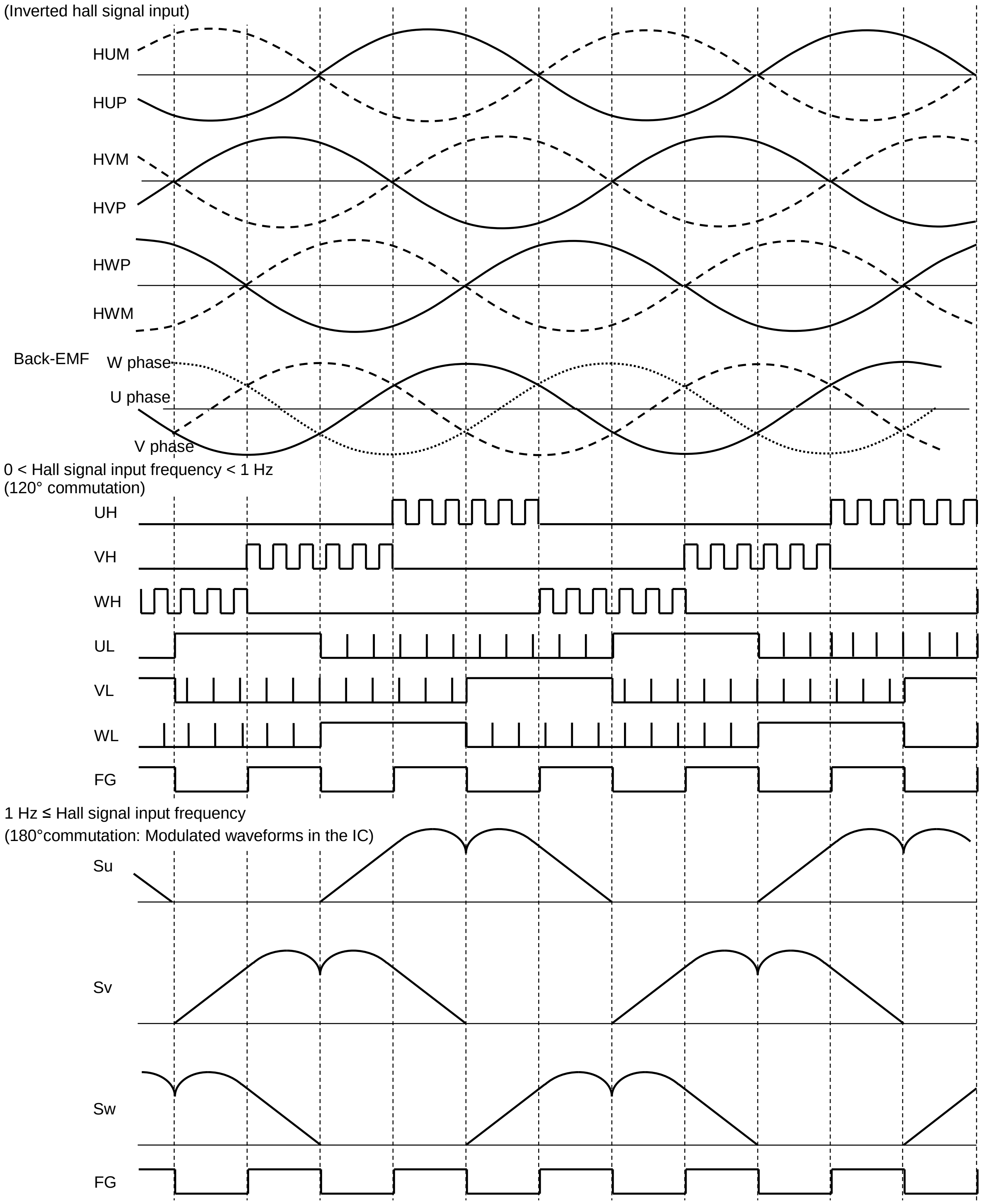
(2) 120° commutation drive timing chart: Forward rotation, Inverted hall signal input (CWCCW = Low, FGC = GND)



Note: When CW/CCW = Low and inverted hall signals are input, the IC operates in 120° commutation mode with a lead angle of 0° (reverse rotation).

The above timing chart is simplified to illustrate the function and behavior of the device.

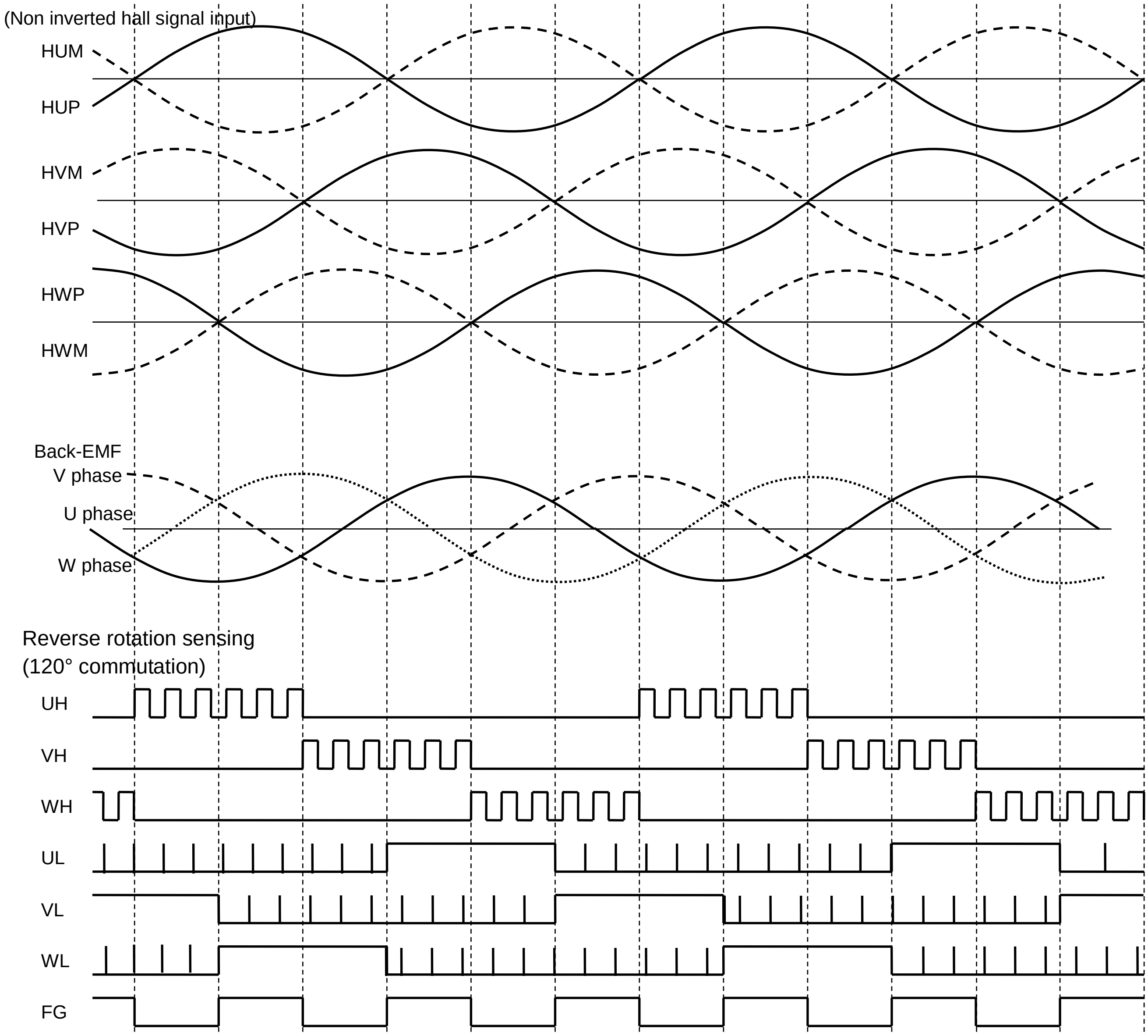
(3) Sine-wave drive timing chart: Reverse rotation, Inverted hall signal input, Lead angle = 0° (CWCCW = High, FGC = GND)



Note: When the Hall signal input frequency is 1 Hz or more (Condition: fosc = 9.22 MHz), lead angle control is activated.

The above timing chart is simplified to illustrate the function and behavior of the device.

(4) 120° commutation drive timing chart: Reverse rotation, Non inverted hall signal input (CWCCW = High, FGC = GND)

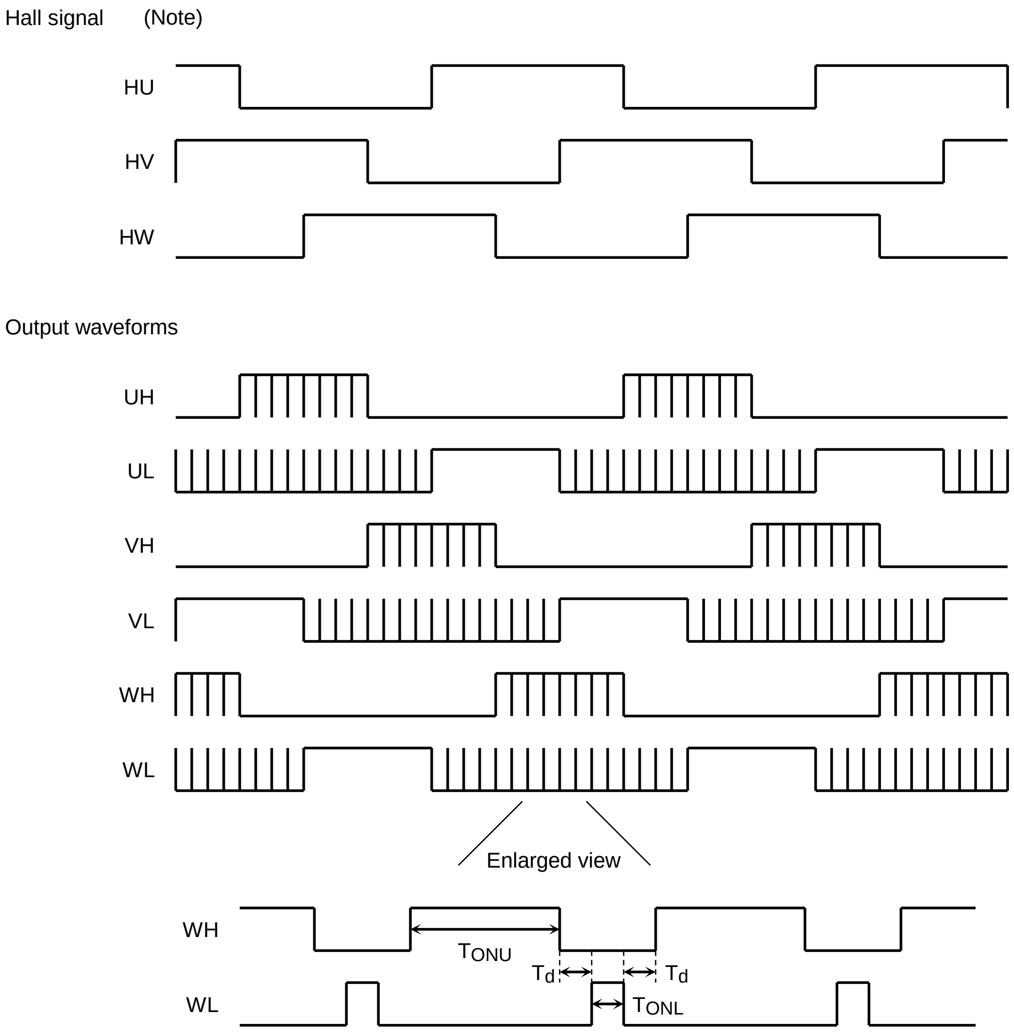


Note: When CW/CCW = High and non-inverted hall signals are input, the IC operates in 120° commutation mode with a lead angle of 0° (reverse rotation).

The above timing chart is simplified to illustrate the function and behavior of the device.

11. Description of driving waveforms

<120° square-wave drive waveforms (CWCCW = Low)>



Note: Square waveforms are used in the above diagram for the sake of simplicity.

To obtain an adequate bootstrap voltage, the low-side outputs (UL, VL and WL) are constantly turned on for every carrier period even during the OFF term. As shown in the above enlarged view, the high-side outputs (UH, VH and WH) have a dead time and are turned off at the ON timing of the low-side outputs.

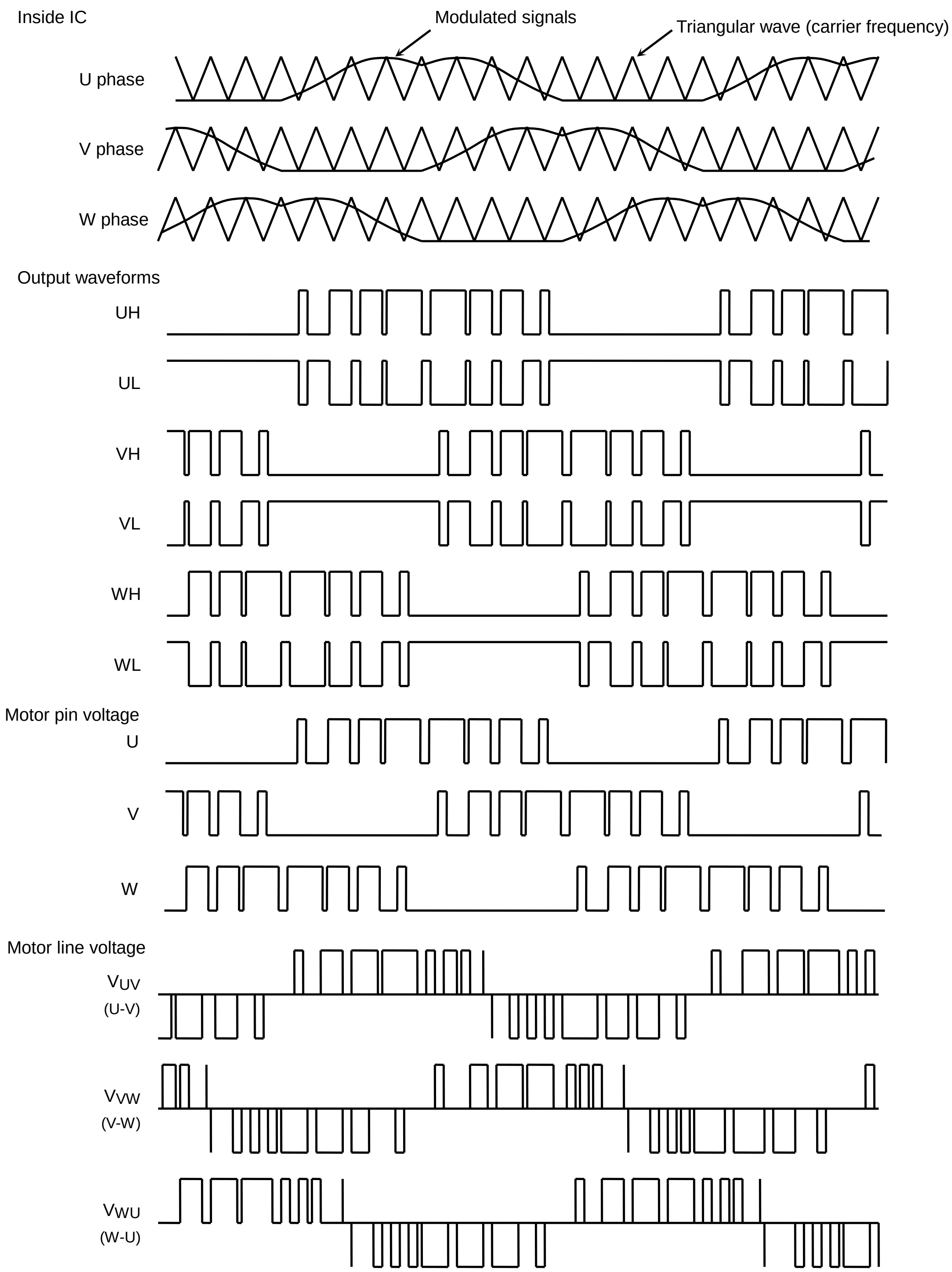
Carrier frequency = fosc/512 (Hz)　　　　Dead time: T_d = 18/ fosc(s)

T_{ONL} = Carrier period × 8% (s) (constant regardless of the V_{SP} input)

In square-wave drive mode, the motor speed is controlled by V_{SP} and conduction duty cycle of T_{ONU}.

Note: At startup, the motor is driven by a square wave when the hall signal frequency is less than 1 Hz (condition: fosc = 9.22 MHz) and when the motor rotating direction is reverse to the configuration.

<Sine-wave PWM drive waveforms (CWCCW = Low)>



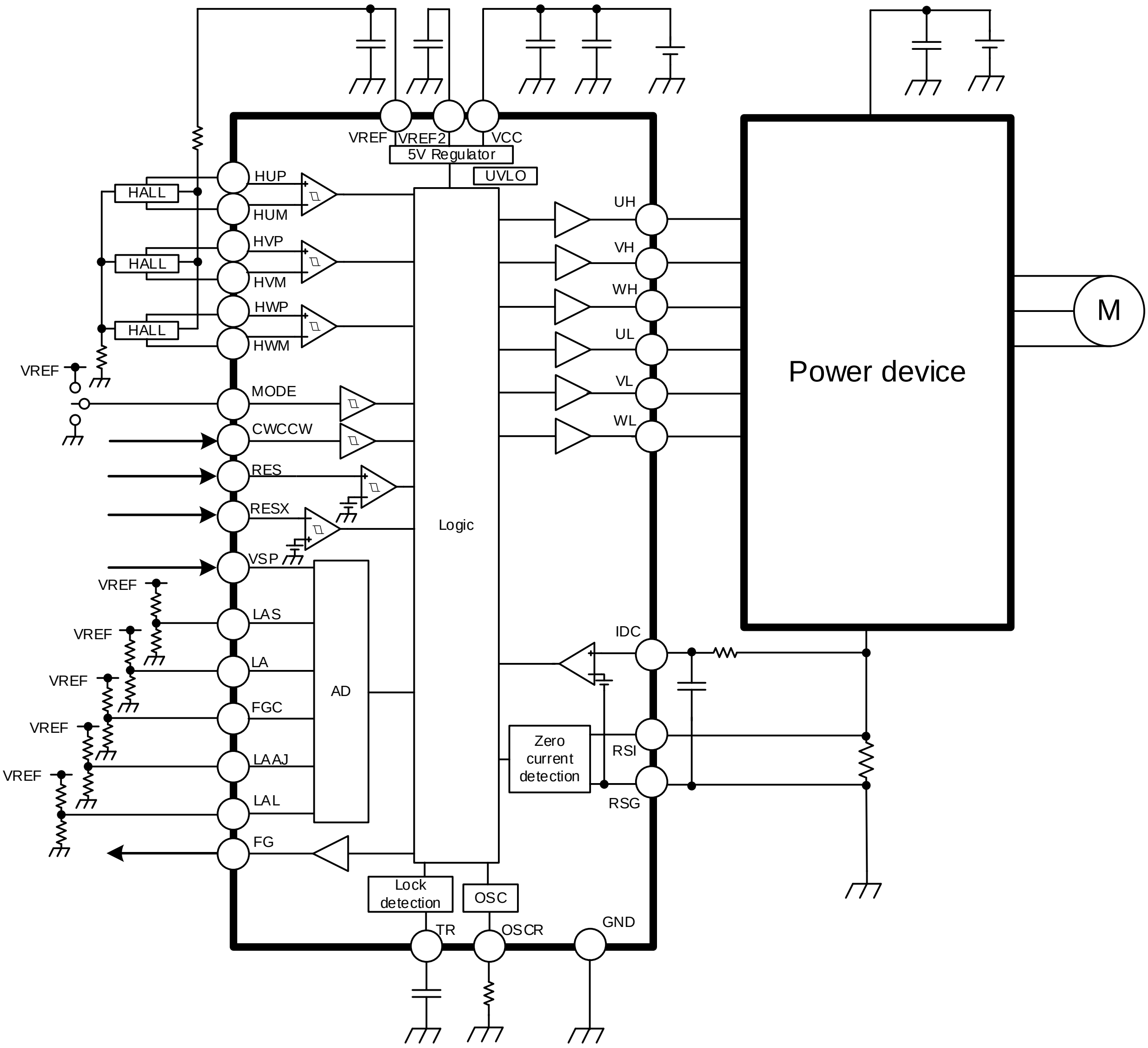
In sine-wave drive mode, the motor speed is controlled by VSP, which changes the amplitude of the modulated signals, and by the conduction duty cycle of the output waveforms.

Triangular wave frequency = Carrier frequency = fosc /512 (Hz)

Note: At startup, the motor is driven by a sine wave when the hall signal frequency is 1 Hz or more (condition: fosc = 9.22 MHz) and when the motor rotating direction is the same as the configuration.

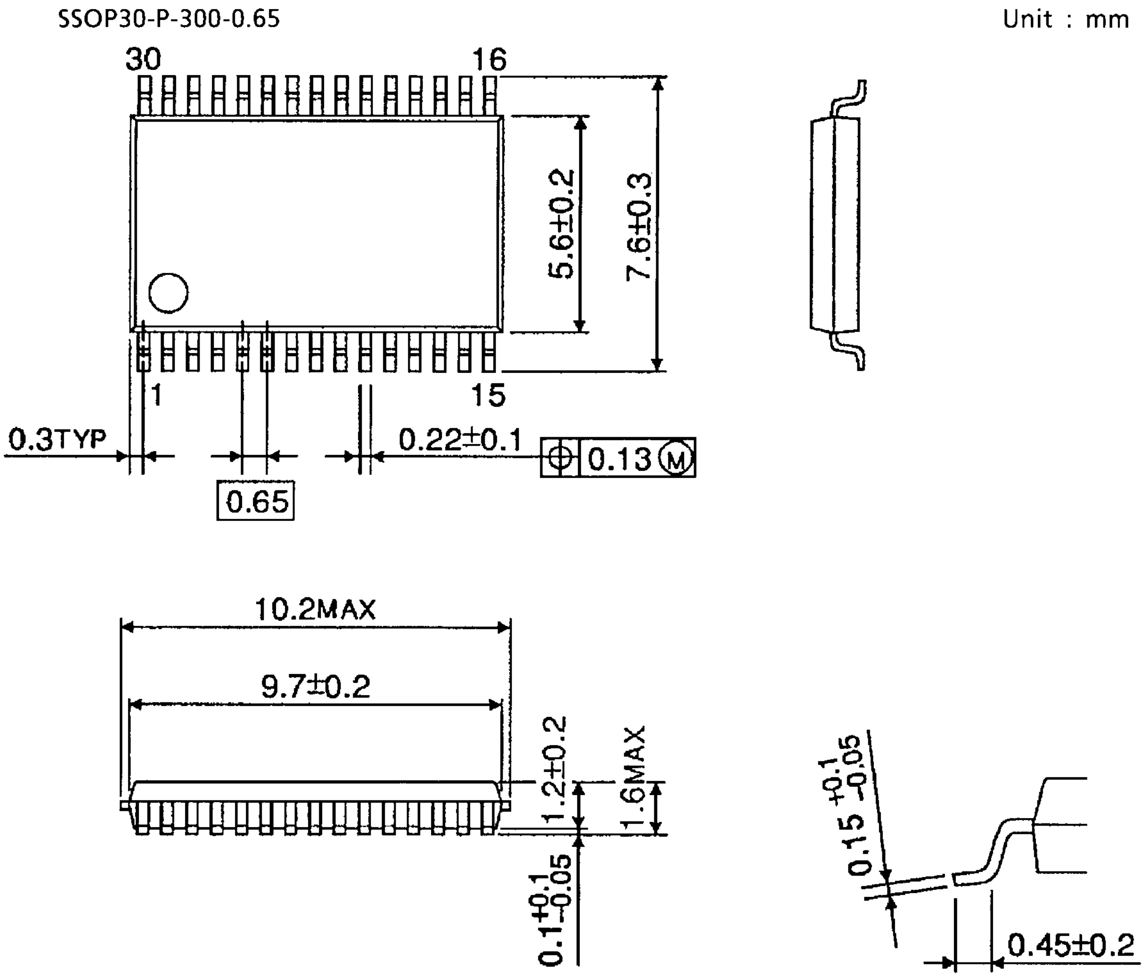
Application circuit example

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes. The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design. No license to any industrial property rights is granted by the provision of the application circuit example.

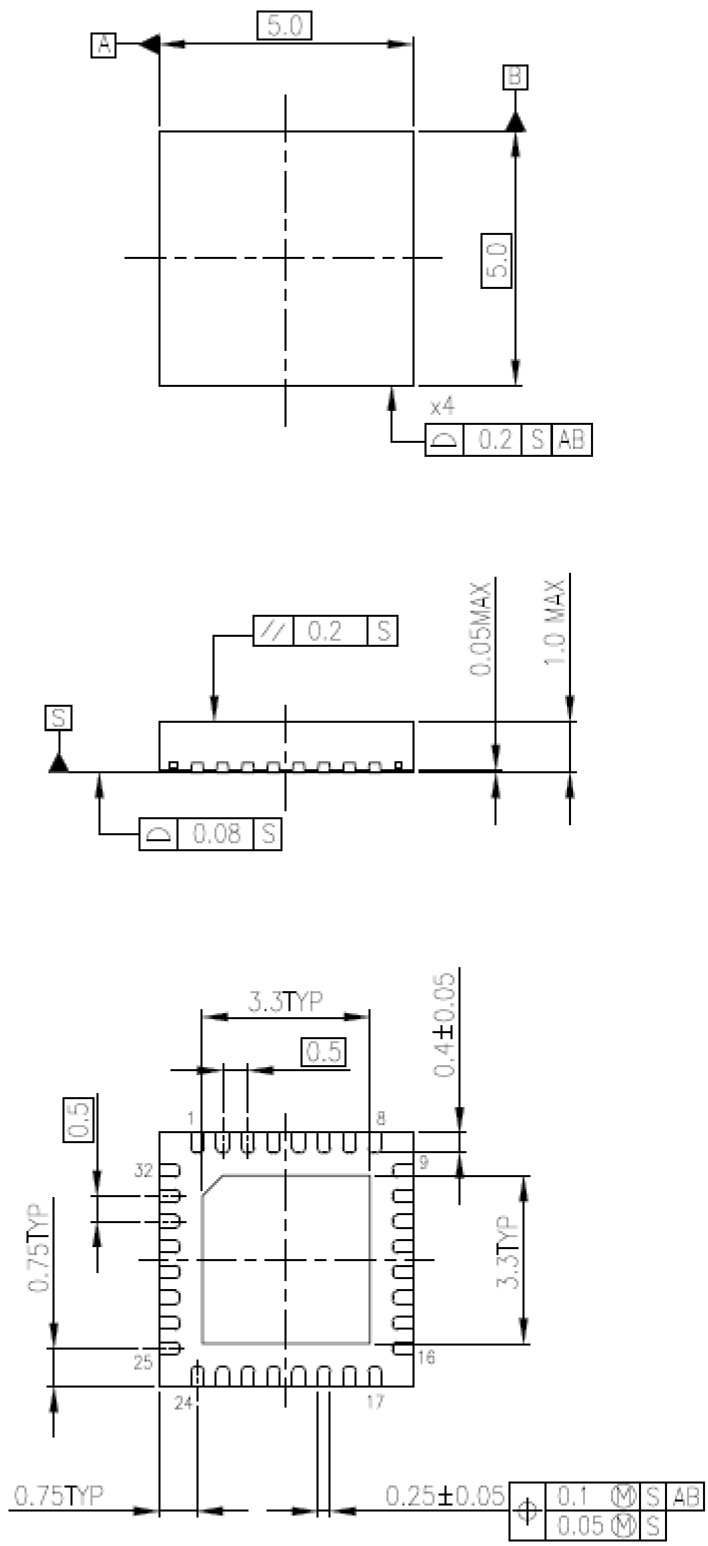


Note: RESX pin and VREF2 pin are only for the TC78B042FTG.

Package dimensions



P−VQFN32−0505−0.50−005 "Unit:mm"



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Over current protection circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Heat radiation design
In using an IC with large current flow such as power amplifier, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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