ANY-FREQUENCY 1–200 MHZ QUAD FREQUENCY 8-OUTPUT CLOCK GENERATOR

Features

- Generates any frequency from 1 to 200 MHz on each of the 4 output banks
- Eight CMOS clock outputs
- Guaranteed 0 ppm frequency synthesis error for any combination of frequencies
- 25 or 27 MHz xtal or 5–200 MHz input clk
- Five programmable control pins (output enable, frequency select, reset)
- Separate OEB pins to disable individual banks or all outputs
- Loss of signal output
- Low 50 ps (typ) pk-pk period jitter
- Phase jitter: 2 ps rms 12 kHz–20 MHz
- Excellent PSRR performance eliminates need for external power supply filtering
- Low power: 45 mA (core)
- Core VDD: 1.8, 2.5, or 3.3 V
- Separate VDDO for each bank of outputs: 1.8, 2.5, or 3.3 V
- Small size: 4x4 mm 24-QFN
- Industrial temperature range: –40 to +85 °C
- Custom versions available using ClockBuilder™ web utility
- Samples available in 2 weeks

Ordering Information:

See page 17.

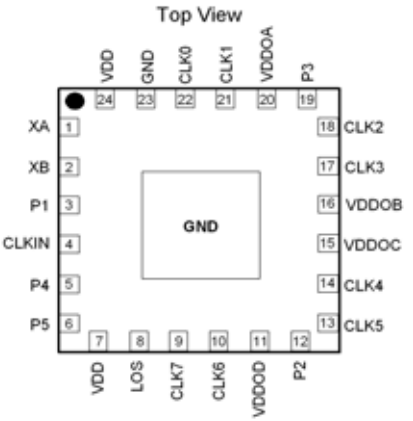
Applications

- Printers
- Audio/video
- Networking
- Communications
- Storage
- Switches/routers
- Computing
- Servers
- OC-3/OC-12 line cards

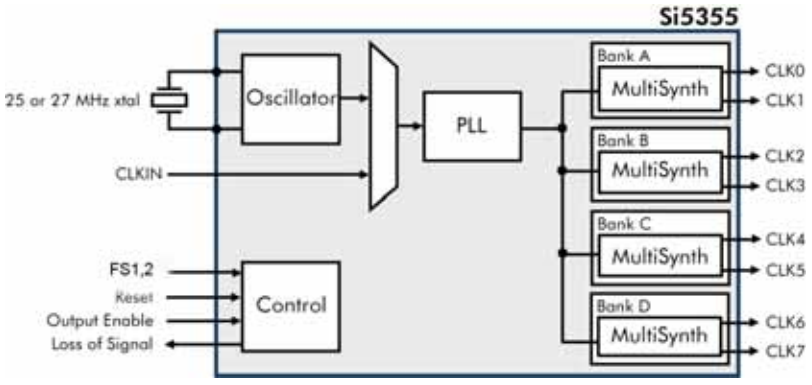
Description

The Si5355 is a highly flexible clock generator capable of synthesizing four completely non-integer related frequencies up to 200 MHz. The device has four banks of outputs with each bank supporting two CMOS outputs at the same frequency. Using Silicon Laboratories' patented MultiSynth fractional divider technology, all outputs are guaranteed to have 0 ppm frequency synthesis error regardless of configuration, enabling the replacement of multiple clock ICs and crystal oscillators with a single device. Through a flexible web configuration utility called ClockBuilder™ (www.silabs.com/ClockBuilder), factory-customized pin-controlled Si5355 devices are available in two weeks without minimum order quantity restrictions. The Si5355 supports up to three independent, pin-selectable device configurations, enabling one device to replace three separate clock ICs.

Pin Assignments



Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions
(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	—	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	
			1.71	1.8	1.98	
Output Buffer Supply Voltage	V_{DDO}		1.71	—	3.63	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.						

Table 2. DC Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Core Supply Current	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
Output Buffer Supply Current	I_{DDOx}	CMOS, 50 MHz 15 pF load	—	6	9	mA
		CMOS, 200 MHz 3.3 V VDD0	—	13	18	mA
		CMOS, 200 MHz 2.5 V	—	10	14	mA
		CMOS, 200 MHz 1.8 V	—	7	10	mA
High Level Input Voltage	V_{IH}	CLKIN, P1	0.8 x V_{DD}	—	3.63	V
		P4, P5	0.85	—	1.3	V
		P2, P3	1.6	—	3.63	V
Low Level Input Voltage	V_{IL}	CLKIN, P1, P2, P3	–0.2	—	0.2 x V_{DD}	V
		P4,P5	—	—	0.3	V
Clock Output High Level Output Voltage	V_{OH}	Pins: CLK0-7 I_{OH} = –4 mA	V_{DDO} – 0.3	—	—	V
Clock Output Low Level Output Voltage	V_{OL}	Pins: CLK0-7 I_{OL} = +4 mA	—	—	0.3	V
LOS Low Level Output Voltage	V_{OLLOS}	Pin: LOS I_{OL} = +3 mA	0	—	0.4	V
Pn Input Resistance	R_{IN}		—	20	—	kΩ

Table 3. AC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock						
Clock Input Frequency	F_{IN}		5	—	200	MHz
Clock Input Rise/Fall Time	T_R/T_F	20–80% V_{DD}	—	—	2.3	ns
		10–90% V_{DD}	—	—	4	ns
Clock Input Duty Cycle	DC	Input tr/tf within specified limits shown above	40	—	60	%
Clock Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks						
Clock Output Frequency	F_O		1	—	200	MHz
Clock Output Frequency Synthesis Resolution	F_{RES}	See "3.3. Input and Output Frequency Configuration" on page 10	0	0	1	ppb
Output Load Capacitance	C_L		—	—	15	pF
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 15 pF	—	—	2.0	ns
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 2 pF	—	0.45	0.85	ns
Clock Output Duty Cycle	DC		45	50	55	%
Powerup Time	T_{PU}	POR to output clock valid	—	—	2	ms
Output Enable Time	T_{OEB}		—	—	10	µs
Reset Minimum Pulse Width	T_{RESET}		—	—	200	ns
Output-Output Skew	T_{SKEW}	Outputs at same frequency, f_{OUT} > 5 MHz	–150	—	+150	ps
Period Jitter	J_{PPKPK}	10000 cycles*	—	50	75	ps pk-pk
Cycle-Cycle Jitter*	J_{CCPK}	10000 cycles*	—	40	70	ps pk
Phase Jitter	J_{PH}	12 kHz to 20 MHz	—	2	—	ps rms
PLL Loop Bandwidth	F_{BW}		—	1.6	—	MHz
Interrupt Status Timing						
CLKIN Loss of Signal Assert Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Deassert Time	t_{LOS_b}		0.01	0.2	1	µs
LOS Rise/Fall Time (20–80%)	T_R/T_F	$C_L \leq$ 10 pF, pullup ≤ 1 kΩ	—	—	10	ns

***Note:** Measured in accordance to JEDEC Standard 65.

Table 4. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{XTAL}	Option 1	—	25	—	MHz
		Option 2	—	27	—	MHz
Load Capacitance (on-chip differential)	c_L (supported)*		11	12	13	pF
	c_L (recommended)		17	18	19	pF
Crystal Output Capacitance	C_O		—	—	5	pF
Equivalent Series Resistance	ESR	25 MHz	—	—	100	Ω
		27 MHz	—	—	75	Ω
Crystal Drive Level Rating	d_L		100	—	—	µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to accommodate a 12 pF crystal C_L.

Table 5. Thermal Conditions

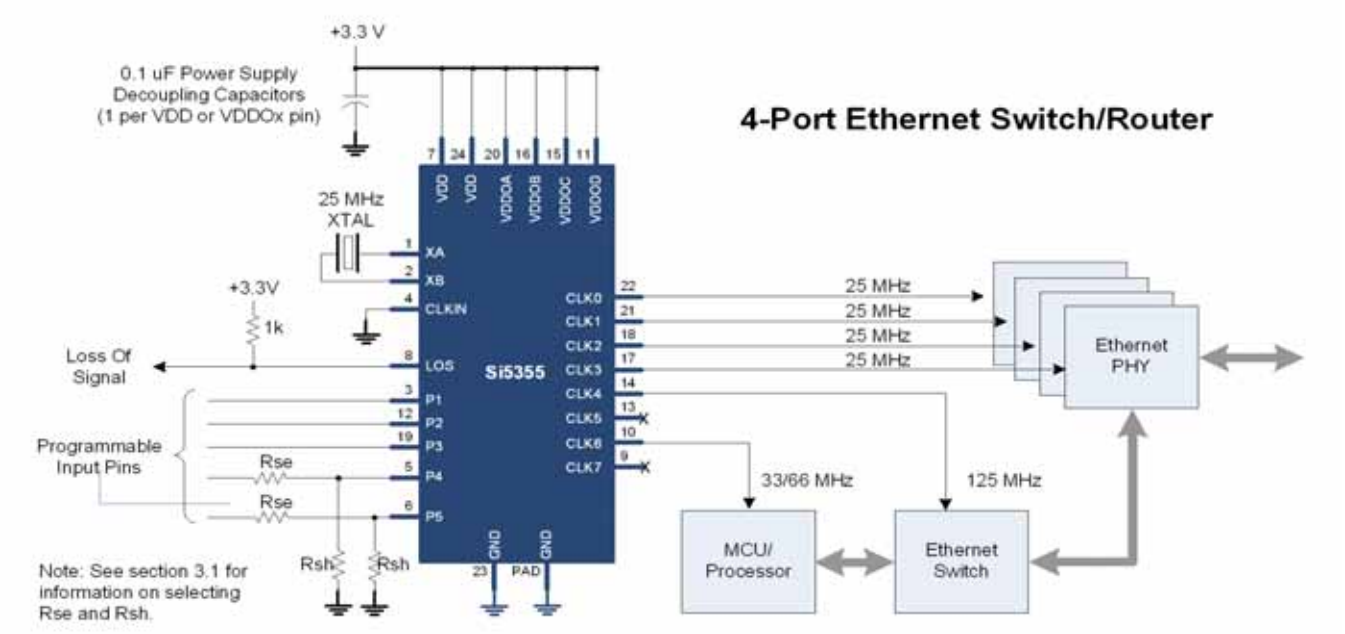
Parameter	Symbol	Test Condition	Value	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

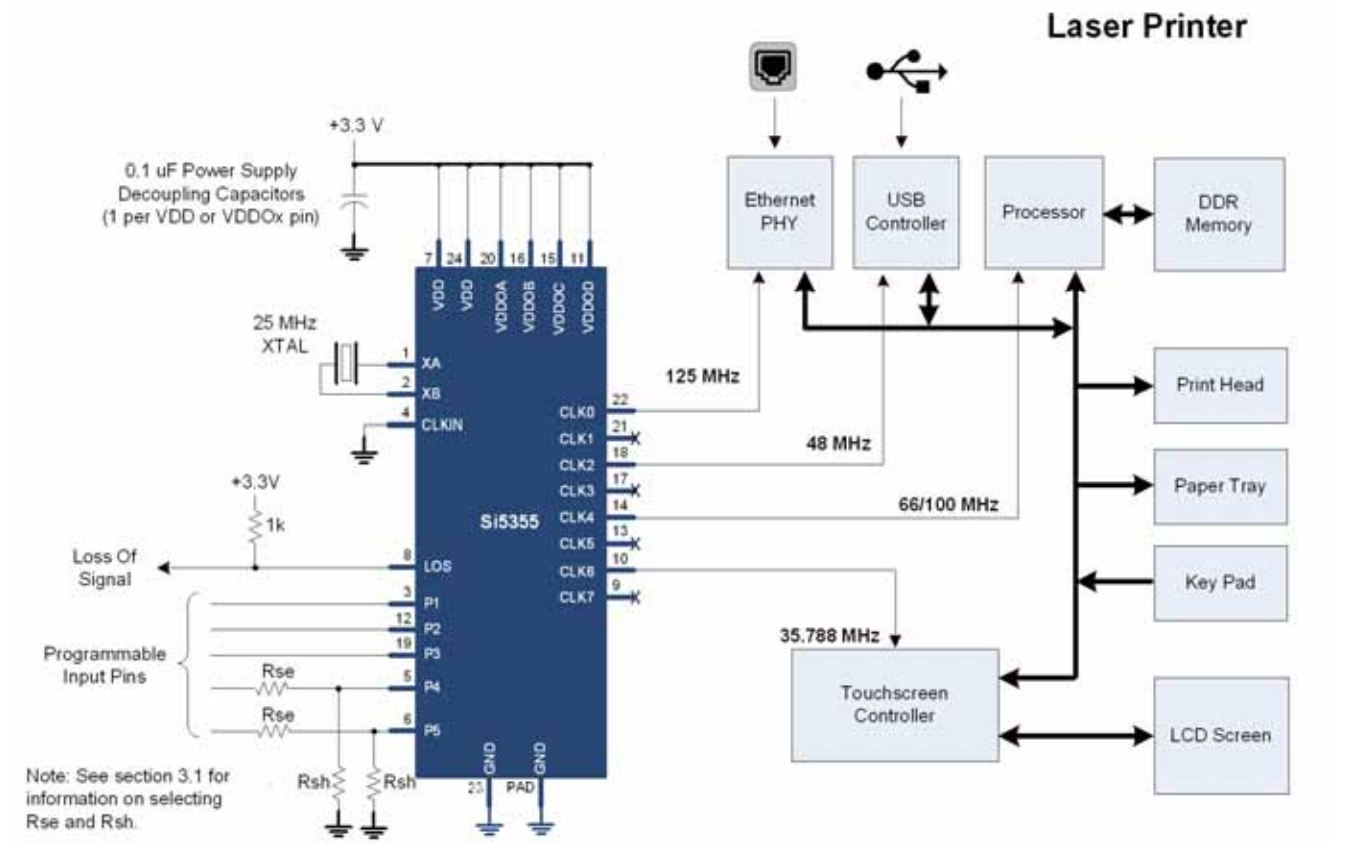
Table 6. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Rating	Units
Supply Voltage Range	V_{DD}	–0.5 to 3.8	V
Input Voltage Range (all pins except pins 1,2,5,6)	V_I	–0.5 to 3.8	V
Input Voltage Range (pins 1,2,5,6)	V_{I2}	–0.5 to 1.3	V
Output Voltage Range	V_O	–0.5 to (V_{DD} + 0.3)	V
Junction Temperature	T_J	–55 to +150	°C
ESD Tolerance	HBM	2.5	kV
	CDM	550	V
	MM	175	V
Latch-up Tolerance	LU	JESD78 Compliant	
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}	260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P	20–40	sec

Notes:
1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. 24-QFN package is RoHS compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

2. Typical Application Circuit





3. Functional Description

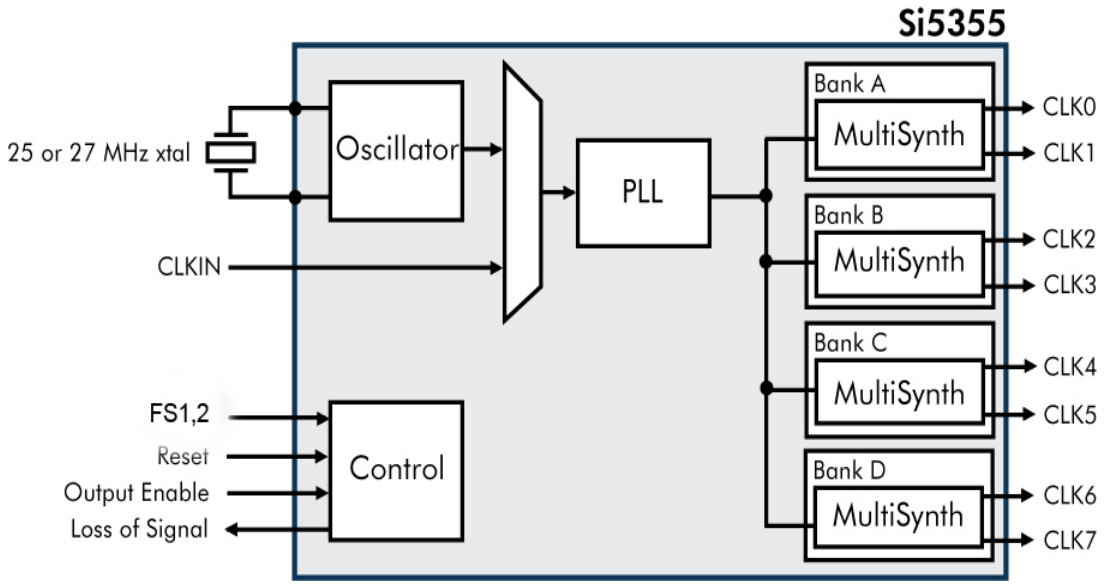


Figure 1. Si5355 Functional Block Diagram

3.1. Input Configuration

The Si5355 input can be driven from either an external crystal or a reference clock. Reference selection is made when the device configuration is specified using the ClockBuilder™ web-based utility available at www.silabs.com/ClockBuilder. If the crystal input option is used, the Si5355 operates as a free-running clock generator. In this mode of operation the device requires a low-cost 25 or 27 MHz fundamental mode crystal connected across XA and XB as shown in Figure 2. Given the Si5355's frequency flexibility, the same 25 or 27 MHz crystal can be reused to generate any combination of output frequencies. Custom frequency crystals are not required. The Si5355 integrates the crystal load capacitors on-chip to reduce external component count. The crystal should be placed very close to the device to minimize stray capacitance. To ensure stable oscillation, the recommended crystal specifications provided in Table 4 on page 6 must be followed. See AN360 for additional details regarding crystal recommendations.

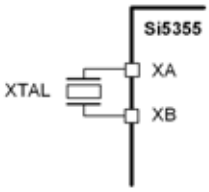


Figure 2. Connecting an XTAL to the Si5355

For synchronous timing applications, the Si5355 can lock to a 5 to 200 MHz CMOS reference clock. A typical interface circuit is shown in Figure 3. A series termination resistor matching the driver's output impedance to the impedance of the transmission line is recommended to reduce reflections.

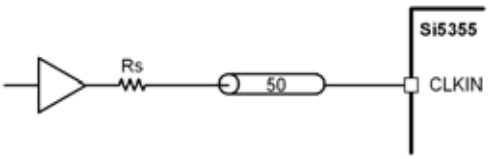


Figure 3. Interfacing CMOS Reference Clocks to the Si5355

Control input signals to P4 and P5 cannot exceed 1.3 V, yet also must meet the V_{OH} and V_{OL} specifications outlined in Table 2 on page 4. When these inputs are driven from CMOS sources, a resistive attenuator as shown in the Typical Application Circuits must be used. Suggested standard 1% resistor values for Rse and Rsh are shown in Table 7.

Table 7. 1% Resistor Values

CMOS Level	Rse (Ω)	Rsh (Ω)
1.8 V	1000	1580
2.5 V	1960	1580
3.3 V	3090	1580

3.2. Breakthrough MultiSynth Technology

Next-generation timing architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using a combination of single PLL ICs, 4-PLL ICs and discrete XOs, often at the expense of BOM complexity and power. The Si5355 uses patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 phase-locked loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions. Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high-frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high-speed fractional divider with Silicon Laboratories' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, the output of each MultiSynth can produce any frequency from 1 to 200 MHz.

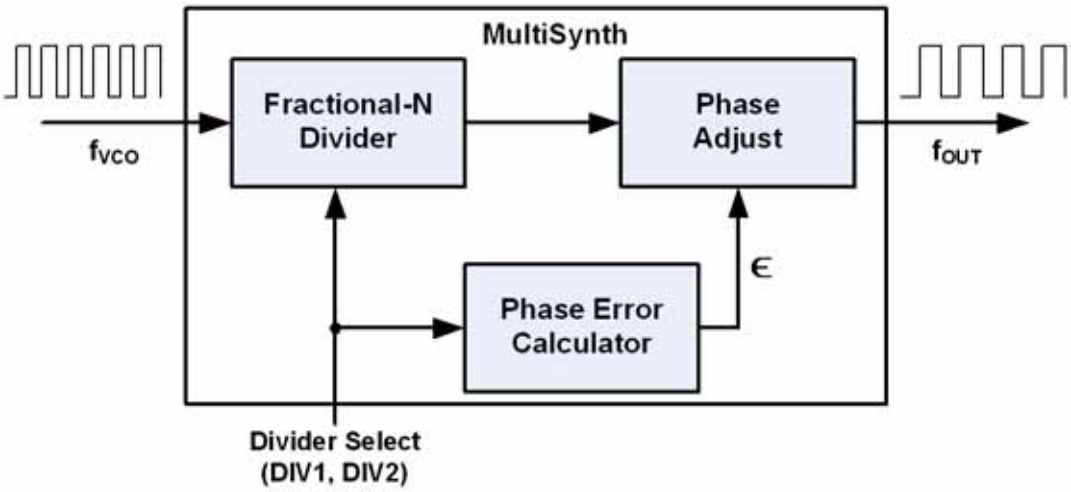


Figure 4. Silicon Labs' MultiSynth Technology

3.3. Input and Output Frequency Configuration

The Si5355 utilizes a single PLL-based architecture, four independent MultiSynth fractional output dividers, and a MultiSynth fractional feedback divider such that a single device provides the clock generation capability of 4 independent PLLs. Unlike competitive multi-PLL solutions, the Si5355 can generate four unique non-integer related output frequencies with 0 ppm frequency error for any combination of output frequencies. In addition, any combination of output frequencies can be generated from a single reference frequency without having to change the crystal or reference clock frequency between frequency configurations.

The Si5355 frequency configuration is set when the device configuration is specified using the ClockBuilder web-based utility available at www.silabs.com/ClockBuilder. Any combination of output frequencies ranging from 1 to 200 MHz can be configured on each of the device outputs. Up to three unique device configurations can be specified in a single device, enabling the Si5355 to replace 3 different clock generators.

3.4. Multi-Function Control Inputs

The Si5355 supports 5 user-defined input pins (pins 3, 5, 6, 12, 19) that are customizable to support the functions listed below. The pinout of each device is customized using the ClockBuilder utility. This enables the device to be custom tailored to a specific application. Each of the different functions is described in Table 8.

Table 8. Multi-Function Control Inputs Description

Pin Function	Description	Assignable Pin Name
OEB_ALL	**Output Enable All.** All outputs enabled when low.	P1, P2, P3, P4, or P5
OEB_A	**Output Enable Bank A.** CLK0/1 enabled when low.	P1, P2, P3, P4, or P5
OEB_B	**Output Enable Bank B.** CLK2/3 enabled when low.	P1, P2, P3, P4, or P5
OEB_C	**Output Enable Bank C.** CLK4/5 enabled when low.	P1, P2, P3, P4, or P5
OEB_D	**Output Enable Bank D.** CLK6/7 enabled when low.	P1, P2, P3, P4, or P5
FS0	**Frequency Select.** Selects active device frequency plan from factory-configured profiles.	P2
FS1	**Frequency Select.** Selects active device frequency plan from factory-configured profiles.	P3
RESET	**Reset.** Device reset required to change FS[1:0] pin setting.	P1, P3, P4, P5

3.5. Output Enable

Each of the device's four banks of CMOS clock outputs can be individually disabled using OEB_A, OEB_B, OEB_C, and OEB_D for CLK0/1, CLK2/3, CLK4/5, and CLK6/7, respectively. Alternatively, all clock outputs can be disabled using the master output enable OEB_ALL. When a Si5355 clock output bank is disabled, both outputs are driven to an active low state. When one or more banks of clock outputs are enabled or disabled, clock start and stop transitions are handled glitchlessly.

3.6. Frequency Select/Device Reset

The device frequency plan is customized using the ClockBuilder web utility. The Si5355 optionally supports up to three unique, pin-selectable configurations per device, enabling one device to replace up to three separate clock ICs. To select a particular frequency plan, set the FS pins as outlined below:

For custom Si5355 devices configured to support two frequency plans, the FS1 pin should be set as shown in Table 9:

Table 9. FS1 Pin Logic for 2 Profile Devices

FS1	Profile
0	1
1	2

For custom Si5355 devices configured to support three frequency plans, the FS1 and FS0 pins should be set as shown in Table 10:

Table 10. FS1/FS0 Pin Logic for 3 Profile Devices

FS1	FS0	Profile
0	0	Reserved
0	1	1
1	0	2
1	1	3

If a change is made to the FS pin settings, the device reset pin (RESET) must be held high for the minimum pulse width specified in Table 3 on page 5 to change the device configuration. The output clocks will be momentarily squelched until the device begins operation with the new frequency plan.

If the RESET pin is not selected in ClockBuilder as one of the five programmable pins, a power-on reset must be applied for an FS pin change to take effect.

3.7. Loss-of-Signal Alarm

The Si5355 includes an interrupt pin that monitors for both loss of PLL lock (LOL) and loss of input signal (LOS) conditions. The LOS pin is asserted whenever LOL or LOS is true. The LOS condition occurs when there is no input clock to the device. When an input clock is removed, the LOS pin will assert, and the output may drift up to 5%. The LOL condition occurs when there is a reference present but it is off in frequency by a significant amount. In this condition, the LOS pin will assert and the output will be disabled. When the input clock with an appropriate frequency is reapplied, the LOS pin will de-assert. Note that the LOS pin is an open-drain output.

3.8. CMOS Output Drivers

The Si5355 has 4 banks of outputs with each bank comprised of 2 clocks for a total of 8 CMOS outputs per device. Each of the output banks can operate from a different VDDO supply (1.8 V, 2.5 V, 3.3 V), simplifying usage in mixed supply applications. All clock outputs between 1 and 200 MHz are in-phase with minimal output-to-output skew (see Table 3 on page 5 for specification). When an output bank is disabled using any of the OEB functions, the clock outputs are stopped low.

The CMOS output driver has a controlled impedance in the range of 42 to 50 Ω, which includes an internal 22 Ω series resistor. An external series resistor is not needed when driving 50 Ω traces. If higher impedance traces are used then a series resistor may be added. A typical configuration is shown in Figure 5.

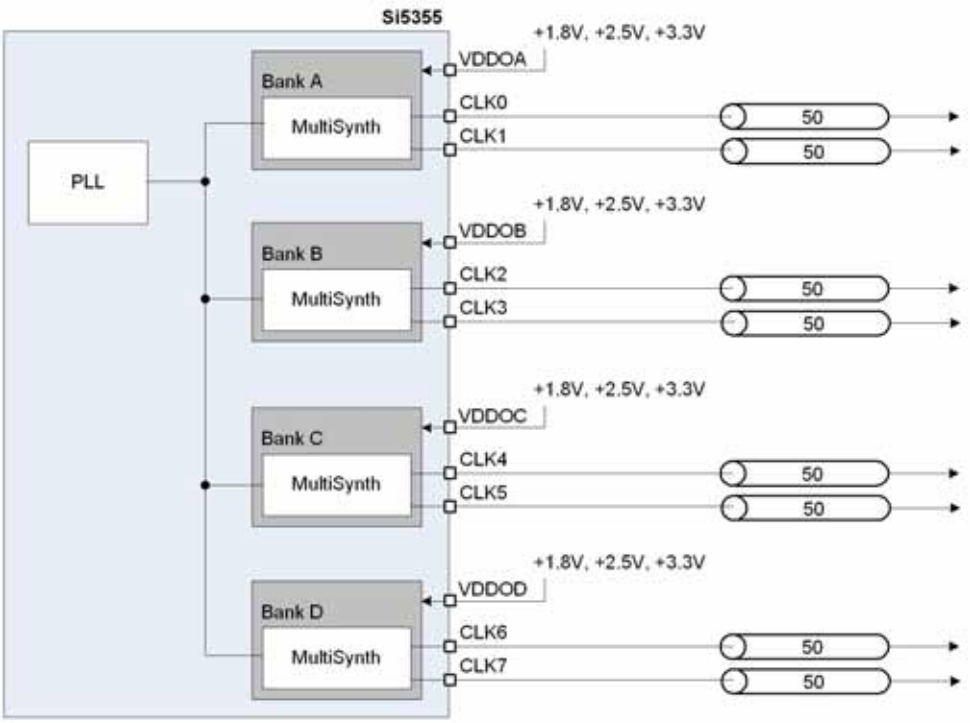


Figure 5. CMOS Output Driver Configuration

3.9. Jitter Performance

The Si5355 provides consistently low jitter for any combination of output frequencies. The device leverages a low phase noise single PLL architecture and Silicon Laboratories' patented MultiSynth fractional output divider technology to deliver excellent jitter performance guaranteed across process, temperature, and voltage. The Si5355 provides superior performance to conventional multi-PLL solutions which may suffer from degraded jitter performance depending on frequency plan and the number of active PLLs.

3.10. Power Supply Considerations

The Si5355 has 2 core supply voltage pins (V_{DD}) and 4 clock output bank supply voltage pins (V_{DDOA}–V_{DDOD}), enabling the device to be used in mixed supply applications. The Si5355 does not require ferrite beads for power supply filtering. The device has extensive on-chip power supply regulation to minimize the impact of power supply noise on output jitter. Figure 6 is a curve of additive phase jitter with power supply noise. Note that even when a significant amount of noise is applied to the device power supply, additive phase jitter is still very small.

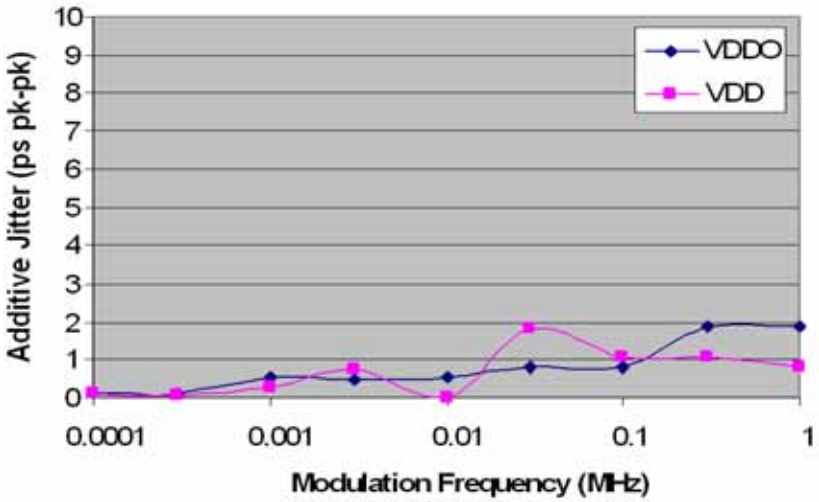


Figure 6. Peak-to-Peak Additive Phase Jitter from 100 mV Sine Wave on Supply

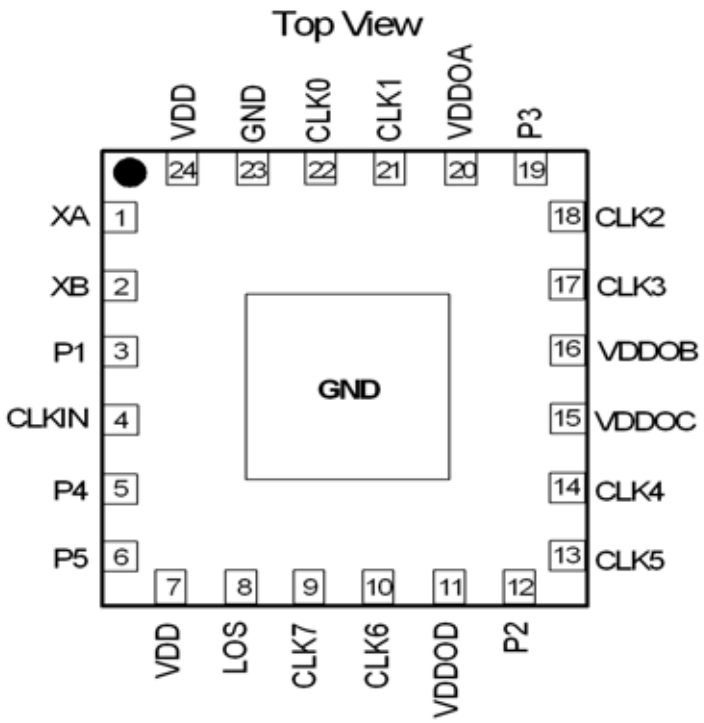
3.11. ClockBuilder Web-Customization Utility

ClockBuilder is a web-based utility available at www.silabs.com/ClockBuilder that allows hardware designers to tailor the Si5355's flexible clock architecture to meet any application-specific requirements and order custom clock samples. Through a simple point-and-click interface, users can specify any combination of input frequency and output frequencies and generate a custom part number for each application-specific configuration. There are no minimum order quantity restrictions.

ClockBuilder enables mass customization of clock generators. This allows a broader range of applications to take advantage of using application-specific pin controlled clocks, simplifying design while eliminating the firmware development required by traditional I^2C-programmable clock generators.

Based on Silicon Labs' patented MultiSynth technology, the device PLL output frequency is constant and all clock output frequencies are synthesized by the four MultiSynth fractional dividers. All PLL parameters, including divider settings, VCO frequency, loop bandwidth, charge pump current, and phase margin are internally set by the device during the configuration process. This ensures optimized jitter performance and loop stability while simplifying design.

4. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 11. Si5355 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	XA	I	**External Crystal.** If a 25 or 27 MHz crystal is used as the device frequency reference, connect it across XA and XB. If an input clock is used on pin 4, this pin should be tied to GND.
2	XB	I	**External Crystal.** If a 25 or 27 MHz crystal is used as the device frequency reference, connect it across XA and XB. If an input clock is used on pin 4, this pin should be tied to GND.
3	P1	I	**Multi-Function Input (3.3 V Tolerant).** This pin functions as a multi-function input pin. The pin function (OEB_ALL, OEB_A, OEB_B, OEB_C, OEB_D, or Reset) is user-selectable at time of configuration using the ClockBuilder configuration utility.
4	CLKIN	I	**Single-Ended Input Clock.** If a single-ended clock is used as the device frequency reference, connect it to this pin. This pin functions as a high-impedance input for CMOS clock signals. The input should be dc coupled. If a crystal is used as the device frequency reference, this pin should be tied to GND.

Table 11. Si5355 Pin Descriptions (Continued)

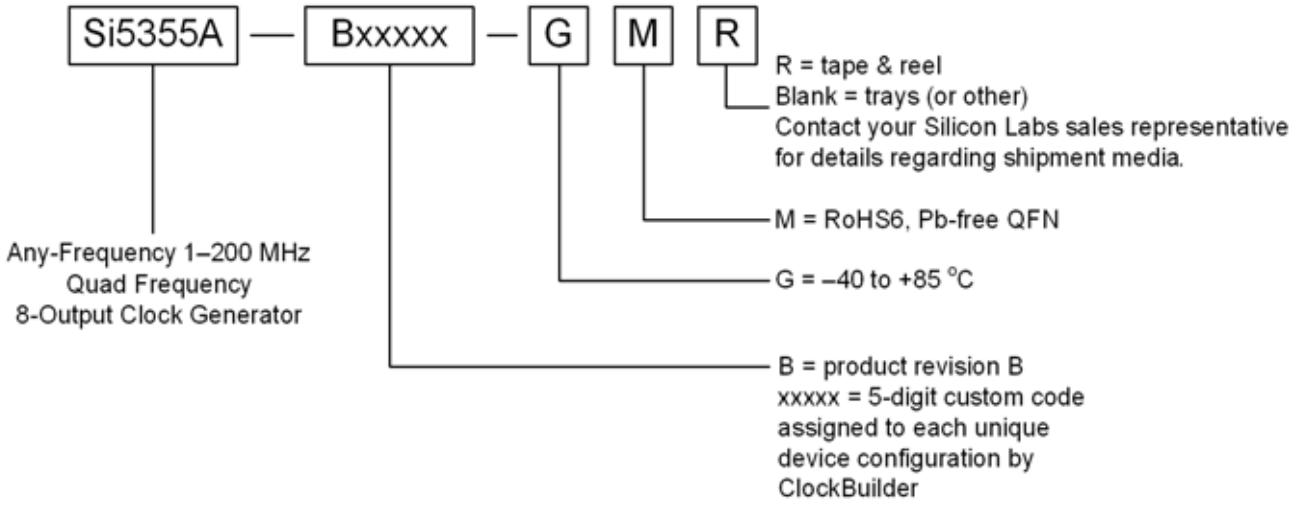
5	P4	I	**Multi-Function Input.** This pin functions as a multi-function input pin. The pin function (OEB_ALL, OEB_A, OEB_B, OEB_C, OEB_D, or Reset) is user-selectable at time of configuration using the ClockBuilder configuration utility. A resistor voltage divider is required when controlled by a signal greater than 1.3 V. See “2. Typical Application Circuit” for details.
6	P5	I	**Multi-Function Input.** This pin functions as a multi-function input pin. The pin function (OEB_ALL, OEB_A, OEB_B, OEB_C, OEB_D, or Reset) is user-selectable at time of configuration using the ClockBuilder configuration utility. A resistor voltage divider is required when controlled by a signal greater than 1.3 V. See “2. Typical Application Circuit” for details.
7	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	LOS	O	**Loss of Signal.** A typical pullup resistor of 1–4 kΩ should be used on this pin. This pin functions as an input clock signal status pin. 0 = no LOS or LOL condition 1 = LOS or LOL condition This pin is open drain and requires an external ≥1 kΩ pullup resistor.
9	CLK7	O	**Output Clock 7.** CMOS output clock. If unused, this pin must be left floating.
10	CLK6	O	**Output Clock 6.** CMOS output clock. If unused, this pin must be left floating.
11	VDDOD	VDD	**Clock Output Bank D Supply Voltage.** Power supply for clock outputs 6 and 7. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK6/7 are not used, this pin must be tied to VDD or a voltage rail of at least 1.5 V.
12	P2	I	**Multi-Function Input (3.3 V Tolerant).** This pin functions as a multi-function input pin. The pin function (OEB_ALL, OEB_A, OEB_B, OEB_C, OEB_D, or Frequency Select) is user-selectable at time of configuration using the ClockBuilder configuration utility
13	CLK5	O	**Output Clock 5.** CMOS output clock. If unused, this pin must be left floating.
14	CLK4	O	**Output Clock 4.** CMOS output clock. If unused, this pin must be left floating.
15	VDDOC	VDD	**Clock Output Bank C Supply Voltage.** Power supply for clock outputs 4 and 5. May be operated from a 1.8, 2.5 or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK4/5 are not used, this pin must be tied to VDD or a voltage rail of at least 1.5 V.
16	VDDOB	VDD	**Clock Output Bank B Supply Voltage.** Power supply for clock outputs 2 and 3. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK2/3 are not used, this pin must be tied to VDD or a voltage rail of at least 1.5 V.

Table 11. Si5355 Pin Descriptions (Continued)

17	CLK3	O	**Output Clock 3.** CMOS output clock. If unused, this pin must be left floating.
18	CLK2	O	**Output Clock 2.** CMOS output clock. If unused, this pin must be left floating.
19	P3	I	**Multi-Function Input (3.3 V Tolerant).** This pin functions as a multi-function input pin. The pin function (OEB_ALL, OEB_A, OEB_B, OEB_C, OEB_D, Frequency Select, or Reset) is user-selectable at time of configuration using the ClockBuilder configuration utility
20	VDDOA	VDD	**Clock Output Bank A Supply Voltage.** Power supply for clock outputs 0 and 1. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK0/1 are not used, this pin must be tied to VDD or a voltage rail of at least 1.5 V.
21	CLK1	O	**Output Clock 1.** CMOS output clock. If unused, this pin must be left floating.
22	CLK0	O	**Output Clock 0.** CMOS output clock. If unused, this pin must be left floating.
23	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of the device.
24	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	**Ground Pad.** This is the large pad in the center of the package. See"7. Recommended PCB Layout" on page 19 for the PCB pad sizes and ground via requirements. The device will not function unless the ground pad is properly connected to a ground plane on the PCB.

5. Ordering Guide

Use the ClockBuilder web-based utility available at www.silabs.com/ClockBuilder to specify a unique Si5355 device configuration. ClockBuilder assigns a unique 5-digit code for each unique device configuration and creates an orderable part number. The utility may also be used to order samples, place production orders and look up existing part numbers. In addition, ClockBuilder generates a data sheet addendum for each unique part number that summarizes the device input frequency, output frequencies and other configuration parameters for that specific part number.



5.1. Evaluation Board

6. Package Outline: 24-Lead QFN

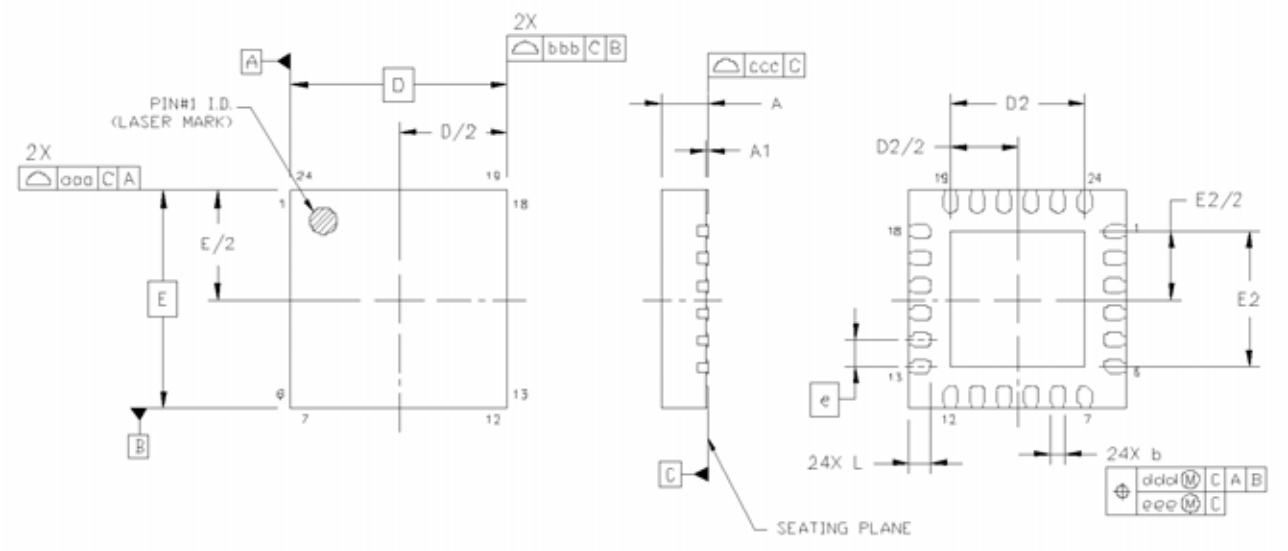


Figure 7. 24-Lead Quad Flat No-Lead (QFN)

Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Terminal base alloy: Cu.
6. Terminal plating/grid array material: Au/NiPd.
7. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.

7. Recommended PCB Layout

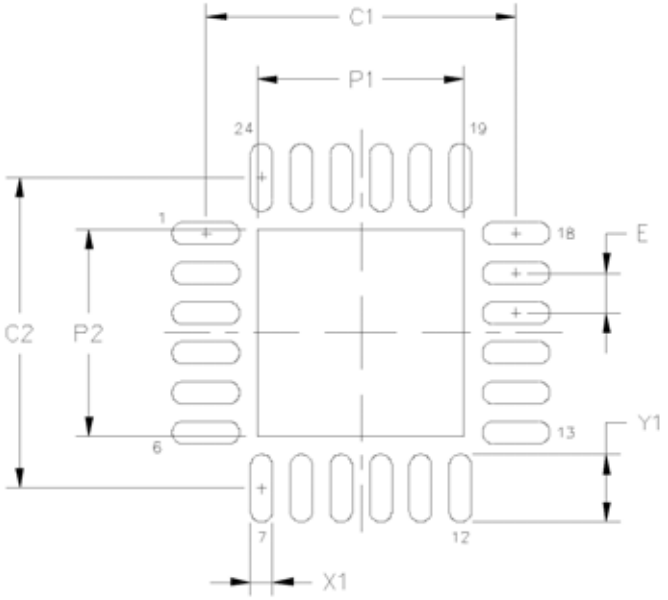


Table 13. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias. These 5 vias should have a length of no more than 20 mils to the ground plane. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Marking

8.1. Si5355 Top Marking

8.2. Top Marking Explanation

Mark Method:	Laser	
Line 1 Marking:	Device Part Number	Si5355
Line 2 Marking:	A = Frequency and configuration code. Pin-controlled, any-frequency 1-200 MHz, quad frequency, 8-Output clock generator xxxxx = NVM code for custom factory-programmed devices. See Ordering Guide section in data sheet for more information.	Axxxxx
Line 3 Marking:	R = Product revision. TTTTT = Manufacturing trace code.	RTTTTT
Line 4 Marking:	Pin 1 indicator.	Circle with 0.5 mm diameter; left-justified
	YY = Year. WW = Work week. Characters correspond to the year and work week of package assembly.	YYWW

Document Change List

Revision 0.1 to Revision 0.2

- Documentation updated to reflect CLKIN is on pin 4, not pin 3.

Revision 0.2 to Revision 0.3

- Added cycle-cycle and phase jitter specifications to Table 3 on page 5.
- Changed period jitter specification from 100 ps to 75 ps pk-pk.
- Added Theta JC specification to Table 5 on page 6.
- Updated "2. Typical Application Circuit" on page 7.
- Added Table 7 on page 9.
- Clarified device operation during an input clock loss of signal.
- Updated Recommended PCB Layout.

Revision 0.3 to Revision 1.0

- Added shipment media information for GM (vs GMR) parts.
- Changed Si5356 references to Si5355.
- Updated VDDO pin descriptions for unused clock banks. VDDOx associated with an unused clock bank should be tied to ≥ 1.5 V.
- Changed the name of output enable/disable control function pins in section 3.5 and Tables 3, 8, and 9 to align better with the actual pin functionality.
- Updated Table 2. DC Characteristics.
  - Added IDDOx specification.
  - Corrected Pn Input Resistance specification.
- Updated Table 3, “AC Characteristics,” on page 5.
  - Added 10–90% input clock rise/fall time.
  - Added LOS assert/deassert time.
  - Added note on jitter test.
  - Updated 20–80% rise/fall time with C_L = 15 pF for output clocks to the maximum value of 2.0 ns.
  - Changed Frequency Synthesis Resolution spec to the correct value of 1ppb max.
- Updated recommended crystal parameters in Table 4 on page 6 to show support for both crystals rated for either 18 or 12 pF load capacitance.
- Updated Table 6 on page 6.
  - Added Soldering profile specification
  - Corrected Input Voltage Range (V_{I2}) to 1.3 V (max).
  - Added packaging/RoHS information.
- Removed jitter spec from section “3.9. Jitter Performance” to prevent duplicating specs in “Table 3. AC Characteristics.”
- Removed output-to-output skew spec from section “3.8. CMOS Output Drivers” text to prevent duplicating specs in “Table 3. AC Characteristics.”
- Added Evaluation Board information to the Ordering Guide.

Revision 1.0 to Revision 1.1

- Updated ordering information to refer to revision B silicon.
- Updated top marking explanation in Section 8.2.

Revision 1.1 to Revision 1.2

- Removed MSL rating.

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