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Si4532DY*

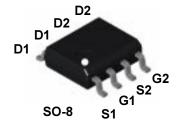
Dual N- and P-Channel Enhancement Mode Field Effect Transistor

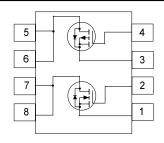
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild's propretary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.9A, $30\text{V.R}_{\text{DS(ON)}} = 0.065\Omega \text{ @V}_{\text{GS}} = 10\text{V}$ $\text{R}_{\text{DS(ON)}} = 0.095\Omega \text{ @V}_{\text{GS}} = 4.5\text{V.}$
- P-Channel -3.5A,-30V.R $_{\rm DS(ON)}$ = 0.085 Ω @V $_{\rm GS}$ = -10V ${\rm R}_{\rm DS(ON)}$ = 0.190 Ω @V $_{\rm GS}$ = -4.5V.
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings TA = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage		30	-30	V
V _{GSS}	Gate-Source Voltage		20	-20	V
I _D	Drain Current - Continuous	(Note 1a)	3.9	-3.5	Α
	- Pulsed		20	-20	
P _D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.	6	
		(Note 1b)	1		
		(Note 1c)	0.	9	
T _J , T _{STG}	Operating and Storage Junction Temperat	ure Range	-55 to	+150	∘C

Thermal Characteristics

R _{eJA}	Thermal Resistance, Junction-to-Ambient		62.5	∘C/W
Raic	Thermal Resistance, Junction-to-Case	(Note 1)	40	∘C/W

Package Marking and Ordering Information

Device Marking	Device Marking Device		Tape Width	Quantity	
4532	Si4532DY	13"	12mm	2500 units	

^{*} Die and manufacturing source subject to change without prior notification.

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Char				•			
BV _{nss}	racteristics Drain-Source Breakdown	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	N-Ch	30			V
DVDSS	Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	P-Ch	-30			V
Inss	Zero Gate Voltage Drain Current		N-Ch			1	цА
500	3	V _{DS} = -24 V, V _{GS} = 0 V	P-Ch			-1	uА
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	AΙΙ			100	nΑ
I _{GSSR}	Gate-Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	All			-100	nA
On Chai	racteristics (Note 2) Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1 1		3	V
		I					
♥ GS(th)	Cate Threehold Voltage	$V_{DS} = V_{GS}, I_D = -250 \mu A$	P-Ch	-1		-3	v
R _{DS(on)}	Static Drain-Source On	V _{GS} = 10 V, I _D = 3.9 A	N-Ch		0.053	0.065	Ω
(,	Resistance	V _{GS} = 4.5 V, I _D = 3.1 A			0.081	0.095	
		$V_{GS} = -10 \text{ V}, I_D = -2.5 \text{ A}$	P-Ch		0.06	0.085	
		$V_{GS} = -4.5 \text{ V}, I_D = -1.8 \text{ A}$			0.095	0.19	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	N-Ch	15			Α
		$V_{GS} = -10 \text{ V}, V_{DS} = -5 \text{ V}$	P-Ch	-15			
g _{FS}	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 3.9 \text{ A}$	N-Ch		7		S
		$V_{DS} = -15 \text{ V}, I_{D} = -2.5 \text{ A}$	P-Ch		5		
Dumami	- Chavastaviatica						
Dynamic C _{iss}	c Characteristics Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V,	N-Ch		235		pF
Oiss	Піриї Сарасііансе	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	P-Ch		420		þΓ
Coss	Input Capacitance	· · · · · · · · · · · · · · · · · · ·	N-Ch		150		pF
Ooss	Imput Gapacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$	P-Ch		140		þι
C _{rss}	Reverse Transfer Capacitance	f = 1.0 MHz	N-Ch		49		рF
Orss	The second of th		P-Ch	1	60		۲۰

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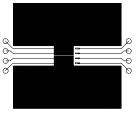
Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Switchin	g Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10 \text{ V}, I_D = 1 \text{ A},$	N-Ch		7	13	ns
		V_{GS} = 10 V, R_{GEN} = 6 Ω	P-Ch		9	18	
tr	Turn-On Rise Time		N-Ch		18	29	ns
			P-Ch		8	16	
t _{d(off)}	Turn-Off Delay Time	$V_{DD} = -10 \text{ V}, I_D = -2.5 \text{ A},$	N-Ch		15	27	ns
		$V_{GS} = -10 \text{ V. } R_{GEN} = 6 \Omega$	P-Ch		18	29	
t _f	Turn-Off Fa∥ Time]	N-Ch		0.8	8	ns
			P-Ch		6	12	
t _{rr}	Drain-Source Reverse Recovery Time	$I_F = 1.7 \text{ A, di/dt} = 100 \text{A/}_{\text{U}} \text{s}$	N-Ch			80	nS
		$I_F = -1.7 \text{ A, di/dt} = 100 \text{A/}_{\text{U}} \text{s}$	P-Ch			80	
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = 10 \text{ V}, I_{D} = 3.9 \text{ A},$	N-Ch		3.7	15	nC
		V _{GS} = 10 V	P-Ch		5	15	
Q _{gs}	Gate-Source Charge		N-Ch		0.9		nC
-		$V_{DS} = -10 \text{ V}, I_{D} = -2.5 \text{ A},$ $V_{GS} = -10 \text{ V}$	P-Ch		1.7		
$\overline{Q_{gd}}$	Gate-Drain Charge	V _{GS} = -10 V	N-Ch		1.9		nC
· ·			P-Ch		1.8		

Drain-Source Diode Characteristics and Maximum Ratings

Diaiii-	Diain-30urce Dioue Onaracteristics and Maximum Natings						
Is	Maximum Continuous Drain-Sour	Maximum Continuous Drain-Source Diode Forward Current			1.7	Α	
			P-Ch		-1.7	Α	
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_S = 1.7 A$ (Note 2)	N-Ch	0.75	1.2	V	
		V _{GS} = 0 V, I _S = -1.7 A	P-Ch	-0.75	-1.2	٧	

Notes:

1. R_{BJA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78° C/W when mounted on a 0.05 in² pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in² pad of 2 oz. copper.



c) 135° C/W when mounted on a minimum mounting pad.

Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width $\leq\!300\,\mu\text{s},\,\text{Duty Cycle}\,\!\leq\!2.0\%$

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