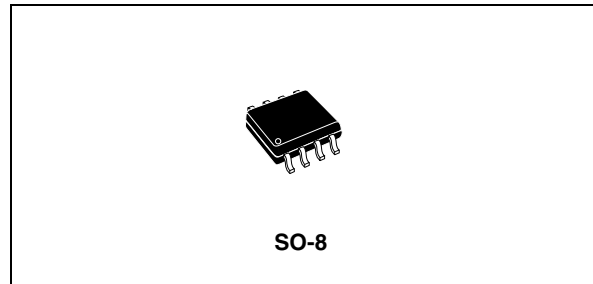


Advanced IGBT/MOSFET driver

Features

- 1.7 A sink / 1.3 A source (typ) current capability
- Active Miller clamp feature
- Desaturation detection
- Adjustable turn-on delay
- UVLO protection
- 2k V ESD protection



Applications

- 1200 V 3-phase inverter
- Motor control systems
- UPS

Description

This device is an advanced gate driver for IGBTs and power MOSFETs. Control and protection functions are included and allow the design of high reliability systems.

The innovative active Miller clamp function eliminates the need for negative gate drive in most applications and allows the use of a simple bootstrap supply for the high side driver.

The TD352 includes an adjustable turn-on delay. This feature can be used to implement reliable deadtime between high and low sides of a half bridge. An external resistor and capacitor are used to provide accurate timing.

Table 1. Device summary

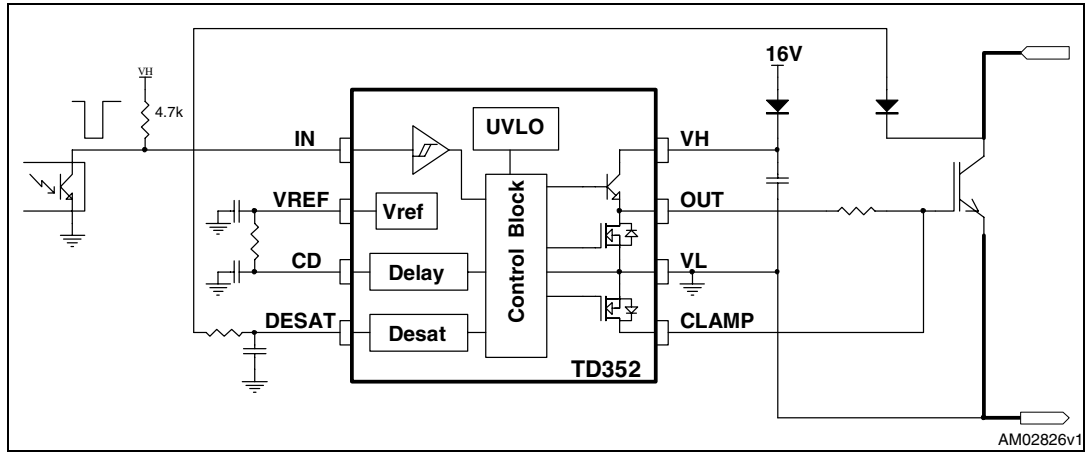
Order codes	Temperature range	Package	Packaging
TD352ID	-40°C, +125°C	SO-8	Tube
TD352IDT			Tape and reel

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1 Block diagram

Figure 1. TD352 block diagram



2 Pin connections

Figure 2. Pin connections (top view)

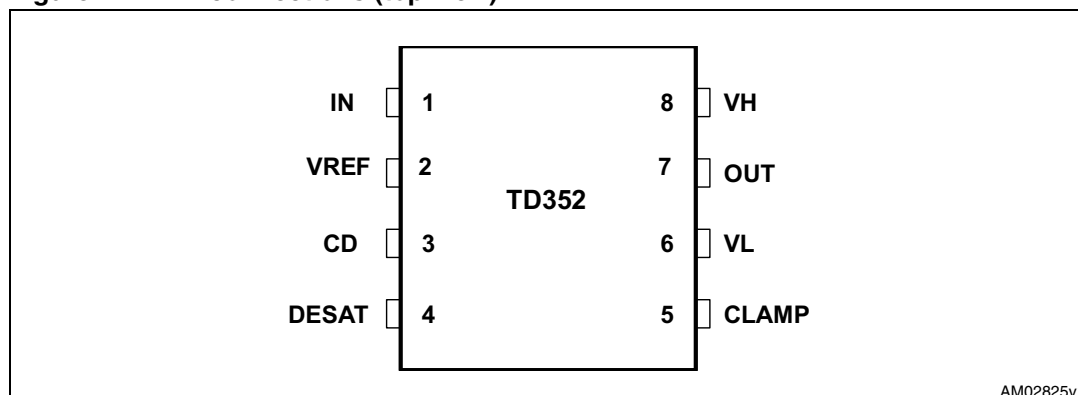


Table 2. Pin description

Pin n°	Name	Type	Function
IN	1	Analog input	Input
VREF	2	Analog output	+5 V reference voltage
CD	3	Timing capacitor	Turn on delay
DESAT	4	Analog input	Desaturation protection
CLAMP	5	Analog output	Miller clamp
VL	6	Power supply	Signal ground
OUT	7	Analog output	Gate drive output
VH	8	Power supply	Positive supply

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _H L	Maximum supply voltage (V _H - V _L)	28	V
V _{out}	Voltage on OUT, CLAMP, DESAT pins	V _L -0.3 to V _H +0.3	V
V _{other}	Voltage on other pins (IN, CD, VREF)	-0.3 to 7	V
P _d	Power dissipation	500	mW
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Maximum junction temperature	150	°C
R _{thJA}	Thermal resistance junction-ambient	150	°C/W
ESD	Electrostatic discharge (HBM)	2	kV

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V _H	Positive supply voltage vs. V _L	UVLO to 26	V
T _{oper}	Operating free air temperature range	-40 to 125	°C

4 Electrical characteristics

$T_A = -20$ to 125 °C, $V_H = 16$ V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Input						
V_{ton}	IN turn-on threshold voltage		0.8	1.0		V
V_{toff}	IN turn-off threshold voltage			4.0	4.2	V
I_{inp}	IN input current	IN input voltage < 4.5V			1	μ A
Voltage reference ⁽¹⁾						
V_{ref}	Voltage reference	$T = 25^\circ\text{C}$	4.85	5.00	5.15	V
I_{ref}	Maximum output current		10			mA
Clamp						
V_{tclamp}	CLAMP pin voltage threshold			2.0		V
V_{CL}	Clamp low voltage	$I_{csink} = 500\text{mA}$			2.5	V
Delay						
V_{tdel}	Voltage threshold			2.5		V
R_{del}	Discharge resistor	$I = 1\text{mA}$			500	Ω
Desaturation protection						
V_{des}	Desaturation threshold			VH-2		V
I_{des}	Source current			250		μ A
Output						
I_{sink}	Output sink current	$V_{out} = 6\text{V}$	1000	1700		mA
I_{src}	Output source current	$V_{out} = \text{VH}-6\text{V}$	750	1300		mA
V_{OL1}	Output low voltage 1	$I_{osink} = 20\text{mA}$			0.35	V
V_{OL2}	Output low voltage 2	$I_{osink} = 500\text{mA}$			2.5	V
V_{OH1}	Output high voltage 1	$I_{osource} = 20\text{mA}$	VH-2.5			V
V_{OH2}	Output high voltage 2	$I_{osource} = 500\text{mA}$	VH-4.0			V
t_r	Rise time	$C_L = 1\text{nF}$, 10% to 90%			100	ns
t_f	Fall time	$C_L = 1\text{nF}$, 90% to 10%			100	ns
t_{don}	Turn on propagation delay	10% OUT change: $R_d = 4.7\text{k}\Omega$, no C_d $R_d = 11\text{k}\Omega$, $C_d = 220\text{pF}$	1.8	2.0	500 2.2	ns μ s
t_{doff}	Turn off propagation delay	10% OUT change			400	ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Under voltage lockout (UVLO)						
UVLOH	UVLO top threshold		10	11	12	V
UVLOL	UVLO bottom threshold		9	10	11	V
V_{hyst}	UVLO hysteresis	UVLOH-UVLOL	0.5	1		V
Supply current						
I_{in}	Quiescent current	OUT = 0V; no load			2.5	mA

1. Recommended capacitor range on VREF pin is 10 nF to 100 nF

5 Functional description

5.1 Input stage

The TD352 IN input is internally clamped at about 5 V to 7 V. The input is triggered by the signal edge. When using an open collector optocoupler, the resistive pull-up resistor can be connected to either VREF or VH.

Recommended pull-up resistor value with VH=16 V is from 4.7 kΩ to 22 kΩ

5.2 Voltage reference

A voltage reference is used to create accurate timing for the turn-on delay with external resistor and capacitor.

A decoupling capacitor (10 nF to 100 nF) on the VREF pin is required to ensure good noise rejection.

5.3 Active Miller clamp

The TD352 offers an alternative solution to the problem of Miller current in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, the TD352 uses a dedicated CLAMP pin to control the Miller current. When the IGBT is off, a low impedance path is established between the IGBT gate and emitter to carry the Miller current, and the voltage spike on the IGBT gate is greatly reduced.

During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2 V (relative to VL). The clamp voltage is VL+4V max for a Miller current up to 500 mA. The clamp is disabled when the IN input is triggered again.

The CLAMP function does not affect the turn-off characteristic, but only keeps the gate at low level throughout the off time. The main benefit is that negative voltage can be avoided in many cases, allowing a bootstrap technique for the high side driver supply.

5.4 Turn-on delay

Turn-on (T_a) delay is programmable through external resistor R_d and capacitor C_d for accurate timing. T_a is approximately given by (see [Figure 5](#)):

$$T_a (\mu\text{s}) = 0.7 * R_d (\text{k}\Omega) * C_d (\text{nF})$$

The turn-on delay can be disabled by connecting the CD pin to VREF with a 4.7 kΩ resistor.

Input signals with ON-time smaller than T_a are ignored.

5.5 Desaturation protection

Desaturation protection ensures the protection of the IGBT in the event of overcurrent. When the DESAT voltage goes higher than $V_H - 2V$, the TD352 OUT pin is driven low. The fault state is only exited after a power-down and power-up cycle.

A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by an internal current source and external C_{des} capacitor. The T_{bdes} blanking time value is given by:

$$T_{bdes} = V_{des} * C_{des} / I_{des}$$

At $V_H = 16V$, T_{bdes} is approximately given by:

$$T_{bdes} (\mu s) = 0.056 * C_{des} (pF)$$

5.6 Output stage

The output stage is able to sink/source 1.7 A/1.3 A (typical) at 25 °C and 1.0 A/0.75 A min. over the full temperature range. This current capability is specified near the usual IGBT Miller plateau.

5.7 Undervoltage protection

Undervoltage detection protects the application in the event of a low V_H supply voltage (during startup or a fault situation). During undervoltage, the OUT pin is driven low (active pull-down for $V_H > 2V$, and passive pull-down for $V_H < 2V$).

Figure 3. Undervoltage protection

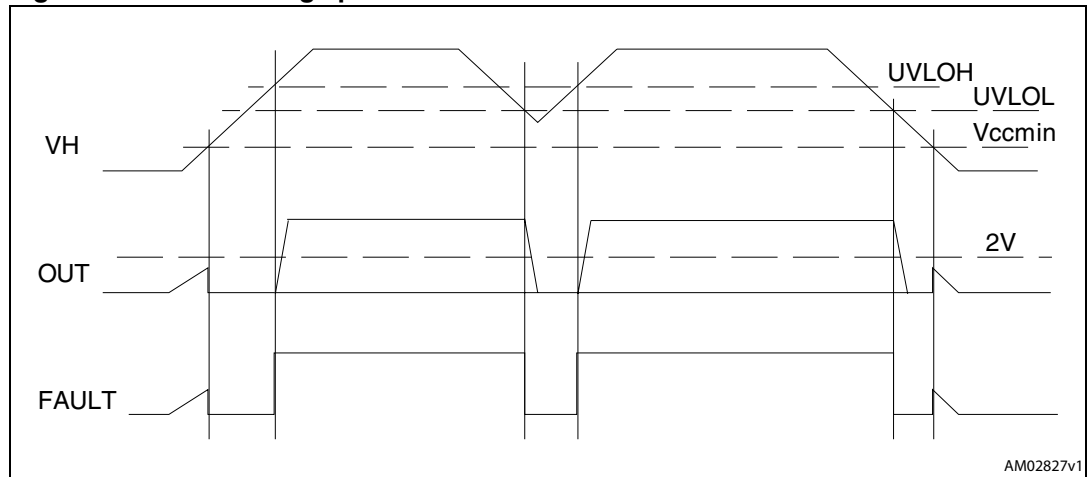
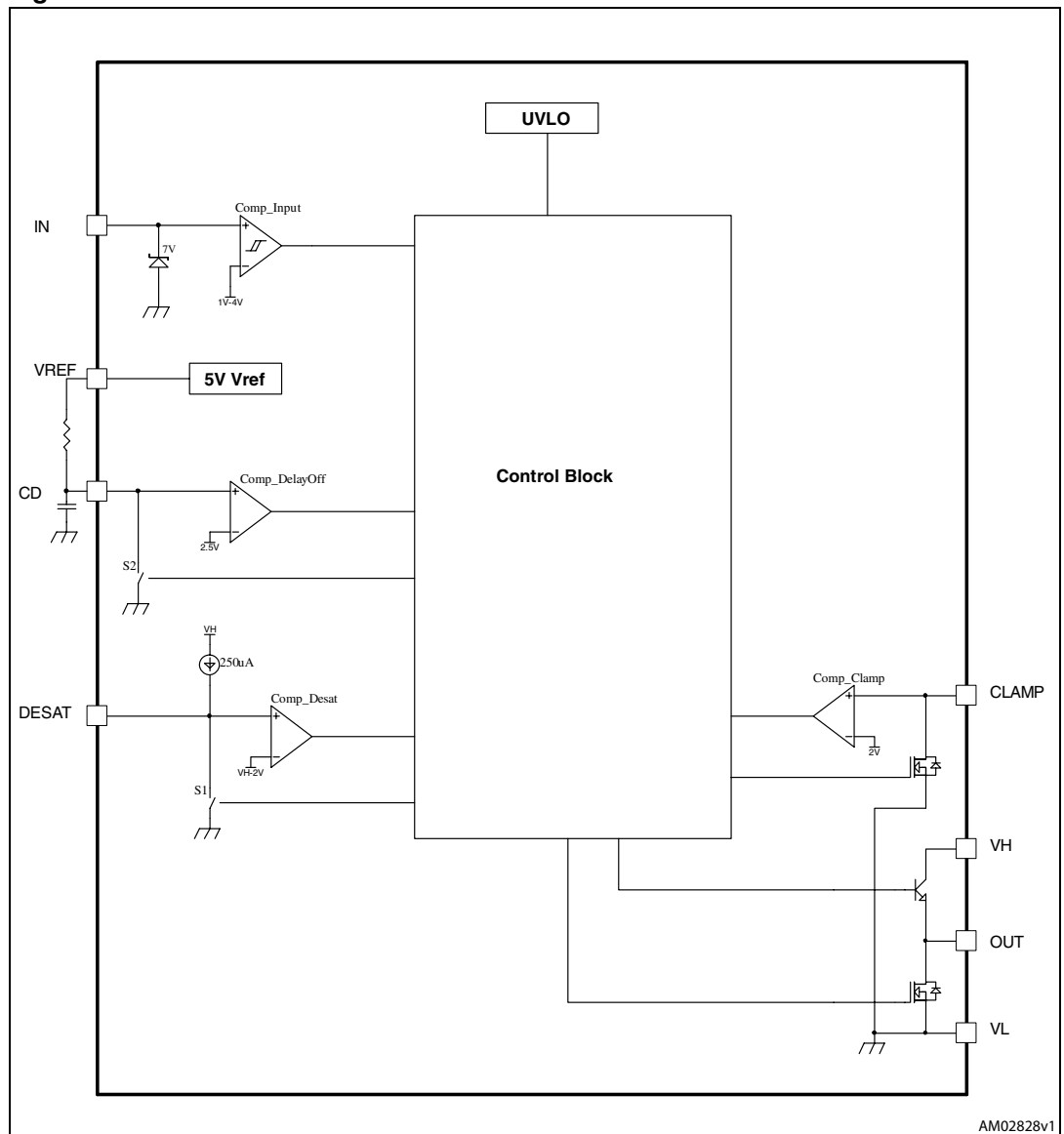
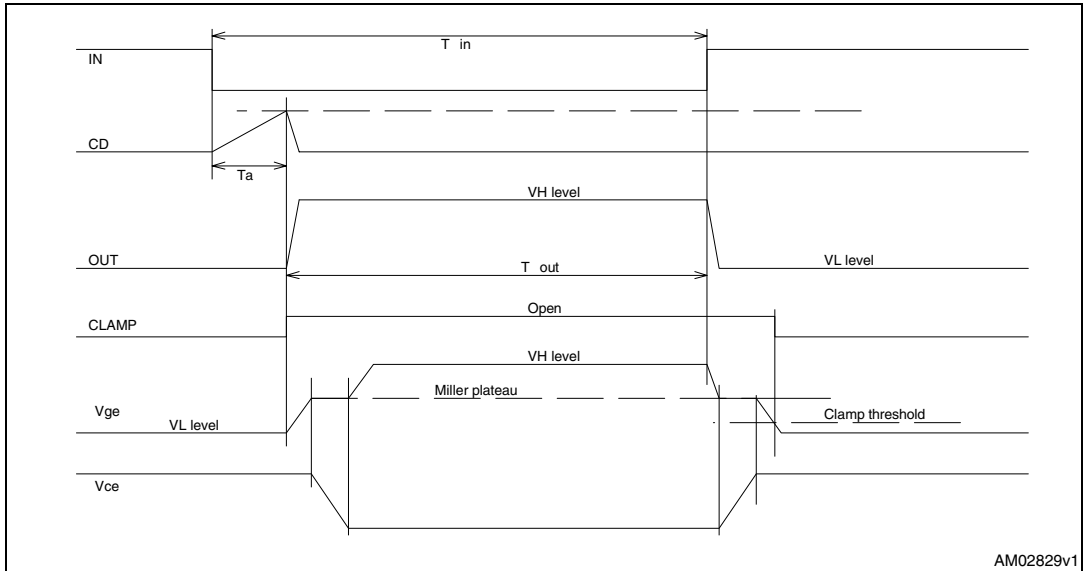


Figure 4. Detailed internal schematic



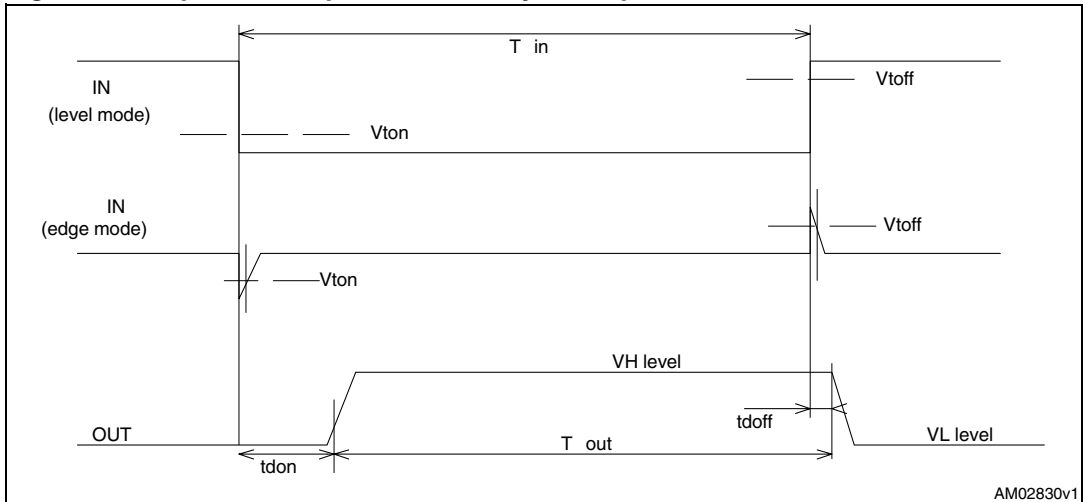
6 Timing diagrams

Figure 5. General turn-on and turn-off sequence



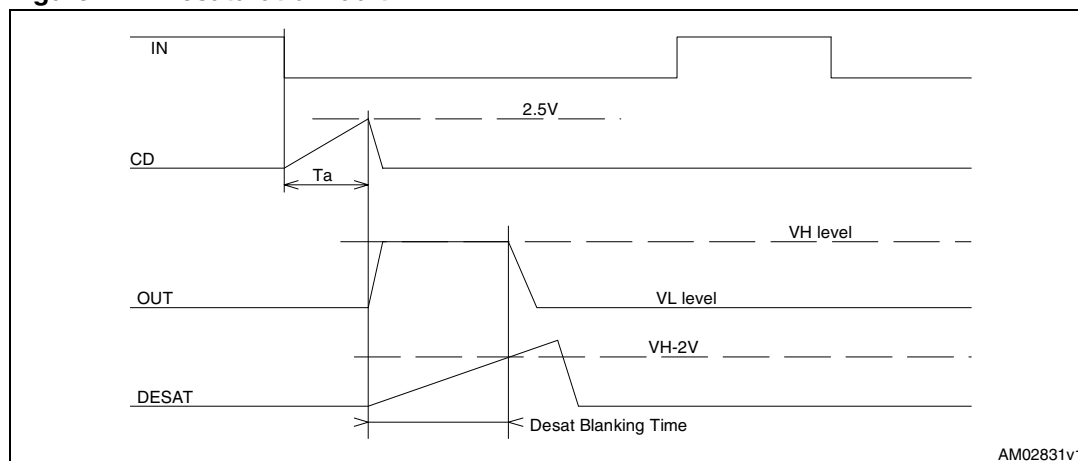
AM02829v1

Figure 6. Input and output waveform dynamic parameters



AM02830v1

Figure 7. Desaturation fault



7 Typical performance curves

Figure 8. Quiescent current vs temperature

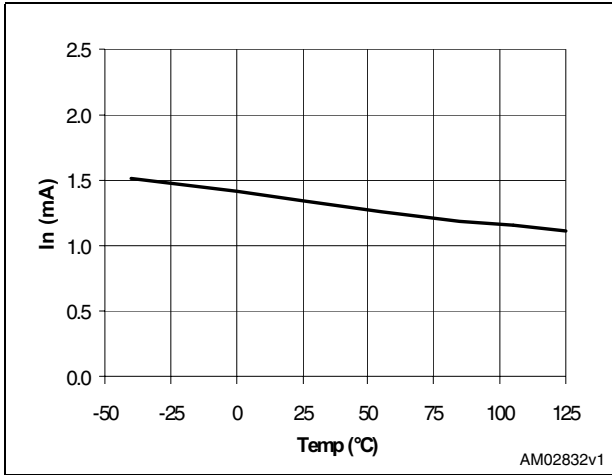


Figure 9. Rdel resistance vs temperature

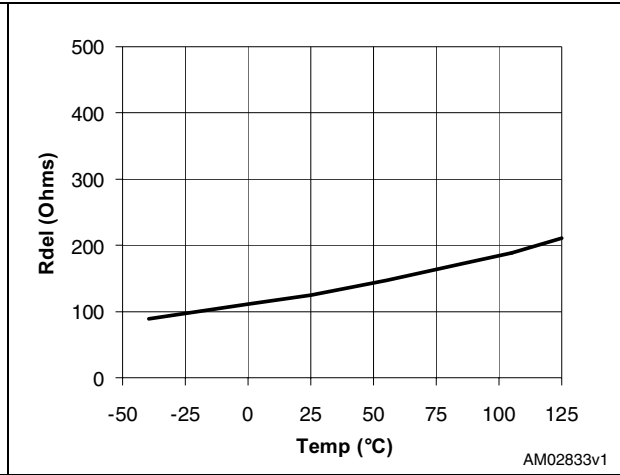


Figure 10. Low level output voltage vs temp.

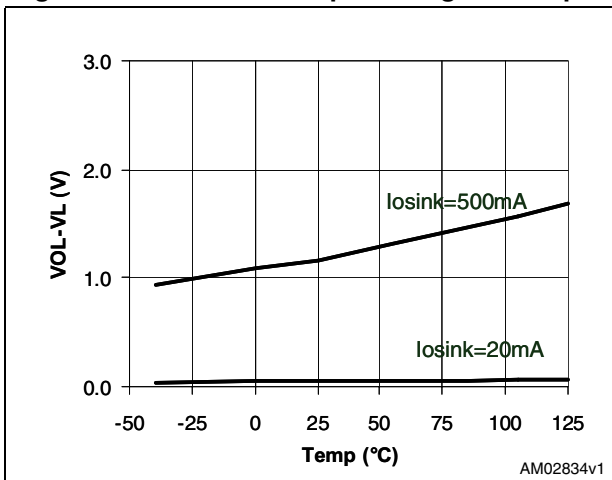


Figure 11. High level output voltage vs temp.

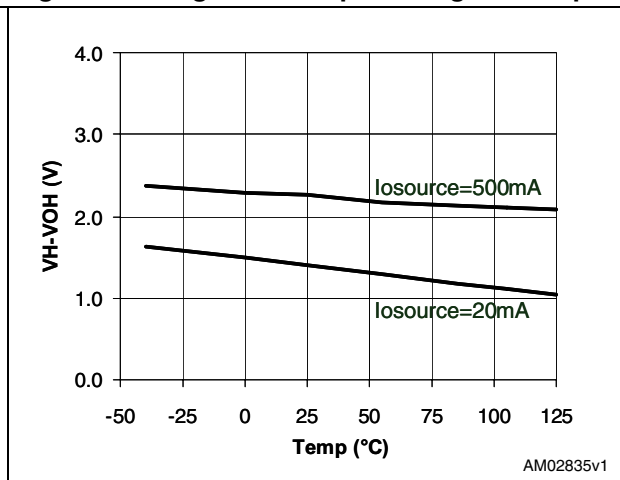


Figure 12. Sink current vs temperature

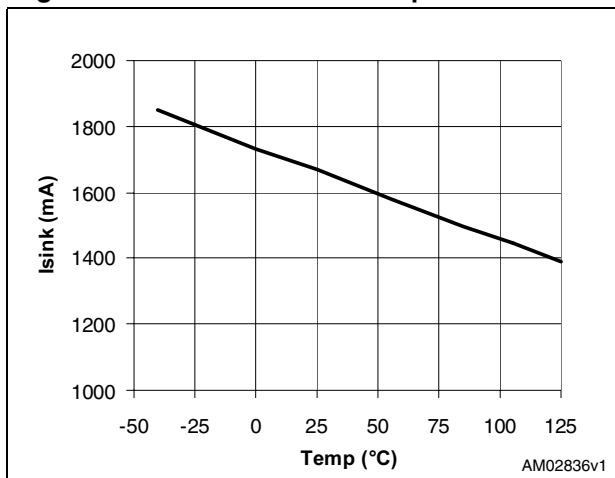
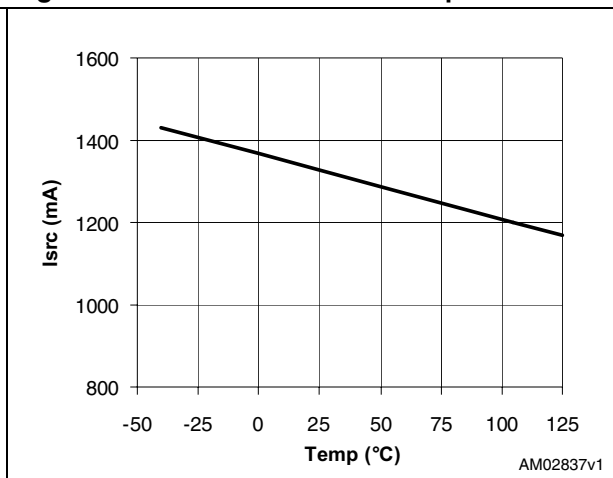


Figure 13. Source current vs temperature



8 Application diagrams

Figure 14. Single supply IGBT drive with active Miller clamp and DESAT protection

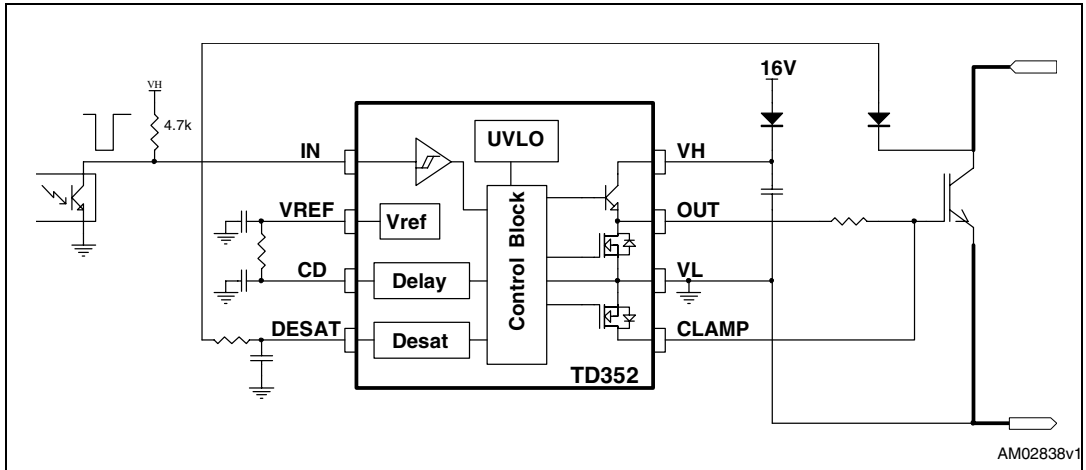


Figure 15. Use of DESAT input for direct overcurrent detection

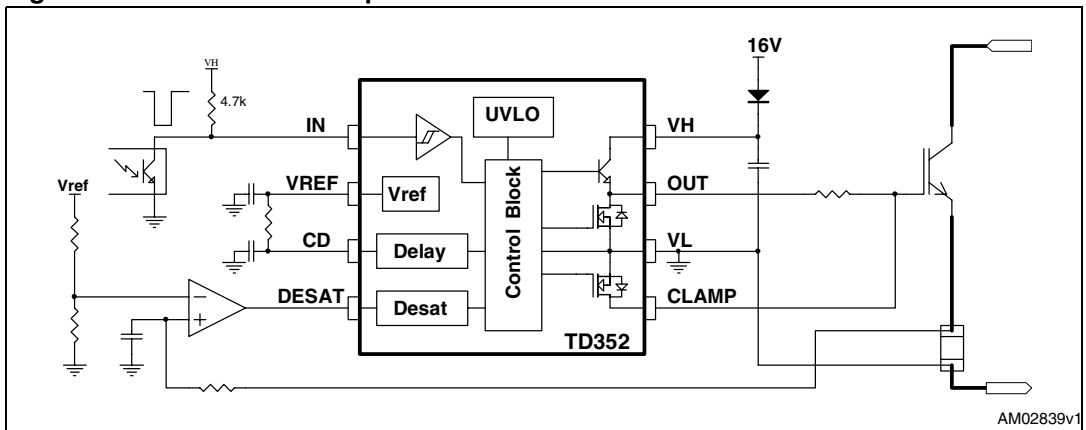
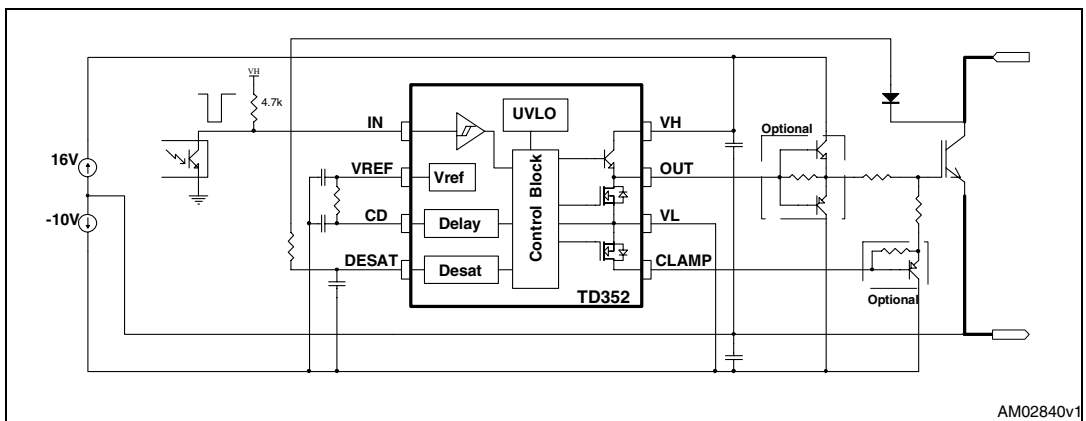


Figure 16. Large IGBT drive with negative voltage gate drive and optional current buffers



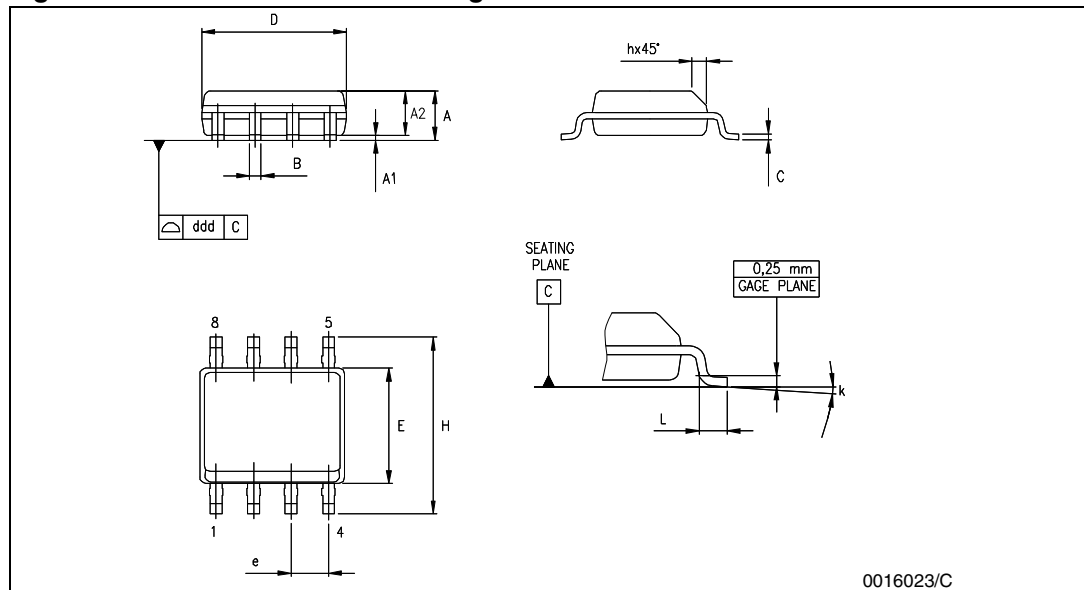
9 Package mechanical data

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Table 6. SO-8 mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	(max.) 8					
ddd			0.1			0.04

Figure 17. SO-8 mechanical drawing



0016023/C

10 Revision history

Table 7. Document revision history

Date	Revision	Changes
01-Nov-2004	1	Initial release
13-Jun-2011	2	Deleted order code TD352IN. Content reworked to improve readability.

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