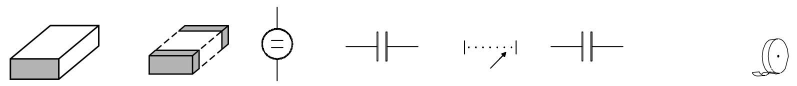
Multilayer ceramic capacitors

Array capacitors, C0G

Date: October 2006

Ordering code system



B37830	R	0	101	K	0	2	1

Packaging

1 ≙ cardboard tape, 180-mm reel
3 ≙ cardboard tape, 330-mm reel

2 ≙ 2-fold array   4 ≙ 4-fold array

Internal coding: 0 or decimal place for cap. values <10 pF

Capacitance tolerance

J ≙ ± 5%
K ≙ ±10% (standard for C0G)
M ≙ ±20% (standard for X7R)

Capacitance, coded (example)

100 ≙ $\underline{10} \cdot 10^0$ pF = 10 pF
101 ≙ $\underline{10} \cdot 10^1$ pF = 100 pF
220 ≙ $\underline{22} \cdot 10^0$ pF = 22 pF

Rated voltage

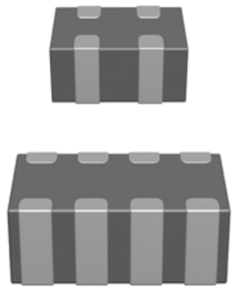
Rated voltage [VDC]	16	25	50
Code	9	0	5

Internal coding “R“ indicates array capacitor

Type and size

Chip size (**inch** / mm)	Temperature characteristic C0G	X7R
0405 / 1012	B37830	B37831
0508 / 1220	B37940	B37941
0612 / 1632	B37871	B37872

SMD



Features

- Reduction of mounting time and mounting costs
- Space saving on the PCB
- To AEC-Q200

Applications

- Suitable for electronic circuits with parallel line layout
- Coupling and filtering, particularly in RF circuits
- Resonant circuits
- Filter circuits

Termination

- For soldering: Nickel barrier terminations (Ni)

Options

- Alternative capacitance tolerances available on request

Delivery mode

- Cardboard tape,180-mm and 330-mm reel available

Electrical data

Temperature characteristic		C0G	
Climatic category (IEC 60068-1)		55/125/56	
Standard		EIA	
Dielectric		Class 1	
Rated voltage	V_R	25, 50	VDC
Test voltage	V_{test}	$2.5 \cdot V_R$/5 s	VDC
Capacitance range / E series	C_R	10 pF … 1.0 nF (E6)	
Temperature coefficient		$0 \pm 30 \cdot 10^{-6}$/K	
Dissipation factor (limit value)	$\tan \delta$	$<1.0 \cdot 10^{-3}$	
Insulation resistance[1)] at + 25 °C	R_{ins}	$>10^5$	MΩ
Insulation resistance[1)] at +125 °C	R_{ins}	$>10^4$	MΩ
Time constant[1)] at + 25 °C	τ	>1000	s
Time constant[1)] at +125 °C	τ	>100	s
Operating temperature range	T_{op}	–55 … +125	°C
Ageing		none	

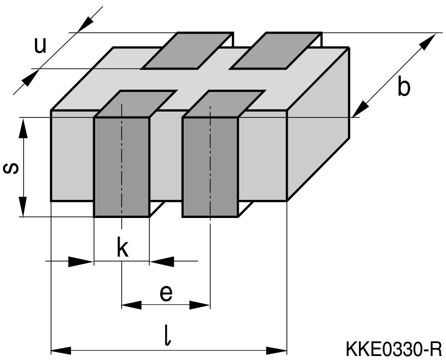
1) For C_R >10 nF the time constant $\tau = C \cdot R_{ins}$ is given.

Capacitance tolerances

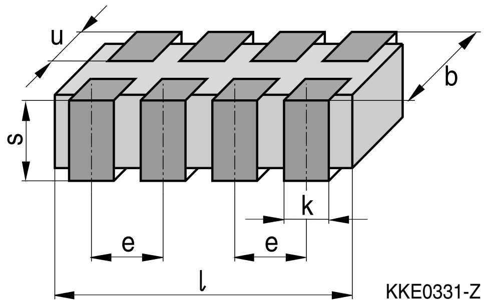
Code letter	J	K (standard)
Tolerance	±5%	±10%

Dimensional drawing

2-fold array (case size 0405)



4-fold array (case sizes 0508 and 0612)



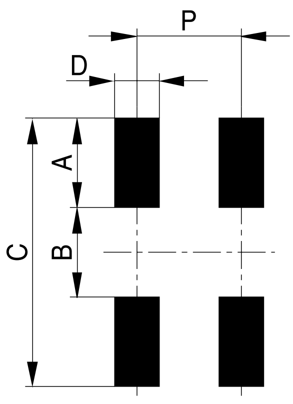
Dimensions (mm)

		2-fold array	4-fold array	
Case size	(inch) (mm)	0405 1012	0508 1220	0612 1632
l		1.37 ±0.15	2.00 ±0.2	3.20 ±0.2
b		1.00 +0/–0.15	1.25 ±0.15	1.60 ±0.2
s		0.70 max.	0.85 ±0.1	0.85 ±0.1
k		0.36 ±0.1	0.30 ±0.1	0.40 ±0.15
e		0.64	0.50 ±0.1	0.80 ±0.15
u		0.20 ±0.1	0.20 +0.3/–0.1	0.20 +0.3/–0.1

Tolerances to CECC 32101-801

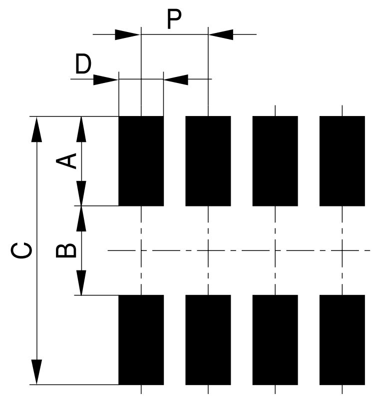
Recommended solder pad

2-fold array (case size 0405)



KKE0302-L

4-fold array (case sizes 0508 and 0612)

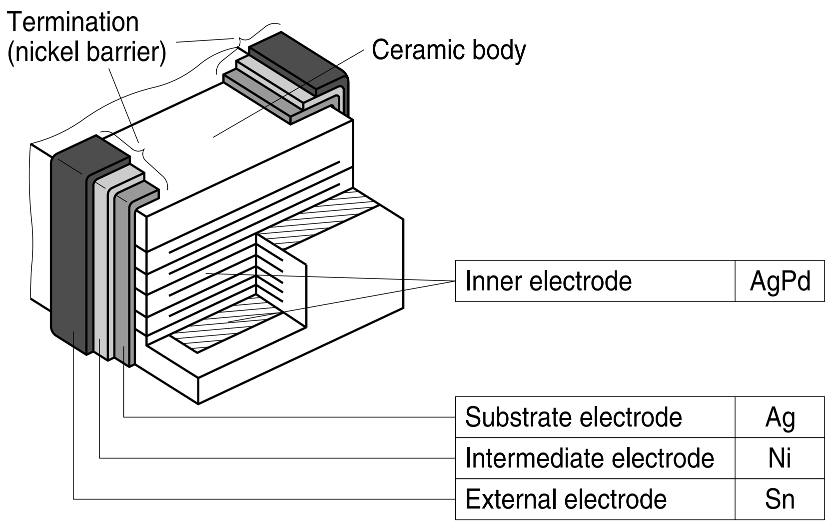


KKE0309-9

Recommended dimensions (mm) for reflow soldering

Case size	(inch/mm)	Type	A	B	C	D	P
	0405/1012	2-fold array	0.50 … 0.55	0.45 … 0.50	1.45 … 1.60	0.30 … 0.35	0.64 ±0.10
	0508/1220	4-fold array	0.50 … 0.70	0.60 … 0.70	1.60 … 2.10	0.25 … 0.35	0.50 ±0.005
	0612/1632	4-fold array	0.70 … 0.90	0.80 … 1.00	2.20 … 2.80	0.30 … 0.40	0.80 ±0.005

Termination



KKE0366-S-E

Product range array capacitors, C0G

	2-fold arrays		4-fold arrays			
Size1) **inch** mm	**0405** 1012		**0508** 1220		**0612** 1632	
Type	B37830		B37940		B37871	
V_R (VDC) / C_R	25		50		50	
10 pF	■		■		■	
15 pF	■		■		■	
22 pF	■		■		■	
33 pF	■		■		■	
47 pF	■		■		■	
68 pF	■		■		■	
100 pF	■		■		■	
150 pF	■		■		■	
180 pF	■					
220 pF			■		■	
330 pF					■	
470 pF					■	
680 pF					■	
1.0 nF					■	

1) l × b (inch) / l × b (mm)

Ordering codes and packing for C0G arrays, 25 VDC, nickel barrier terminations

C_R[1)]	Ordering code[2)]	Chip thickness mm	Cardboard tape, ∅ 180-mm reel * ≙ 1 pcs/reel	Cardboard tape, ∅ 330-mm reel * ≙ 3 pcs/reel
Case size 0405, 25 VDC, 2-fold arrays				
10 pF	B37830R0100K02*	0.6 ±0.1	5000	20000
15 pF	B37830R0150K02*	0.6 ±0.1	5000	20000
22 pF	B37830R0220K02*	0.6 ±0.1	5000	20000
33 pF	B37830R0330K02*	0.6 ±0.1	5000	20000
47 pF	B37830R0470K02*	0.6 ±0.1	5000	20000
68 pF	B37830R0680K02*	0.6 ±0.1	5000	20000
100 pF	B37830R0101K02*	0.6 ±0.1	5000	20000
150 pF	B37830R0151K02*	0.6 ±0.1	5000	20000
180 pF	B37830R0181K02*	0.6 ±0.1	5000	20000

1) Other capacitance values on request.
2) The table contains the ordering codes for the standard capacitance tolerance.
For other available capacitance tolerances see page 128.

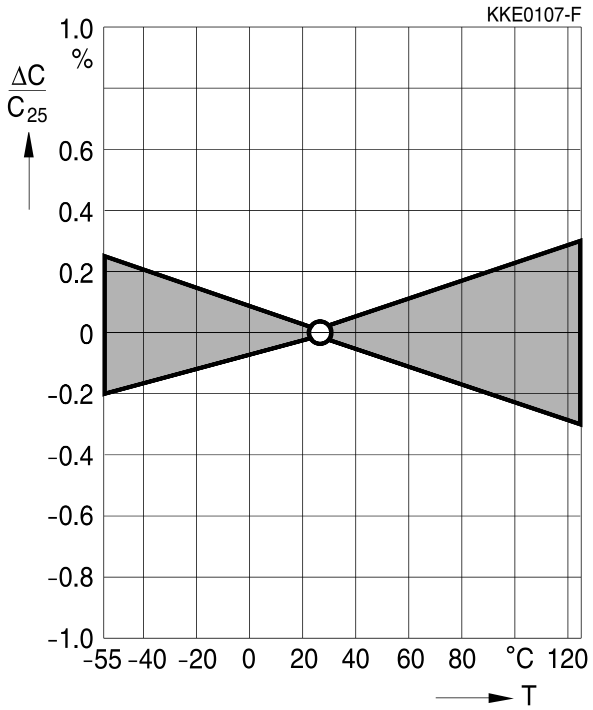
Ordering codes and packing for C0G arrays, 50 VDC, nickel barrier terminations

C_R[1)]	Ordering code[2)]	Chip thickness mm	Cardboard tape, ∅ 180-mm reel * ≙ 1 pcs/reel	Cardboard tape, ∅ 330-mm reel * ≙ 3 pcs/reel
Case size 0508, 50 VDC, 4-fold arrays				
10 pF	B37940R5100K04*	0.85 ±0.1	4000	16000
15 pF	B37940R5150K04*	0.85 ±0.1	4000	16000
22 pF	B37940R5220K04*	0.85 ±0.1	4000	16000
33 pF	B37940R5330K04*	0.85 ±0.1	4000	16000
47 pF	B37940R5470K04*	0.85 ±0.1	4000	16000
68 pF	B37940R5680K04*	0.85 ±0.1	4000	16000
100 pF	B37940R5101K04*	0.85 ±0.1	4000	16000
150 pF	B37940R5151K04*	0.85 ±0.1	4000	16000
220 pF	B37940R5221K04*	0.85 ±0.1	4000	16000
Case size 0612, 50 VDC, 4-fold arrays				
10 pF	B37871R5100K04*	0.85 ±0.1	4000	16000
15 pF	B37871R5150K04*	0.85 ±0.1	4000	16000
22 pF	B37871R5220K04*	0.85 ±0.1	4000	16000
33 pF	B37871R5330K04*	0.85 ±0.1	4000	16000
47 pF	B37871R5470K04*	0.85 ±0.1	4000	16000
68 pF	B37871R5680K04*	0.85 ±0.1	4000	16000
100 pF	B37871R5101K04*	0.85 ±0.1	4000	16000
150 pF	B37871R5151K04*	0.85 ±0.1	4000	16000
220 pF	B37871R5221K04*	0.85 ±0.1	4000	16000
330 pF	B37871R5331K04*	0.85 ±0.1	4000	16000
470 pF	B37871R5471K04*	0.85 ±0.1	4000	16000
680 pF	B37871R5681K04*	0.85 ±0.1	4000	16000
1.0 nF	B37871R5102K04*	0.85 ±0.1	4000	16000

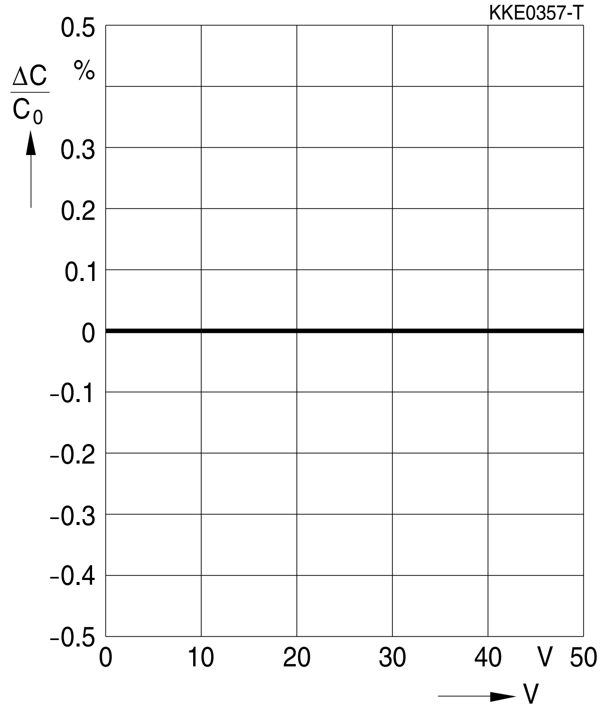
1) Other capacitance values on request.
2) The table contains the ordering codes for the standard capacitance tolerance.
For other available capacitance tolerances see page 128.

Typical characteristics1)

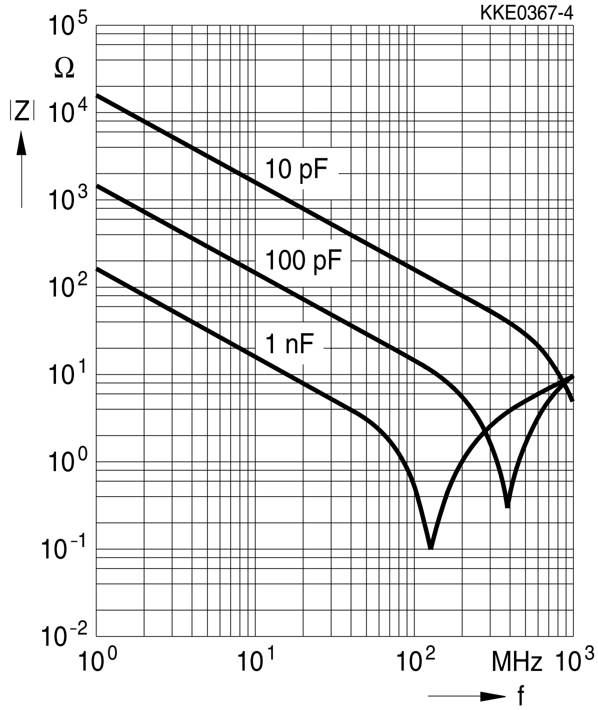
Capacitance change $\Delta C/C_{25}$ versus temperature T (tolerance range ▇)



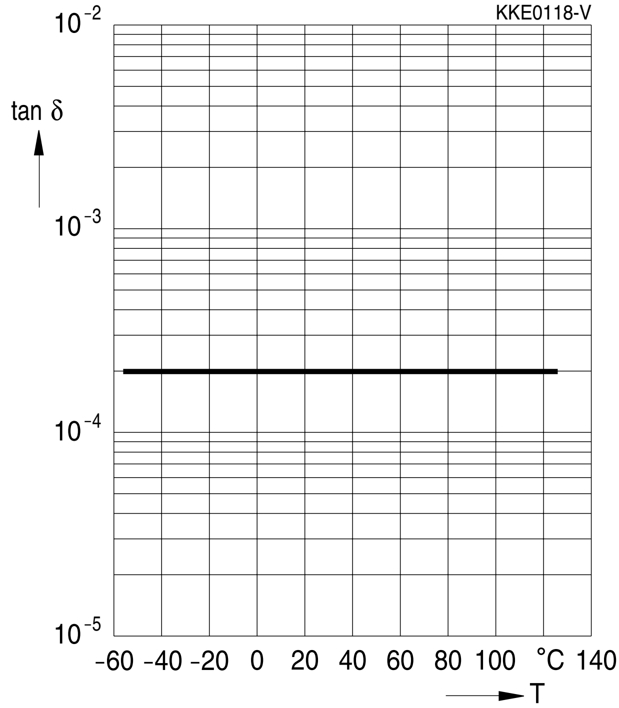
Capacitance change $\Delta C/C_0$ versus superimposed DC voltage V



Impedance |Z| versus frequency f



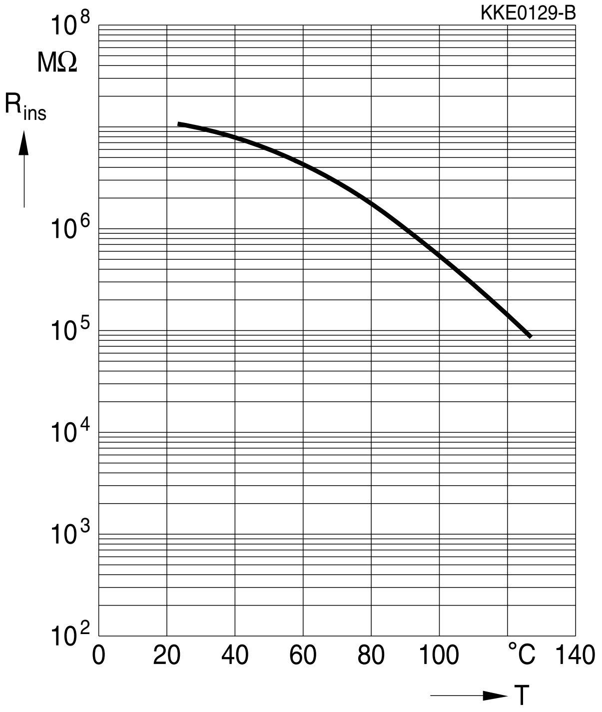
Dissipation factor tan δ versus temperature T



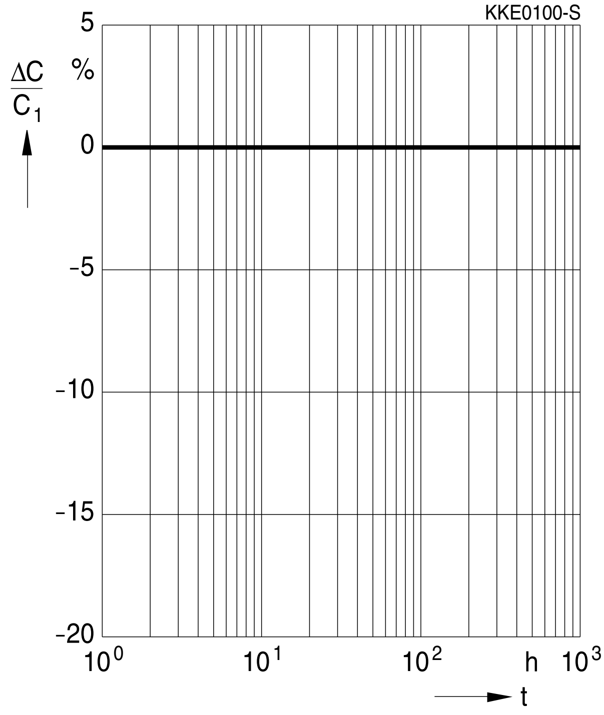
1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Typical characteristics 1)

Insulation resistance R_{ins} versus temperature T



Capacitance change $\Delta C/C_1$ versus time t



1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc_impedance.

Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

1. Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter “Effects on mechanical, thermal and electrical stress”, point 1.4).
5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter “Reliability”).

The following should be considered in circuit board design

1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
2. At least FR4 circuit board material should be used.
3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).

The following should be considered in the placement process

1. Ensure correct positioning of the ceramic capacitor on the solder pad.
2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
3. Support the circuit board and reduce the placement forces.
4. A board should not be straightened (manually) if it has been distorted by soldering.
5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter “Soldering directions”).
10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
11. Ensure the correct solder meniscus height and solder quantity.
12. Ensure correct dosing of the cement quantity.
13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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The following applies to all products named in this publication:

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2. We also point out that **in individual cases, a malfunction of passive electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of a passive electronic component.
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