ZMDI
The Analog Mixed Signal Company

User Guide

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ZSPM8010-KIT Open-Loop **Evaluation Board**

For Evaluation of the ZSPM9010 High-Performance DrMOS

Power and Precision

Restrictions:

Zentrum Mikroelektronik Dresden AG's ZSPM8010-KIT Open-Loop Evaluation Board is designed for evaluation of the ZSPM9010, laboratory setup, and module development only. The Evaluation Board must not be used for module production and production test setups.

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Important Safety Reminder: These procedures can result in high currents, which can cause severe injury or death and/or equipment damage. Only trained professional staff should connect external equipment and operate the software.

For more information, contact ZMDI via SPM@zmdi.com.

Contents

1 Introduction 5
1.1. ZSPM8010-KIT Open-Loop Evaluation Board Overview 5
2 Evaluation Board Description 7
2.1. User-Selected Input and Output Capacitors 9
2.2. Recommended Values for Key Passive Components 10
3 Test Setup and Procedure 11
3.1. Test Setup 11
3.2. Evaluation Board Setup and Evaluation Procedures 13
3.3. Evaluation Board Operation and Part Description 15
3.3.1. SMOD# Operation 15
3.3.2. Filter Resistor R4 between VDRV and VCIN 15
3.3.3. Decoupling Capacitors C3 and C1 on VDRV and VCIN 16
3.3.4. Bootstrap Capacitor C5 and Series Bootstrap Resistor R9 16
3.3.5. Resistor R8 between the PHASE Pin and VSWH Node 16
3.3.6. Resistor R7 Open Footprint (Not Applicable to the ZSPM9010) 17
3.3.7. Pull-up Resistor R1 from SMOD# to VCIN 17
3.3.8. Pull-up Resistor R6 from DISB# to VCIN 17
3.3.9. Pull-up Resistor R12 from THWN# to VCIN 17
3.3.10. Resistor R11 between DISB# and THWN# 17
3.3.11. R2 Pull-up and R5 Pull-down Resistors on PWM 18
3.3.12. RC Snubber Components R13 and C34 18
3.3.13. RC Filter Components R14, C42, and C43 18
4 Evaluation Board Performance 19
4.1. Efficiency and Power Loss Calculation 19
4.2. Efficiency and Power Loss Measurement 20
4.3. Switching Waveform Measurements 21
5 Evaluation Board Bill of Materials 22

6 Related Documents 23
7 Definitions of Acronyms 24
8 Document Revision History 24
Appendix A: ZSPM8010-KIT Physical Specifications and Layout 25
Appendix B: ZSPM8010-KIT Open-Loop Evaluation Board Schematic 29

List of Figures

Figure 1.1 ZSPM8010-KIT Open-Loop Evaluation Board – Top View 5
Figure 2.1 Bottom View of the ZSPM8010-KIT Open-Loop Evaluation Board Showing Capacitor Footprints 9
Figure 4.1 Circuit Diagram for Power Loss Measurement 19
Figure 4.2 Efficiency and Power Loss vs. I_{OUT} 20
Figure 4.3 Switching Waveform 21

List of Tables

Table 2.1 ZSPM8010-KIT Open-Loop Evaluation Board Electrical Specifications 7
Table 2.2 ZSPM8010-KIT Open-Loop Evaluation Board Jumper Descriptions 7
Table 2.3 ZSPM8010-KIT Open-Loop Evaluation Board Test Point Descriptions 8
Table 2.4 J18 Efficiency Port Jumper Settings 8
Table 2.5 Key Component Values and Power Supply Configuration 10
Table 3.1 Recommended Test Equipment 12
Table 4.1 Efficiency Test Conditions 20
Table 5.1 Bill of Materials 22

1 Introduction

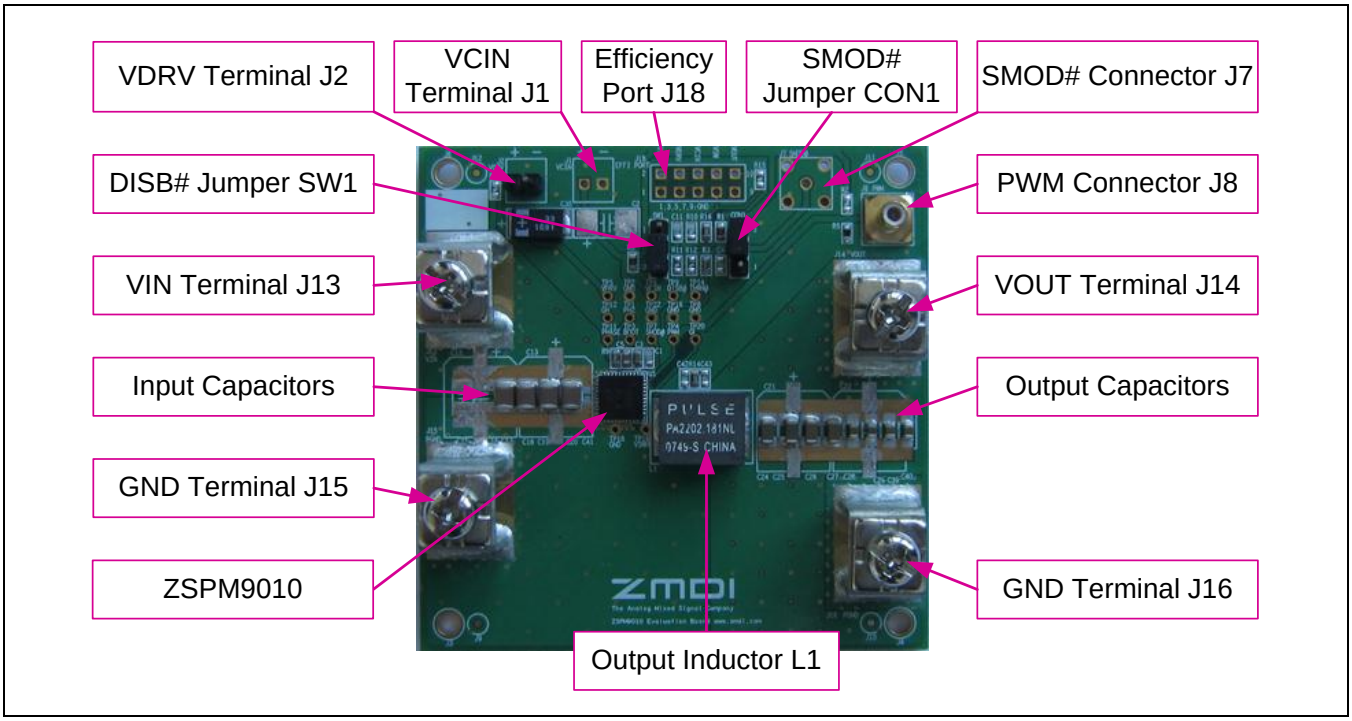
1.1. ZSPM8010-KIT Open-Loop Evaluation Board Overview

The ZSPM8010-KIT single-phase open-loop evaluation board is a design platform providing the minimum circuitry needed to characterize critical performance of the ZSPM9010, a 6x6 mm DrMOS driver plus MOSFET multi-chip module. The scope of this user guide includes using the ZSPM8010-KIT Evaluation Board for internal testing as a reference and for customer support. See section 3.1 for the test equipment needed for the evaluation.

Note: The ZSPM8000-KIT Evaluation Kit is an example of an application for the ZSPM9010. It can be used to evaluate the features of the ZSPM9010 in a closed loop configuration with the ZSPM1000 digital single-phase PWM controller.

This document provides details of the construction of the ZSPM8010-KIT as a guide for modifying the Evaluation Board as needed for the user's specific application.

Figure 1.1 ZSPM8010-KIT Open-Loop Evaluation Board – Top View



The ZSPM9010 DrMOS device is a fully optimized integrated driver plus MOSFET power stage solution for high-current synchronous buck DC-DC applications. The device integrates a driver IC and two power MOSFETs in a space-saving, 6x6mm, 40-pin PQFN package. This integrated approach optimizes the complete switching power stage for the driver and MOSFET in terms of dynamic performance, system inductance and the power MOSFET's on-resistance. Package parasitic and layout issues associated with conventional fully discrete solutions are greatly reduced. This integrated approach results in a significant reduction of board space, maximizing footprint power density. The ZSPM9010 solution is based on the Intel™ DrMOS 4.0 specification.

Key Features of the ZSPM9010

- Ultra-compact 6x6 mm PQFN, 72% space saving compared to conventional full discrete solutions
- Fully optimized system efficiency: > 93 peak
- Clean switching waveforms with minimal ringing
- High current handling: up to 50A
- High performance PQFN copper clip package
- Tri-state 3.3V PWM input driver
- Skip Mode SMOD# (low side gate turn off) input
- Thermal warning flag for over-temperature conditions
- Driver output disable function (DISB# pin)
- Internal pull-up and pull-down for SMOD# and DISB# inputs, respectively
- Integrated Schottky diode technology in low side MOSFET
- Integrated bootstrap Schottky diode
- Adaptive gate drive timing for shoot-through protection
- Under voltage lockout (UVLO)
- Optimized for switching frequencies up to 1 MHz
- Based on the Intel® 4.0 DrMOS standard

2 Evaluation Board Description

The ZSPM8010-KIT Open-Loop Evaluation Board is designed to demonstrate the optimized small size, high-efficiency performance of the ZSPM9010 DrMOS multi-chip module. The board is a high density, high-efficiency design, with a 1 MHz operating frequency and peak efficiency of over 92% with a 1.0V Vout condition. This board also demonstrates the ease of layout for printed circuit board artwork.

The board was designed as an open-loop control to have only common passive components in a synchronous buck converter without a PWM controller. The open-loop control method is more reliable and flexible allowing performance testing with identical conditions. Since the ZSPM9010 pin map is industry standard, it is easy to compare its performance to other DrMOS devices without changing other components.

See Appendix B for the schematic for the Evaluation Board. See Appendix A for the Evaluation Board's physical specifications and layouts for the individual layers of the circuit board.

Table 2.1 ZSPM8010-KIT Open-Loop Evaluation Board Electrical Specifications

Parameter	Description	Notes
Switching Device	ZSPM9010	
PWM Control	0~100% duty by pulse generator	Open-loop control
VIN for Main DC/DC	12V DC typical	Set by power supply 1
VDRV for MOSFET Driving	5V DC typical	Set by power supply 2
VCIN for Gate Driver Vcc	5V DC typical	Set by power supply 3 or power supply 2 depending on configuration (see section 2.2)
VOUT	PWM duty cycle	Set by pulse generator
f_{SW}	PWM switching frequency	Set by pulse generator
Max. Iout	Maximum current handled by the ZSPM9010 (See ZSPM9010 for details)	Set by electronic load

Table 2.2 ZSPM8010-KIT Open-Loop Evaluation Board Jumper Descriptions

Jumper Name	Pin 1-2 Short	Pin 2-3 Short	Notes
SW1 DISB#	LO	HI	The ZSPM9010 is enabled when the SW1 DISB# jumper position = HI
CON1 SMOD#	LO	HI	SMOD is enabled when the SMOD# jumper position = LO

Table 2.3 ZSPM8010-KIT Open-Loop Evaluation Board Test Point Descriptions

Test Point	Test Point Name	Notes
TP5	VDRV	VDRV test point (pin 3 on the ZSPM9010)
TP6	VCIN	VCIN test point (pin 2 on the ZSPM9010)
TP9	DISB#	DISB# test point (pin 39 on the ZSPM9010)
TP14	THWN#	THWN# test point (pin 38 on the ZSPM9010)
TP12	GH	GH test point (pin 6 on the ZSPM9010)
TP1	PH2	PH2 net test point
TP11	PHASE	PHASE test point (pin 7 on the ZSPM9010)
TP3	BOOT	BOOT test point (pin 4 on the ZSPM9010)
TP7	SMOD#	SMOD# test point (pin 1 on the ZSPM9010)
TP4	PWM	PWM test point (pin 40 on the ZSPM9010)
TP20	GL	GL test point (pin 36 on the ZSPM9010)
TP19	VSWH	VSWH test point (pins 15, 29 to 35, and 43 on the ZSPM9010)

Table 2.4 J18 Efficiency Port Jumper Settings

Jumper Pin	Jumper Name	Notes
2-1	VIN-GND	Pin 2 and 1 are connected to the C41 positive and negative pads by a differential pair.
4-3	VDRV-GND	Pin 4 and 3 are connected to C3 positive and negative pads by a differential pair.
6-5	VCIN-GND	Pin 6 and 5 are connected to the C1 positive and negative pads by a differential pair.
8-7	VSW-GND	Pin 8 is connected to the C42 positive pad. Pin 7 is connected to the R16 positive pad.
10-9	VOUT-GND	Pin 10 and 9 are connected to the C24 positive and negative pads by a differential pair.

2.1. User-Selected Input and Output Capacitors

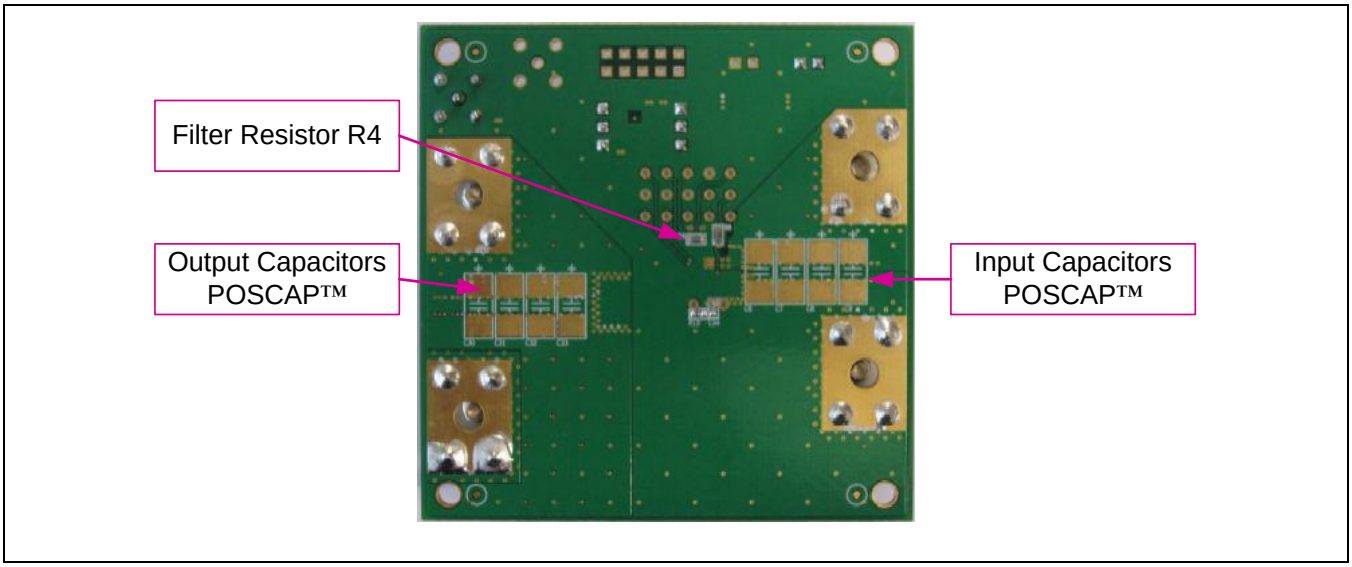
The top side of the Evaluation Board has multiple unpopulated footprints for the user to add input and output capacitors as shown in Figure 1.1. For input capacitors, the board can accommodate up to six 1210-size ceramic capacitors or up to two 10x10 mm SMT-type OS-CON™*. C41 is a size 0603 ceramic capacitor used to reduce noise on VIN.

For output capacitors, up to eight 1210-sized ceramic capacitors or up to two 10x10 mm SMT-type OS-CON™ can be placed on the top side.

On the bottom side of the board, up to four 7x4 mm POSCAP™* can be placed in each set of footprints for the input and output capacitors as shown in Figure 2.1.

All three types of capacitors (ceramic, OS-CON™ and POSCAP™) can be placed on the top side VIN-GND and VOUT-GND coppers to support various test requirements.

Figure 2.1 Bottom View of the ZSPM8010-KIT Open-Loop Evaluation Board Showing Capacitor Footprints



* OS-CON™ and POSCAP™ are trademarks of Sanyo, Inc.

2.2. Recommended Values for Key Passive Components

Table 2.5 provides the recommended values for key passive components on the ZSPM8010-KIT Open-Loop Evaluation Board for the ZSPM9010 for the two alternatives for the power supply setup: either using a shared power supply for VDRV and VCIN or using separate power supplies. The VDRV and VCIN columns give the voltage required from the supplies. See Table 3.1 regarding the effect of filter resistor R4, located on the bottom of the board as shown in Figure 2.1. The Evaluation Board is delivered with component values for the shared power supply.

Table 2.5 Key Component Values and Power Supply Configuration

Power Supply Setup	R4	R7	C3	C1	VDRV	VCIN
Shared power supply for VDRV and VCIN	0Ω	Open	1µF	N/A	5V	NC
Separate power supplies for VDRV and VCIN	Open	Open	1µF	1µF	5V	5V

3 Test Setup and Procedure

3.1. Test Setup

The following equipment is recommended for the using the Evaluation Board to test/evaluate the ZSPM9010.

Efficiency Measurements:

- Power supply 1 for VIN and I_{IN} rated for at least 20V/10A.
- Power supply 2 for VDRV and I_{DRV}; rated for at least 10V/5A.
- Optional power supply 3 for VCIN and I_{CIN} rated for at least 10V/5A. Typically VCIN and ICIN can be shared with VDRV and IDRV from power supply 2 instead of using a third power supply.
- Pulse generator for PWM pulse signaling.
- Electronic load rated for 3V/60A.
- Precise voltmeter to measure input and output voltage.
- Precise current sense resistors in series with each power rail to measure input and output currents. See Table 3.1 for recommended values.
  Recommendation: For efficiency measurements, use precise current sense resistors in series with the input and output power rails. Some vendors offer high-current, high-precision shunt resistors that perform well in this application. They are designed and calibrated at the factory to have a standard accuracy of ±0.25 %.

Waveform Measurements:

- Power supply 1 for VIN and IIN; rated for at least 20V/10A.
- Power supply 2 for VDRV and IDRV; rated for at least 10V/5A.
- Optional power supply 3 for VCIN and ICIN; rated for at least 10V/5A. Typically VCIN and ICIN can be shared with VDRV and IDRV from power supply 2 instead of using a third power supply.
- Pulse generator for PWM pulse signaling.
- Electronic load; rated for 3 V/60 A.
- Precise voltmeter to measure input and output voltage.

- Four-channel oscilloscope; bandwidth (BW) of at least 1GHz.
- For measuring fast-switching waveforms such as VSWH, an active differential probe provides the best accuracy. It should be rated for at least 25V differential input and a BW of at least 500MHz. A standard single-ended probe with a BW of at least 500 MHz will also provide acceptable results.

The output cables for the board must be made with large gauge wire to ensure that they do not cause excessive heating of the board by copper loss. In a normal test setup, use two parallel audio cables with 8 gauge thickness for the maximum 60A output current. Cables must be clamped to the board with large cross-section connectors.

An alternative connector arrangement would be to use large ring or spade terminals attached to the ends of the cables. The cables should then be firmly bolted to the board.

Table 3.1 Recommended Test Equipment

Equipment Type	Name	Notes
Power Supply 1	Agilent E3633A	
Power Supply 2	Agilent E3648A	Power Supply 2 is connected to VDRV. The 0~10 Ω R4 filter resistor can be placed between VDRV and VCIN to supply VCIN power so that Power Supply 3 is not needed.
Power Supply 3		
Pulse Generator	Agilent 81101A	
Electronic Load	Chroma 6312/63106	High-current electronic load
Voltmeter	Agilent 34970A	Multi-channel DMM or data logger
Current Sense Resistor	Deltec	1mΩ / 20A for IIN 50mΩ / 5A for IDRV and ICIN 0.25mΩ / 100A for IOUT
Oscilloscope	Tektronix DPO7104	

3.2. Evaluation Board Setup and Evaluation Procedures

Use the following procedures when operating the ZSPM8010-KIT Open-Loop Evaluation Board. For this example setup, power supply 2 provides both VDRV and VCIN (see Table 2.5) and a PWM pulse generator is used to control VOUT.

Operating Conditions

- VIN for main conversion: 12V typical
- VDRV for gate driving power and VCIN for gate driver logic: 5 V typical
- VOUT for output load: 1V typical (set by PWM duty cycle from pulse generator)
- PWM pulse: 5V high and 0V low, 300 kHz f_{SW}, 10% duty cycle (depending on VOUT), 50Ω output impedance (R5 pull-down resistor on board should be the same value, 50Ω = typical value on delivery)

Operating Procedures

Important: During the following procedures, do not turn on the power supplies until indicated in the steps.

1. On the Evaluation Board, ensure that the DISB# jumper (SW1) is at the LO position (1-2 short).
2. Ensure that the SMOD# jumper (CON1) is at the HI position (2-3 short).
3. Ensure that the filter resistor (R4, 0~10 Ω) is connected on the bottom of the board between the VDRV and VCIN pins (see Figure 2.1).
4. Connect the electronic load to the J14 VOUT and J16 PGND terminals.
5. Connect power supply 1 to the J13 VIN and J15 PGND terminals.
6. Connect power supply 2 to the J2 VDRV (and GND) connector.
7. Connect the pulse generator to the J8 PWM connector.
8. Connect the data logger to the J18 Efficiency Port connector if needed.
9. Set the pulse generator for high and low levels (5V and 0V respectively), f_{SW} (300 kHz), duty cycle (10%), output impedance (50Ω), and other requirements.
10. Connect oscilloscope channels and probes to the desired voltage nodes; for example, CH1 PWM, CH2 GH, CH3 VSWH, and CH4 GL. See Table 2.3 for descriptions of the test points.

Important: Ensure that probes for voltage measurements are in place before powering up the board in step 18 and ensure that probes do not create any unwanted shorts since the board has very thin traces and sensitive noise immunity. If a short situation occurs, the board could malfunction or be damaged.

11. Set oscilloscope channels to appropriate voltage and time divisions.
12. Set the power supply 1 output voltage and current: 12V / 10A typical.
13. Set the power supply 2 output voltage and current: 5V / 1A typical.
14. Set the electronic load operating mode and current level: CC (Constant Current) / 1A typical.
15. Turn on the pulse generator to supply pulses into the PWM connector on board.
16. Turn on power supply 1. Check the 12V at the VIN terminal (across J13 and J15) and the VIN pins (2-1) on the J18 Efficiency Port. Check that no voltage is present on the VOUT terminal (across J14 and J16) or the VOUT pins 10-9 on the J18 Efficiency Port.
17. Turn on power supply 2. Check the 5V at the VDRV connector (J2) and across the VDRV pins (4-3) and VCIN pins (6-5) on the J18 Efficiency Port. Check that no voltage is present on the VSW pins (8-7) of the J18 Efficiency Port. Check that no voltage is present on the VOUT terminal (across J14 and J16) or the VOUT pins (10-9) on the J18 Efficiency Port. Check for 5V pulses at the PWM test point (TP4 PWM).
18. Turn on the Evaluation Board by setting the SW1 jumper on the HI (2-3) position. The board will turn on and all switching waveforms will appear on the oscilloscope.
19. Check that all input and output voltages and currents show proper values.
20. Apply the desired value for load current by setting the electronic load; for example, 1 to 10A for light loads, 10 to 20A for medium loads, or >30A for heavy loads.
21. Set all user-definable parameters such as VIN, VDRV/VCIN, fsw, VOUT, and IOUT as needed to test the board with various conditions.

Since the ZSPM9010 does not have a specific power sequence for VIN, VDRV, VCIN, DISB#, and PWM, it is possible to turn on the board with any power-up sequence. However, to get proper operation and to avoid sudden extreme conditions caused by user errors, using the power up sequence mentioned above is recommended.

3.3. Evaluation Board Operation and Part Description

This section describes the Evaluation Board operation and components.

3.3.1. SMOD# Operation

When the SMOD# jumper (CON1) is set to the HI position, the board operates as a synchronous buck converter. In this mode, the internal low-side MOSFET of the ZSPM9010 is turning on and off according to the PWM signal. The power stage operates in Continuous Conduction Mode (CCM), allowing the inductor current to go negative if there are low output current values.

When the SMOD# jumper (CON1) is set LOW, the Skip Mode is activated and the board operates as an asynchronous buck converter. In this operating mode, the low-side MOSFET of the ZSPM9010 is always off, so the low-side MOSFET free-wheeling current is flowing through the low-side MOSFET body diode when the inductor current is positive, but it is blocked when the inductor current would have gone negative. This prevents discharge of the output capacitors by preventing reversal of the current flow through the inductor.

Diode emulation is performed via the SMOD# connector (J7 SMOD#): this connector is intended to supply a separate, dedicated, cycle-by-cycle-based SMOD signal to turn on the low-side MOSFET when the inductor current is positive, while turning off the low-side MOSFET when the inductor current would have gone negative. The SMOD signal input on the SMOD# connector should be synchronized with the PWM signal to guarantee precise gate signaling for the high-side and low-side MOSFETs. The SMOD# feature is designed for the ZSPM9010.

3.3.2. Filter Resistor R4 between VDRV and VCIN

The R4 filter resistor is located on the bottom of the board across the VDRV and VCIN pins of the ZSPM9010. The VDRV pin is connected to an internal boot diode to supply the gate driving voltage. VCIN is connected to the supply voltage of the logic circuitry (VCC) of the gate driver. In normal applications, both power rails are connected together and can be powered by a single 5V power rail. Situations such as improper supply of VDRV and VCIN, defective/ incorrect decoupling capacitors placed on the VDRV and VCIN pins, or poor board layout design can result in higher noise on the VCIN pin, which could cause gate driver malfunction or damage. The resistor R4 placed between VDRV and VCIN is therefore intended to reduce the noise level on the VCIN pin. The typical value for normal applications is 0 Ω. Recommended range of values is 0~10 Ω.

3.3.3. Decoupling Capacitors C3 and C1 on VDRV and VCIN

The C3 and C1 decoupling capacitors for VDRV and VCIN are located on the top side of the board. The typical value for the C3 ceramic decoupling capacitor on the VDRV pin is 1µF/10V/0603/X5R or better. Decoupling capacitors with a smaller size (e.g., 0402) or an inadequate temperature characteristic (e.g., Y5V) on the VDRV pin can degrade board dynamic performance.

In general, the VCIN pin does not consume as much power as the VDRV pin. A decoupling capacitor with the same values as for the VDRV pin (1µF/10V/0603/X5R or better) or with a larger physical size and X5R or better temperature characteristic is recommended for the VCIN pin. When R4 is used, the decoupling capacitor on the VCIN pin can be removed; however, the user must select the correct values for R4 and for the decoupling capacitor C3 using the experimental results obtained for the testing conditions.

3.3.4. Bootstrap Capacitor C5 and Series Bootstrap Resistor R9

The C5 bootstrap capacitor and R9 series bootstrap resistor are located on the top side of the board. The typical value for the C5 ceramic bootstrap capacitor on the BOOT pin is 0.1µF/50V/0603/X5R or better in terms of physical size and temperature characteristic.

The bootstrap resistor R9 is connected between the C5 bootstrap capacitor and the PHASE pin. Its value can be changed to reduce the high-side MOSFET switching speed. Due to EMI issues, many users use the bootstrap resistor to reduce VSWH spikes and ringing. However, the bootstrap resistor can decrease system efficiency while increasing high-side MOSFET switching loss. The value on delivery for R9 is 0 Ω on the Evaluation Board. The typical range for normal applications is 0~5 Ω.

3.3.5. Resistor R8 between the PHASE Pin and VSWH Node

The R8 resistor is located on the bottom of the board between the PHASE pin (via R9) and the VSWH node (pins 15, 29 to 35, and 43 on the ZSPM9010). The PHASE pin and VSWH node of the ZSPM9010 are connected together via internal bonding wire. To increase noise immunity of the gate driver under extreme conditions, this 0Ω resistor is placed between the PHASE pin and VSWH copper trace. This resistor is in parallel with the internal bonding wire, so it helps reduce noise spikes on the VSWH node. The recommended value for R8 is 0Ω. R8 values greater than 0Ω will lead to degradation of the noise immunity for the gate driver. This resistor can be removed if the board layout is well-designed so that parasitic noise from spikes on VSWH is minimal.

3.3.6. Resistor R7 Open Footprint (Not Applicable to the ZSPM9010)

Important: Do not use R7 with the ZSPM9010 (unpopulated footprint for R7 is located on the top of the board between VIN and VDRV). It is only applicable to the ZSPM9000, which is a related product.

3.3.7. Pull-up Resistor R1 from SMOD# to VCIN

The R1 pull-up resistor is located on the top side of the Evaluation Board between VCIN and the ZSPM9010's SMOD# pin via the SMOD# jumper CON1. This 10kΩ pull-up resistor is used on the SMOD# pin to ensure the 5V HIGH level on the SMOD# pin. The value can be changed; however, a minimum of 10kΩ is recommended.

3.3.8. Pull-up Resistor R6 from DISB# to VCIN

The R6 pull-up resistor is located on the top side of the board from VCIN to the ZSPM9010's DISB# pin via the DISB# jumper SW1. This 10kΩ pull-up resistor is used on the DISB# pin to ensure the 5V HIGH level on the DISB# pin. The value can be changed; however, a minimum of 10kΩ is recommended.

3.3.9. Pull-up Resistor R12 from THWN# to VCIN

The R12 pull-up resistor is located on the top side of the board from the ZSPM9010's THWN# pin to VCIN. The purpose of the THWN# pin is to go LOW indicating the over-temperature warning flag if the temperature of the gate driver is too high. The THWN# pin is an open-drain output. When the gate driver temperature is lower than 150°C, the THWN# pin will remain HIGH via the R12 pull-up resistor. If the gate driver temperature rises to 150°C or higher, the THWN# pin will be set LOW. A minimum value of 10kΩ for R12 is recommended.

3.3.10. Resistor R11 between DISB# and THWN#

The R11 resistor is located on the top side of the board between the ZSPM9010's DISB# and THWN# pins. This 0Ω resistor can be used to shut down the ZSPM9010 when the THWN# flag is set LOW due to an over-temperature condition.

If THWN# is set LOW due to the gate driver temperature rising to 150°C or higher, the DISB# pin will be set LOW via R11 and the ZSPM9010 will shut down. When the gate driver has cooled to 135°C or lower, the THWN# pin will reset to HIGH so DISB# will also reset to HIGH. In this case, the ZSPM9010 will turn on again. The recommended value for R11 is 0Ω.

3.3.11. R2 Pull-up and R5 Pull-down Resistors on PWM

The R2 pull-up and R5 pull-down resistors are located on the top side of the board on the ZSPM9010's PWM pin (adjacent to the J8 PWM connector). The ZSPM9010's PWM pin supports three different logic levels: logic HIGH level, logic LOW level, and a tri-state open voltage window. The R2 pull-up and R5 pull-down resistors can be used to match the PWM open voltage from the pulse generator to the ZSPM9010 and to match the output impedance of the pulse generator to the impedance of the PWM pin. Default values: R2 = open and R5 = 50Ω.

3.3.12. RC Snubber Components R13 and C34

The R13 resistor and C34 capacitor are located on the bottom of the board. The RC snubber for reducing VSWH spikes and ringing comprises R13 and C34. Their values can be calculated based on snubber theory for the operating conditions of the board. Typical values are R13=2.2Ω and C34=1nF. Recommended range of values are 0 to 3.3Ω for R13 and 0 to 2.2nF for C34.

3.3.13. RC Filter Components R14, C42, and C43

R14, C42, and C43 are located on the top side of the board. The default condition of the board is that R14=0Ω and C42 and C43 are not populated. In this condition, there is no RC filtering for the VSWH voltage.

An RC filter can be added to change the VSWH AC voltage to a VSWH DC voltage by replacing R14 with a resistor value >0Ω and adding C42, and C43. Typical values are R14=10kΩ, C42 =10nF, and C43 =10nF. The filtered VSWH DC voltage can be used to measure DC voltage on the VSWH node. This information can be used to calculate the power loss at the VSWH node. Note that some low-end voltmeters or digital multimeters cannot measure the correct DC value of the VSWH node, leading to an incorrect power loss computation and therefore an incorrect efficiency result.

4 Evaluation Board Performance

4.1. Efficiency and Power Loss Calculation

For power loss and efficiency calculations, refer to the equations below and Figure 4.1.

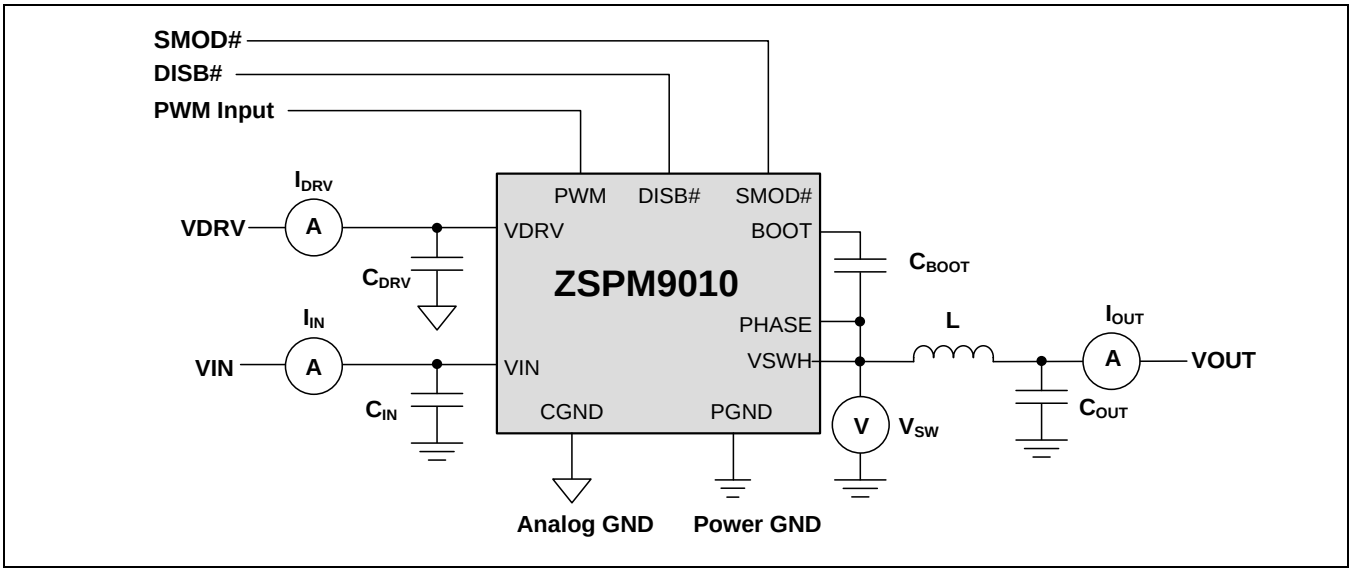
$$P_{IN\_TOT} = P_{IN} + P_{DRV} = (V_{IN} * I_{IN}) + (V_{DRV} * I_{DRV}) \quad \text{(Watts)} \tag{1}$$

$$P_{OUT} = V_{OUT} * I_{OUT} \quad \text{(Watts)} \tag{2}$$

$$P_{LOSS} = P_{IN\_TOT} - P_{OUT} \quad \text{(Watts)} \tag{3}$$

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN\_TOT}} x100\% = \frac{P_{OUT}}{(P_{IN} + P_{DVR})} x100\% \tag{4}$$

Figure 4.1 Circuit Diagram for Power Loss Measurement



4.2. Efficiency and Power Loss Measurement

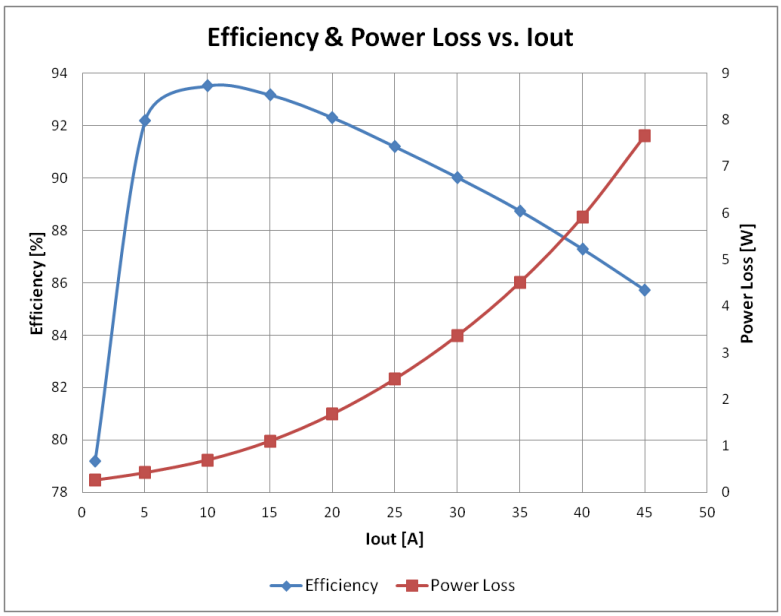
Table 4.1 shows an example of test setup parameters for efficiency and power loss measurements.

Table 4.1 Efficiency Test Conditions

VIN	VDRV / VCIN	VOUT	FSW	Inductor	IOUT	Cooling
12V	5V	1V	300kHz	320nH	0~45A, 5A step, 3 minute soaking	No

Figure 4.2 shows the measured and calculated efficiency and power loss of the ZSPM8010-KIT Open-Loop Evaluation Board with the test conditions above.

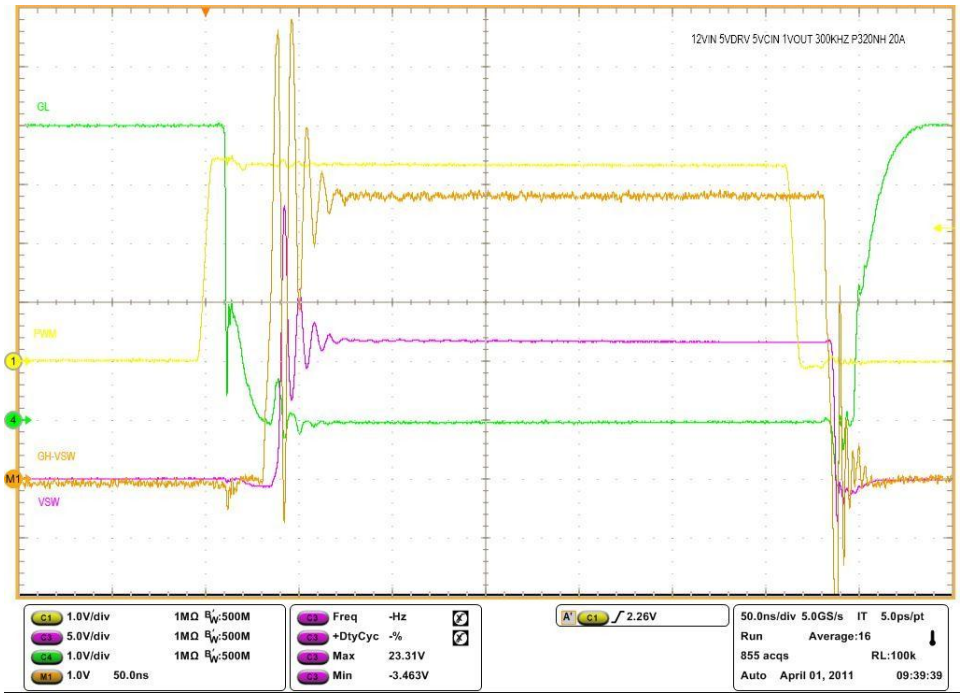
Figure 4.2 Efficiency and Power Loss vs. I_{OUT}



4.3. Switching Waveform Measurements

Figure 4.3 illustrates a switching waveform example.

Figure 4.3 Switching Waveform



5 Evaluation Board Bill of Materials

Table 5.1 shows the complete bill of materials for the ZSPM8010-KIT Open-Loop Evaluation Board. Also see the schematic given in Appendix A.

Table 5.1 Bill of Materials

Qty	Reference	Value	Size	Remark
2	CON1, SW1	3P (1x3) header		
1	J1	2P (1x2) header		Optional
1	J2	2P (1x2) header		
1	J18	10P (2x5) header		
2	J7, J8	RF connector		Mini BNC
4	J13, J14, J15, J16	Terminal		BR-113
1	U1	ZSPM9010	6 x 6 mm	DrMOS
1	L1	180 nH	10 x 12 mm	Pulse PA2202.181NL
1	C1	1µF / 10V	0603	MLCC, X5R. OPTION
1	C3	1µF / 10V	0603	MLCC, X5R
1	C2	33µF / 25V	7 x 4 mm	POSCAP™™, OPTION
1	C35	33µF / 25V	7 x 4 mm	POSCAP™
4	C6, C7, C8, C9	33µF / 25V	7 x 4 mm	POSCAP™, OPTION
2	C4, C11	10nF / 50V	0603	MLCC, X5R, OPTION
2	C42, C43	10nF / 50V (Default is open.)	0603	MLCC, X5R, OPTION Note: If C42 and C43 are added to create an RC filter on VSWH, replace R14 with a value >0Ω; typical = 10kΩ. See section 3.3.13.
1	C34	1nF/ 50V	0603	MLCC, X5R, OPTION
1	C5	0.1µF / 50V	0603	MLCC, X5R
1	C41	0.1µF / 50V	0603	MLCC, X5R. OPTION
2	C12, C13	330µF / 16V	10 x 10 mm	OS-CON™, OPTION
2	C15, C16	22µF / 25V	1210	MLCC, X5R, OPTION
4	C17, C18, C19, C20	22µF / 25V	1210	MLCC, X5R
2	C21, C22	560µF / 4V	10 x 10 mm	OS-CON™, OPTION

Qty	Reference	Value	Size	Remark
4	C24, C25, C26, C27	100µF/ 6.3V	1206	MLCC, X5R
4	C28, C29, C39, C40	22 µF / 6.3V	0805	MLCC, X5R
4	C30, C31, C32, C33	470µF / 6.3V	7 x 4 mm	POSCAP™, OPTION
2	R1, R6	10kΩ	0603	
1	R12	10kΩ	0603	OPTION
1	R14	Default value = 0 *	0603	* If adding an RC filter to the VSWH voltage, add C42 and C43 and replace R14 with >0Ω; typical 10kΩ. See section 3.3.13.
3	R2, R7, R10	Open	0603	OPTION
5	R3, R4, R8, R9, R16	0Ω	0603	
1	R11	0Ω	0603	OPTION
1	R5	49.9Ω	0603	
1	R13	2.2Ω	0603	OPTION
1	R15	0Ω	0603	OPTION

6 Related Documents

Note: X.xy represents the current version of the document.

Documents Related to All Products	File Name
ZSPM9010 Data Sheet	*ZSPM9010_Data_Sheet_revX_xy.pdf*
ZSPM9010 Feature Sheet	*ZSPM9010_Feature_Sheet_revX_xy.pdf*

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

7 Definitions of Acronyms

Term	Description
DISB	Driver Output Disable Function
HS	High Side
LS	Low Side
NC	No connection
SMOD	Skip Mode Input (low-side gate turn-off)

8 Document Revision History

Revision	Date	Description
1.00	June 13, 2012	First release.
1.01	October 22, 2012	Revision of kit name and update of contact information.
1.02	November 19, 2012	Identified default values for R14, C42, and C43 in Table 5.1 and clarified instructions for adding an RC filter to the output in section 3.3.13. Update of contact information.

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Appendix A: ZSPM8010-KIT Physical Specifications and Layout

A.1 Evaluation Board Physical Specifications

Figure A 1 shows the physical information for the individual layers of the board. The board's physical parameters are typical of values used for standard desktop and server motherboard design.

- Board size: 70 x 70 mm
- Copper layer count: 8 layer
- Board total thickness: 2.066mm
- Outer layer copper thickness: 1.5 oz (0.5 oz base + 1 oz plating)
- Inner layer copper thickness: 1 oz for IN1/IN2/IN5/IN6; 2 oz for IN3 and IN4
- Via design rule: 0.25mm for drill hole, 0.4mm for pad diameter

Figure A 1 ZSPM8010-KIT Open-Loop Evaluation Board Stack-up Structure

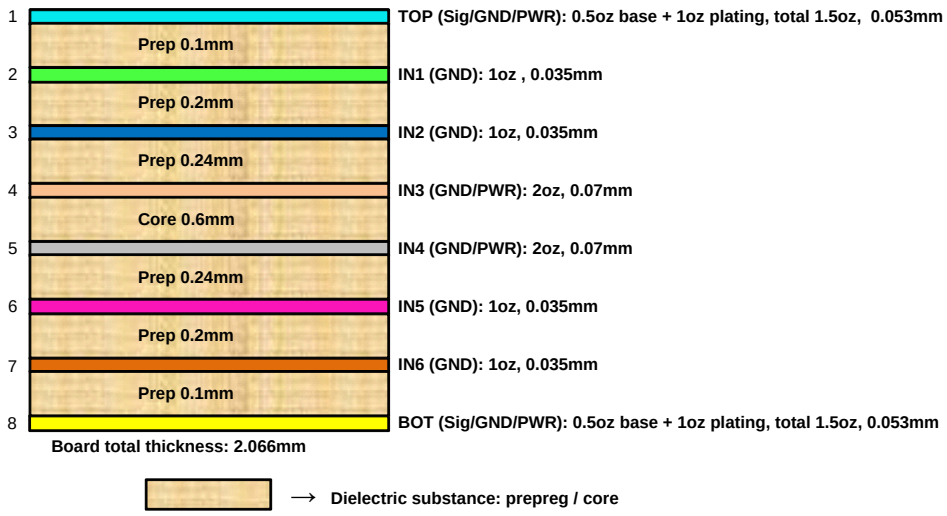
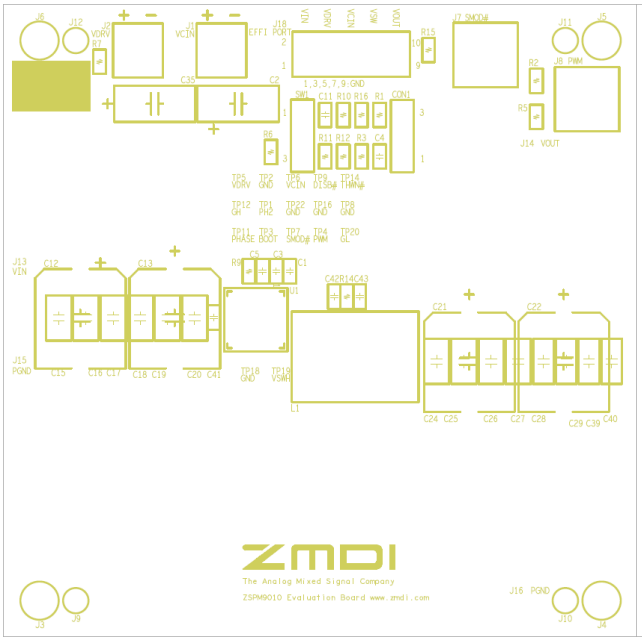
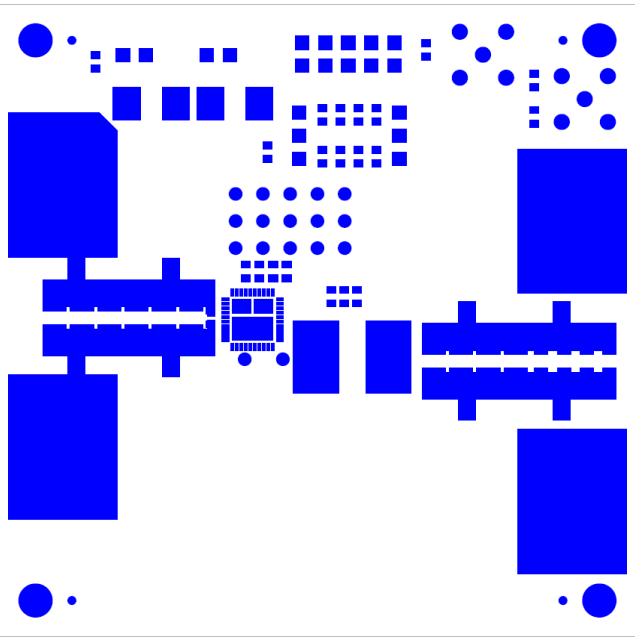


Figure A 2 Evaluation Board Layout

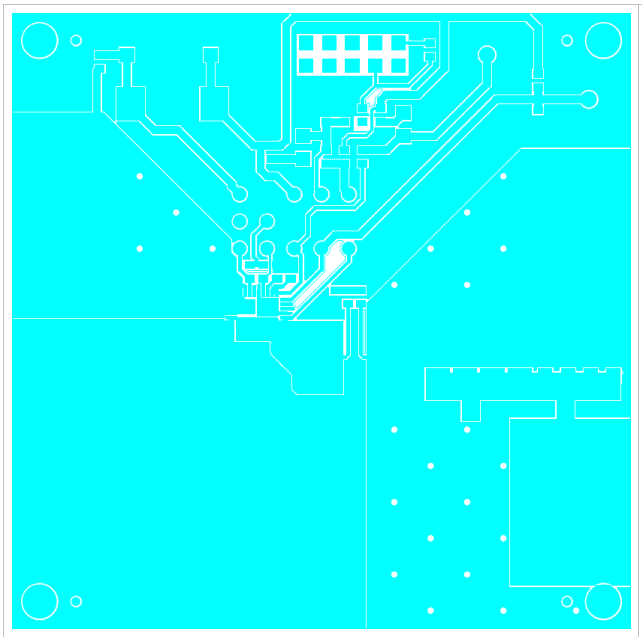
SST Layer



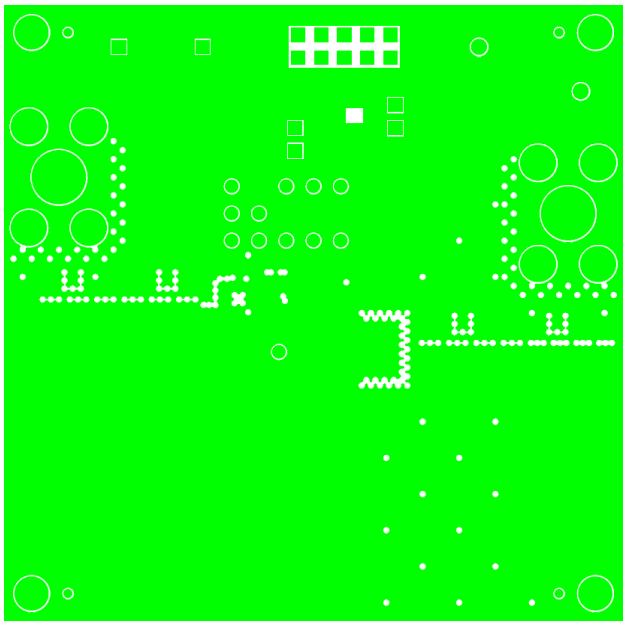
SMT Layer



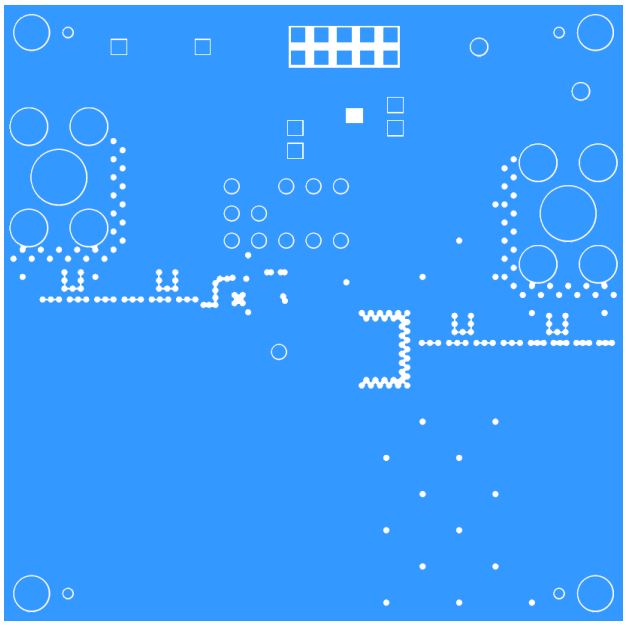
TOP Layer



IN1 Layer

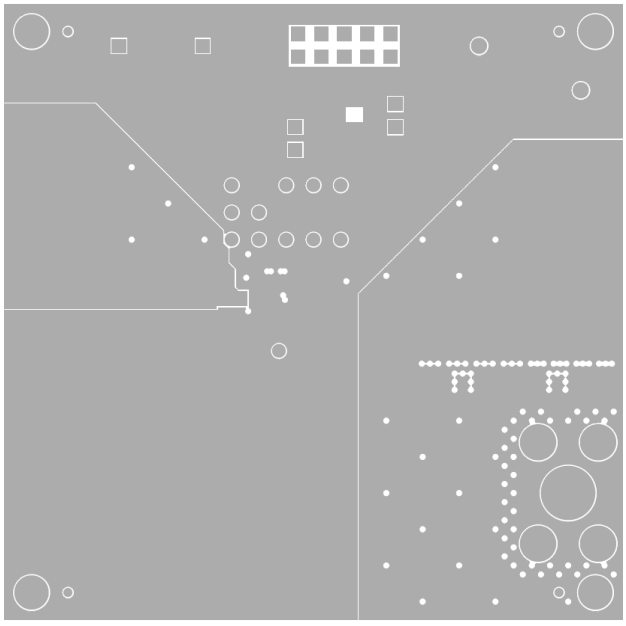


IN2 Layer

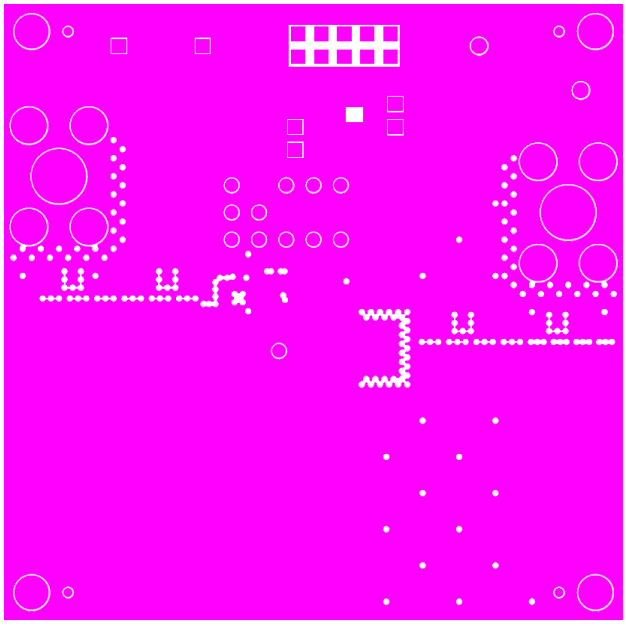


IN3 Layer

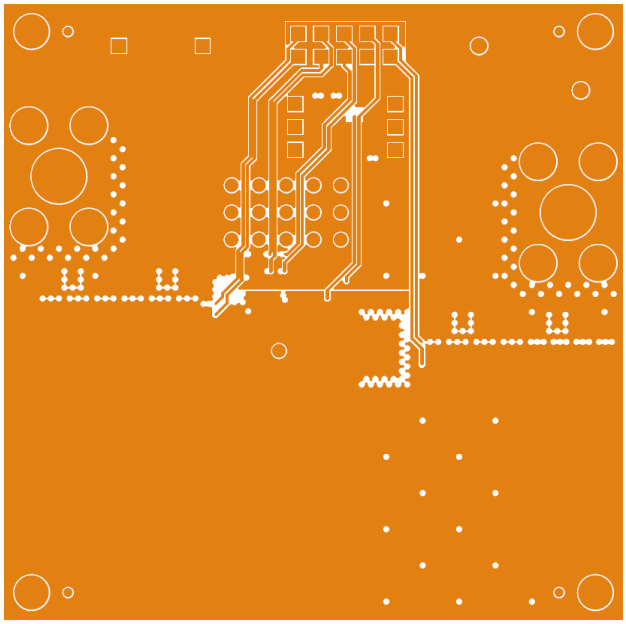
IN4 Layer



IN5 Layer

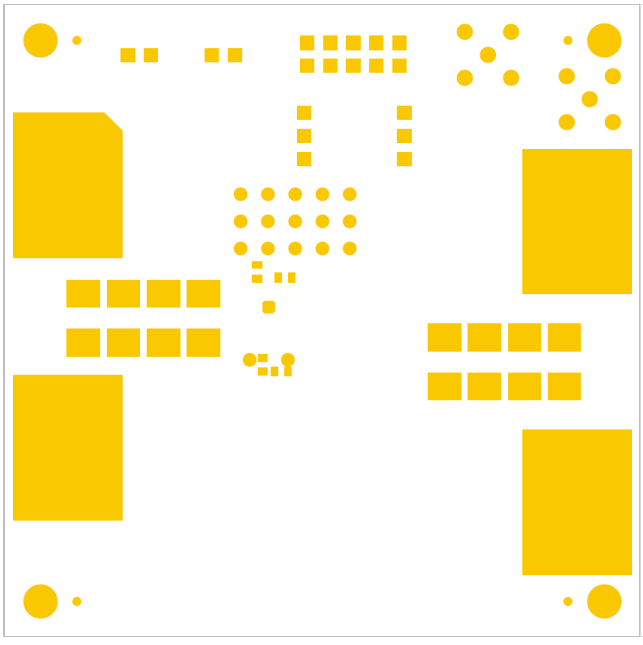


IN6 Layer

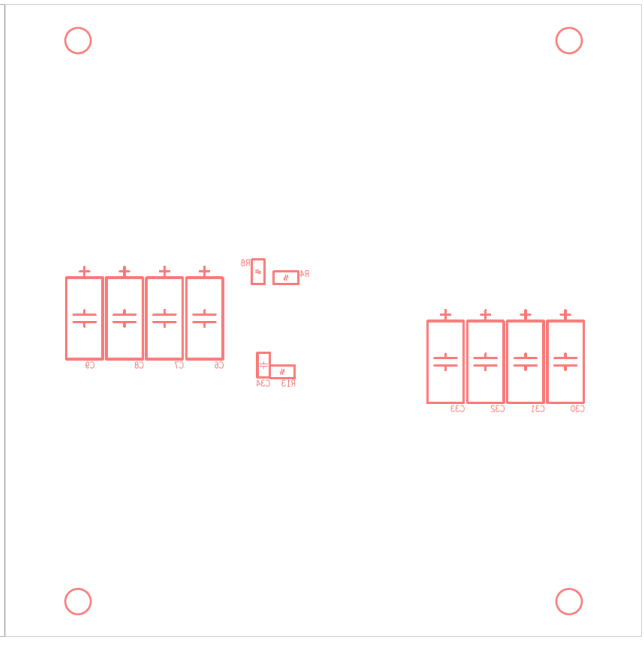


BOT Layer

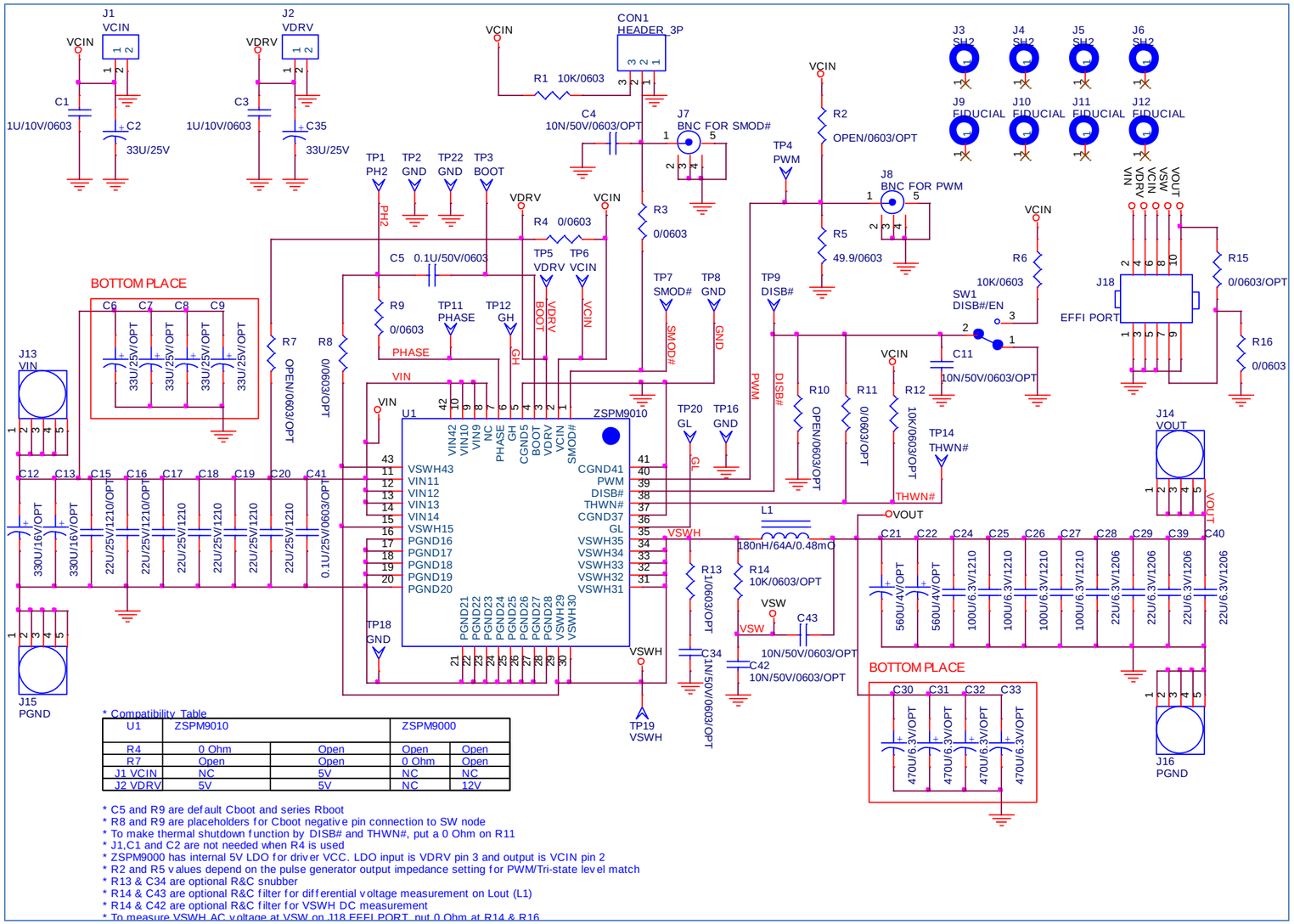
SMB Layer



SSB Layer



Appendix B: ZSPM8010-KIT Open-Loop Evaluation Board Schematic



* Compatibility Table

U1	ZSPM9010		ZSPM9000	
R4	0 Ohm	Open	Open	Open
R7	Open	Open	0 Ohm	Open
J1 VCIN	NC	5V	NC	NC
J2 VDRV	5V	5V	NC	12V

* C5 and R9 are default Cboot and series Rboot
* R8 and R9 are placeholders for Cboot negative pin connection to SW node
* To make thermal shutdown function by DISB# and THWN#, put a 0 Ohm on R11
* J1,C1 and C2 are not needed when R4 is used
* ZSPM9000 has internal 5V LDO for driver VCC. LDO input is VDRV pin 3 and output is VCIN pin 2
* R2 and R5 values depend on the pulse generator output impedance setting for PWM/Tri-state level match
* R13 & C34 are optional R&C snubber
* R14 & C43 are optional R&C filter for differential voltage measurement on Lout (L1)
* R14 & C42 are optional R&C filter for VSWH DC measurement
* To measure VSWH AC voltage at VSW on J18 EFFI PORT, put 0 Ohm at R14 & R16

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