

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 3.5 μ A
 - Maximum standby current: 8.7 μ A
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP II) and 32-pin small-outline integrated circuit (SOIC) packages

Functional Description

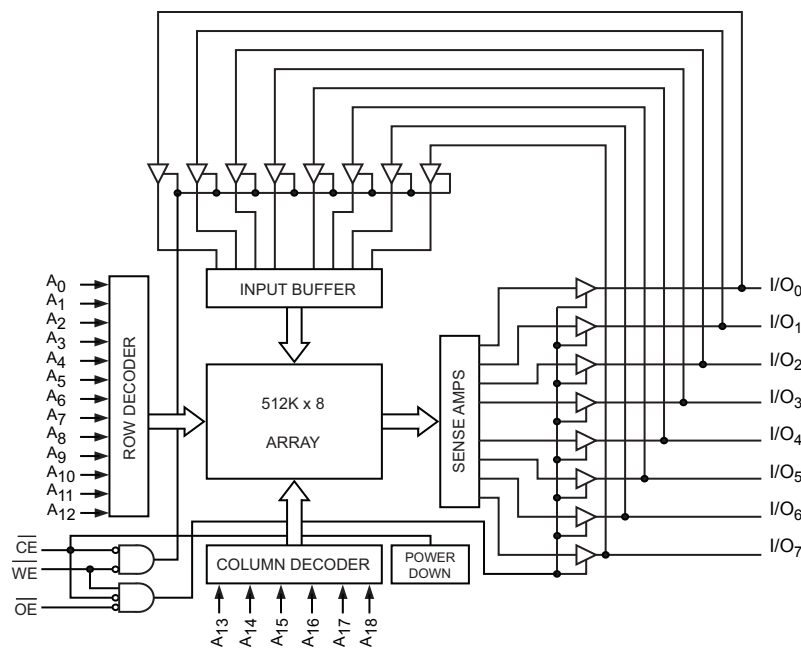
The CY62148GN is a high-performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The eight input and output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), Outputs are disabled (\overline{OE} HIGH), or during an active Write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

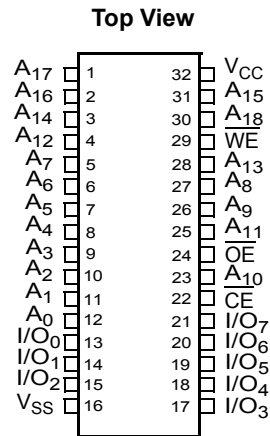


Contents

Pin Configurations	3	Ordering Information	11
Product Portfolio	3	Ordering Code Definitions	11
Maximum Ratings	4	Package Diagrams	12
Operating Range	4	Acronyms	13
Electrical Characteristics	4	Document Conventions	13
Capacitance	5	Units of Measure	13
Thermal Resistance	5	Document History Page	14
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	15
Data Retention Characteristics	6	Worldwide Sales and Design Support	15
Data Retention Waveform	6	Products	15
Switching Characteristics	7	PSoC® Solutions	15
Switching Waveforms	8	Cypress Developer Community	15
Truth Table	10	Technical Support	15

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation					
				Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
				f = 1 MHz		f = f _{max}			
				Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62148GN30	Industrial	2.2 V–3.6 V	45	–	6	–	20	3.5	8.7
CY62148GN		4.5 V–5.5 V							

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs
in high Z state^[2, 3] -0.5 V to V_{CC} + 0.5 V

DC input voltage^[2, 3] -0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[4]
CY62148GN	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V, 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[5]	Max	
V _{OH}	Output HIGH voltage	2.2 V to 2.7 V V _{CC} = Min, I _{OH} = -0.1 mA	2	-	-	V
		2.7 V to 3.6 V V _{CC} = Min, I _{OH} = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V V _{CC} = Min, I _{OH} = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V V _{CC} = Min, I _{OH} = -0.1 mA	V _{CC} - 0.5 ^[6]	-	-	
V _{OL}	Output LOW voltage	2.2 V to 2.7 V V _{CC} = Min, I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 V to 3.6 V V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	
		4.5 V to 5.5 V V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	
V _{IH}	Input HIGH voltage	2.2 V to 2.7 V	1.8	-	V _{CC} + 0.3 ^[3]	V
		2.7 V to 3.6 V	2	-	V _{CC} + 0.3 ^[3]	
		4.5 V to 5.5 V	2.2	-	V _{CC} + 0.5	
V _{IL}	Input LOW voltage	2.2 V to 2.7 V	-0.3 ^[2]	-	0.6	V
		2.7 V to 3.6 V	-0.3 ^[2]	-	0.8	
		4.5 V to 5.5 V	-0.5	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC} V _{CC} = V _{CC(max)} , I _{OUT} = 0 mA CMOS levels	-	-	20	mA
		f = 1 MHz	-	-	6	
I _{SB1} ^[7]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, f = f _{max} (address and data only), f = 0 (\overline{OE} and \overline{WE}) V _{CC} = V _{CC(max)}	-	3.5	8.7	μA
I _{SB2} ^[7]	Automatic \overline{CE} power-down current – CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, f = 0, V _{CC} = V _{CC(max)}	-	3.5	8.7	μA

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- This parameter is guaranteed by design and not tested.
- Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

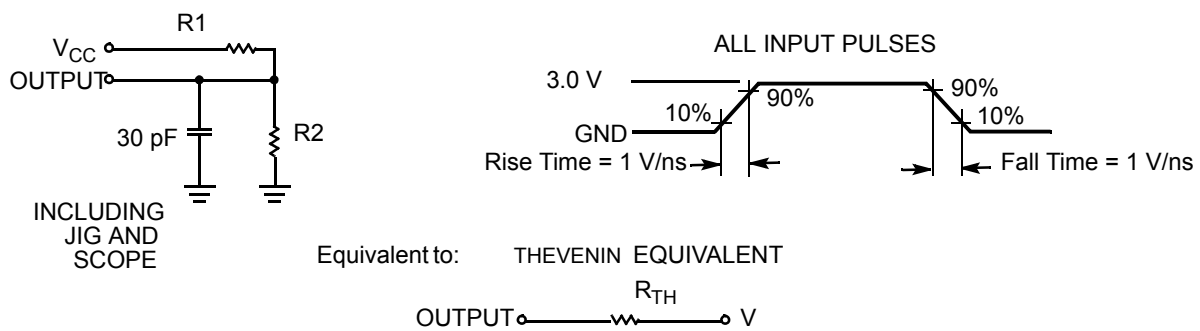
Parameter ^[8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(Typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	°C/W
Θ _{JC}	Thermal resistance (junction to case)		25.12	17.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms^[9]



Parameter ^[8]	2.5 V	3.0 V	5.0 V	Unit
R ₁	16667	1103	1800	Ω
R ₂	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V_{CC} ramp from VDR to V_{CC(min)} > 100 μs or stable at V_{CC(min)} > 100 μs.

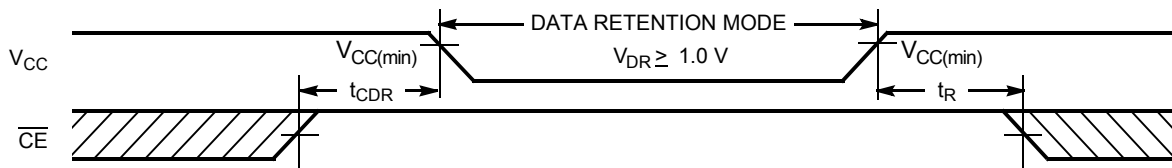
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR} ^[11, 12]	Data retention current	$V_{CC} = 1.2V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	–	13	μA
t_{CDR} ^[13]	Chip deselect to data retention time		0	–	–	ns
t_R ^[13, 14]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ C$.
11. Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR} .
13. These parameters are guaranteed by design.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} > 100 \mu s$ or stable at $V_{CC(min)} > 100 \mu s$.

Switching Characteristics

Over the operating range

Parameter ^[15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[16]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[16, 17]	–	18	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[16]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[16, 17]	–	18	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	45	ns
Write Cycle^[18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[16, 17]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[16]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 5](#).
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

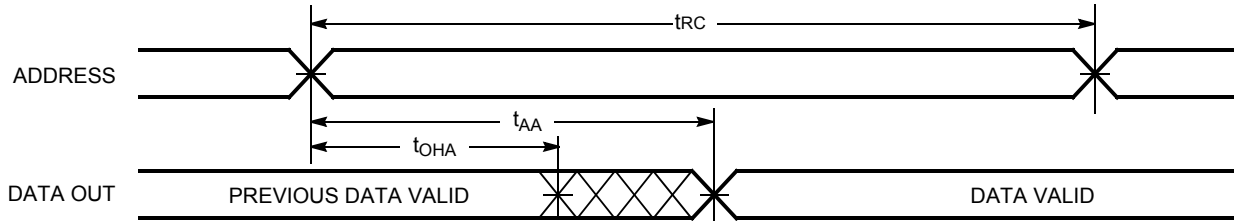


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [21, 22]

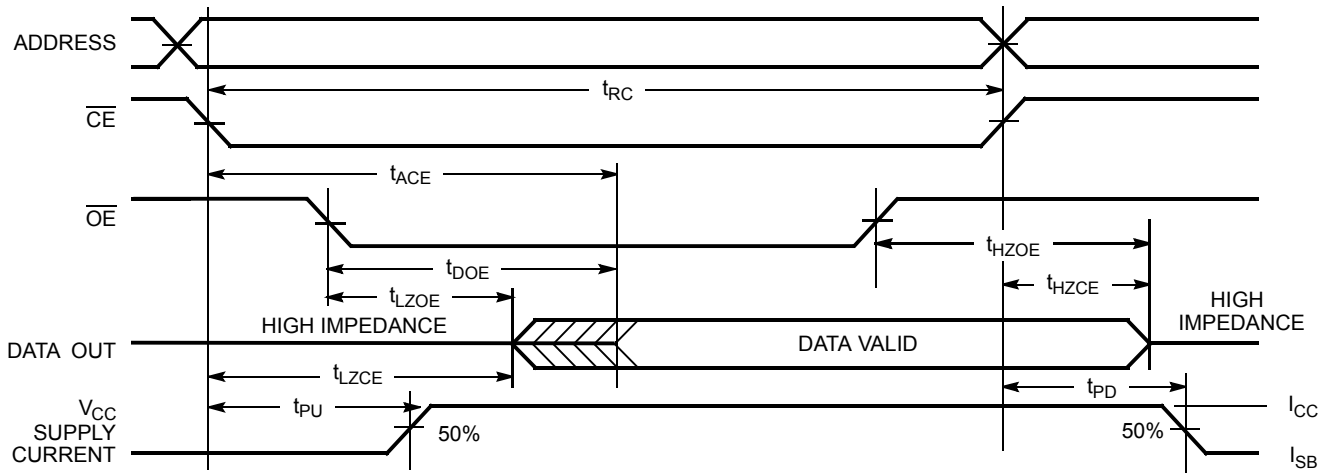
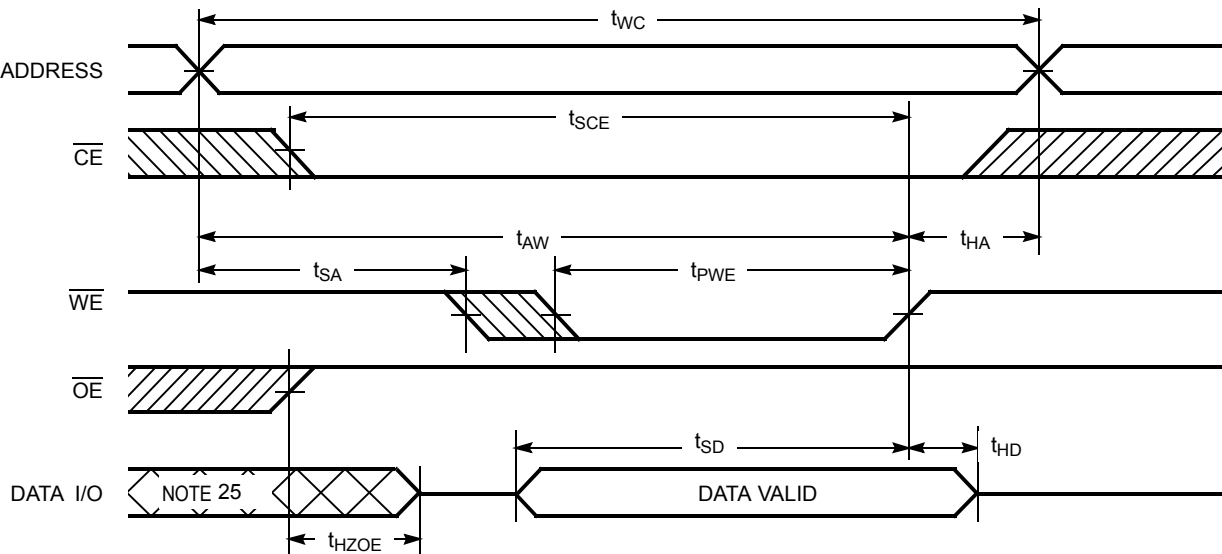


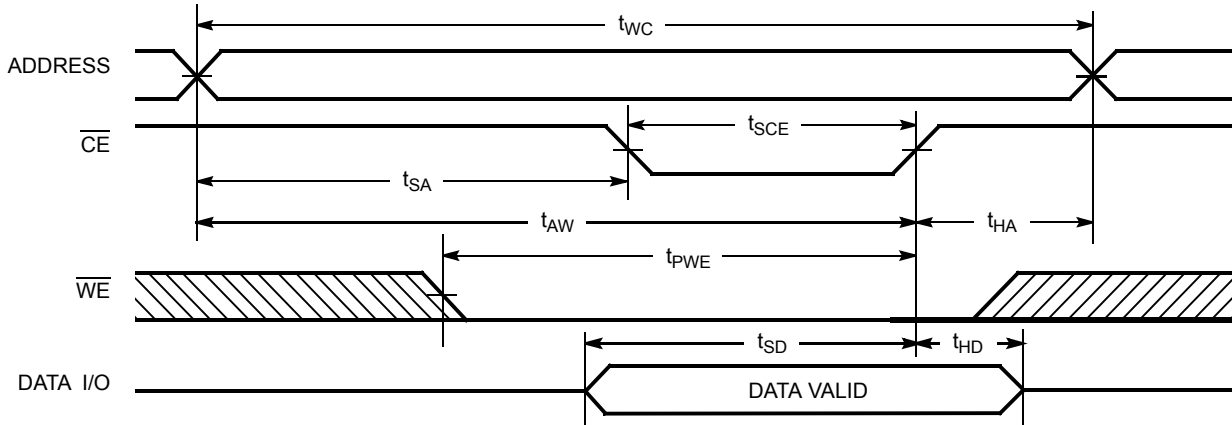
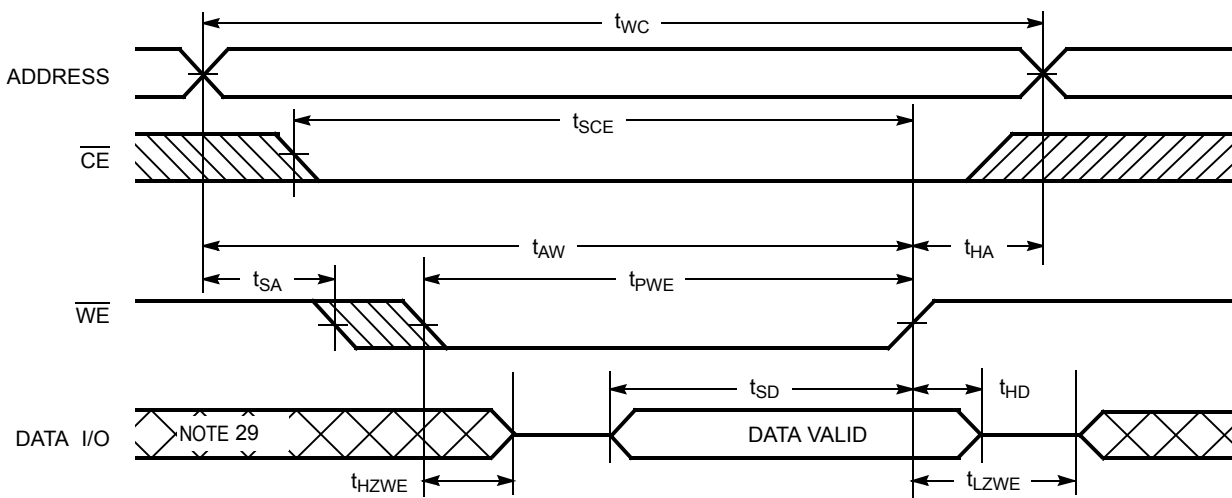
Figure 6. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [23, 24]



Notes

- 20. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
- 21. \overline{WE} is HIGH for read cycles.
- 22. Address valid before or similar to \overline{CE} transition LOW.
- 23. Data I/O is high impedance if \overline{OE} = V_{IH} .
- 24. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 25. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [26, 27]

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [27, 28]

Notes

26. Data I/O is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

27. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in high impedance state.

28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .

29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Mode	Power
H ^[30]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note

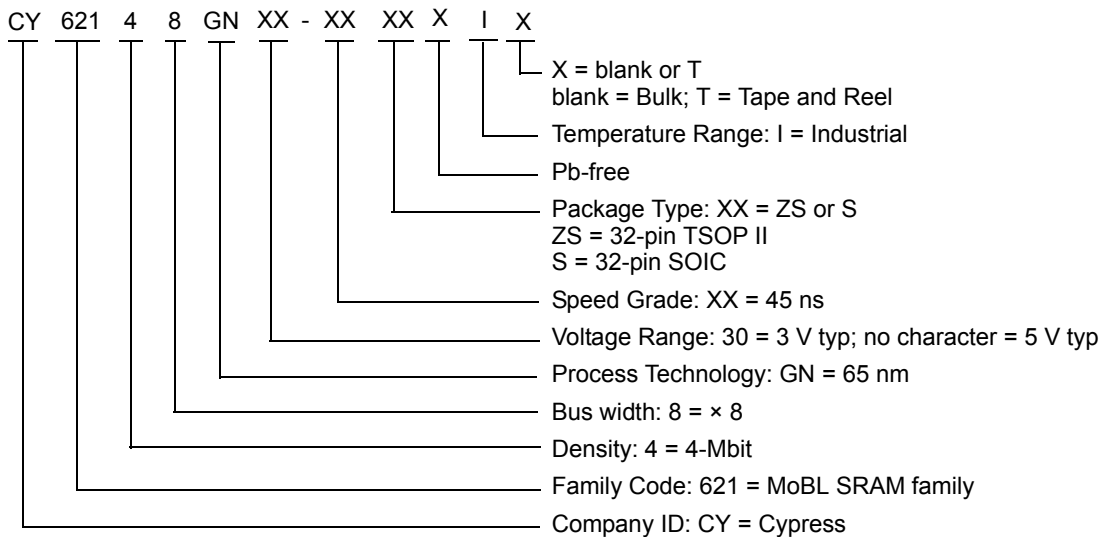
30. Chip enable ($\overline{\text{CE}}$) must be HIGH at CMOS level to meet the $I_{\text{SB2}} / I_{\text{CCDR}}$ spec. Other inputs can be left floating.

Ordering Information

Table 1. Key features and Ordering Information

Speed (ns)	Voltage Range (V)	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148GN30-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
		CY62148GN30-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN30-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN30-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	
	4.5 V–5.5 V	CY62148GN-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
		CY62148GN-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095

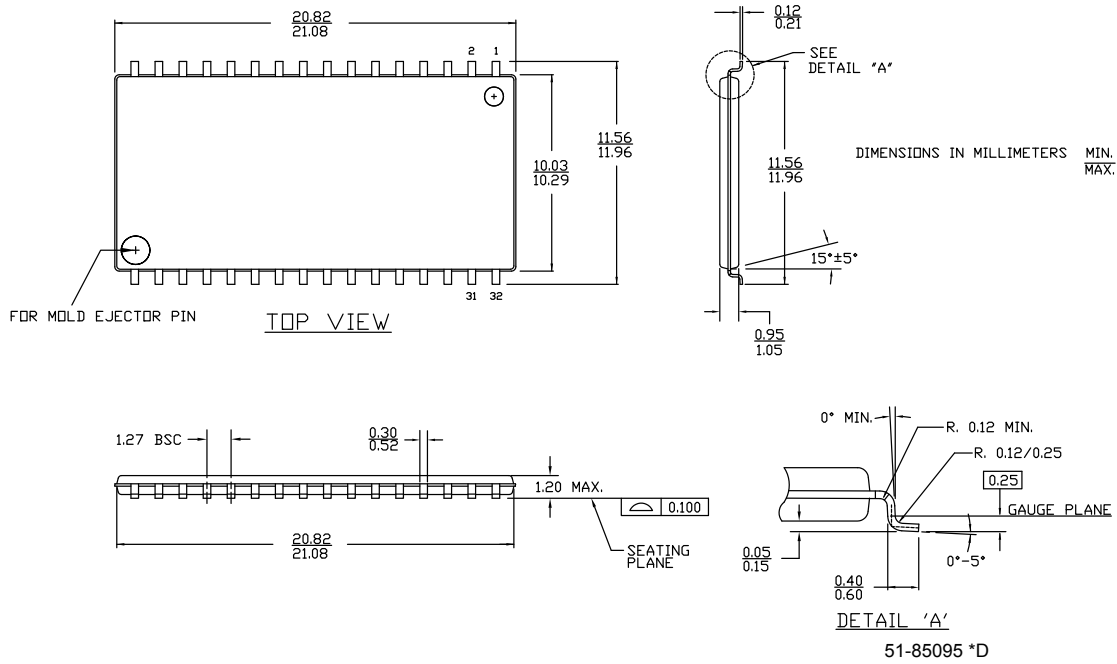
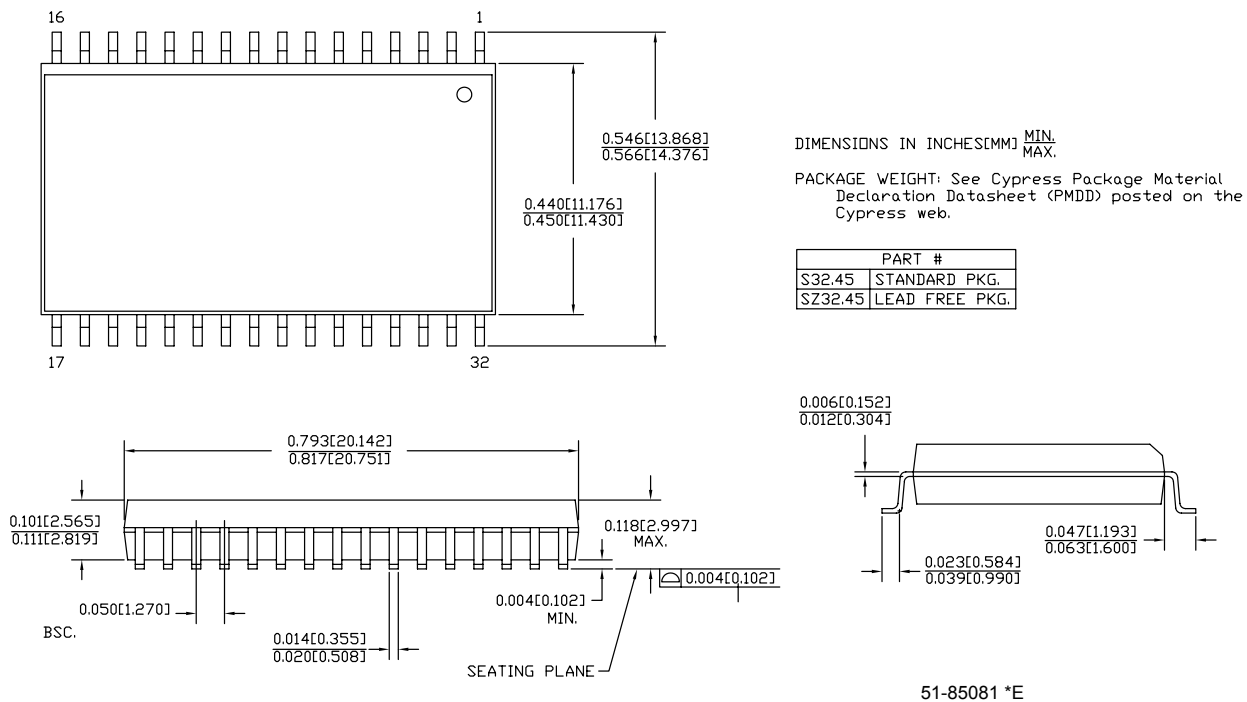


Figure 10. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
MoBL	More Battery Life
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
WE	write enable

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62148GN MoBL [®] , 4-Mbit (512K × 8) Static RAM				
Document Number: 001-95418				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5056496	NILE	12/29/2015	New data sheet.
*A	5092456	NILE	01/19/2016	Added "2.2 V to 3.6 V" range related information in all instances across the document. Updated Ordering Information : Updated part numbers.
*B	5422041	NILE	09/09/2016	Updated Electrical Characteristics : Changed minimum value of V _{OH} parameter corresponding to "2.7 V to 3.6 V" from 2.2 V to 2.4 V. Changed minimum value of V _{IH} parameter corresponding to "2.2 V to 2.7 V" from 2.0 V to 1.8 V. Updated Ordering Information : Updated part numbers. Updated Disclaimer. Updated to new template.
*C	5546908	NILE	12/08/2016	Updated Ordering Information : No change in part numbers. Removed Disclaimer (text referencing to contact sales). Completing Sunset Review.
*D	6002325	AESATMP9	12/21/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».



JONHON

«**JONHON**» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А