Synchronous Buck Controller with Constant On-Time and Valley Current Mode

Data Sheet

ADP1870/ADP1871

FEATURES

- Power input voltage range: 2.95 V to 20 V
- On-board bias regulator
- Minimum output voltage: 0.6 V
- 0.6 V reference voltage with ±1.0% accuracy
- Supports all N-channel MOSFET power stages
- Available in 300 kHz, 600 kHz, and 1.0 MHz options
- No current-sense resistor required
- Power saving mode (PSM) for light loads (ADP1871 only)
- Resistor-programmable current-sense gain
- Thermal overload protection
- Short-circuit protection
- Precision enable input
- Integrated bootstrap diode for high-side drive
- Starts into a precharged load
- Small, 10-lead MSOP and LFCSP packages

APPLICATIONS

- Telecom and networking systems
- Mid to high end servers
- Set-top boxes
- DSP core power supplies
- 12 V input POL supplies

GENERAL DESCRIPTION

The ADP1870/ADP1871 are versatile current-mode, synchronous step-down controllers that provide superior transient response, optimal stability, and current-limit protection by using a constant on-time, pseudo-fixed frequency with a programmable current-limit, current-control scheme. In addition, these devices offer optimum performance at low duty cycles by utilizing valley current-mode control architecture. This allows the ADP1870/ADP1871 to drive all N-channel power stages to regulate output voltages as low as 0.6 V.

The ADP1871 is the power saving mode (PSM) version of the device and is capable of pulse skipping to maintain output regulation while achieving improved system efficiency at light loads (see the Power Saving Mode (PSM) Version (ADP1871) section for more information).

Available in three frequency options (300 kHz, 600 kHz, and 1.0 MHz, plus the PSM option), the ADP1870/ADP1871 are well suited for a wide range of applications that require a single-input power supply range from 2.95 V to 20 V. Low voltage biasing is supplied via a 5 V internal LDO.

TYPICAL APPLICATIONS CIRCUIT

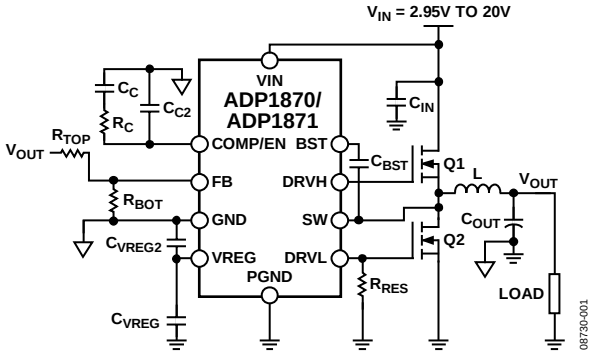

Figure 1.

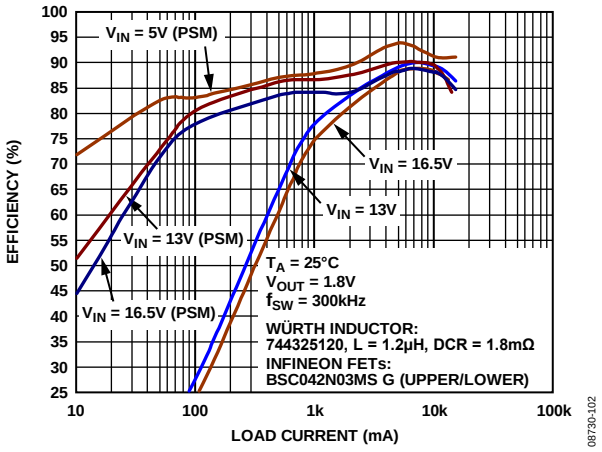

Figure 2. Efficiency vs. Load Current (V_{OUT} = 1.8 V, 300 kHz)

In addition, an internally fixed soft start period is included to limit input in-rush current from the input supply during startup and to provide reverse current protection during soft start for a pre-charged output. The low-side current-sense, current-gain scheme and integration of a boost diode, along with the PSM/forced pulse-width modulation (PWM) option, reduce the external part count and improve efficiency.

The ADP1870/ADP1871 operate over the −40°C to +125°C junction temperature range and are available in a 10-lead MSOP and LFCSP packages.

Rev. B

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7/12—Rev. A to Rev. B

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6/10—Rev. 0 to Rev. A

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3/10—Revision 0: Initial Version

SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). V_{REG} = 5 V, $V_{BST} - V_{SW} = V_{REG} - V_{RECT\_DROP}$ (see Figure 40 to Figure 42). V_{IN} = 12 V. The specifications are valid for T_J = −40°C to +125°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY CHARACTERISTICS						
High Input Voltage Range	V_{IN}	C_{IN} = 22 µF to PGND (at Pin 1)				
		ADP1870ARMZ-0.3/ADP1871ARMZ-0.3 (300 kHz)	2.95	12	20	V
		ADP1870ARMZ-0.6/ADP1871ARMZ-0.6 (600 kHz)	2.95	12	20	V
		ADP1870ARMZ-1.0/ADP1871ARMZ-1.0 (1.0 MHz)	3.25	12	20	V
Quiescent Current	$I_{Q\_REG} + I_{Q\_BST}$	V_{FB} = 1.5 V, no switching		1.1		mA
Shutdown Current	$I_{REG,SD} + I_{BST,SD}$	COMP/EN < 285 mV		190	280	µA
Undervoltage Lockout	UVLO	Rising V_{IN} (see Figure 35 for temperature variation)		2.65		V
UVLO Hysteresis		Falling V_{IN} from operational state		190		mV
INTERNAL REGULATOR CHARACTERISTICS		VREG should not be loaded externally because it is intended to only bias internal circuitry.				
VREG Operational Output Voltage	V_{REG}	C_{VREG} = 1 µF to PGND, 0.22 µF to GND, V_{IN} = 2.95 V to 20 V				
		ADP1870ARMZ-0.3/ADP1871ARMZ-0.3 (300 kHz)	2.75	5	5.5	V
		ADP1870ARMZ-0.6/ADP1871ARMZ-0.6 (600 kHz)	2.75	5	5.5	V
		ADP1870ARMZ-1.0/ADP1871ARMZ-1.0 (1.0 MHz)	3.05	5	5.5	V
VREG Output in Regulation		V_{IN} = 7 V, 100 mA	4.8	4.981	5.16	V
		V_{IN} = 12 V, 100 mA	4.8	4.982	5.16	V
Load Regulation		0 mA to 100 mA, V_{IN} = 7 V		32		mV
		0 mA to 100 mA, V_{IN} = 20 V		33		mV
Line Regulation		V_{IN} = 7 V to 20 V, 20 mA		2.5		mV
		V_{IN} = 7 V to 20 V, 100 mA		2.0		mV
V_{IN} to V_{REG} Dropout Voltage		100 mA out of V_{REG}, $V_{IN} \leq$ 5 V		300	415	mV
Short VREG to PGND		V_{IN} = 20 V		229	320	mA
SOFT START						
Soft Start Period		See Figure 58		3.0		ms
ERROR AMPLIFER						
FB Regulation Voltage	V_{FB}	T_J = +25°C		600		mV
		T_J = −40°C to +85°C	596	600	604	mV
		T_J = −40°C to +125°C	594.2	600	605.8	mV
Transconductance	G_m		320	496	670	µS
FB Input Leakage Current	$I_{FB, Leak}$	V_{FB} = 0.6 V, COMP/EN = released		1	50	nA
CURRENT-SENSE AMPLIFIER GAIN						
Programming Resistor (RES) Value from DRVL to PGND		RES = 47 kΩ ± 1%	2.7	3	3.3	V/V
		RES = 22 kΩ ± 1%	5.5	6	6.5	V/V
		RES = none	11	12	13	V/V
		RES = 100 kΩ ± 1%	22	24	26	V/V
SWITCHING FREQUENCY		Typical values measured at 50% time points with 0 nF at DRVH and DRVL; maximum values are guaranteed by bench evaluation[1]				
ADP1870ARMZ-0.3/ ADP1871ARMZ-0.3 (300 kHz)				300		kHz
On-Time		V_{IN} = 5 V, V_{OUT} = 2 V, T_J = 25°C	1120	1200	1280	ns
Minimum On-Time		V_{IN} = 20 V		146	190	ns
Minimum Off-Time		84% duty cycle (maximum)		340	400	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADP1870ARMZ-0.6/ ADP1871ARMZ-0.6 (600 kHz)				600		kHz
On-Time		V_{IN} = 5 V, V_{OUT} = 2 V, T_J = 25°C	500	540	580	ns
Minimum On-Time		V_{IN} = 20 V, V_{OUT} = 0.8 V		82	110	ns
Minimum Off-Time		65% duty cycle (maximum)		340	400	ns
ADP1870ARMZ-1.0/ ADP1871ARMZ-1.0 (1.0 MHz)				1.0		MHz
On-Time		V_{IN} = 5 V, V_{OUT} = 2 V, T_J = 25°C	285	312	340	ns
Minimum On-Time		V_{IN} = 20 V		60	85	ns
Minimum Off-Time		45% duty cycle (maximum)		340	400	ns
OUTPUT DRIVER CHARACTERISTICS						
High-Side Driver						
Output Source Resistance		I_{SOURCE} = 1.5 A, 100 ns, positive pulse (0 V to 5 V)		2.25	3	Ω
Output Sink Resistance		I_{SINK} = 1.5 A, 100 ns, negative pulse (5 V to 0 V)		0.7	1	Ω
Rise Time[2]	$t_{r,DRVH}$	$V_{BST} - V_{SW}$ = 4.4 V, C_{IN} = 4.3 nF (see Figure 60)		25		ns
Fall Time[2]	$t_{f,DRVH}$	$V_{BST} - V_{SW}$ = 4.4 V, C_{IN} = 4.3 nF (see Figure 61)		11		ns
Low-Side Driver						
Output Source Resistance		I_{SOURCE} = 1.5 A, 100 ns, positive pulse (0 V to 5 V)		1.6	2.2	Ω
Output Sink Resistance		I_{SINK} = 1.5 A, 100 ns, negative pulse (5 V to 0 V)		0.7	1	Ω
Rise Time[2]	$t_{r,DRVL}$	V_{REG} = 5.0 V, C_{IN} = 4.3 nF (see Figure 61)		18		ns
Fall Time[2]	$t_{f,DRVL}$	V_{REG} = 5.0 V, C_{IN} = 4.3 nF (see Figure 60)		16		ns
Propagation Delays						
DRVL Fall to DRVH Rise[2]	$t_{tpdhDRVH}$	$V_{BST} - V_{SW}$ = 4.4 V (see Figure 60)		15.4		ns
DRVH Fall to DRVL Rise[2]	$t_{tpdhDRVL}$	$V_{BST} - V_{SW}$ = 4.4 V (see Figure 61)		18		ns
SW Leakage Current	I_{SWLEAK}	V_{BST} = 25 V, V_{SW} = 20 V, V_{REG} = 5 V			110	µA
Integrated Rectifier						
Channel Impedance		I_{SINK} = 10 mA		22		Ω
PRECISION ENABLE THRESHOLD						
Logic High Level		V_{IN} = 2.9 V to 20 V, V_{REG} = 2.75 V to 5.5 V	245	285	330	mV
Enable Hysteresis		V_{IN} = 2.9 V to 20 V, V_{REG} = 2.75 V to 5.5 V		37		mV
COMP VOLTAGE						
COMP Clamp Low Voltage	$V_{COMP(low)}$	From disabled state, release COMP/EN pin to enable device (2.75 V ≤ V_{REG} ≤ 5.5 V)	0.47			V
COMP Clamp High Voltage	$V_{COMP(high)}$	(2.75 V ≤ V_{REG} ≤ 5.5 V)			2.55	V
COMP Zero Current Threshold	V_{COMP_ZCT}	(2.75 V ≤ V_{REG} ≤ 5.5 V)		1.07		V
THERMAL SHUTDOWN	T_{TMSD}					
Thermal Shutdown Threshold		Rising temperature		155		°C
Thermal Shutdown Hysteresis				15		°C
Hiccup Current Limit Timing				6		ms

[1] The maximum specified values are with the closed loop measured at 10% to 90% time points (see Figure 60 and Figure 61), C_{GATE} = 4.3 nF, and the upper- and lower-side MOSFETs being Infineon BSC042N03MSG.
[2] Not automatic test equipment (ATE) tested.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VREG to PGND, GND	−0.3 V to +6 V
VIN to PGND	−0.3 V to +28 V
FB, COMP/EN to GND	−0.3 V to (V_{REG} + 0.3 V)
DRVL to PGND	−0.3 V to (V_{REG} + 0.3 V)
SW to PGND	−2.0 V to +28 V
BST to SW	−0.6 V to (V_{REG} + 0.3 V)
BST to PGND	−0.3 V to 28 V
DRVH to SW	−0.3 V to V_{REG}
PGND to GND	±0.3 V
θ_{JA} (10-Lead MSOP)	
2-Layer Board	213.1°C/W
4-Layer Board	171.7°C/W
θ_{JA} (10-Lead LFCSP)	
4-Layer Board	40°C/W
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
Maximum Soldering Lead Temperature (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to PGND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
θ_{JA} (10-Lead MSOP)		
2-Layer Board	213.1	°C/W
4- Layer Board	171.7	°C/W
θ_{JA} (10-Lead LFCSP)		
4- Layer Board	40	°C/W

[1] θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for the device soldered in a circuit board for surface-mount packages.

BOUNDARY CONDITION

In determining the values given in Table 2 and Table 3, natural convection was used to transfer heat to a 4-layer evaluation board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

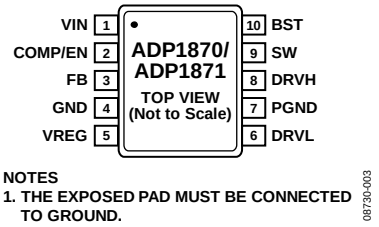

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	High Input Voltage. Connect VIN to the drain of the upper-side MOSFET.
2	COMP/EN	Output of the Internal Error Amplifier/IC Enable. When this pin functions as EN, applying 0 V to this pin disables the IC.
3	FB	Noninverting Input of the Internal Error Amplifier. This is the node where the feedback resistor is connected.
4	GND	Analog Ground Reference Pin of the IC. All sensitive analog components should be connected to this ground plane (see the Layout Considerations section).
5	VREG	Internal Regulator Supply Bias Voltage for the ADP1870/ADP1871 Controller (Includes the Output Gate Drivers). A bypass capacitor of 1 µF directly from this pin to PGND and a 0.1 µF across VREG and GND are recommended. VREG should not be loaded externally because it is intended to only bias internal circuitry.
6	DRVL	Drive Output for the External Lower-Side, N-Channel MOSFET. This pin also serves as the current-sense gain setting pin (see Figure 69).
7	PGND	Power GND. Ground for the lower-side gate driver and lower-side, N-channel MOSFET.
8	DRVH	Drive Output for the External Upper-Side, N-Channel MOSFET.
9	SW	Switch Node Connection.
10	BST	Bootstrap for the Upper-Side MOSFET Gate Drive Circuitry. An internal boot rectifier (diode) is connected between VREG and BST. A capacitor from BST to SW is required. An external Schottky diode can also be connected between VREG and BST for increased gate drive capability.

TYPICAL PERFORMANCE CHARACTERISTICS

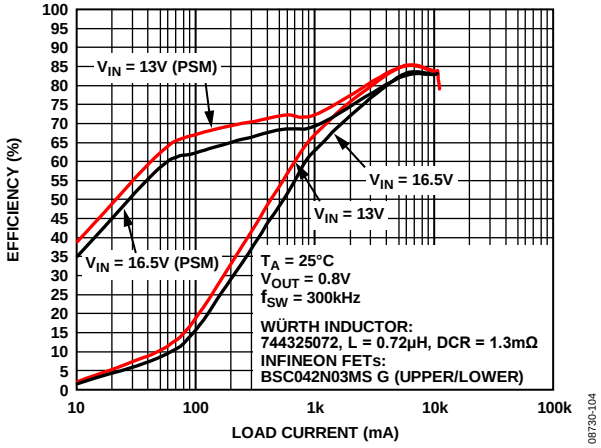

Figure 4. Efficiency—300 kHz, V_{OUT} = 0.8 V

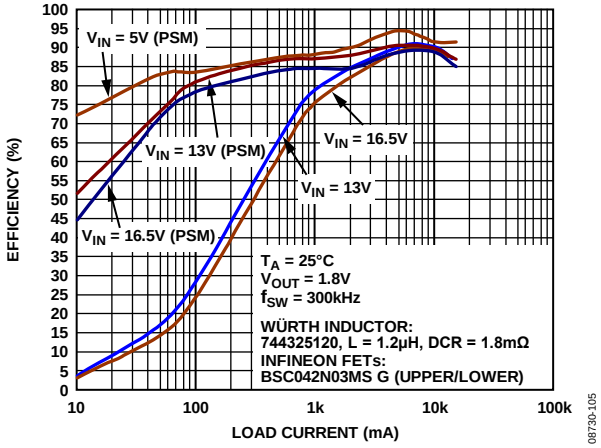

Figure 5. Efficiency—300 kHz, V_{OUT} = 1.8 V

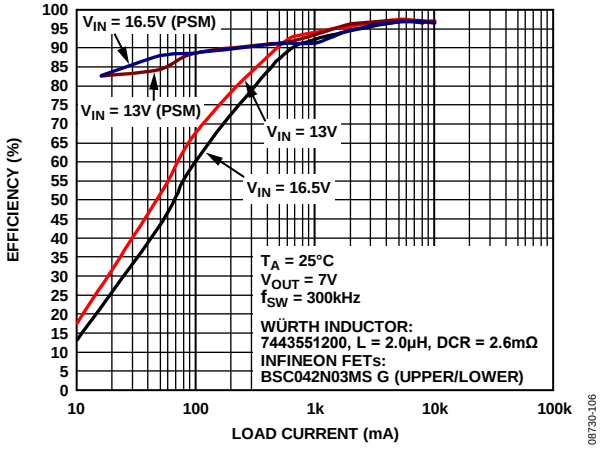

Figure 6. Efficiency—300 kHz, V_{OUT} = 7 V

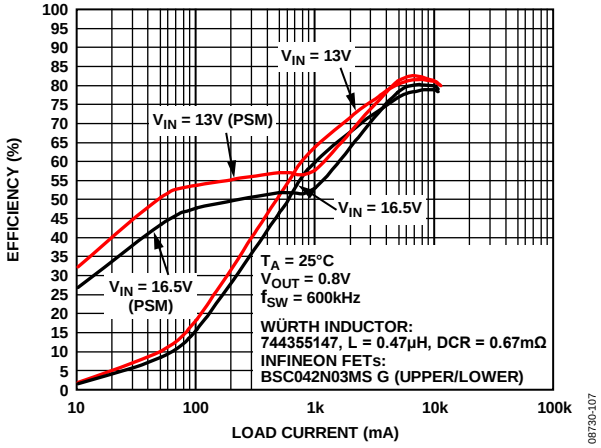

Figure 7. Efficiency—600 kHz, V_{OUT} = 0.8 V

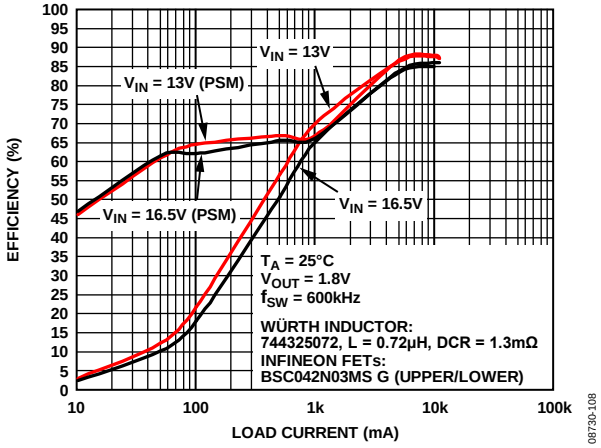

Figure 8. Efficiency—600 kHz, V_{OUT} = 1.8 V

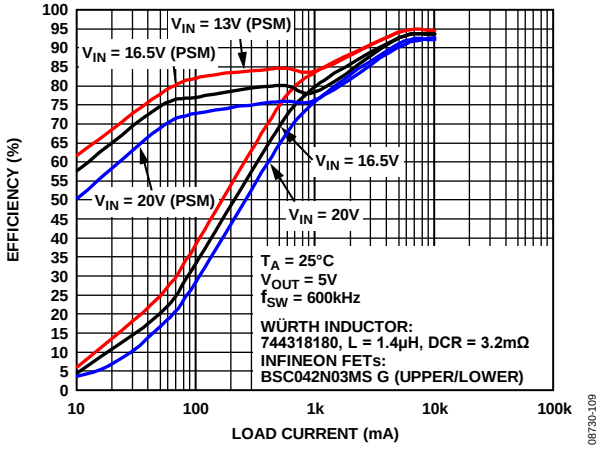

Figure 9. Efficiency—600 kHz, V_{OUT} = 5 V

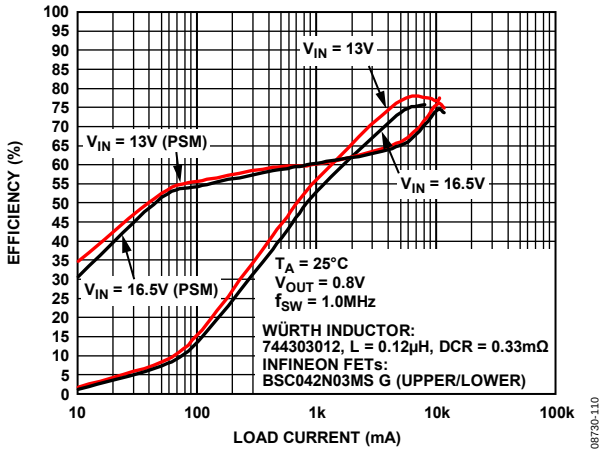

Figure 10. Efficiency—1.0 MHz, V_{OUT} = 0.8 V

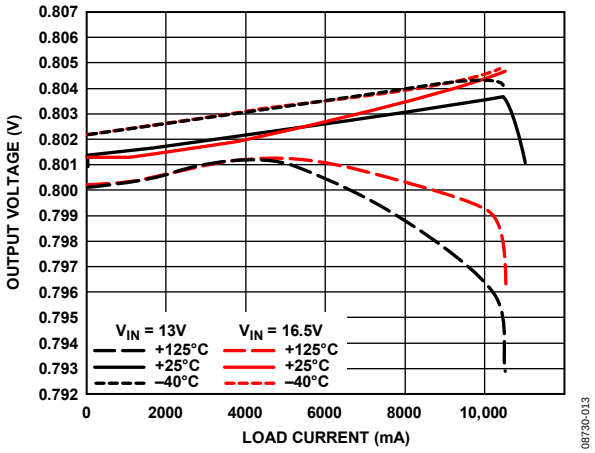

Figure 13. Output Voltage Accuracy—300 kHz, V_{OUT} = 0.8 V

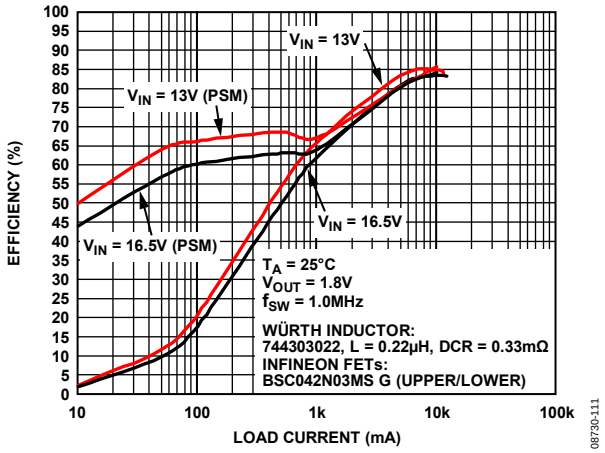

Figure 11. Efficiency—1.0 MHz, V_{OUT} = 1.8 V

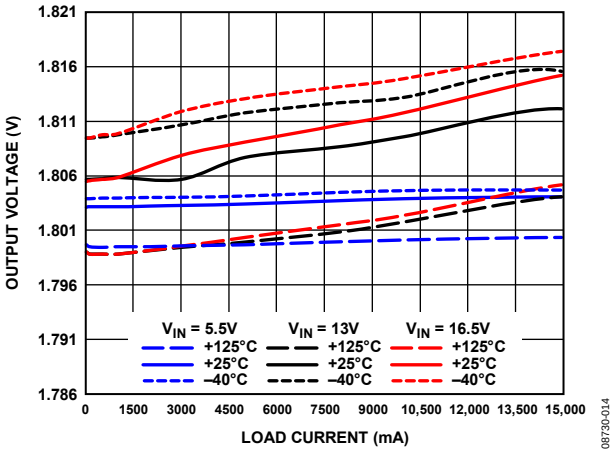

Figure 14. Output Voltage Accuracy—300 kHz, V_{OUT} = 1.8 V

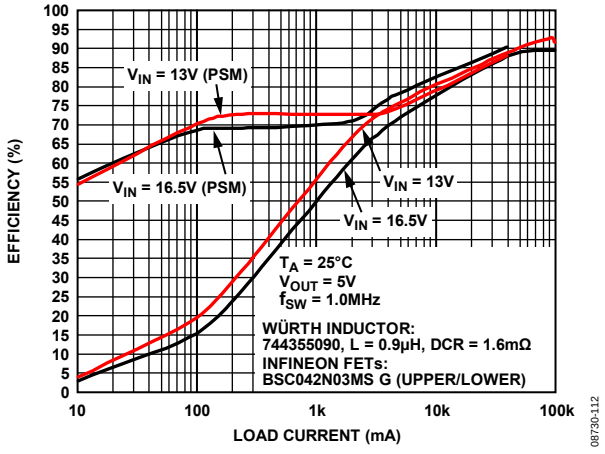

Figure 12. Efficiency—1.0 MHz, V_{OUT} = 5 V

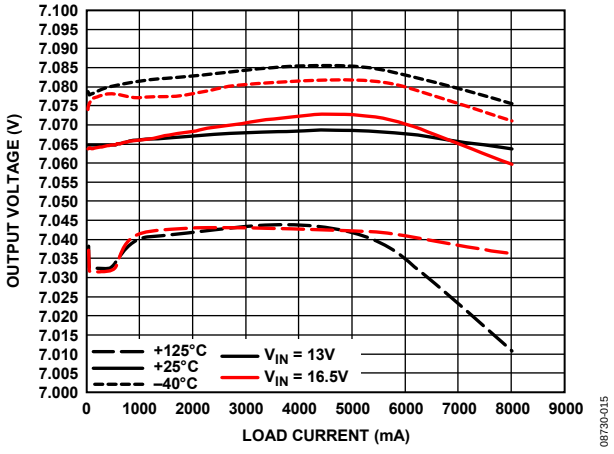

Figure 15. Output Voltage Accuracy—300 kHz, V_{OUT} = 7 V

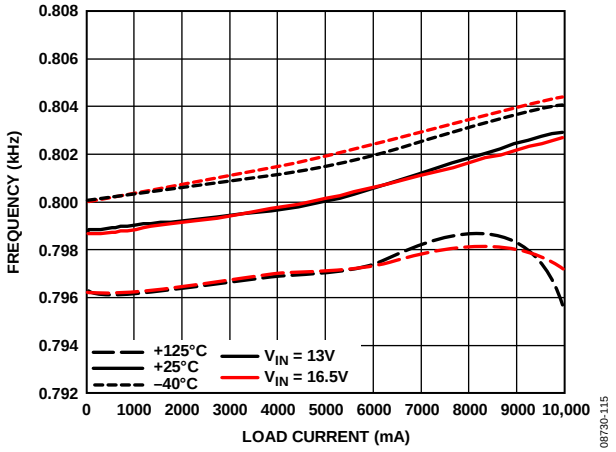

Figure 16. Output Voltage Accuracy—600 kHz, V_{OUT} = 0.8 V

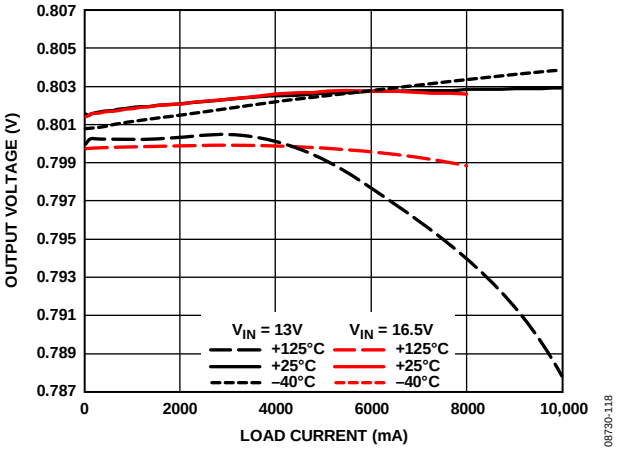

Figure 19. Output Voltage Accuracy—1.0 MHz, V_{OUT} = 0.8 V

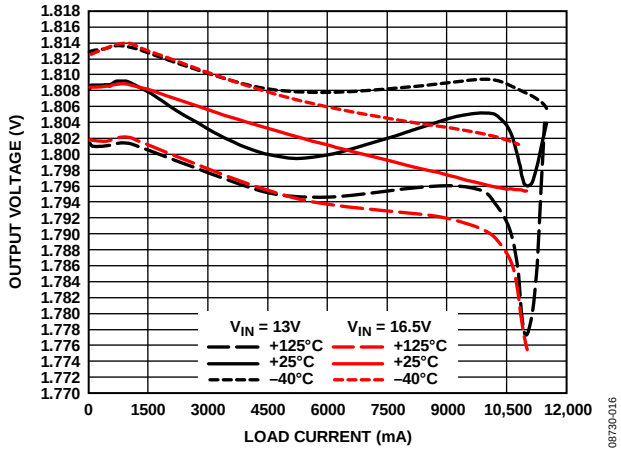

Figure 17. Output Voltage Accuracy—600 kHz, V_{OUT} = 1.8 V

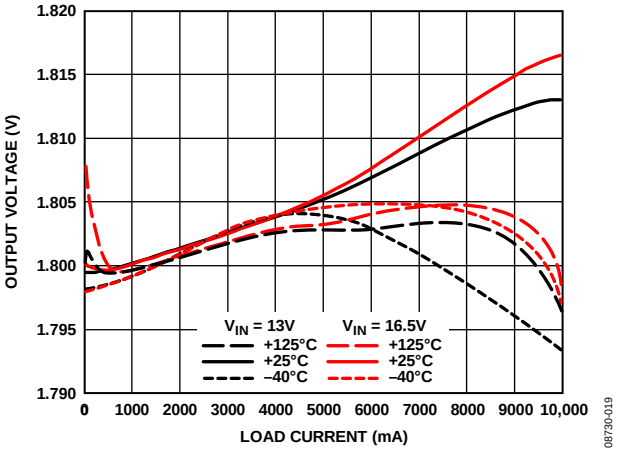

Figure 20. Output Voltage Accuracy—1.0 MHz, V_{OUT} = 1.8 V

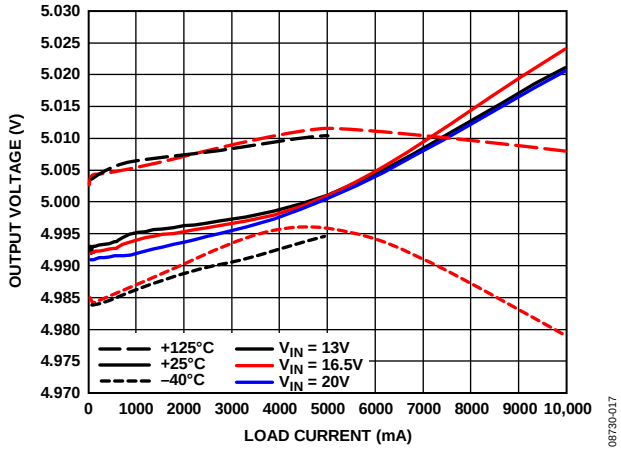

Figure 18. Output Voltage Accuracy—600 kHz, V_{OUT} = 5 V

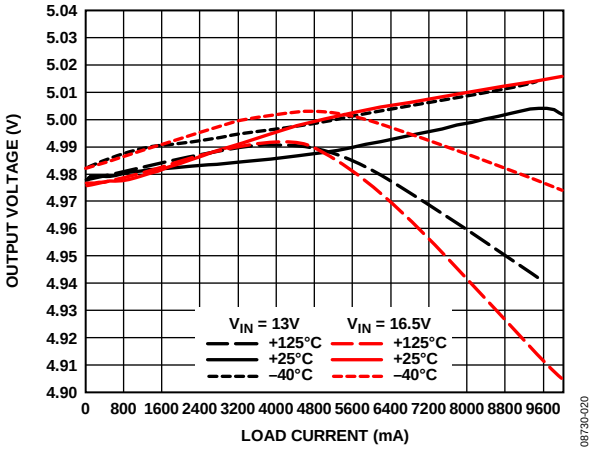

Figure 21. Output Voltage Accuracy—1.0 MHz, V_{OUT} =5 V

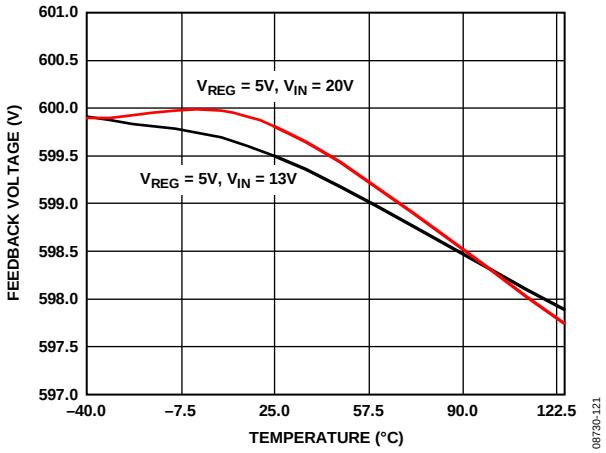

Figure 22. Feedback Voltage vs. Temperature

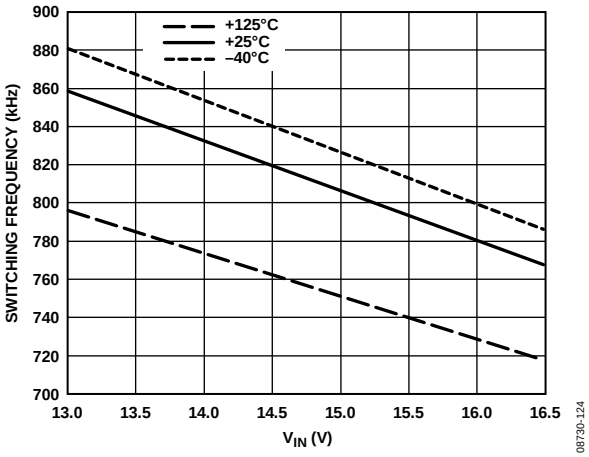

Figure 25. Switching Frequency vs. High Input Voltage, 1.0 MHz, V_{IN} Range = 13 V to 16.5 V

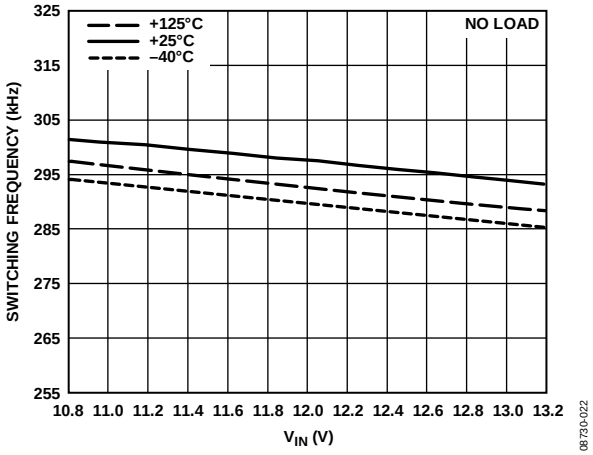

Figure 23. Switching Frequency vs. High Input Voltage, 300 kHz, ±10% of 12 V

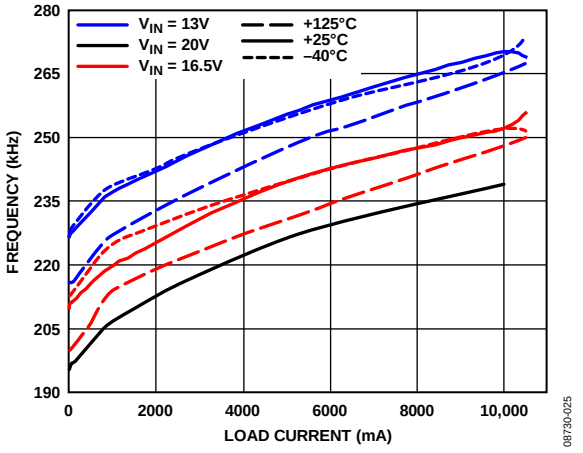

Figure 26. Frequency vs. Load Current, 300 kHz, V_{OUT} = 0.8 V

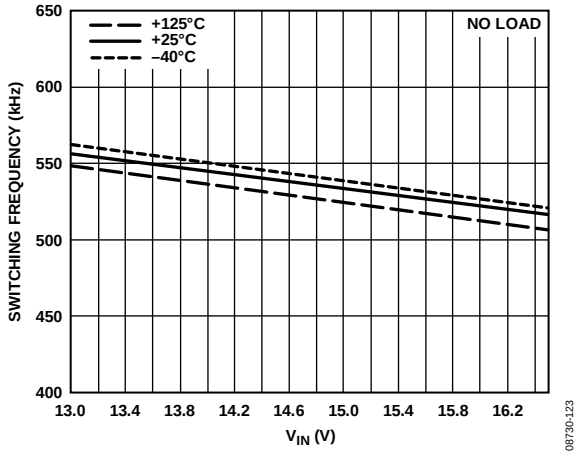

Figure 24. Switching Frequency vs. High Input Voltage, 600 kHz, V_{OUT} = 1.8 V, V_{IN} Range = 13 V to 16.5 V

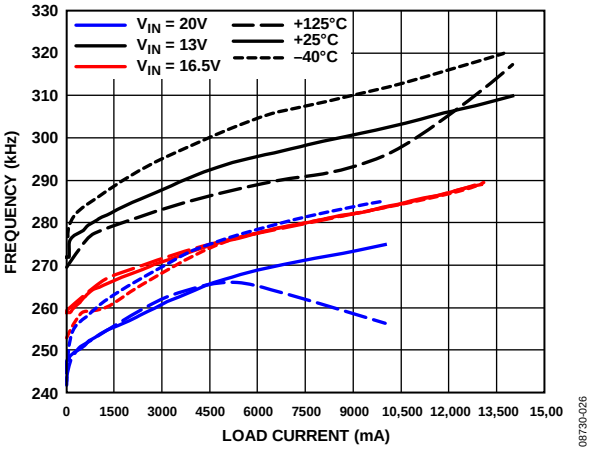

Figure 27. Frequency vs. Load Current, 300 kHz, V_{OUT} = 1.8 V

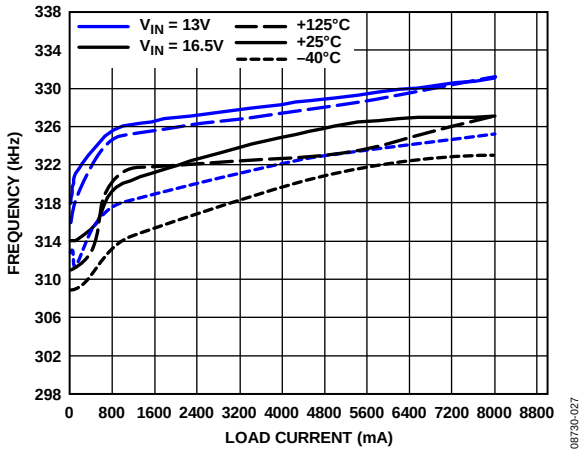

Figure 28. Frequency vs. Load Current, 300 kHz, V_{OUT} = 7 V

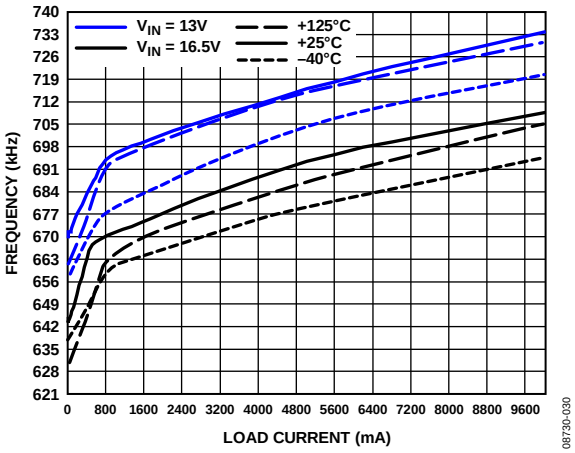

Figure 31. Frequency vs. Load Current, 600 kHz, V_{OUT} = 5 V

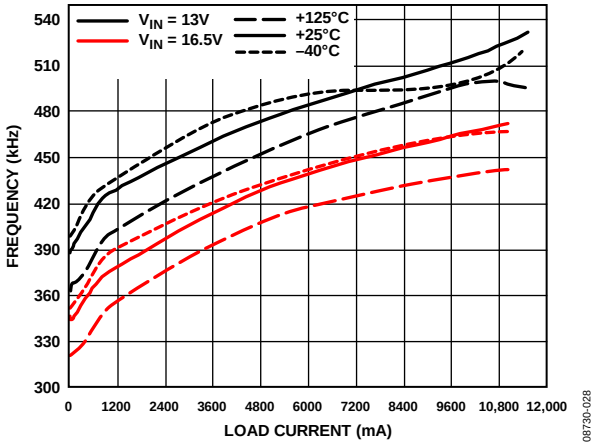

Figure 29. Frequency vs. Load Current, 600 kHz, V_{OUT} = 0.8 V

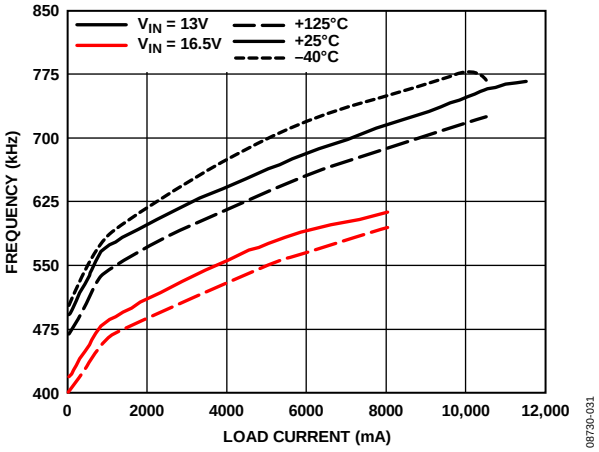

Figure 32. Frequency vs. Load Current, V_{OUT} = 1.0 MHz, 0.8 V

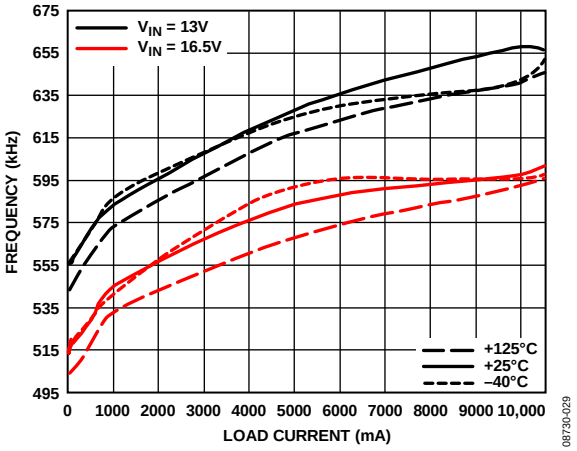

Figure 30. Frequency vs. Load Current, 600 kHz, V_{OUT} = 1.8 V

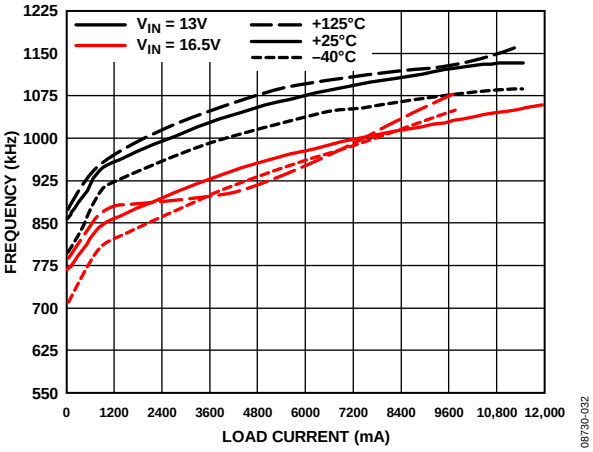

Figure 33. Frequency vs. Load Current, 1.0 MHz, V_{OUT} = 1.8 V

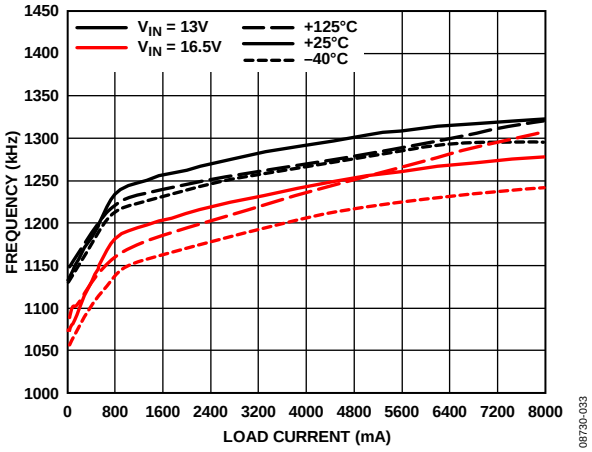

Figure 34. Frequency vs. Load Current, 1.0 MHz, V_{OUT} = 5 V

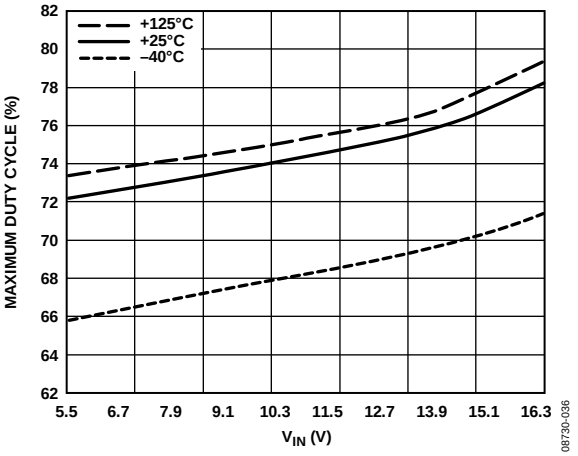

Figure 37. Maximum Duty Cycle vs. High Voltage Input (V_{IN})

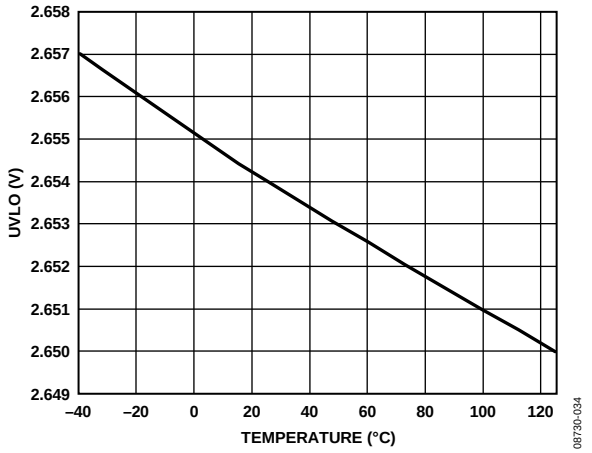

Figure 35. UVLO vs. Temperature

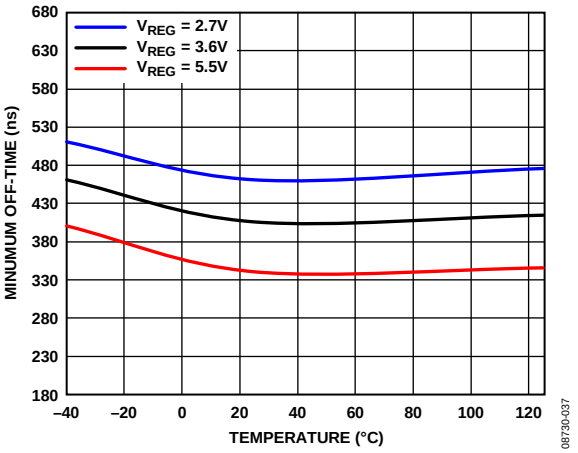

Figure 38. Minimum Off-Time vs. Temperature

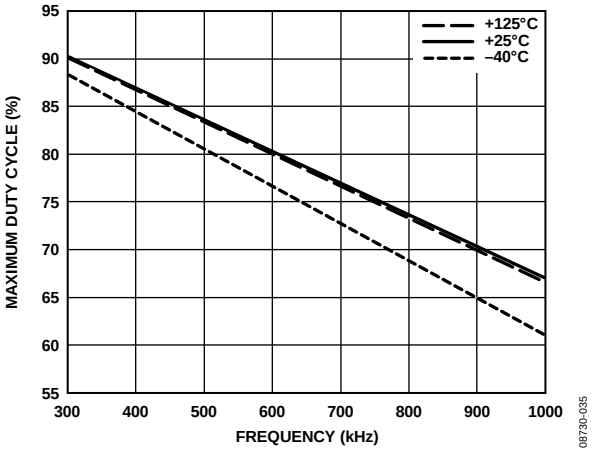

Figure 36. Maximum Duty Cycle vs. Frequency

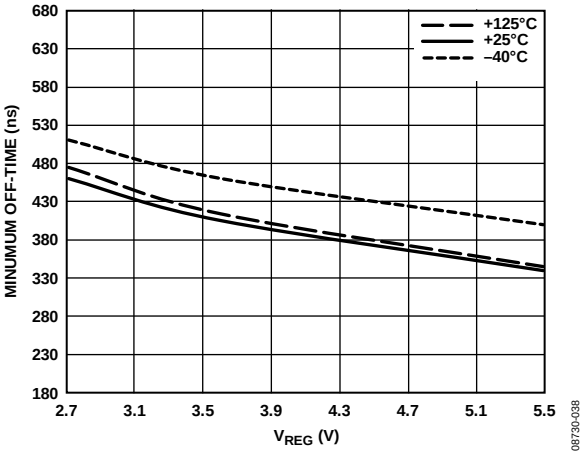

Figure 39. Minimum Off-Time vs. V_{REG} (Low Input Voltage)

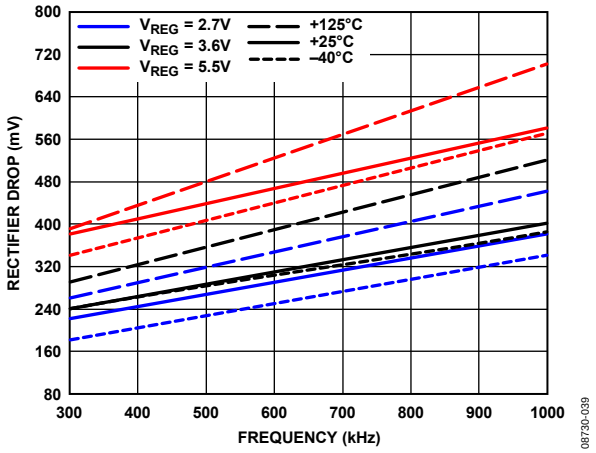

Figure 40. Internal Rectifier Drop vs. Frequency

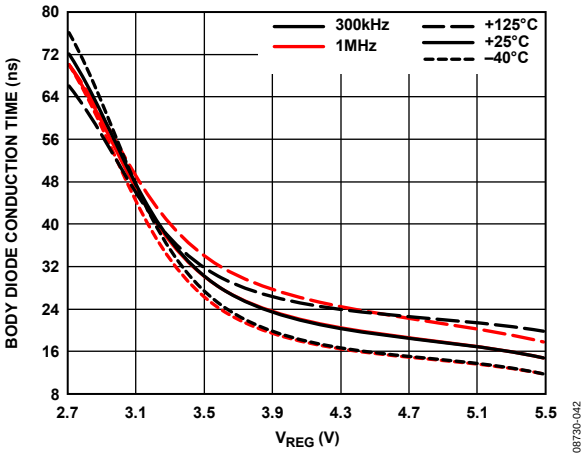

Figure 43. Lower-Side MOSFET Body Diode Conduction Time vs. V_{REG}

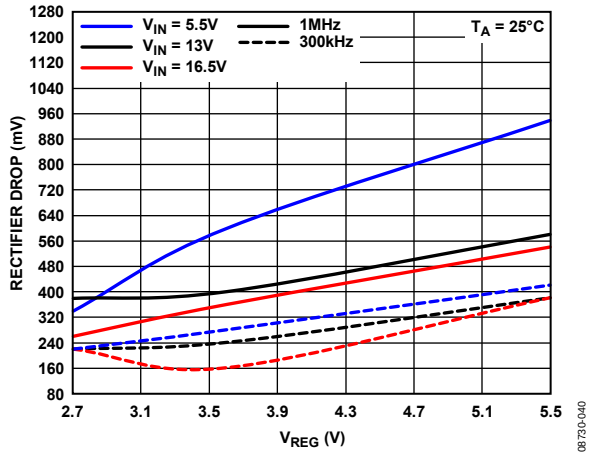

Figure 41. Internal Boost Rectifier Drop vs. V_{REG} (Low Input Voltage) Over V_{IN} Variation

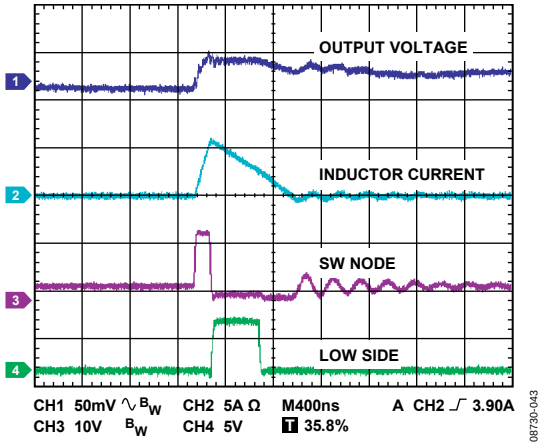

Figure 44. Power Saving Mode (PSM) Operational Waveform, 100 mA

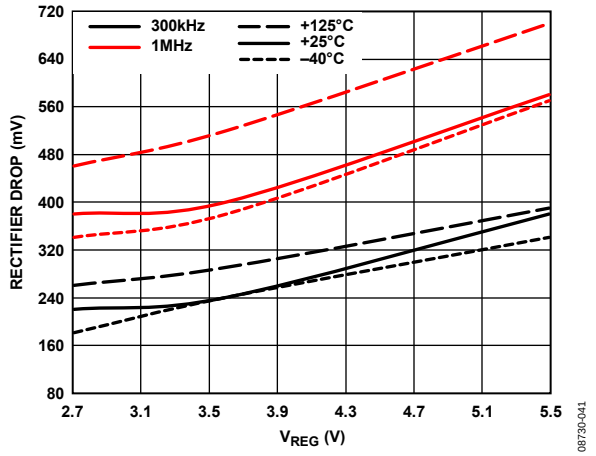

Figure 42. Internal Boost Rectifier Drop vs. V_{REG}

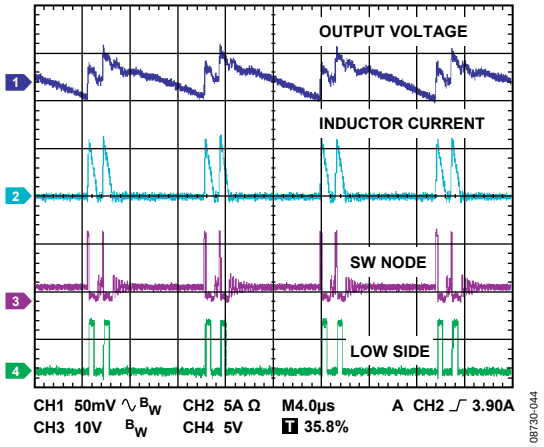

Figure 45. PSM Waveform at Light Load, 500 mA

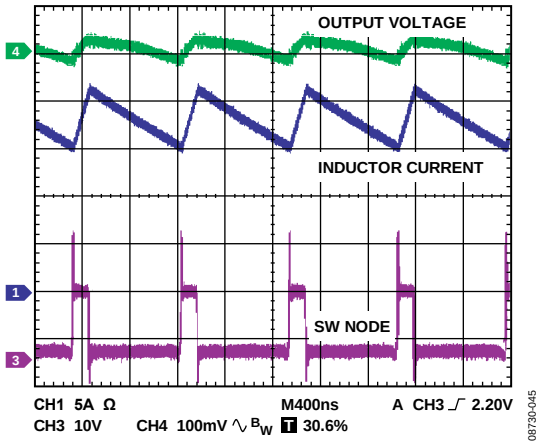

Figure 46. CCM Operation at Heavy Load, 12 A
(See Figure 94 for Application Circuit)

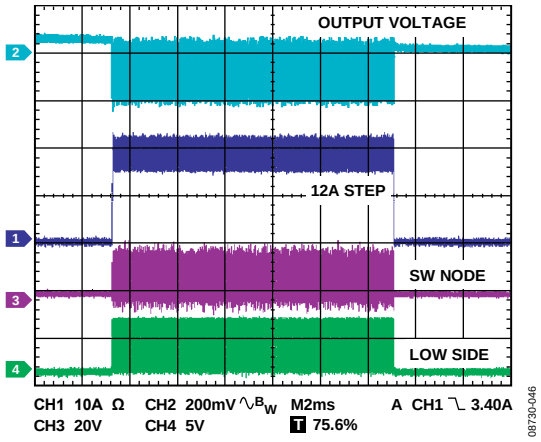

Figure 47. Load Transient Step—PSM Enabled, 12 A
(See Figure 94 Application Circuit)

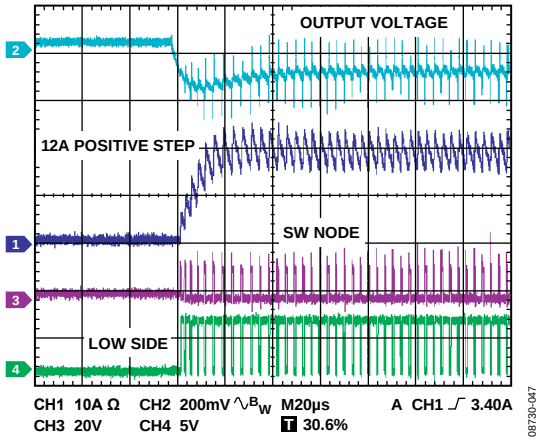

Figure 48. Positive Step During Heavy Load Transient Behavior—PSM Enabled, 12 A, V_{OUT} = 1.8 V (See Figure 94 Application Circuit)

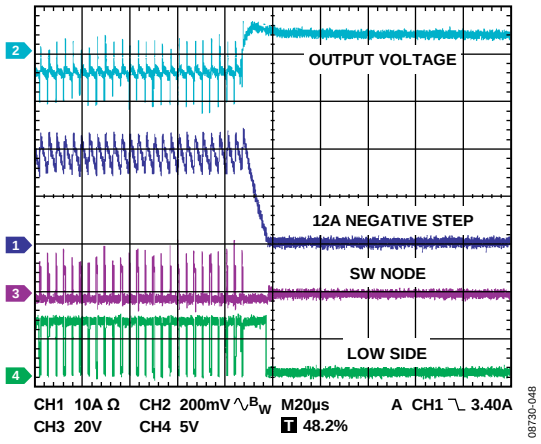

Figure 49. Negative Step During Heavy Load Transient Behavior—PSM Enabled, 12 A (See Figure 94 Application Circuit)

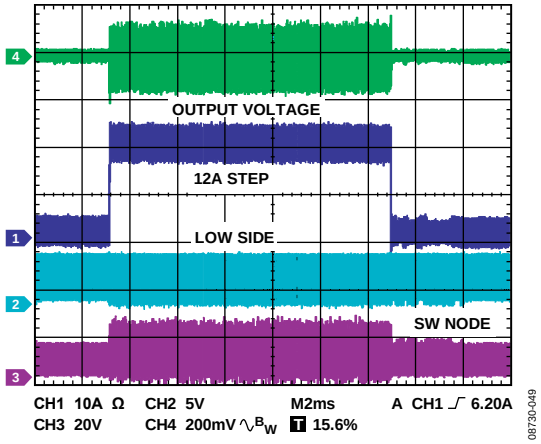

Figure 50. Load Transient Step—Forced PWM at Light Load, 12 A
(See Figure 94 Application Circuit)

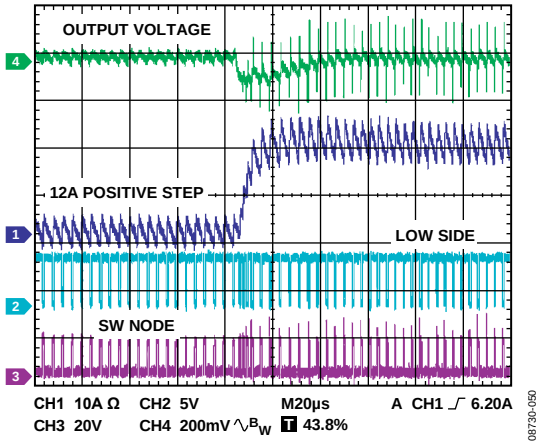

Figure 51. Positive Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 12 A, V_{OUT} = 1.8 V (See Figure 94 Application Circuit)

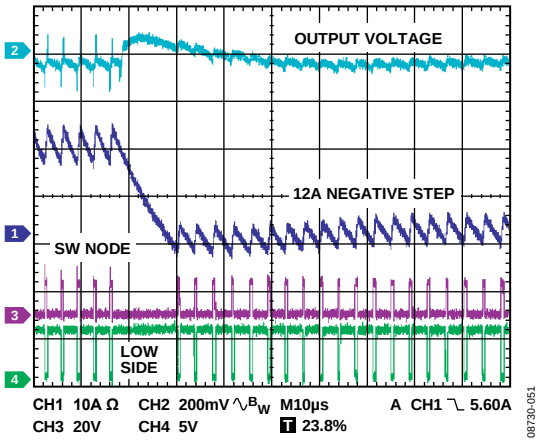

Figure 52. Negative Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 12 A (See Figure 94 Application Circuit)

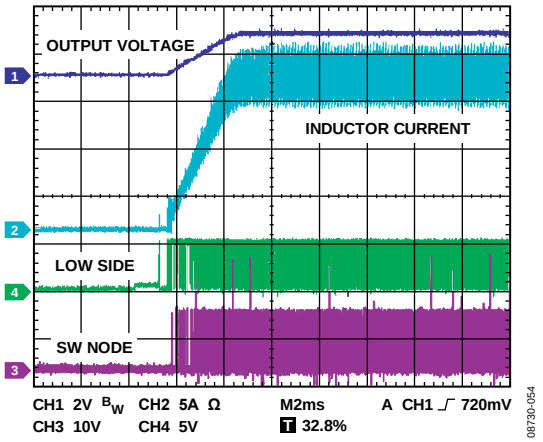

Figure 55. Start-Up Behavior at Heavy Load, 12 A, 300 kHz (See Figure 94 Application Circuit)

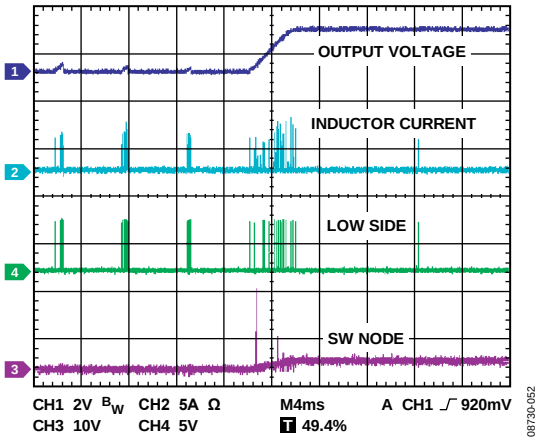

Figure 53. Output Short-Circuit Behavior Leading to Hiccup Mode

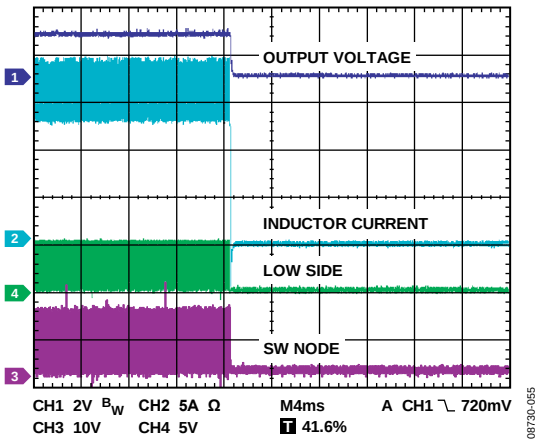

Figure 56. Power-Down Waveform During Heavy Load

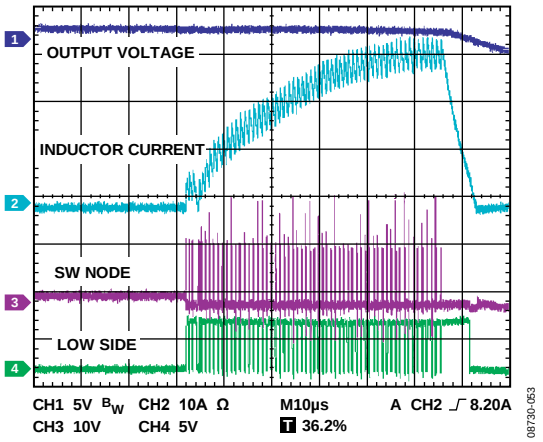

Figure 54. Magnified Waveform During Hiccup Mode

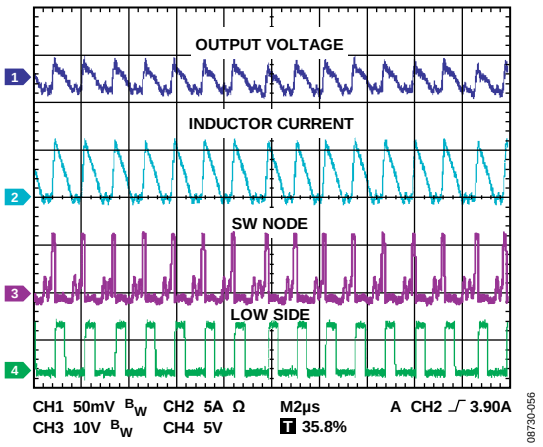

Figure 57. Output Voltage Ripple Waveform During PSM Operation at Light Load, 2 A

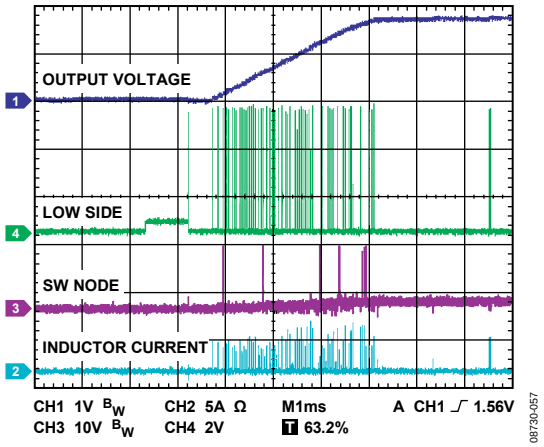

Figure 58. Soft Start and RES Detect Waveform

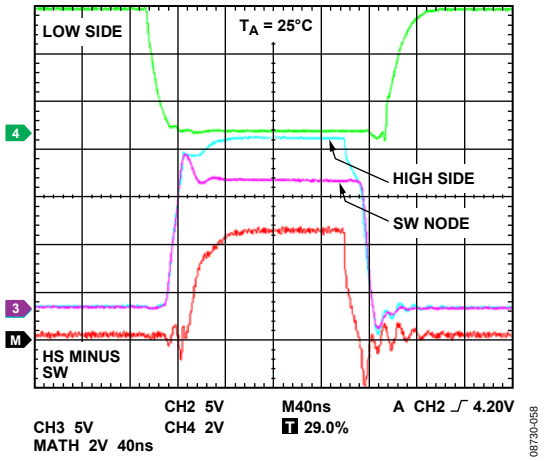

Figure 59. Output Drivers and SW Node Waveforms

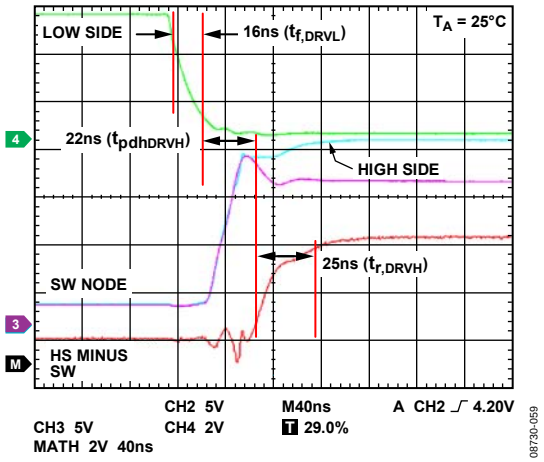

Figure 60. Upper-Side Driver Rising and Lower-Side Falling Edge Waveforms (C_{IN} = 4.3 nF (Upper-/Lower-Side MOSFET), Q_{TOTAL} = 27 nC (V_{GS} = 4.4 V (Q1), V_{GS} = 5 V (Q3))

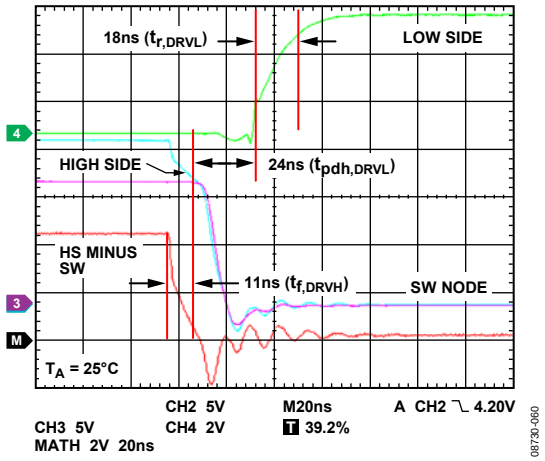

Figure 61. Upper-Side Driver Falling and Lower-Side Rising Edge Waveforms (C_{IN} = 4.3 nF (Upper-/Lower-Side MOSFET), Q_{TOTAL} = 27 nC (V_{GS} = 4.4 V (Q1), V_{GS} = 5 V (Q3))

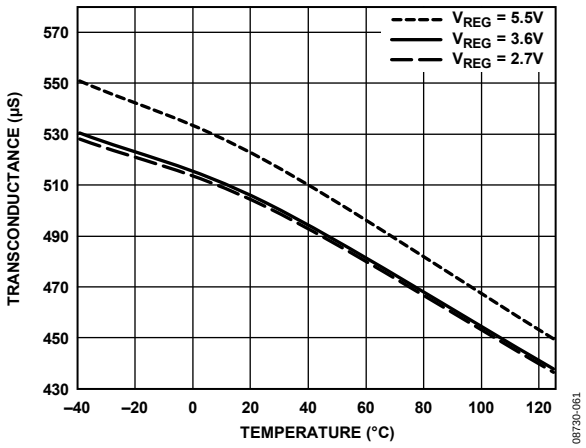

Figure 62. Transconductance (G_m) vs. Temperature

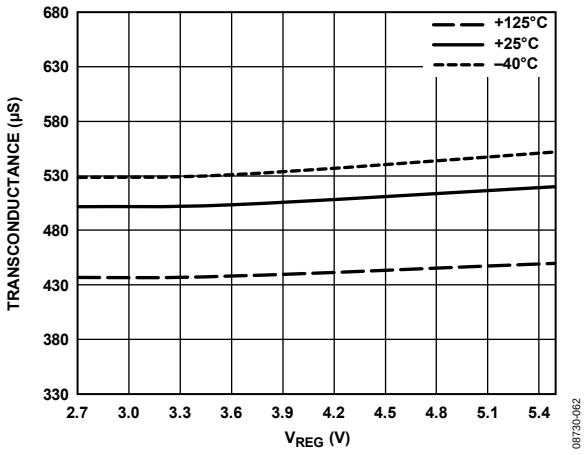

Figure 63. Transconductance (G_m) vs. V_{REG}

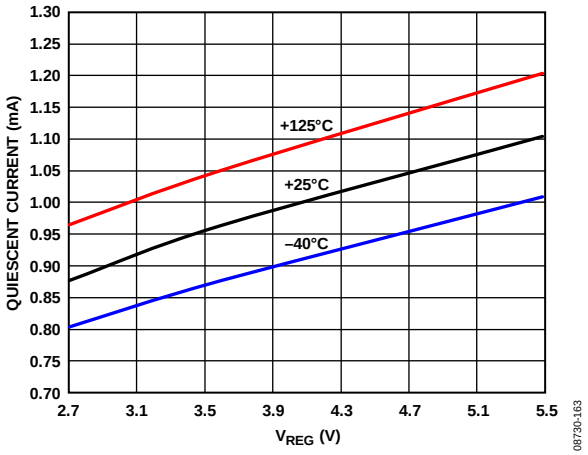

Figure 64. Quiescent Current vs. V_{REG}

ADP1870/ADP1871 BLOCK DIAGRAM

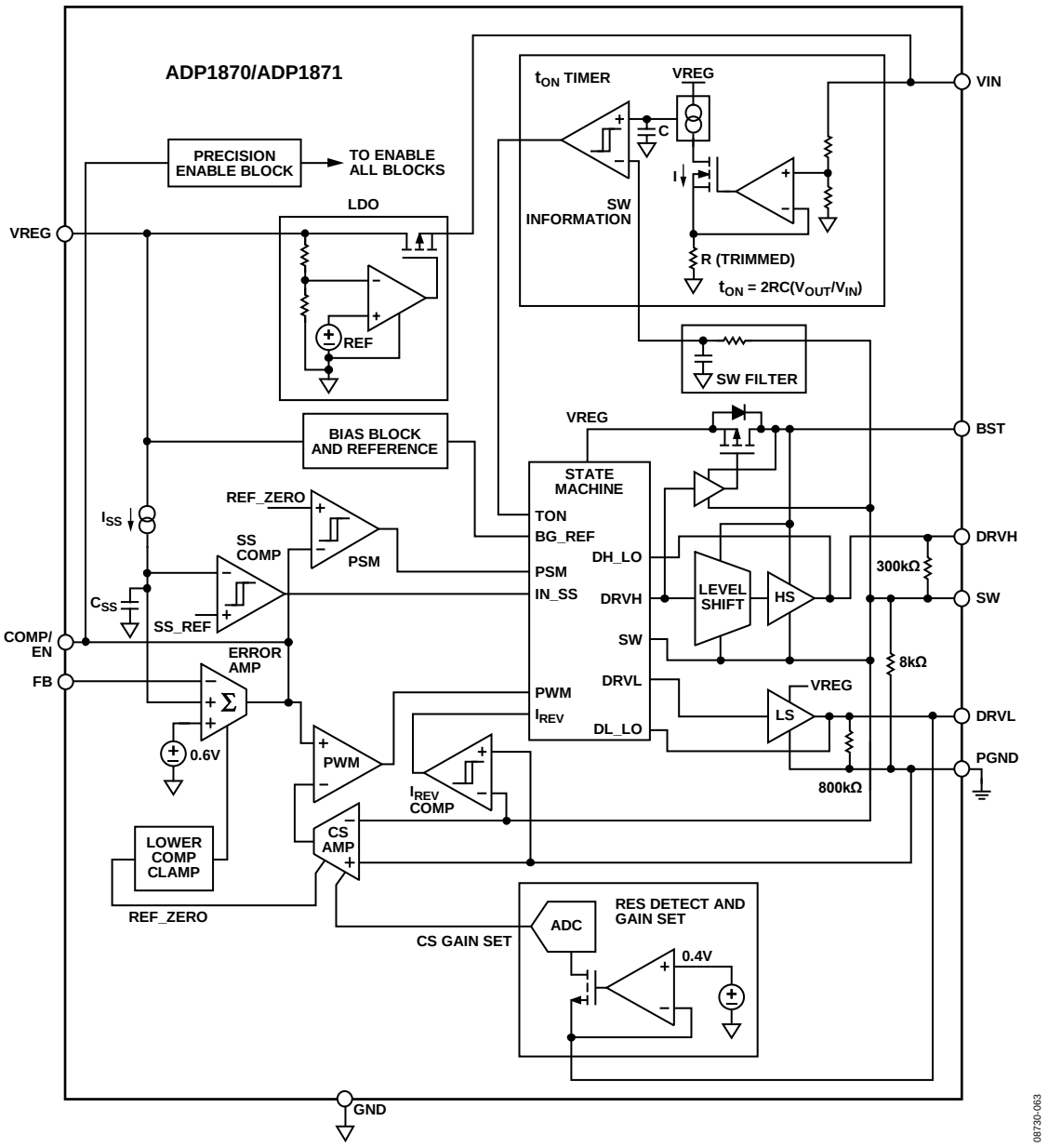

Figure 65. ADP1870/ADP1871 Block Diagram

THEORY OF OPERATION

The ADP1870/ADP1871 are versatile current-mode, synchronous step-down controllers that provide superior transient response, optimal stability, and current limit protection by using a constant on-time, pseudo-fixed frequency with a programmable current-sense gain, current-control scheme. In addition, these devices offer optimum performance at low duty cycles by utilizing valley current-mode control architecture. This allows the ADP1870/ADP1871 to drive all N-channel power stages to regulate output voltages as low as 0.6 V.

STARTUP

The ADP1870/ADP1871 have an internal regulator (VREG) for biasing and supplying power for the integrated MOSFET drivers. A bypass capacitor should be located directly across the VREG (Pin 5) and PGND (Pin 7) pins. Included in the power-up sequence is the biasing of the current-sense amplifier, the current-sense gain circuit (see the Programming Resistor (RES) Detect Circuit section), the soft start circuit, and the error amplifier.

The current-sense blocks provide valley current information (see the Programming Resistor (RES) Detect Circuit section) and are a variable of the compensation equation for loop stability (see the Compensation Network section). The valley current information is extracted by forcing 0.4 V across the DRVL output and PGND pin, which generates a current depending on the resistor across DRVL and PGND in a process performed by the RES detect circuit. The current through the resistor is used to set the current-sense amplifier gain. This process takes approximately 800 µs, after which the drive signal pulses appear at the DRVL and DRVH pins synchronously and the output voltage begins to rise in a controlled manner through the soft start sequence.

The rise time of the output voltage is determined by the soft start and error amplifier blocks (see the Soft Start section). At the beginning of a soft start, the error amplifier charges the external compensation capacitor, causing the COMP/EN pin to rise above the enable threshold of 285 mV, thus enabling the ADP1870/ADP1871.

SOFT START

The ADP1870/ADP1871 have digital soft start circuitry, which involves a counter that initiates an incremental increase in current, by 1 µA, via a current source on every cycle through a fixed internal capacitor. The output tracks the ramping voltage by producing PWM output pulses to the upper-side MOSFET. The purpose is to limit the in-rush current from the high voltage input supply (V_{IN}) to the output (V_{OUT}).

PRECISION ENABLE CIRCUITRY

The ADP1870/ADP1871 employ precision enable circuitry. The enable threshold is 285 mV typical with 35 mV of hysteresis. The devices are enabled when the COMP/EN pin is released, allowing the error amplifier output to rise above the enable threshold (see Figure 66). Grounding this pin disables the ADP1870/ADP1871, reducing the supply current of the devices to approximately 140 µA. For more information, see Figure 67.

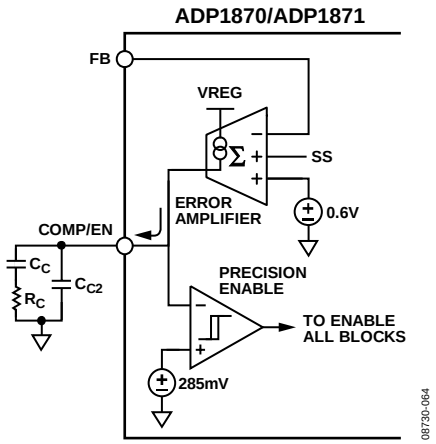

Figure 66. Release COMP/EN Pin to Enable the ADP1870/ADP1871

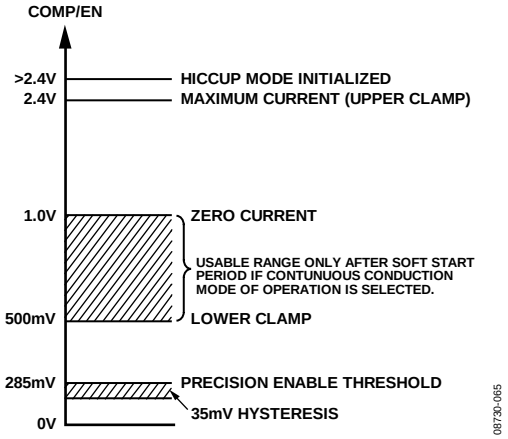

Figure 67. COMP/EN Voltage Range

UNDERVOLTAGE LOCKOUT

The undervoltage lockout (UVLO) feature prevents the part from operating both the upper- and lower-side MOSFETs at extremely low or undefined input voltage (V_{IN}) ranges. Operation at an undefined bias voltage may result in the incorrect propagation of signals to the high-side power switches. This, in turn, results in invalid output behavior that can cause damage to the output devices, ultimately destroying the device tied to the output. The UVLO level has been set at 2.65 V (nominal).

ON-BOARD LOW DROPOUT REGULATOR

The ADP1870 uses an on-board LDO to bias the internal digital and analog circuitry. With proper bypass capacitors connected to the VREG pin (output of internal LDO), this pin also provides power for the internal MOSFET drivers. It is recommended to float VREG if VIN is utilized for greater than 5.5 V operation. The minimum voltage where bias is guaranteed to operate is 2.75 V at VREG.

For applications where VIN is decoupled from VREG, the minimum voltage at VIN must be 2.9 V. It is recommended that

VIN and VREG be tied together if the VIN pin is subjected to a 2.75 V rail.

Table 5. Power Input and LDO Output Configurations

VIN	VREG	Comments
>5.5 V	Float	Must use the LDO
<5.5 V	Connect to VIN	LDO drop voltage is not realized (that is, if V_{IN} = 2.75 V, then V_{REG} = 2.75 V)
<5.5 V	Float	LDO drop is realized
Ranges above and below 5.5 V	Float	LDO drop is realized, minimum V_{IN} recommendation is 2.95 V

THERMAL SHUTDOWN

The thermal shutdown is a self-protection feature to prevent the IC from damage due to a very high operating junction temperature. If the junction temperature of the device exceeds 155°C, the part enters the thermal shutdown state. In this state, the device shuts off both the upper- and lower-side MOSFETs and disables the entire controller immediately, thus reducing the power consumption of the IC. The part resumes operation after the junction temperature of the part cools to less than 140°C.

PROGRAMMING RESISTOR (RES) DETECT CIRCUIT

Upon startup, one of the first blocks to become active is the RES detect circuit. This block powers up before soft start begins. It forces a 0.4 V reference value at the DRVL output (see Figure 68) and is programmed to identify four possible resistor values: 47 kΩ, 22 kΩ, open, and 100 kΩ.

The RES detect circuit digitizes the value of the resistor at the DRVL pin (Pin 6). An internal ADC outputs a 2-bit digital code that is used to program four separate gain configurations in the current-sense amplifier (see Figure 69). Each configuration corresponds to a current-sense gain (A_{CS}) of 3 V/V, 6 V/V, 12 V/V, 24 V/V, respectively (see Table 6 and Table 7). This variable is used for the valley current-limit setting, which sets up the appropriate current-sense gain for a given application and sets the compensation necessary to achieve loop stability (see the Valley Current-Limit Setting and Compensation Network sections).

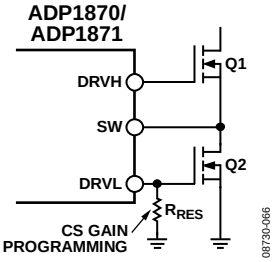

Figure 68. Programming Resistor Location

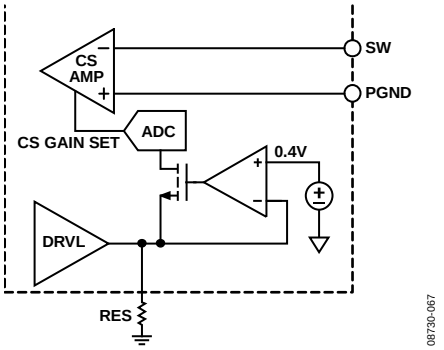

Figure 69. RES Detect Circuit for Current-Sense Gain Programming

Table 6. Current-Sense Gain Programming

Resistor	A_{CS}
47 kΩ	3 V/V
22 kΩ	6 V/V
Open	12 V/V
100 kΩ	24 V/V

VALLEY CURRENT-LIMIT SETTING

The architecture of the ADP1870/ADP1871 is based on valley current-mode control. The current limit is determined by three components: the R_{ON} of the lower-side MOSFET, the error amplifier output voltage swing (COMP), and the current-sense gain. The COMP range is internally fixed at 1.4 V. The current-sense gain is programmable via an external resistor at the DRVL pin (see the Programming Resistor (RES) Detect Circuit section). The R_{ON} of the lower-side MOSFET can vary over temperature and usually has a positive T_C (meaning that it increases with temperature); therefore, it is recommended to program the current-sense gain resistor based on the rated R_{ON} of the MOSFET at 125°C.

Because the ADP1870/ADP1871 are based on valley current control, the relationship between I_{CLIM} and I_{LOAD} is as follows:

$$I_{CLIM} = I_{LOAD} \times \left(1 - \frac{K_I}{2}\right)$$

where:
K_I is the ratio between the inductor ripple current and the desired average load current (see Figure 70).
I_{CLIM} is the desired valley current limit.
I_{LOAD} is the current load.

Establishing K_I helps to determine the inductor value (see the Inductor Selection section), but in most cases K_I = 0.33.

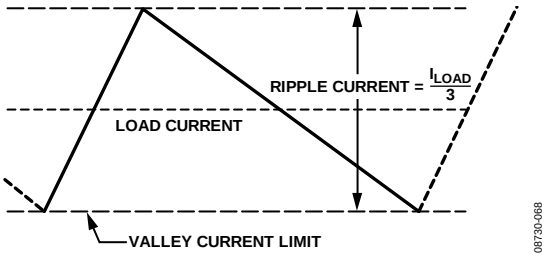

Figure 70. Valley Current Limit to Average Current Relation

When the desired valley current limit (I_{CLIM}) has been determined, the current-sense gain can be calculated as follows:

$$I_{CLIM} = \frac{1.4\ V}{A_{CS} \times R_{ON}}$$

where:
R_{ON} is the channel impedance of the lower-side MOSFET.
A_{CS} is the current-sense gain multiplier (see Table 6 and Table 7).

Although the ADP1870/ADP1871 have only four discrete current-sense gain settings for a given R_{ON} variable, Table 7 and Figure 71 outline several available options for the valley current setpoint based on various R_{ON} values.

Table 7. Valley Current Limit Program[1]

	Valley Current Level			
R_{ON} (mΩ)	47 kΩ A_{CS} = 3 V/V	22 kΩ A_{CS} = 6 V/V	Open A_{CS} = 12 V/V	100 kΩ A_{CS} = 24 V/V
1.5				38.9
2				29.2
2.5				23.3
3			39.0	19.5
3.5			33.4	16.7
4.5			26.0	13
5			23.4	11.7
5.5			21.25	10.6
10		23.3	11.7	5.83
15	31.0	15.5	7.75	3.87
18	26.0	13.0	6.5	3.25

[1] Refer to Figure 71 for more information and a graphical representation.

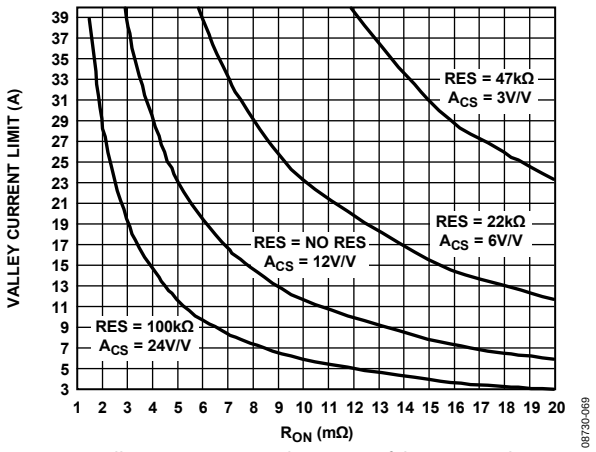

Figure 71. Valley Current-Limit Value vs. R_{ON} of the Lower-Side MOSFET for Each Programming Resistor (RES)

The valley current limit is programmed as outlined in Table 7 and Figure 71. The inductor chosen must be rated to handle the peak current, which is equal to the valley current from Table 7 plus the peak-to-peak inductor ripple current (see the Inductor Selection section). In addition, the peak current value must be used to compute the worst-case power dissipation in the MOSFETs (see Figure 72).

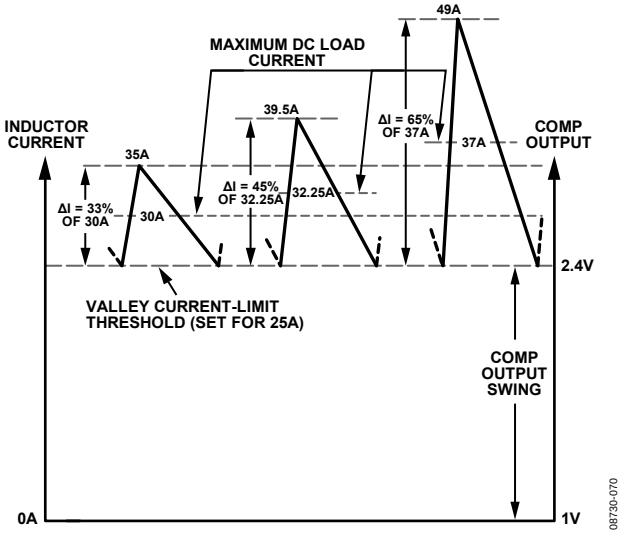

Figure 72. Valley Current-Limit Threshold in Relation to Inductor Ripple Current

HICCUP MODE DURING SHORT CIRCUIT

A current-limit violation occurs when the current across the source and drain of the lower-side MOSFET exceeds the current-limit setpoint. When 32 current-limit violations are detected, the controller enters idle mode and turns off the MOSFETs for 6 ms, allowing the converter to cool down. Then, the controller reestablishes soft start and begins to cause the output to ramp up again (see Figure 73). While the output ramps up, COMP is monitored to determine if the violation is still present. If it is still present, the idle event occurs again, followed by the full-chip power-down sequence. This cycle continues until the violation no longer exists. If the violation disappears, the converter is allowed to switch normally, maintaining regulation.

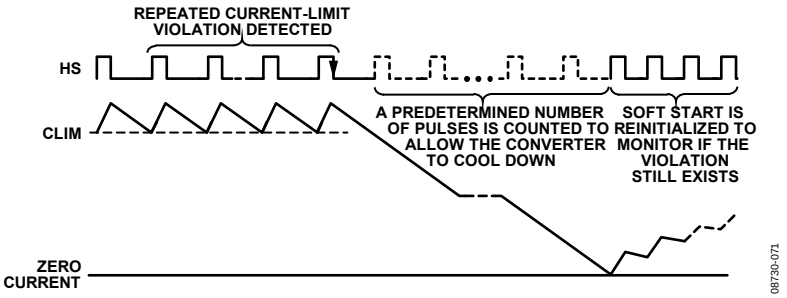

Figure 73. Idle Mode Entry Sequence Due to Current-Limit Violation

SYNCHRONOUS RECTIFIER

The ADP1870/ADP1871 employ an internal lower-side MOSFET driver to drive the external upper- and lower-side MOSFETs. The synchronous rectifier not only improves overall conduction efficiency, but also ensures proper charging to the bootstrap capacitor located at the upper-side driver input. This is beneficial during startup to provide sufficient drive signal to the external upper-side MOSFET and to attain fast turn-on response, which is essential for minimizing switching losses. The integrated upper- and lower-side MOSFET drivers operate in complementary fashion with built-in anticross conduction circuitry to prevent unwanted shoot-through current that may potentially damage the MOSFETs or reduce efficiency as a result of excessive power loss.

POWER SAVING MODE (PSM) VERSION (ADP1871)

The power saving mode version of the ADP1870 is the ADP1871. The ADP1871 operates in the discontinuous conduction mode (DCM) and pulse skips at light load to mid load currents. It outputs pulses as necessary to maintain output regulation. Unlike the continuous conduction mode (CCM), DCM operation prevents negative current, thus allowing improved system efficiency at light loads. Current in the reverse direction through this pathway, however, results in power dissipation and therefore a decrease in efficiency.

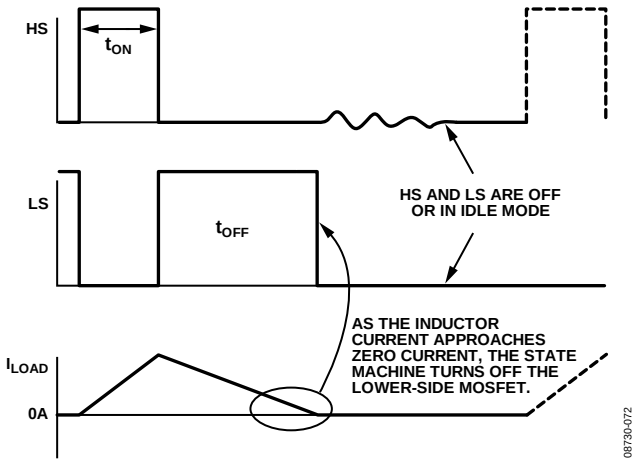

Figure 74. Discontinuous Mode of Operation (DCM)

To minimize the chance of negative inductor current buildup, an on-board zero-cross comparator turns off all upper- and lower-side switching activities when the inductor current approaches the zero current line, causing the system to enter idle mode, where the upper- and lower-side MOSFETs are turned off. To ensure idle mode entry, a 10 mV offset, connected in series at the SW node, is implemented (see Figure 75).

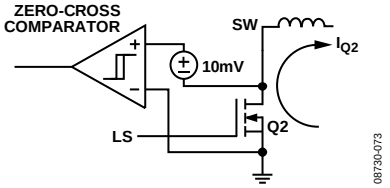

Figure 75. Zero-Cross Comparator with 10 mV of Offset

As soon as the forward current through the lower-side MOSFET decreases to a level where

$$10\ \text{mV} = I_{Q2} \times R_{ON(Q2)}$$

the zero-cross comparator (or I_{REV} comparator) emits a signal to turn off the lower-side MOSFET. From this point, the slope of the inductor current ramping down becomes steeper (see Figure 76) as the body diode of the lower-side MOSFET begins to conduct current and continues conducting current until the remaining energy stored in the inductor has been depleted.

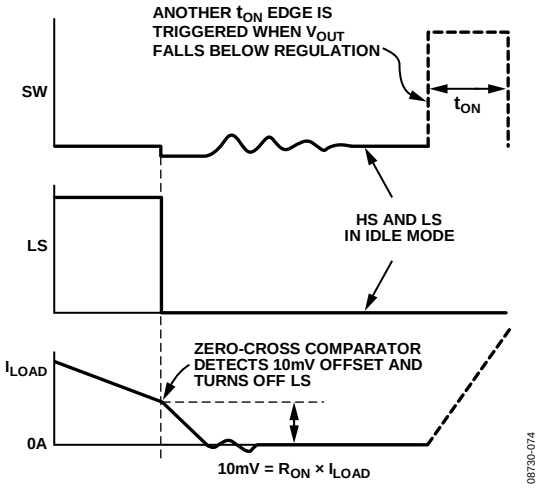

Figure 76. 10 mV Offset to Ensure Prevention of Negative Inductor Current

The system remains in idle mode until the output voltage drops below regulation. A PWM pulse is then produced, turning on the upper-side MOSFET to maintain system regulation. The ADP1871 does not have an internal clock, so it switches purely as a hysteretic controller as described in this section.

TIMER OPERATION

The ADP1870/ADP1871 employ a constant on-time architecture, which provides a variety of benefits, including improved load and line transient response when compared with a constant (fixed) frequency current-mode control loop of comparable loop design. The constant on-time timer, or t_{ON} timer, senses the high input voltage (V_{IN}) and the output voltage (V_{OUT}) using SW waveform information to produce an adjustable one-shot PWM pulse that varies the on-time of the upper-side MOSFET in response to dynamic changes in input voltage, output voltage, and load current conditions to maintain regulation. It then generates an on-time (t_{ON}) pulse that is inversely proportional to V_{IN}.

$$t_{ON} = K \times \frac{V_{OUT}}{V_{IN}}$$

where:

K is a constant that is trimmed using an RC timer product for the 300 kHz, 600 kHz, and 1.0 MHz frequency options.

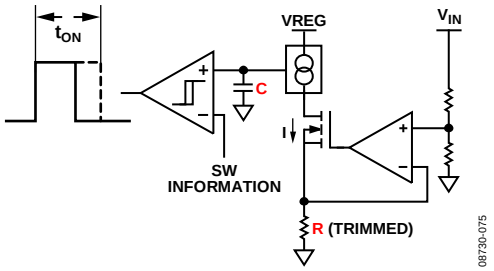

Figure 77. Constant On-Time Time

The constant on-time (t_{ON}) is not strictly "constant" because it varies with V_{IN} and V_{OUT}. However, this variation occurs in such a way as to keep the switching frequency virtually independent of V_{IN} and V_{OUT}.

The t_{ON} timer uses a feedforward technique, applied to the constant on-time control loop, making it a pseudo-fixed frequency to a first order. Second-order effects, such as dc losses in the external power MOSFETs (see the Efficiency Consideration section), cause some variation in frequency vs. load current and line voltage. These effects are shown in Figure 23 to Figure 34. The variations in frequency are much reduced compared with the variations generated when the feedforward technique is not utilized.

The feedforward technique establishes the following relationship:

$$f_{SW} = \frac{1}{K}$$

where f_{SW} is the controller switching frequency (300 kHz, 600 kHz, and 1.0 MHz).

The t_{ON} timer senses V_{IN} and V_{OUT} to minimize frequency variation as previously explained. This provides a pseudo-fixed frequency as explained in the Pseudo-Fixed Frequency section. To allow headroom for V_{IN} and V_{OUT} sensing, adhere to the following equations:

$$V_{REG} \geq V_{IN}/8 + 1.5$$

$$V_{REG} \geq V_{OUT}/4$$

For typical applications where V_{REG} is 5 V, these equations are not relevant; however, for lower V_{REG} inputs, care may be required.

PSEUDO-FIXED FREQUENCY

The ADP1870/ADP1871 employ a constant on-time control scheme. During steady state operation, the switching frequency stays relatively constant, or pseudo-fixed. This is due to the one-shot t_{ON} timer that produces a high-side PWM pulse with a "fixed" duration, given that external conditions such as input voltage, output voltage, and load current are also at steady state. During load transients, the frequency momentarily changes for the duration of the transient event so that the output comes back within regulation more quickly than if the frequency were fixed or if it were to remain unchanged. After the transient event is complete, the frequency returns to a pseudo-fixed frequency value to a first order.

To illustrate this feature more clearly, this section describes one such load transient event—a positive load step—in detail. During load transient events, the high-side driver output pulse width stays relatively consistent from cycle to cycle; however, the off-time (DRVL on-time) dynamically adjusts according to the instantaneous changes in the external conditions mentioned.

When a positive load step occurs, the error amplifier (out of phase of the output, V_{OUT}) produces new voltage information at its output (COMP). In addition, the current-sense amplifier senses new inductor current information during this positive load transient event. The error amplifier's output voltage reaction is compared with the new inductor current information that sets the start of the next switching cycle. Because current information is produced from valley current sensing, it is sensed at the down ramp of the inductor current, whereas the voltage loop information is sensed through the counter action upswing of the error amplifier's output (COMP).

The result is a convergence of these two signals (see Figure 78), which allows an instantaneous increase in switching frequency during the positive load transient event. In summary, a positive load step causes V_{OUT} to transient down, which causes COMP to transient up and therefore shortens the off-time. This resulting increase in frequency during a positive load transient helps to quickly bring V_{OUT} back up in value and within the regulation window.

Similarly, a negative load step causes the off-time to lengthen in response to V_{OUT} rising. This effectively increases the inductor demagnetizing phase, helping to bring V_{OUT} within regulation. In this case, the switching frequency decreases, or experiences a foldback, to help facilitate output voltage recovery.

Because the ADP1870/ADP1871 has the ability to respond rapidly to sudden changes in load demand, the recovery period in which the output voltage settles back to its original steady state operating point is much quicker than it would be for a fixed-frequency equivalent. Therefore, using a pseudo-fixed frequency results in significantly better load transient performance than using a fixed frequency.

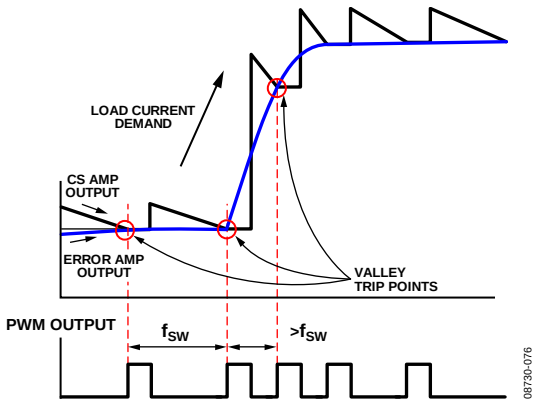

Figure 78. Load Transient Response Operation

APPLICATIONS INFORMATION

FEEDBACK RESISTOR DIVIDER

The required resistor divider network can be determined for a given V_{OUT} value because the internal band gap reference (V_{REF}) is fixed at 0.6 V. Selecting values for R_T and R_B determines the minimum output load current of the converter. Therefore, for a given value of R_B, the R_T value can be determined through the following expression:

$$R_T = R_B \times \frac{(V_{OUT} - 0.6\text{ V})}{0.6\text{ V}}$$

INDUCTOR SELECTION

The inductor value is inversely proportional to the inductor ripple current. The peak-to-peak ripple current is given by

$$\Delta I_L = K_I \times I_{LOAD} \approx \frac{I_{LOAD}}{3}$$

where K_I is typically 0.33.

The equation for the inductor value is given by

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

where:
V_{IN} is the high voltage input.
V_{OUT} is the desired output voltage.
f_{SW} is the controller switching frequency (300 kHz, 600 kHz, and 1.0 MHz).

When selecting the inductor, choose an inductor saturation rating that is above the peak current level, and then calculate the inductor current ripple (see the Valley Current-Limit Setting section and Figure 79).

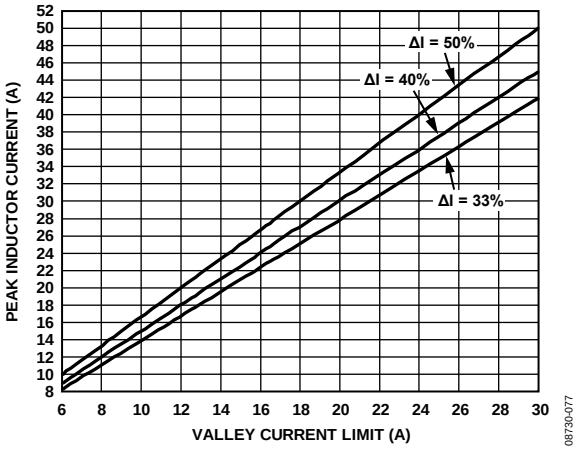

Figure 79. Peak Inductor Current vs. Valley Current Limit for 33%, 40%, and 50% of Inductor Ripple Current

Table 8. Recommended Inductors

L (µH)	DCR (mΩ)	I_{SAT} (A)	Dimensions (mm)	Manufacturer	Model Number
0.12	0.33	55	10.2 × 7	Würth Elek.	744303012
0.22	0.33	30	10.2 × 7	Würth Elek.	744303022
0.47	0.67	50	13.2 × 12.8	Würth Elek.	744355147
0.72	1.3	35	10.5 × 10.2	Würth Elek.	744325072
0.9	1.6	28	13 × 12.8	Würth Elek.	744355090
1.2	1.8	25	10.5 × 10.2	Würth Elek.	744325120
1.0	3.3	20	10.5 × 10.2	Würth Elek.	7443552100
1.4	3.2	24	14 × 12.8	Würth Elek.	744318180
2.0	2.6	22	13.2 × 12.8	Würth Elek.	7443551200
0.8	2.5	16.5	12.5 × 12.5	AIC Technology	CEP125U-R80

OUTPUT RIPPLE VOLTAGE (ΔV_{RR})

The output ripple voltage is the ac component of the dc output voltage during steady state. For a ripple error of 1.0%, the output capacitor value needed to achieve this tolerance can be determined using the following equation. (Note that an accuracy of 1.0% is possible only during steady state conditions, not during load transients.)

$$\Delta V_{RR} = (0.01) \times V_{OUT}$$

OUTPUT CAPACITOR SELECTION

The primary objective of the output capacitor is to facilitate the reduction of the output voltage ripple; however, the output capacitor also assists in the output voltage recovery during load transient events. For a given load current step, the output voltage ripple generated during this step event is inversely proportional to the value chosen for the output capacitor. The speed at which the output voltage settles during this recovery period depends on where the crossover frequency (loop bandwidth) is set. This crossover frequency is determined by the output capacitor, the equivalent series resistance (ESR) of the capacitor, and the compensation network.

To calculate the small-signal voltage ripple (output ripple voltage) at the steady state operating point, use the following equation:

$$C_{OUT} = \Delta I_L \times \left(\frac{1}{8 \times f_{SW} \times \left[\Delta V_{RIPPLE} - (\Delta I_L \times ESR) \right]} \right)$$

where *ESR* is the equivalent series resistance of the output capacitors.

To calculate the output load step, use the following equation:

$$C_{OUT} = 2 \times \frac{\Delta I_{LOAD}}{f_{SW} \times (\Delta V_{DROOP} - (\Delta I_{LOAD} \times ESR))}$$

where ΔV_{DROOP} is the amount that V_{OUT} is allowed to deviate for a given positive load current step (ΔI_{LOAD}).

Ceramic capacitors are known to have low ESR. However, the trade-off of using X5R technology is that up to 80% of its capacitance might be lost due to derating as the voltage applied across the capacitor is increased (see Figure 80). Although X7R series capacitors can also be used, the available selection is limited to only up to 22 µF.

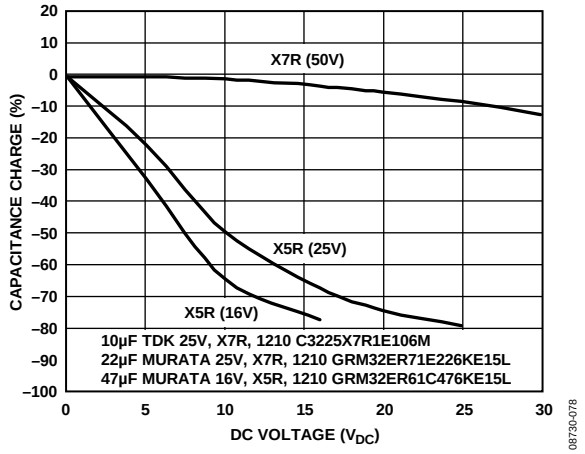

Figure 80. Capacitance vs. DC Voltage Characteristics for Ceramic Capacitors

Electrolytic capacitors satisfy the bulk capacitance requirements for most high current applications. Because the ESR of electrolytic capacitors is much higher than that of ceramic capacitors, when using electrolytic capacitors, several MLCCs should be mounted in parallel to reduce the overall series resistance.

COMPENSATION NETWORK

Due to their current-mode architecture, the ADP1870/ADP1871 require Type II compensation. To determine the component values needed for compensation (resistance and capacitance values), it is necessary to examine the converter's overall loop gain (H) at the unity gain frequency ($f_{SW}/10$) when H = 1 V/V:

$$H = 1\text{ V/V} = G_M \times G_{CS} \times \frac{V_{OUT}}{V_{REF}} \times Z_{COMP} \times Z_{FILT}$$

Examining each variable at high frequency enables the unity-gain transfer function to be simplified to provide expressions for the R_{COMP} and C_{COMP} component values.

Output Filter Impedance (Z_{FILT})

Examining the filter's transfer function at high frequencies simplifies to

$$Z_{FILTER} = \frac{1}{sC_{OUT}}$$

at the crossover frequency ($s = 2\pi f_{CROSS}$).

Error Amplifier Output Impedance (Z_{COMP})

Assuming that C_{C2} is significantly smaller than C_{COMP}, C_{C2} can be omitted from the output impedance equation of the error amplifier. The transfer function simplifies to

$$Z_{COMP} = \frac{R_{COMP}(f_{CROSS} + f_{ZERO})}{f_{CROSS}}$$

and

$$f_{CROSS} = \frac{1}{12} \times f_{SW}$$

where f_{ZERO}, the zero frequency, is set to be 1/4th of the crossover frequency for the ADP1870.

Error Amplifier Gain (G_M)

The error amplifier gain (transconductance) is

$$G_M = 500\ \mu\text{A/V}$$

Current-Sense Loop Gain (G_{CS})

The current-sense loop gain is

$$G_{CS} = \frac{1}{A_{CS} \times R_{ON}}\ \text{(A/V)}$$

where:
A_{CS} (V/V) is programmable for 3 V/V, 6 V/V, 12 V/V, and 24 V/V (see the Programming Resistor (RES) Detect Circuit and Valley Current-Limit Setting sections).
R_{ON} is the channel impedance of the lower-side MOSFET.

Crossover Frequency

The crossover frequency is the frequency at which the overall loop (system) gain is 0 dB (H = 1 V/V). For current-mode converters, such as the ADP1870, it is recommended that the user set the crossover frequency between 1/10th and 1/15th of the switching frequency.

$$f_{CROSS} = \frac{1}{12} f_{SW}$$

The relationship between C_{COMP} and f_{ZERO} (zero frequency) is as follows:

$$f_{ZERO} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}})$$

The zero frequency is set to 1/4th of the crossover frequency.

Combining all of the above parameters results in

$$R_{COMP} = \frac{f_{CROSS}}{f_{CROSS} + f_{ZERO}} \times \frac{2\pi f_{CROSS} C_{OUT}}{G_M G_{CS}} \times \frac{V_{OUT}}{V_{REF}}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{ZERO}}$$

EFFICIENCY CONSIDERATIONS

One of the important criteria to consider in constructing a dc-to-dc converter is efficiency. By definition, efficiency is the ratio of the output power to the input power. For high power applications at load currents up to 20 A, the following are important MOSFET parameters that aid in the selection process:

- $V_{GS(TH)}$: the MOSFET threshold voltage applied between the gate and the source
- $R_{DS(ON)}$: the MOSFET on resistance during channel conduction
- Q_G: the total gate charge
- C_{N1}: the input capacitance of the upper-side switch
- C_{N2}: the input capacitance of the lower-side switch

The following are the losses experienced through the external component during normal switching operation:

- Channel conduction loss (both of the MOSFETs)
- MOSFET driver loss
- MOSFET switching loss
- Body diode conduction loss (lower-side MOSFET)
- Inductor loss (copper and core loss)

Channel Conduction Loss

During normal operation, the bulk of the loss in efficiency is due to the power dissipated through MOSFET channel conduction. Power loss through the upper-side MOSFET is directly proportional to the duty cycle (D) for each switching period, and the power loss through the lower-side MOSFET is directly proportional to 1 − D for each switching period. The selection of MOSFETs is governed by the amount of maximum dc load current that the converter is expected to deliver. In particular, the selection of the lower-side MOSFET is dictated by the maximum load current because a typical high current application employs duty cycles of less than 50%. Therefore, the lower-side MOSFET is in the on state for most of the switching period.

$$P_{N1,N2(CL)} = \left[D \times R_{N1(ON)} + (1-D) \times R_{N2(ON)}\right] \times I_{LOAD}^2$$

MOSFET Driver Loss

Other dissipative elements are the MOSFET drivers. The contributing factors are the dc current flowing through the driver during operation and the Q_{GATE} parameter of the external MOSFETs.

$$P_{DR(LOSS)} = \left[V_{DR} \times \left(f_{SW} C_{upperFET} V_{DR} + I_{BIAS}\right)\right] + \left[V_{REG} \times \left(f_{SW} C_{lowerFET} V_{REG} + I_{BIAS}\right)\right]$$

where:
$C_{upperFET}$ is the input gate capacitance of the upper-side MOSFET.
$C_{lowerFET}$ is the input gate capacitance of the lower-side MOSFET.
I_{BIAS} is the dc current flowing into the upper- and lower-side drivers.
V_{DR} is the driver bias voltage (that is, the low input voltage (V_{REG}) minus the rectifier drop (see Figure 81)).
V_{REG} is the bias voltage.
f_{SW} is the controller switching frequency (300 kHz, 600 kHz, and 1.0 MHz)

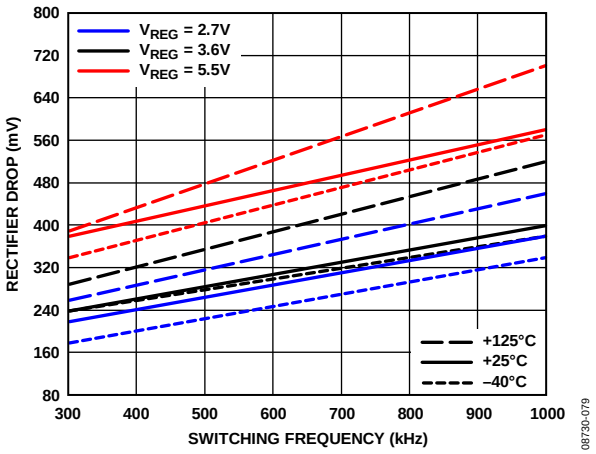

Figure 81. Internal Rectifier Voltage Drop vs. Switching Frequency

Switching Loss

The SW node transitions due to the switching activities of the upper- and lower-side MOSFETs. This causes removal and replenishing of charge to and from the gate oxide layer of the MOSFET, as well as to and from the parasitic capacitance associated with the gate oxide edge overlap and the drain and source terminals. The current that enters and exits these charge paths presents additional loss during these transition times. This loss can be approximately quantified by using the following equation, which represents the time in which charge enters and exits these capacitive regions:

$$t_{SW\text{-}TRANS} = R_{GATE} \times C_{TOTAL}$$

where:
C_{TOTAL} is the C_{GD} + C_{GS} of the external MOSFET.
R_{GATE} is the gate input resistance of the external MOSFET.

The ratio of this time constant to the period of one switching cycle is the multiplying factor to be used in the following expression:

$$P_{SW(LOSS)} = \frac{t_{SW\text{-}TRANS}}{t_{SW}} \times I_{LOAD} \times V_{IN} \times 2$$

or

$$P_{SW(LOSS)} = f_{SW} \times R_{GATE} \times C_{TOTAL} \times I_{LOAD} \times V_{IN} \times 2$$

Diode Conduction Loss

The ADP1870/ADP1871 employ anticross conduction circuitry that prevents the upper- and lower-side MOSFETs from conducting current simultaneously. This overlap control is beneficial, avoiding large current flow that may lead to irreparable damage to the external components of the power stage. However, this blanking period comes with the trade-off of a diode conduction loss occurring immediately after the MOSFETs change states and continuing well into idle mode. The amount of loss through the body diode of the lower-side MOSFET during the antioverlap state is given by the following expression:

$$P_{BODY(LOSS)} = \frac{t_{BODY(LOSS)}}{t_{SW}} \times I_{LOAD} \times V_F \times 2$$

where:
$t_{BODY(LOSS)}$ is the body conduction time (refer to Figure 82 for dead time periods).
t_{SW} is the period per switching cycle.
V_F is the forward drop of the body diode during conduction. (Refer to the selected external MOSFET data sheet for more information about the V_F parameter.)

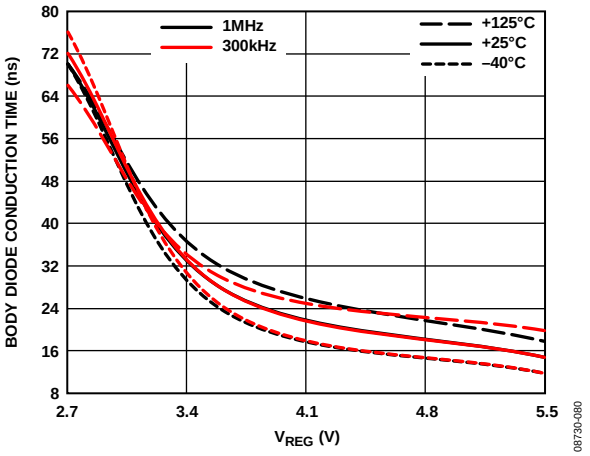

Figure 82. Body Diode Conduction Time vs. Low Voltage Input (V_{REG})

Inductor Loss

During normal conduction mode, further power loss is caused by the conduction of current through the inductor windings, which have dc resistance (DCR). Typically, larger sized inductors have smaller DCR values.

The inductor core loss is a result of the eddy currents generated within the core material. These eddy currents are induced by the changing flux, which is produced by the current flowing through the windings. The amount of inductor core loss depends on the core material, the flux swing, the frequency, and the core volume. Ferrite inductors have the lowest core losses, whereas powdered iron inductors have higher core losses. It is recommended that shielded ferrite core material type inductors be used with the ADP1870/ADP1871 for a high current, dc-to-dc switching application to achieve minimal loss and negligible electromagnetic interference (EMI).

$$P_{DCR(LOSS)} = DCR \times I^2_{LOAD} + Core\ Loss$$

INPUT CAPACITOR SELECTION

The goal in selecting an input capacitor is to reduce or minimize input voltage ripple and to reduce the high frequency source impedance, which is essential for achieving predictable loop stability and transient performance.

The problem with using bulk capacitors, other than their physical geometries, is their large equivalent series resistance (ESR) and large equivalent series inductance (ESL). Aluminum electrolytic capacitors have such high ESR that they cause undesired input voltage ripple magnitudes and are generally not effective at high switching frequencies.

If bulk capacitors are to be used, it is recommended that muli-layered ceramic capacitors (MLCC) be used in parallel due to their low ESR values. This dramatically reduces the input voltage ripple amplitude as long as the MLCCs are mounted directly across the drain of the upper-side MOSFET and the source terminal of the lower-side MOSFET (see the Layout Considerations section). Improper placement and mounting of these MLCCs may cancel their effectiveness due to stray inductance and an increase in trace impedance.

$$I_{CIN,rms} = I_{LOAD,max} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{OUT}}$$

The maximum input voltage ripple and maximum input capacitor rms current occur at the end of the duration of 1 − D while the upper-side MOSFET is in the off state. The input capacitor rms current reaches its maximum at Time D. When calculating the maximum input voltage ripple, account for the ESR of the input capacitor as follows:

$$V_{RIPPLE,max} = V_{RIPP} + (I_{LOAD,max} \times ESR)$$

where:
V_{RIPP} is usually 1% of the minimum voltage input.
$I_{LOAD,max}$ is the maximum load current.
ESR is the equivalent series resistance rating of the input capacitor.

Inserting $V_{RIPPLE,max}$ into the charge balance equation to calculate the minimum input capacitor requirement gives

$$C_{IN,min} = \frac{I_{LOAD,max}}{V_{RIPPLE,max}} \times \frac{D(1-D)}{f_{SW}}$$

or

$$C_{IN,min} = \frac{I_{LOAD,max}}{4 f_{SW} V_{RIPPLE,max}}$$

where D = 50%.

THERMAL CONSIDERATIONS

The ADP1870/ADP1871 are used for dc-to-dc, step down, high current applications that have an on-board controller, an on-board LDO, and on-board MOSFET drivers. Because applications may require up to 20 A of load current delivery and be subjected to high ambient temperature surroundings, the selection of external upper- and lower-side MOSFETs must be associated with careful thermal consideration to not exceed the maximum allowable junction temperature of 125°C. To avoid permanent or irreparable damage if the junction temperature reaches or exceeds 155°C, the part enters thermal shutdown, turning off both external MOSFETs, and does not reenable until the junction temperature cools to 140°C (see the On-Board Low Dropout Regulator section).

In addition, it is important to consider the thermal impedance of the package. Because the ADP1870/ADP1871 employ an on-board LDO, the ac current (fxCxV) consumed by the internal drivers to drive the external MOSFETs adds another element of power dissipation across the internal LDO. Equation 3 shows the power dissipation calculations for the integrated drivers and for the internal LDO.

Table 9 lists the thermal impedance for the ADP1870/ADP1871, which are available in both 10-lead MSOP and 10-lead LFCSP packages.

Table 9. Thermal Impedance for 10-lead MSOP

Parameter	Thermal Impedance
10-Lead MSOP θ_{JA}	
2-Layer Board	213.1°C/W
4-Layer Board	171.7°C/W
10-Lead LFCSP θ_{JA}	
4-Layer Board	40°C/W

Figure 83 specifies the maximum allowable ambient temperature that can surround the ADP1870/ADP1871 IC for a specified high input voltage (V_{IN}). Figure 83 illustrates the temperature derating conditions for each available switching frequency for low, typical, and high output setpoints for both the 10-lead MSOP and LFCSP packages. All temperature derating criteria are based on a maximum IC junction temperature of 125°C.

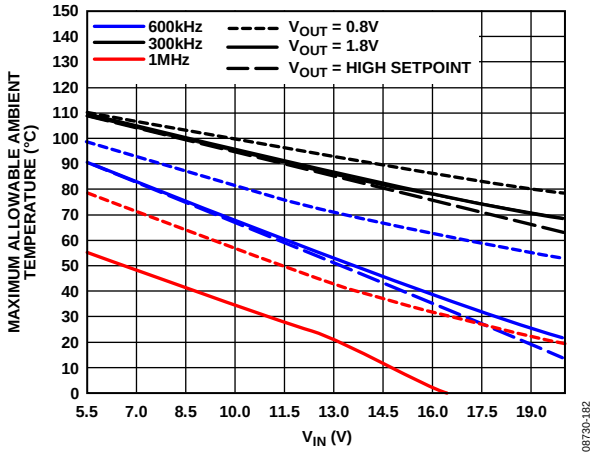

Figure 83. Ambient Temperature vs. V_{IN} for 10-Lead MSOP (171°C/W), 4-Layer EVB, CIN = 4.3 nF (Upper-/Lower-Side MOSFET)

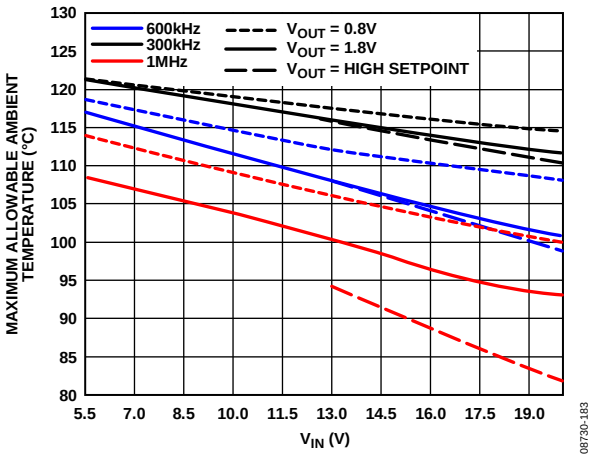

Figure 84. Ambient Temperature vs. V_{IN} for 10-Lead LFCSP (40°C/W), 4-Layer EVB, CIN = 4.3 nF (Upper-/Lower-Side MOSFET)

The maximum junction temperature allowed for the ADP1870/ADP1871 ICs is 125°C. This means that the sum of the ambient temperature (T_A) and the rise in package temperature (T_R), which is caused by the thermal impedance of the package and the internal power dissipation, should not exceed 125°C, as dictated by the following expression:

$$T_J = T_R \times T_A \quad (1)$$

where:
T_A is the ambient temperature.
T_J is the maximum junction temperature.
T_R is the rise in package temperature due to the power dissipated from within.

The rise in package temperature is directly proportional to its thermal impedance characteristics. The following equation represents this proportionality relationship:

$$T_R = \theta_{JA} \times P_{DR(LOSS)} \quad (2)$$

where:
θ_{JA} is the thermal resistance of the package from the junction to the outside surface of the die, where it meets the surrounding air.
$P_{DR(LOSS)}$ is the overall power dissipated by the IC.

The bulk of the power dissipated is due to the gate capacitance of the external MOSFETs and current running through the on-board LDO. The power loss equations for the MOSFET drivers and internal low dropout regulator (see the MOSFET Driver Loss section in the Efficiency Consideration section) are:

$$P_{DR(LOSS)} = [V_{DR} \times (f_{SW}C_{upperFET}V_{DR} + I_{BIAS})] + [V_{REG} \times (f_{SW}C_{lowerFET}\ V_{REG} + I_{BIAS})] \quad (3)$$

where:
$C_{upperFET}$ is the input gate capacitance of the upper-side MOSFET.
$C_{lowerFET}$ is the input gate capacitance of the lower-side MOSFET.
I_{BIAS} is the dc current (2 mA) flowing into the upper- and lower-side drivers.
V_{DR} is the driver bias voltage (the low input voltage (V_{REG}) minus the rectifier drop (see Figure 81)).
V_{REG} is the LDO output/bias voltage.

$$P_{DISS(LDO)} = P_{DR(LOSS)} + (V_{IN} - V_{REG}) \times (f_{SW} \times C_{total} \times V_{REG} + I_{BIAS}) \quad (4)$$

where:
$P_{DISS(LDO)}$ is the power dissipated through the pass device in the LDO block across VIN and VREG.
C_{total} is the C_{GD} + C_{GS} of the external MOSFET.
V_{REG} is the LDO output voltage and bias voltage.
V_{IN} is the high voltage input.
I_{BIAS} is the dc input bias current.
$P_{DR(LOSS)}$ is the MOSFET driver loss.

For example, if the external MOSFET characteristics are θ_{JA} (10-lead MSOP) = 171.2°C/W, f_{SW} = 300 kHz, I_{BIAS} = 2 mA, $C_{upperFET}$ = 3.3 nF, $C_{lowerFET}$ = 3.3 nF, V_{DR} = 4.62 V, and V_{REG} = 5.0 V, then the power loss is

$$\begin{aligned} P_{DR(LOSS)} &= \left[V_{DR} \times \left(f_{SW} C_{upperFET} V_{DR} + I_{BIAS}\right)\right] \\ &+ \left[V_{REG} \times \left(f_{SW} C_{lowerFET} V_{REG} + I_{BIAS}\right)\right] \\ &= (4.62 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 4.62 + 0.002)) \\ &+ (5.0 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.0 + 0.002)) \\ &= 57.12 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{DISS(LDO)} &= (V_{IN} - V_{REG}) \times (f_{SW} \times C_{total} \times V_{REG} + I_{BIAS}) \\ &= (13 \text{ V} - 5 \text{ V}) \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5 + 0.002) \\ &= 55.6 \text{ mW} \end{aligned}$$

$$\begin{aligned} P_{DISS(TOTAL)} &= P_{DISS(LDO)} + P_{DR(LOSS)} \\ &= 77.13 \text{ mW} + 55.6 \text{ mW} \\ &= 132.73 \text{ mW} \end{aligned}$$

The rise in package temperature (for 10-lead MSOP) is

$$\begin{aligned} T_R &= \theta_{JA} \times P_{DR(LOSS)} \\ &= 171.2°\text{C} \times 132.05 \text{ mW} \\ &= 22.7°\text{C} \end{aligned}$$

Assuming a maximum ambient temperature environment of 85°C,

$$T_J = T_R \times T_A = 22.7°\text{C} + 85°\text{C} = 107.72°\text{C}$$

which is below the maximum junction temperature of 125°C.

DESIGN EXAMPLE

The ADP1870/ADP1871 are easy to use, requiring only a few design criteria. For example, the example outlined in this section uses only four design criteria: V_{OUT} = 1.8 V, I_{LOAD} = 15 A (pulsing), V_{IN} = 12 V (typical), and f_{SW} = 300 kHz.

Input Capacitor

The maximum input voltage ripple is usually 1% of the minimum input voltage (11.8 V × 0.01 = 120 mV).

$$V_{RIPP} = 120 \text{ mV}$$

$$\begin{aligned} V_{MAX,RIPPLE} &= V_{RIPP} - (I_{LOAD,MAX} \times ESR) \\ &= 120 \text{ mV} - (15 \text{ A} \times 0.001) = 45 \text{ mV} \end{aligned}$$

$$\begin{aligned} C_{IN,min} &= \frac{I_{LOAD,MAX}}{4 f_{SW} V_{MAX,RIPPLE}} = \frac{15 \text{ A}}{4 \times 300 \times 10^3 \times 105 \text{ mV}} \\ &= 120 \text{ µF} \end{aligned}$$

Choose five 22 µF ceramic capacitors. The overall ESR of five 22 µF ceramic capacitors is less than 1 mΩ.

$$I_{RMS} = I_{LOAD}/2 = 7.5 \text{ A}$$

$$P_{CIN} = (I_{RMS})^2 \times ESR = (7.5 \text{ A})^2 \times 1 \text{ mΩ} = 56.25 \text{ mW}$$

Inductor

Determine inductor ripple current amplitude as follows:

$$\Delta I_L \approx \frac{I_{LOAD}}{3} = 5 \text{ A}$$

so calculating for the inductor value

$$\begin{aligned} L &= \frac{(V_{IN,MAX} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN,MAX}} \\ &= \frac{(13.2 \text{ V} - 1.8 \text{ V})}{5 \text{ V} \times 300 \times 10^3} \times \frac{1.8 \text{ V}}{13.2 \text{ V}} \\ &= 1.03 \text{ µH} \end{aligned}$$

The inductor peak current is approximately

$$15 \text{ A} + (5 \text{ A} \times 0.5) = 17.5 \text{ A}$$

Therefore, an appropriate inductor selection is 1.0 µH with DCR = 3.3 mΩ (Würth Elektronik 7443552100) from Table 8 with peak current handling of 20 A.

$$\begin{aligned} P_{DCR(LOSS)} &= DCR \times I_L^2 \\ &= 0.003 \times (15 \text{ A})^2 = 675 \text{ mW} \end{aligned}$$

Current Limit Programming

The valley current is approximately

$$15 \text{ A} - (5 \text{ A} \times 0.5) = 12.5 \text{ A}$$

Assuming a lower-side MOSFET R_{ON} of 4.5 mΩ and 13 A as the valley current limit from Table 7 and Figure 71 indicates, a programming resistor (RES) of 100 kΩ corresponds to an A_{CS} of 24 V/V.

Choose a programmable resistor of R_{RES} = 100 kΩ for a current-sense gain of 24 V/V.

Output Capacitor

Assume that a load step of 15 A occurs at the output and no more than 5% is allowed for the output to deviate from the steady state operating point. In this case, the ADP1870's advantage is that because the frequency is pseudo-fixed, the converter is able to respond quickly because of the immediate, though temporary, increase in switching frequency.

$$\Delta V_{DROOP} = 0.05 \times 1.8 \text{ V} = 90 \text{ mV}$$

Assuming that the overall ESR of the output capacitor ranges from 5 mΩ to 10 mΩ,

$$\begin{aligned} C_{OUT} &= 2 \times \frac{\Delta I_{LOAD}}{f_{SW} \times (\Delta V_{DROOP})} \\ &= 2 \times \frac{15 \text{ A}}{300 \times 10^3 \times (90 \text{ mV})} \\ &= 1.11 \text{ mF} \end{aligned}$$

Therefore, an appropriate inductor selection is five 270 µF polymer capacitors with a combined ESR of 3.5 mΩ.

Assuming an overshoot of 45 mV, determine if the output capacitor that was calculated previously is adequate:

$$C_{OUT} = \frac{(L \times I^2_{LOAD})}{\left((V_{OUT} - \Delta V_{OVSHT})^2 - (V_{OUT})^2\right)}$$
$$= \frac{1 \times 10^{-6} \times (15\text{ A})^2}{(1.8 - 45\text{ mV})^2 - (1.8)^2}$$
$$= 1.4\text{ mF}$$

Choose five 270 µF polymer capacitors.

The rms current through the output capacitor is

$$I_{RMS} = \frac{1}{2} \times \frac{1}{\sqrt{3}} \frac{(V_{IN,MAX} - V_{OUT})}{L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN,MAX}}$$
$$= \frac{1}{2} \times \frac{1}{\sqrt{3}} \frac{(13.2\text{ V} - 1.8\text{ V})}{1\text{ µF} \times 300 \times 10^3} \times \frac{1.8\text{ V}}{13.2\text{ V}} = 1.49\text{ A}$$

The power loss dissipated through the ESR of the output capacitor is

$$P_{COUT} = (I_{RMS})^2 \times ESR = (1.5\text{ A})^2 \times 1.4\text{ mΩ} = 3.15\text{ mW}$$

Feedback Resistor Network Setup

It is recommended to use R_B = 15 kΩ. Calculate R_T as follows:

$$R_T = 15\text{ kΩ} \times \frac{(1.8\text{ V} - 0.6\text{ V})}{0.6\text{ V}} = 30\text{ kΩ}$$

Compensation Network

To calculate R_{COMP}, C_{COMP}, and C_{PAR}, the transconductance parameter and the current-sense gain variable are required. The transconductance parameter (G_M) is 500 µA/V, and the current-sense loop gain is

$$G_{CS} = \frac{1}{A_{CS} R_{ON}} = \frac{1}{24 \times 0.005} = 8.33\text{ A/V}$$

where A_{CS} and R_{ON} are taken from setting up the current limit (see the Programming Resistor (RES) Detect Circuit and Valley Current-Limit Setting sections).

The crossover frequency is 1/12th of the switching frequency:

300 kHz/12 = 25 kHz

The zero frequency is 1/4th of the crossover frequency:

25 kHz/4 = 6.25 kHz

$$R_{COMP} = \frac{f_{CROSS}}{f_{CROSS} + f_{ZERO}} \times \frac{2\pi f_{CROSS} C_{OUT}}{G_M G_{CS}} \times \frac{V_{OUT}}{V_{REF}}$$
$$= \frac{25 \times 10^3}{25 \times 10^3 + 6.25 \times 10^3} \times \frac{2 \times 3.141 \times 25 \times 10^3 \times 1.11 \times 10^{-3}}{500 \times 10^{-6} \times 8.3} \times \frac{1.8}{0.6}$$
$$= 100\text{ kΩ}$$

$$C_{COMP} = \frac{1}{2\pi R_{COMP} f_{ZERO}}$$
$$= \frac{1}{2 \times 3.14 \times 100 \times 10^3 \times 6.25 \times 10^3}$$
$$= 250\text{ pF}$$

Loss Calculations

Duty cycle = 1.8/12 V = 0.15

$R_{ON\,(N2)}$ = 5.4 mΩ

$t_{BODY(LOSS)}$ = 20 ns (body conduction time)

V_F = 0.84 V (MOSFET forward voltage)

C_{IN} = 3.3 nF (MOSFET gate input capacitance)

$Q_{N1,N2}$ = 17 nC (total MOSFET gate charge)

R_{GATE} = 1.5 Ω (MOSFET gate input resistance)

$$P_{N1,N2(CL)} = \left[D \times R_{N1(ON)} + (1 - D) \times R_{N2(ON)}\right] \times I^2_{LOAD}$$
$$= (0.15 \times 0.0054 + 0.85 \times 0.0054) \times (15\text{ A})^2$$
$$= 1.215\text{ W}$$

$$P_{BODY(LOSS)} = \frac{t_{BODY(LOSS)}}{t_{SW}} \times I_{LOAD} \times V_F \times 2$$
$$= 20\text{ ns} \times 300 \times 10^3 \times 15\text{ A} \times 0.84 \times 2$$
$$= 151.2\text{ mW}$$

$$P_{SW(LOSS)} = f_{SW} \times R_{GATE} \times C_{TOTAL} \times I_{LOAD} \times V_{IN} \times 2$$
$$= 300 \times 10^3 \times 1.5\text{ Ω} \times 3.3 \times 10^{-9} \times 15\text{ A} \times 12 \times 2$$
$$= 534.6\text{ mW}$$

$$P_{DR(LOSS)} = \left[V_{DR} \times \left(f_{SW} C_{upperFET} V_{DR} + I_{BIAS}\right)\right]$$
$$+ \left[V_{REG} \times \left(f_{SW} C_{lowerFET} V_{REG} + I_{BIAS}\right)\right]$$
$$= (4.62 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 4.62 + 0.002))$$
$$+ (5.0 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.0 + 0.002))$$
$$= 57.12\text{ mW}$$

$$P_{DISS(LDO)} = (V_{IN} - V_{REG}) \times (f_{SW} \times C_{total} \times V_{REG} + I_{BIAS})$$
$$= (13\text{ V} - 5\text{ V}) \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5 + 0.002)$$
$$= 55.6\text{ mW}$$

$P_{COUT} = (I_{RMS})^2 \times ESR = (1.5\text{ A})^2 \times 1.4\text{ mΩ} = 3.15\text{ mW}$

$P_{DCR(LOSS)} = DCR \times I^2_{LOAD} = 0.003 \times (15\text{ A})^2 = 675\text{ mW}$

$P_{CIN} = (I_{RMS})^2 \times ESR = (7.5\text{ A})^2 \times 1\text{ mΩ} = 56.25\text{ mW}$

$P_{LOSS} = P_{N1,N2} + P_{BODY(LOSS)} + P_{SW} + P_{DCR} + P_{DR} + P_{DISS(LDO)} + P_{COUT} + P_{CIN}$
$= 1.215\text{ W} + 151.2\text{ mW} + 534.6\text{ mW} + 57.12\text{ mW} + 55.6 + 3.15\text{ mW} + 675\text{ mW} + 56.25\text{ mW}$
$= 2.655\text{ W}$

EXTERNAL COMPONENT RECOMMENDATIONS

The configurations listed in Table 10 are with f_{CROSS} = 1/12 × f_{SW}, f_{ZERO} = ¼ × f_{CROSS}, R_{RES} = 100 kΩ, R_{BOT} = 15 kΩ, R_{ON} = 5.4 mΩ (BSC042N03MS G), V_{REG} = 5 V (float), and a maximum load current of 14 A.

The ADP1871 models listed in Table 10 are the PSM versions of the device.

Table 10. External Component Values

SAP Model	Marking Code		V_{OUT} (V)	V_{IN} (V)	C_{IN} (µF)	C_{OUT} (µF)	L[1] (µH)	R_C (kΩ)	C_{COMP} (pF)	C_{PAR} (pF)	R_{TOP} (kΩ)
	ADP1870	ADP1871									
ADP1870ARMZ-0.3-R7/ ADP1871ARMZ-0.3-R7	LDW	LDG	0.8	13	5 × 22[2]	5 × 560[3]	0.72	47	740	74	5.0
	LDW	LDG	1.2	13	5 × 22[2]	4 × 560[3]	1.0	47	740	74	15.0
	LDW	LDG	1.8	13	4 × 22[2]	4 × 270[4]	1.0	47	571	57	30.0
	LDW	LDG	2.5	13	4 × 22[2]	3 × 270[4]	1.53	47	571	57	47.5
	LDW	LDG	3.3	13	5 × 22[2]	2 × 330[5]	2.0	47	571	57	67.5
	LDW	LDG	5	13	4 × 22[2]	330[5]	3.27	34	800	80	110.0
	LDW	LDG	7	13	4 × 22[2]	22[2] + (4 × 47[6])	3.44	34	800	80	160.0
	LDW	LDG	1.2	16.5	4 × 22[2]	4 × 560[3]	1.0	47	740	74	15.0
	LDW	LDG	1.8	16.5	3 × 22[2]	4 × 270[4]	1.0	47	592	59	30.0
	LDW	LDG	2.5	16.5	3 × 22[2]	4 × 270[4]	1.67	47	592	59	47.5
	LDW	LDG	3.3	16.5	3 × 22[2]	2 × 330[5]	2.00	47	592	59	67.5
	LDW	LDG	5	16.5	3 × 22[2]	2 × 150[7]	3.84	34	829	83	110.0
	LDW	LDG	7	16.5	3 × 22[2]	22[2] + 4 × 47[6]	4.44	34	829	83	160.0
ADP1870ARMZ-0.6-R7/ ADP1871ARMZ-0.6-R7	LDX	LDM	0.8	5.5	5 × 22[2]	4 × 560[3]	0.22	47	339	34	5.0
	LDX	LDM	1.2	5.5	5 × 22[2]	4 × 270[4]	0.47	47	326	33	15.0
	LDX	LDM	1.8	5.5	5 × 22[2]	3 × 270[4]	0.47	47	271	27	30.0
	LDX	LDM	2.5	5.5	5 × 22[2]	3 × 180[8]	0.47	47	271	27	47.5
	LDX	LDM	1.2	13	3 × 22[2]	5 × 270[4]	0.47	47	407	41	15.0
	LDX	LDM	1.8	13	5 × 10[9]	3 × 330[5]	0.47	47	307	31	30.0
	LDX	LDM	2.5	13	5 × 10[9]	3 × 270[4]	0.90	47	307	31	47.5
	LDX	LDM	3.3	13	5 × 10[9]	2 × 270[4]	1.00	47	307	31	67.5
	LDX	LDM	5	13	5 × 10[9]	150[7]	1.76	34	430	43	110.0
	LDX	LDM	1.2	16.5	3 × 10[9]	4 × 270[4]	0.47	47	362	36	15.0
	LDX	LDM	1.8	16.5	4 × 10[9]	2 × 330[5]	0.72	47	326	33	30.0
	LDX	LDM	2.5	16.5	4 × 10[9]	3 × 270[4]	0.90	47	326	33	47.5
	LDX	LDM	3.3	16.5	4 × 10[9]	330[5]	1.0	47	296	30	67.5
	LDX	LDM	5	16.5	4 × 10[9]	4 × 47[6]	2.0	34	415	41	110.0
	LDX	LDM	7	16.5	4 × 10[9]	3 × 47[6]	2.0	34	380	38	160.0
ADP1870ARMZ-1.0-R7/ ADP1871ARMZ-1.0-R7	LDY	LDN	0.8	5.5	5 × 22[2]	4 × 270[4]	0.22	47	223	22	5.0
	LDY	LDN	1.2	5.5	5 × 22[2]	2 × 330[5]	0.22	47	223	22	15.0
	LDY	LDN	1.8	5.5	3 × 22[2]	3 × 180[8]	0.22	47	163	16	30.0
	LDY	LDN	2.5	5.5	3 × 22[2]	270[4]	0.22	47	163	16	47.5
	LDY	LDN	1.2	13	3 × 10[9]	3 × 330[5]	0.22	47	233	23	15.0
	LDY	LDN	1.8	13	4 × 10[9]	3 × 270[4]	0.47	47	210	21	30.0
	LDY	LDN	2.5	13	4 × 10[9]	270[4]	0.47	47	210	21	47.5
	LDY	LDN	3.3	13	5 × 10[9]	270[4]	0.72	47	210	21	67.5
	LDY	LDN	5	13	4 × 10[9]	3 × 47[6]	1.0	34	268	27	110.0
	LDY	LDN	1.2	16.5	3 × 10[9]	4 × 270[4]	0.47	47	326	33	15.0
	LDY	LDN	1.8	16.5	3 × 10[9]	3 × 270[4]	0.47	47	261	26	30.0
	LDY	LDN	2.5	16.5	4 × 10[9]	3 × 180[8]	0.72	47	233	23	47.5
	LDY	LDN	3.3	16.5	4 × 10[9]	270[4]	0.72	47	217	22	67.5

SAP Model	Marking Code		V_{OUT} (V)	V_{IN} (V)	C_{IN} (µF)	C_{OUT} (µF)	L[1] (µH)	R_C (kΩ)	C_{COMP} (pF)	C_{PAR} (pF)	R_{TOP} (kΩ)
	ADP1870	ADP1871									
	LDY	LDN	5	16.5	3 × 10[9]	3 × 47[6]	1.0	34	268	27	110.0
	LDY	LDN	7	16.5	3 × 10[9]	22[2] + 47[6]	1.0	34	228	23	160.0

[1] See the Inductor Selection section and Table 11.
[2] 22 µF Murata 25 V, X7R, 1210 GRM32ER71E226KE15L (3.2 mm × 2.5 mm × 2.5 mm).
[3] 560 µF Panasonic (SP-series) 2 V, 7 mΩ, 3.7 A EEFUE0D561LR (4.3 mm × 7.3 mm × 4.2 mm).
[4] 270 µF Panasonic (SP-series) 4 V, 7 mΩ, 3.7 A EEFUE0G271LR (4.3 mm × 7.3 mm × 4.2 mm).
[5] 330 µF Panasonic (SP-series) 4 V, 12 mΩ, 3.3 A EEFUE0G331R (4.3 mm × 7.3 mm × 4.2 mm).
[6] 47 µF Murata 16 V, X5R, 1210 GRM32ER61C476KE15L (3.2 mm × 2.5 mm × 2.5 mm).
[7] 150 µF Panasonic (SP-series) 6.3 V, 10 mΩ, 3.5 A EEFUE0J151XR (4.3 mm × 7.3 mm × 4.2 mm).
[8] 180 µF Panasonic (SP-series) 4 V, 10 mΩ, 3.5 A EEFUE0G181XR (4.3 mm × 7.3 mm × 4.2 mm).
[9] 10 µF TDK 25 V, X7R, 1210 C3225X7R1E106M.

Table 11. Recommended Inductors

L (µH)	DCR (mΩ)	I_{SAT} (A)	Dimension (mm)	Manufacturer	Model Number
0.12	0.33	55	10.2 × 7	Würth Elektronik	744303012
0.22	0.33	30	10.2 × 7	Würth Elektronik	744303022
0.47	0.67	50	13.2 × 12.8	Würth Elektronik	744355147
0.72	1.3	35	10.5 × 10.2	Würth Elektronik	744325072
0.9	1.6	28	13 × 12.8	Würth Elektronik	744355090
1.2	1.8	25	10.5 × 10.2	Würth Elektronik	744325120
1.0	3.3	20	10.5 × 10.2	Würth Elektronik	7443552100
1.4	3.2	24	14 × 12.8	Würth Elektronik	744318180
2.0	2.6	22	13.2 × 10.8	Würth Elektronik	7443551200
0.8	2.5	16.5	12.5 × 12.5	AIC Technology	CEP125U-R80

Table 12. Recommended MOSFETs

V_{GS} = 4.5 V	R_{ON} (mΩ)	I_D (A)	V_{DS} (V)	C_{IN} (nF)	Q_{TOTAL} (nC)	Package	Manufacturer	Model Number
Upper-Side MOSFET (Q1/Q2)	5.4	47	30	3.2	20	PG-TDSON8	Infineon	BSC042N03MS G
	10.2	53	30	1.6	10	PG-TDSON8	Infineon	BSC080N03MS G
	6.0	19	30		35	SO-8	Vishay	Si4842DY
	9	14	30	2.4	25	SO-8	International Rectifier	IRF7811
Lower-Side MOSFET (Q3/Q4)	5.4	47	30	3.2	20	PG-TDSON8	Infineon	BSC042N03MS G
	10.2	82	30	1.6	10	PG-TDSON8	Infineon	BSC080N03MS G
	6.0	19	30		35	SO-8	Vishay	Si4842DY

LAYOUT CONSIDERATIONS

The performance of a dc-to-dc converter depends highly on how the voltage and current paths are configured on the printed circuit board (PCB). Optimizing the placement of sensitive analog and power components is essential to minimize output ripple, maintain tight regulation specifications, and reduce PWM jitter and electromagnetic interference.

Figure 85 shows the schematic of a typical ADP1870/ADP1871 used for a high current application. Blue traces denote high current pathways. VIN, PGND, and V_{OUT} traces should be wide and possibly replicated, descending down into the multiple layers. Vias should populate, mainly around the positive and negative terminals of the input and output capacitors, alongside the source of Q1/Q2, the drain of Q3/Q4, and the inductor.

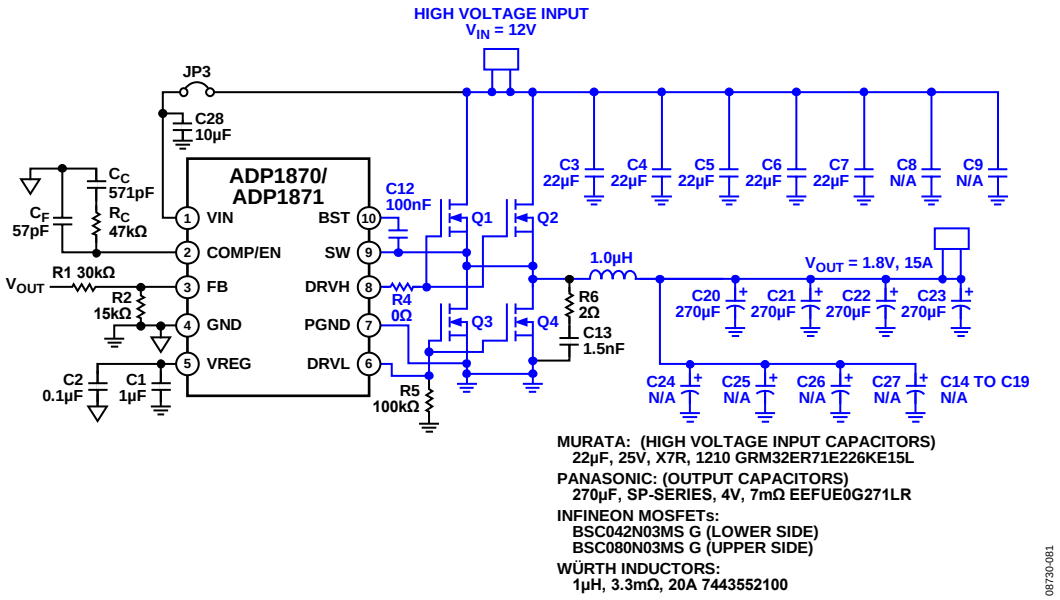

Figure 85. ADP1870 High Current Evaluation Board Schematic (Blue Traces Indicate High Current Paths)

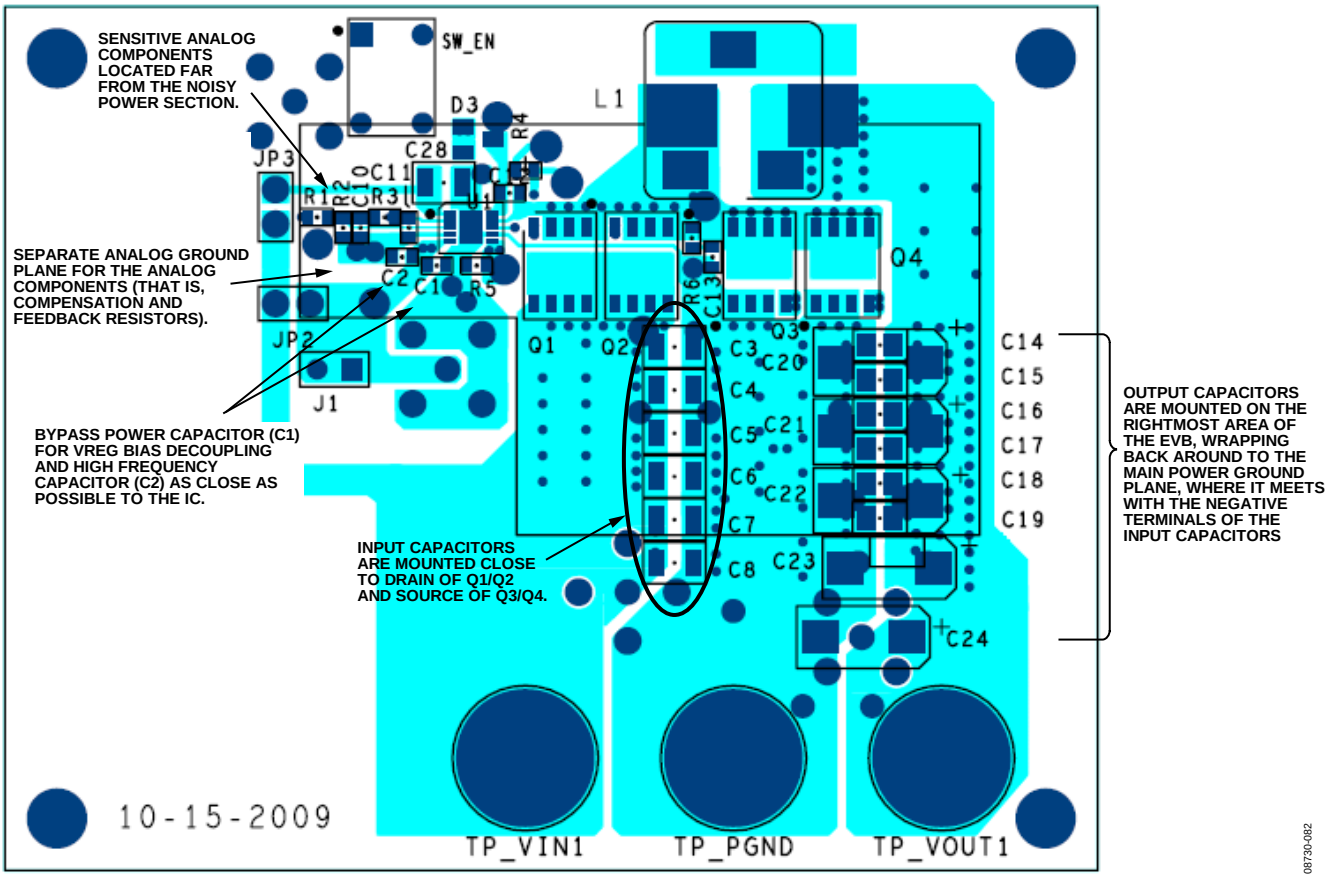

Figure 86. Overall Layout of the ADP1870 High Current Evaluation Board

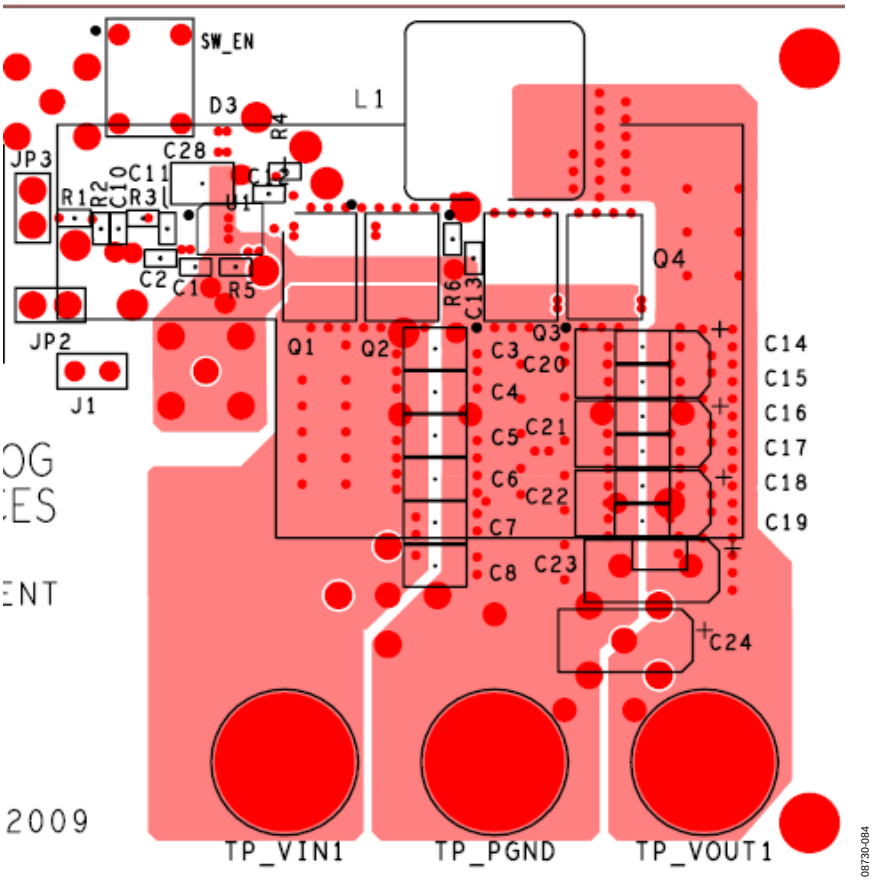

Figure 87. Layer 2 of Evaluation Board

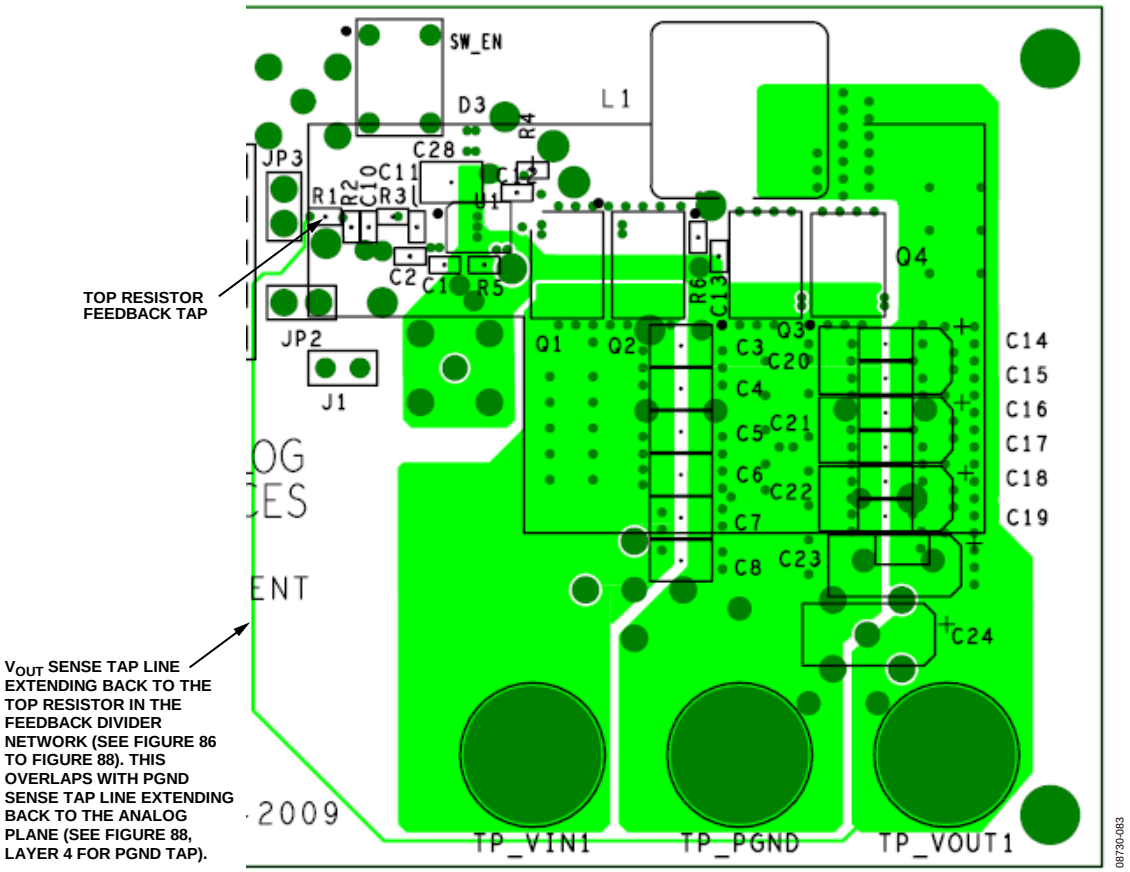

Figure 88. Layer 3 of Evaluation Board

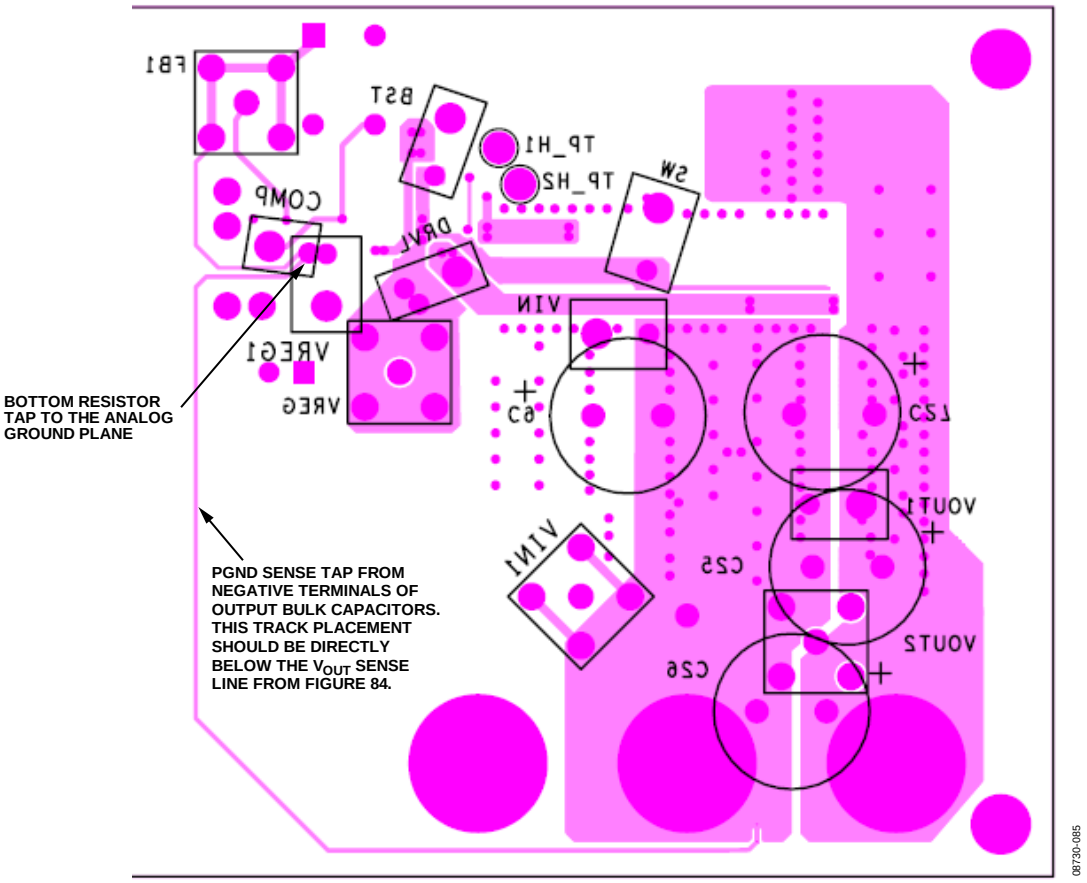

Figure 89. Layer 4 (Bottom Layer) of Evaluation Board

IC SECTION (LEFT SIDE OF EVALUATION BOARD)

A dedicated plane for the analog ground plane (GND) should be separate from the main power ground plane (PGND). With the shortest path possible, connect the analog ground plane to the GND pin (Pin 4). This plane should be on only the top layer of the evaluation board. To avoid crosstalk interference, there should not be any other voltage or current pathway directly below this plane on Layer 2, Layer 3, or Layer 4. Connect the negative terminals of all sensitive analog components to the analog ground plane. Examples of such sensitive analog components include the resistor divider's bottom resistor, the high frequency bypass capacitor for biasing (0.1 µF), and the compensation network.

Mount a 1 µF bypass capacitor directly across the VREG pin (Pin 5) and the PGND pin (Pin 7). In addition, a 0.1 µF should be tied across the VREG pin (Pin 5) and the GND pin (Pin 4).

POWER SECTION

As shown in Figure 86, an appropriate configuration to localize large current transfer from the high voltage input (V_{IN}) to the output (V_{OUT}) and then back to the power ground is to put the V_{IN} plane on the left, the output plane on the right, and the main power ground plane in between the two. Current transfers from the input capacitors to the output capacitors, through Q1/Q2, during the on state (see Figure 90). The direction of this current (yellow arrow) is maintained as Q1/Q2 turns off and Q3/Q4 turns on. When Q3/Q4 turns on, the current direction continues to be maintained (red arrow) as it circles from the bulk capacitor's power ground terminal to the output capacitors, through the Q3/Q4. Arranging the power planes in this manner minimizes the area in which changes in flux occur if the current through Q1/Q2 stops abruptly. Sudden changes in flux, usually at source terminals of Q1/Q2 and drain terminal of Q3/Q4, cause large dV/dt's at the SW node.

The SW node is near the top of the evaluation board. The SW node should use the least amount of area possible and be away from any sensitive analog circuitry and components because this is where most sudden changes in flux density occur. When possible, replicate this pad onto Layer 2 and Layer 3 for thermal relief and eliminate any other voltage and current pathways directly beneath the SW node plane. Populate the SW node plane with vias, mainly around the exposed pad of the inductor terminal and around the perimeter of the source of Q1/Q2 and the drain of Q3/Q4. The output voltage power plane (V_{OUT}) is at the rightmost end of the evaluation board. This plane should be replicated, descending down to multiple layers with vias surrounding the inductor terminal and the positive terminals of the output bulk capacitors. Ensure that the negative terminals of the output capacitors are placed close to the main power ground (PGND), as previously mentioned. All of these points form a tight circle

(component geometry permitting) that minimizes the area of flux change as the event switches between D and 1 − D.

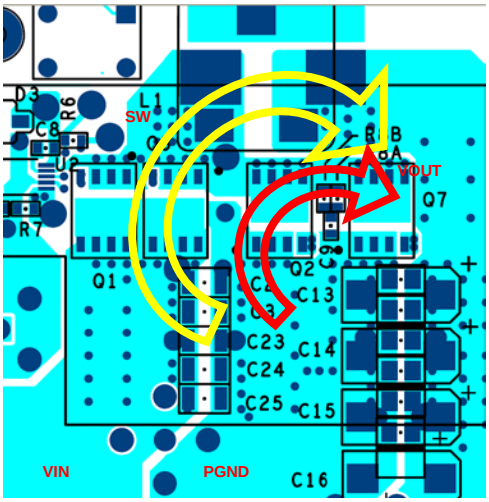

Figure 90. Primary Current Pathways During the On State of the Upper-Side MOSFET (Left Arrow) and the On State of the Lower-Side MOSFET (Right Arrow)

DIFFERENTIAL SENSING

Because the ADP1870/ADP1871 operate in valley current-mode control, a differential voltage reading is taken across the drain and source of the lower-side MOSFET. The drain of the lower-side MOSFET should be connected as close as possible to the SW pin (Pin 9) of the IC. Likewise, the source should be connected as close as possible to the PGND pin (Pin 7) of the IC. When possible, both of these track lines should be narrow and away from any other active device or voltage/current path.

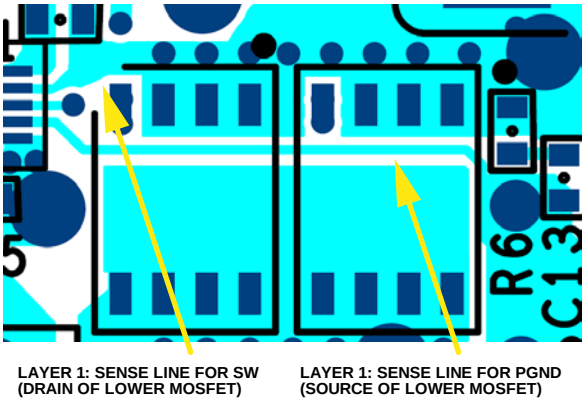

Figure 91. Drain/Source Tracking Tapping of the Lower-Side MOSFET for CS Amp Differential Sensing (Yellow Sense Line on Layer 2)

Differential sensing should also be applied between the outermost output capacitor to the feedback resistor divider (see Figure 88 and Figure 89). Connect the positive terminal of the output capacitor to the top resistor (R_T). Connect the negative terminal of the output capacitor to the negative terminal of the bottom resistor, which connects to the analog ground plane as well. Both of these track lines, as previously mentioned, should be narrow and away from any other active device or voltage/current path.

TYPICAL APPLICATIONS CIRCUITS

15 A, 300 kHz HIGH CURRENT APPLICATION CIRCUIT

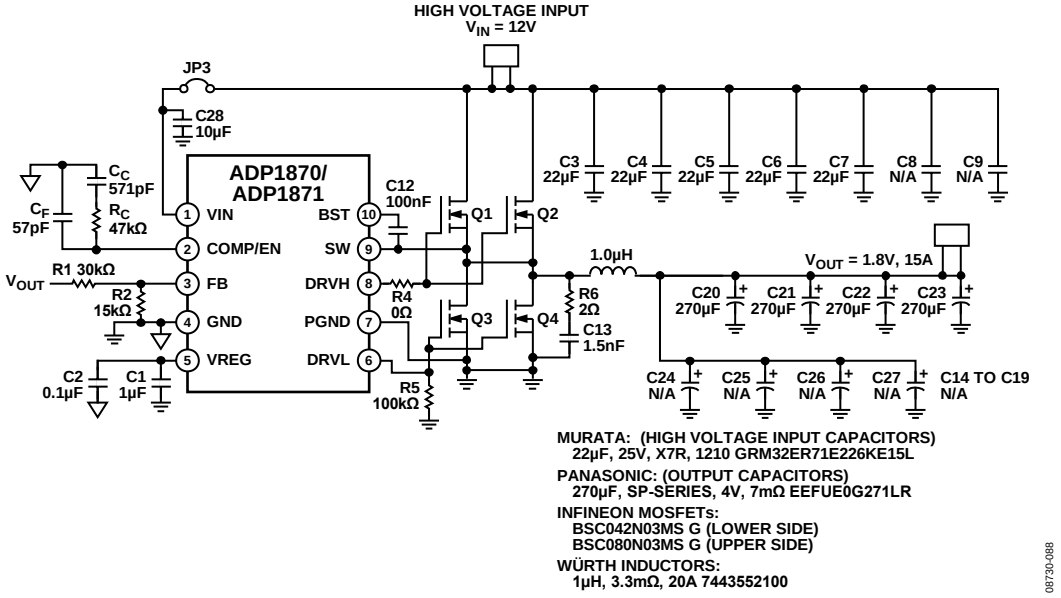

Figure 92. Application Circuit for 12 V Input, 1.8 V Output, 15 A, 300 kHz (Q2/Q4 No Connect)

5.5 V INPUT, 600 kHz APPLICATION CIRCUIT

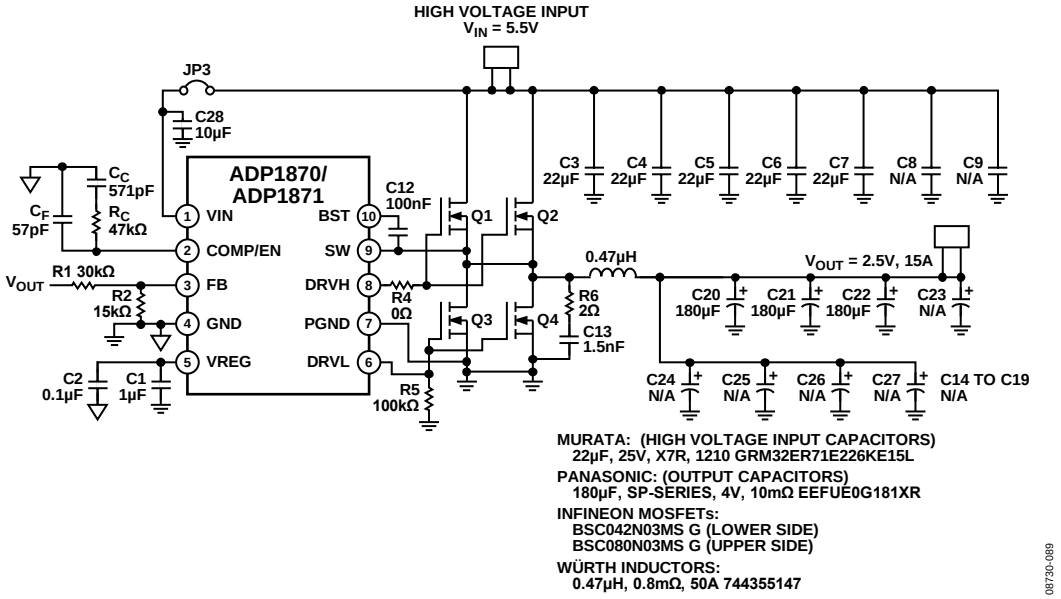

Figure 93. Application Circuit for 5.5 V Input, 2.5 V Output, 15 A, 600 kHz (Q2/Q4 No Connect)

300 kHz HIGH CURRENT APPLICATION CIRCUIT

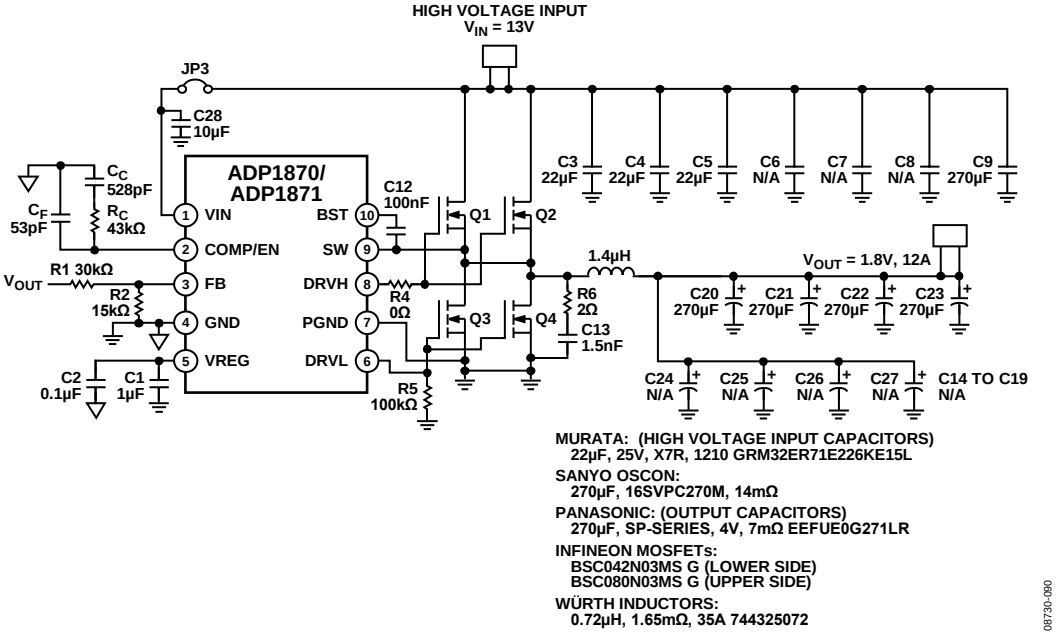

Figure 94. Application Circuit for 13 V Input, 1.8 V Output, 12 A, 300 kHz (Q2/Q4 No Connect)

OUTLINE DIMENSIONS

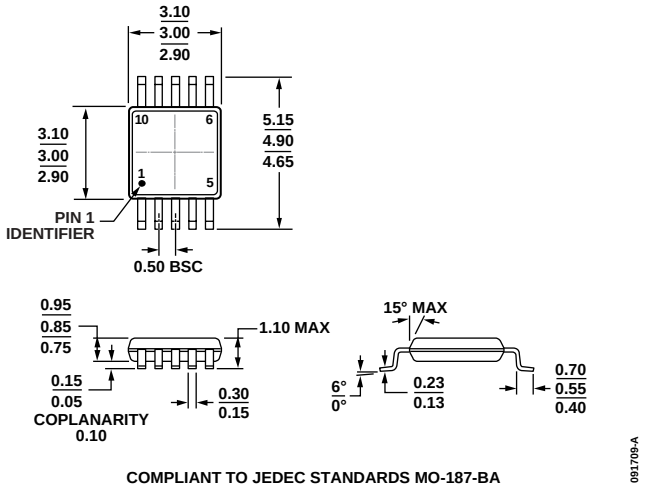

Figure 95. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

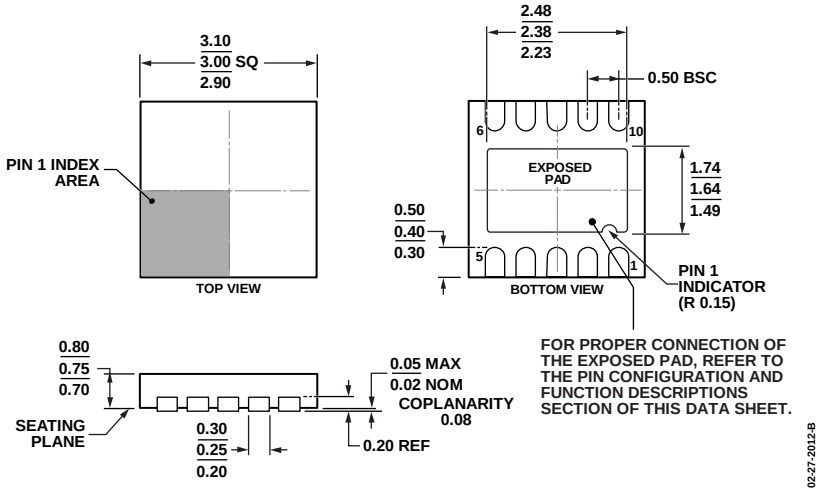

Figure 96. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP1870ARMZ-0.3-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDW
ADP1870ARMZ-0.6-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDX
ADP1870ARMZ-1.0-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDY
ADP1871ARMZ-0.3-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDG
ADP1871ARMZ-0.6-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDM
ADP1871ARMZ-1.0-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	LDN
ADP1870ACPZ-0.3-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDW
ADP1870ACPZ-0.6-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDX
ADP1870ACPZ-1.0-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDY
ADP1871ACPZ-0.3-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDG
ADP1871ACPZ-0.6-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDM
ADP1871ACPZ-1.0-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	LDN
ADP1870-0.3-EVALZ		Evaluation Board		
ADP1870-0.6-EVALZ		Evaluation Board		
ADP1870-1.0-EVALZ		Evaluation Board		
ADP1871-0.3-EVALZ		Evaluation Board		
ADP1871-0.6-EVALZ		Evaluation Board		
ADP1871-1.0-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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