

FEATURES

- High accuracy over line and load: $\pm 0.9\%$ at 25°C , $\pm 1.8\%$ over temperature
- Ultralow dropout voltage: 200 mV (typical) at 500 mA
- Requires only $C_o = 1.0\ \mu\text{F}$ for stability
- anyCAP[®] = stable with any type of capacitor (including MLCC)
- Current and thermal limiting
- Low noise
- Low shutdown current: $< 10\ \text{nA}$ (typical)
- 2.6 V to 12 V supply range
- -40°C to $+85^\circ\text{C}$ ambient temperature range

APPLICATIONS

- PCMCIA cards
- Cellular phones
- Camcorders, cameras
- Networking systems, DSL/cable modems
- Cable set-top box
- MP3/CD players
- DSP supplies

GENERAL DESCRIPTION

The ADP3335 is a member of the ADP333x family of precision, low dropout, anyCAP voltage regulators. It operates with an input voltage range of 2.6 V to 12 V, and delivers a continuous load current up to 500 mA. The ADP3335 stands out from conventional low dropout regulators (LDOs) by using an enhanced process enabling it to offer performance advantages beyond its competition. Its patented design requires only a $1.0\ \mu\text{F}$ output capacitor for stability. This device is insensitive to output capacitor equivalent series resistance (ESR), and is stable with any good quality capacitor—including ceramic (MLCC) types for space-restricted applications. The ADP3335 achieves exceptional accuracy of $\pm 0.9\%$ at room temperature and $\pm 1.8\%$ over temperature, line, and load.

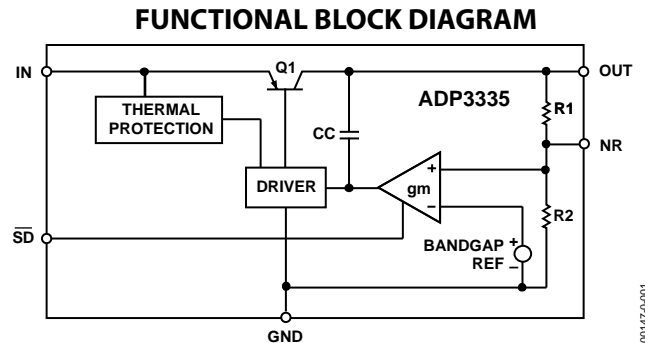


Figure 1.

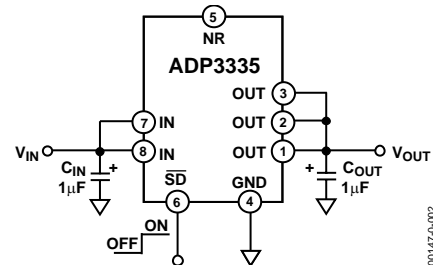


Figure 2. Typical Application Circuit

The dropout voltage of the ADP3335 is only 200 mV (typical) at 500 mA. This device also includes a safety current limit, thermal overload protection, and a shutdown feature. In shutdown mode, the ground current is reduced to less than $1\ \mu\text{A}$. The ADP3335 has a low quiescent current of $80\ \mu\text{A}$ (typical) in light load situations.

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REVISION HISTORY

10/13—Rev. C to Rev. D

Updated Outline Dimensions	12
Changes to Ordering Guide	13

12/12—Rev. B to Rev. C

Changes to Figure 14 and Figure 16.....	7
Updated Outline Dimensions	12
Changes to Ordering Guide	13

6/10—Rev. A to Rev. B

Added Exposed Pad Notation to Figure 4 and Table 3.....	5
Added Exposed Pad Notation to Outline Dimensions	12
Changes to Ordering Guide	13

1/04—Rev. 0 to Rev. A

Format Updated.....	Universal
Renumbered Figures	Universal
Removed Figure 22.....	6
Change to Printed Circuit Board Layout Considerations Section.....	11
Added LFCSP Layout Considerations Section	11
Added Package Drawing	Universal
Changes to Ordering Guide	16

SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods. Ambient temperature of 85°C corresponds to a junction temperature of 125°C under pulsed full-load test conditions. Application stable with no load. $V_{IN} = 6.0\text{ V}$, $C_{IN} = C_{OUT} = 1.0\ \mu\text{F}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy ¹	V_{OUT}	$V_{IN} = V_{OUT(NOM)} + 0.4\text{ V to }12\text{ V}$ $I_L = 0.1\text{ mA to }500\text{ mA}$ $T_A = 25^\circ\text{C}$	-0.9		+0.9	%
		$V_{IN} = V_{OUT(NOM)} + 0.4\text{ V to }12\text{ V}$ $I_L = 0.1\text{ mA to }500\text{ mA}$ $T_A = 85^\circ\text{C}$	-1.8		+1.8	%
		$V_{IN} = V_{OUT(NOM)} + 0.4\text{ V to }12\text{ V}$ $I_L = 0.1\text{ mA to }500\text{ mA}$ $T_J = 150^\circ\text{C}$	-2.3		+2.3	%
Line Regulation ¹		$V_{IN} = V_{OUT(NOM)} + 0.4\text{ V to }12\text{ V}$ $I_L = 0.1\text{ mA}$ $T_A = 25^\circ\text{C}$		0.04		mV/V
Load Regulation		$I_L = 0.1\text{ mA to }500\text{ mA}$ $T_A = 25^\circ\text{C}$		0.04		mV/mA
Dropout Voltage	V_{DROP}	$V_{OUT} = 98\%$ of $V_{OUT(NOM)}$ $I_L = 500\text{ mA}$ $I_L = 300\text{ mA}$ $I_L = 50\text{ mA}$ $I_L = 0.1\text{ mA}$		200	370	mV
				140	230	mV
				30	110	mV
				10	40	mV
Peak Load Current	I_{LDPK}	$V_{IN} = V_{OUT(NOM)} + 1\text{ V}$		800		mA
Output Noise	V_{NOISE}	$f = 10\text{ Hz to }100\text{ kHz}$, $C_L = 10\ \mu\text{F}$ $I_L = 500\text{ mA}$, $C_{NR} = 10\text{ nF}$		47		$\mu\text{V rms}$
		$f = 10\text{ Hz to }100\text{ kHz}$, $C_L = 10\ \mu\text{F}$ $I_L = 500\text{ mA}$, $C_{NR} = 0\text{ nF}$		95		$\mu\text{V rms}$
GROUND CURRENT						
In Regulation	I_{GND}	$V_{IN} = V_{OUT(NOM)} + 0.4\text{ V to }12\text{ V}$ $I_L = 500\text{ mA}$ $I_L = 300\text{ mA}$ $I_L = 50\text{ mA}$ $I_L = 0.1\text{ mA}$		4.5	10	mA
				2.6	6	mA
				0.5	2.5	mA
				80	110	μA
In Dropout	I_{GND}	$V_{IN} = V_{OUT(NOM)} - 100\text{ mV}$ $I_L = 0.1\text{ mA}$		120	400	μA
In Shutdown	I_{GNDSD}	$\overline{SD} = 0\text{ V}$, $V_{IN} = 12\text{ V}$		0.01	1	μA
SHUTDOWN						
Threshold Voltage	$V_{\overline{THSD}}$	ON	2.0			V
		OFF			0.4	V
\overline{SD} Input Current	$I_{\overline{SD}}$	$0 \leq \overline{SD} \leq 5\text{ V}$		1.2	3	μA
Output Current in Shutdown	$I_{\overline{OSD}}$	$V_{IN} = 12\text{ V}$, $V_{OUT} = 0\text{ V}$		0.01	5	μA

¹ $V_{IN} = 2.6\text{ V to }12\text{ V}$ for models with $V_{OUT(NOM)} \leq 2.2\text{ V}$.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage	-0.3 V to +16 V
Shutdown Input Voltage	-0.3 V to +16 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +150°C
θ_{JA} , 2-layer MSOP-8	220°C/W
θ_{JA} , 4-layer MSOP-8	158°C/W
θ_{JA} , 2-layer LFCSP-8	62°C/W
θ_{JA} , 4-layer LFCSP-8	48°C/W
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

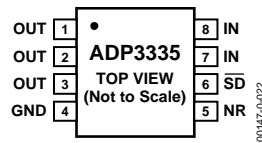


Figure 3. 8-Lead MSOP



NOTES

1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE ENHANCES THE THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO DIE SUBSTRATE. THERMAL VIAS MUST BE ISOLATED OR CONNECTED TO IN. DO NOT CONNECT THE THERMAL PAD TO GROUND.

Figure 4. 8-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 3	OUT	Output of the Regulator. Bypass to ground with a 1.0 μ F or larger capacitor. All pins must be connected together for proper operation.
4	GND	Ground Pin.
5	NR	Noise Reduction Pin. Used for further reduction of output noise (see the Noise Reduction section for further details).
6	\overline{SD}	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.
7, 8	IN	Regulator Input. All pins must be connected together for proper operation.
EP	Exposed Pad	The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to the die substrate, which is electrically common with the input pins, IN (Pin 7 and Pin 8), inside the package.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

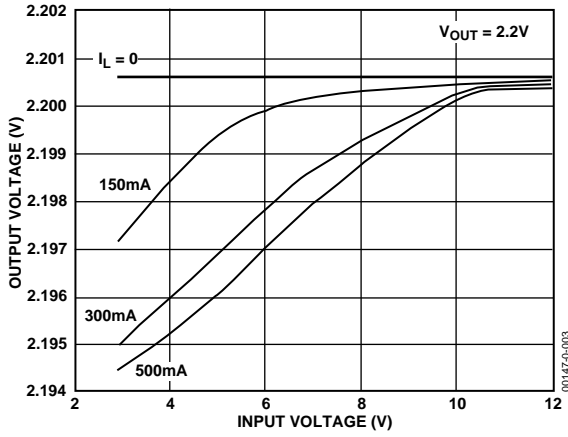


Figure 5. Line Regulation Output Voltage vs. Supply Voltage

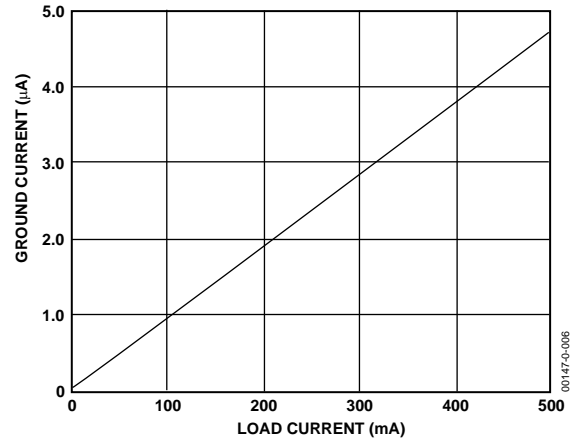


Figure 8. Ground Current vs. Load Current

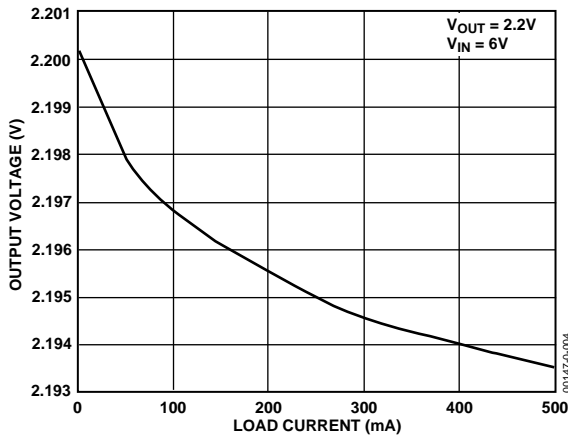


Figure 6. Output Voltage vs. Load Current

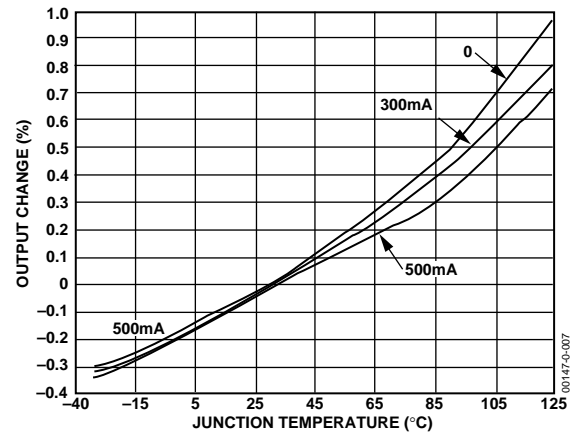


Figure 9. Output Voltage Variation vs. Junction Temperature

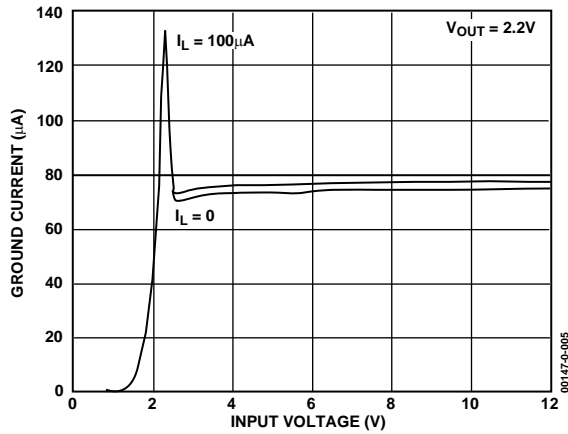


Figure 7. Ground Current vs. Supply Voltage

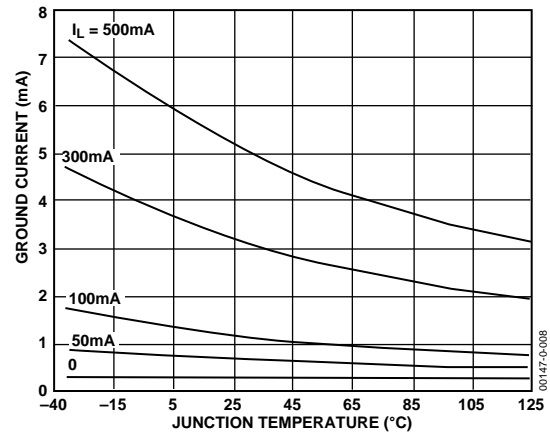


Figure 10. Ground Current vs. Junction Temperature

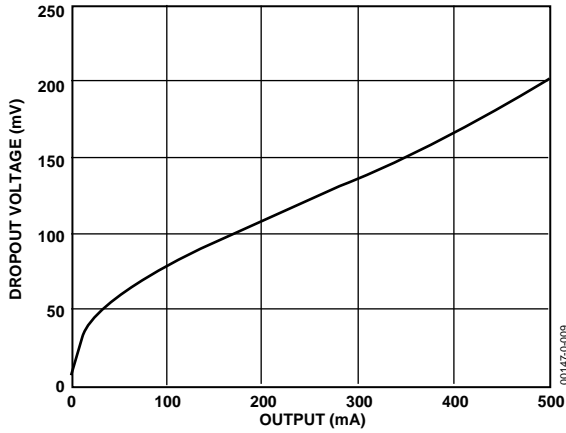


Figure 11. Dropout Voltage vs. Output Current

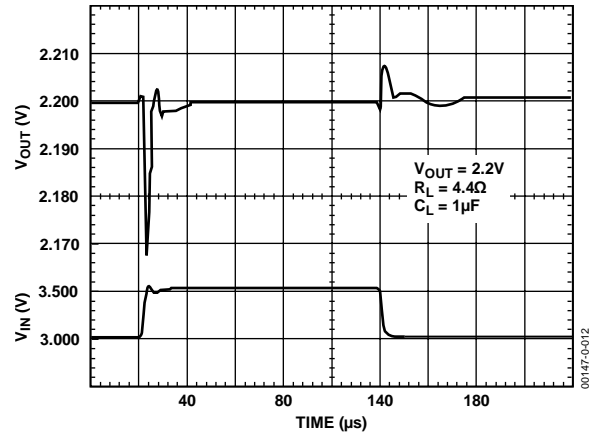


Figure 14. Line Transient Response

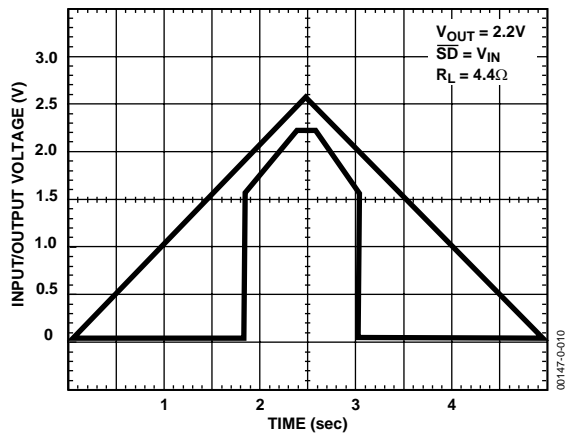


Figure 12. Power-Up/Power-Down

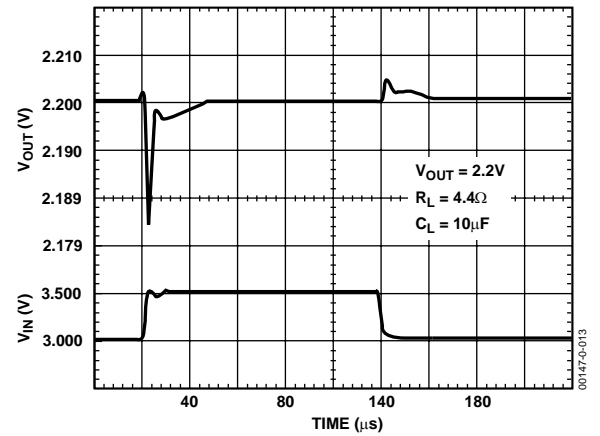


Figure 15. Line Transient Response

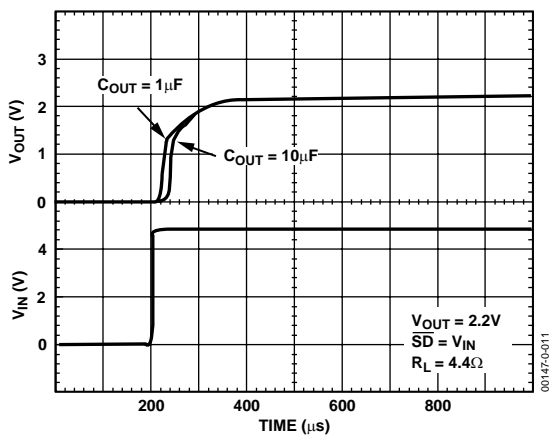


Figure 13. Power-Up Response

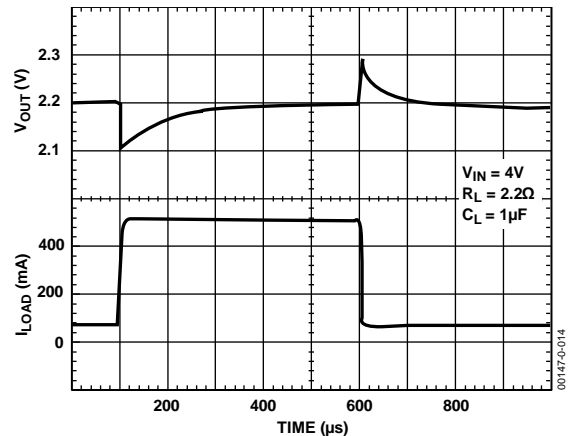


Figure 16. Load Transient Response

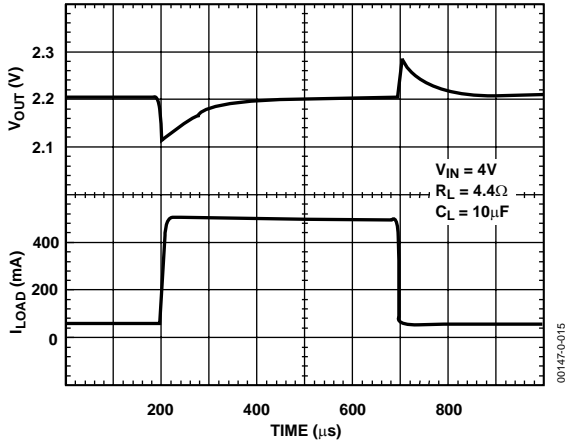


Figure 17. Load Transient Response

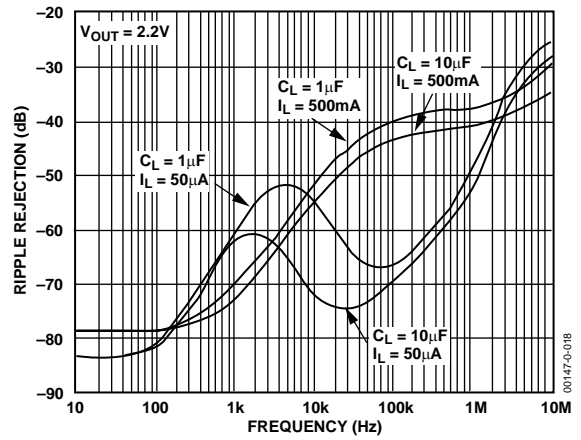


Figure 20. Power Supply Ripple Rejection

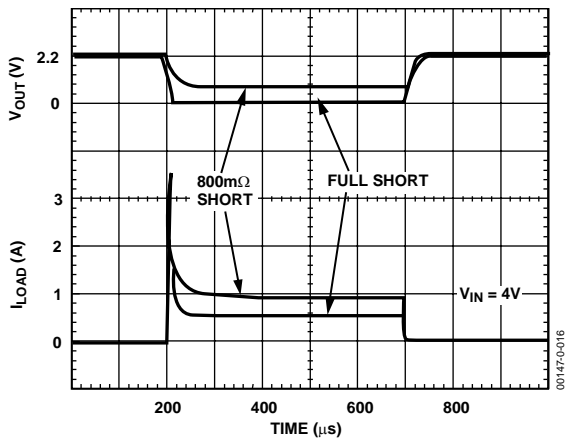


Figure 18. Short-Circuit Current

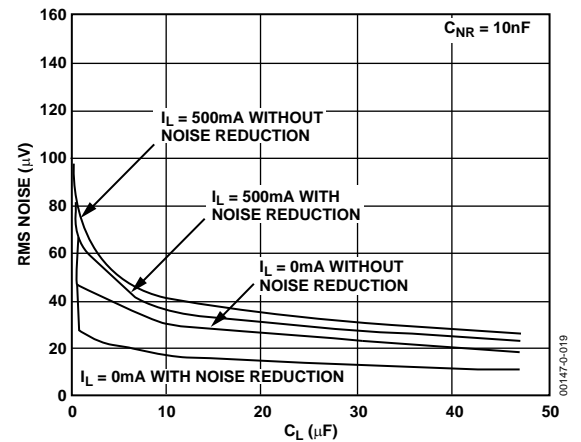


Figure 21. RMS Noise versus C_L (10 Hz to 100 kHz)

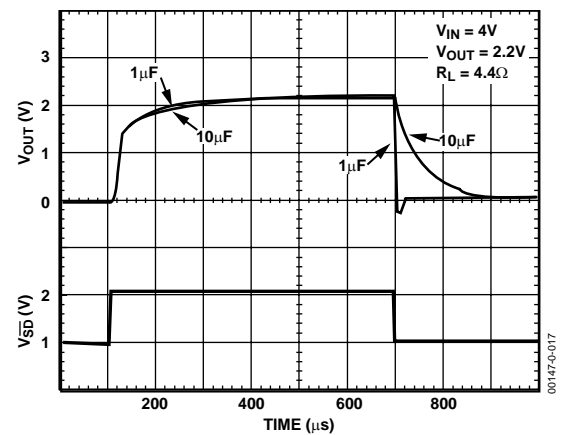


Figure 19. Turn On/Turn Off Response

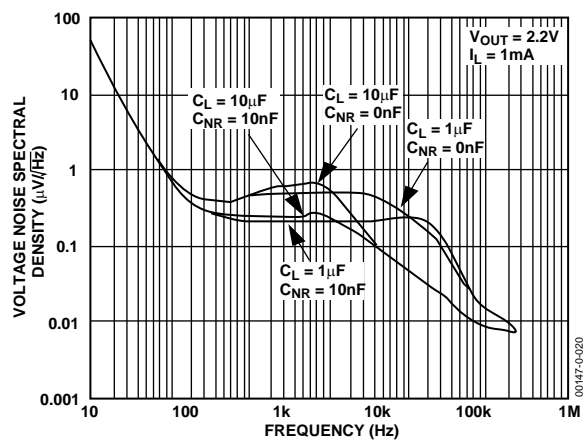


Figure 22. Output Noise Density

APPLICATIONS INFORMATION

OUTPUT CAPACITOR SELECTION

As with any micropower device, output transient response is a function of the output capacitance. The ADP3335 is stable over a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1 μF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3335 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or organic semiconductor electrolytic capacitors (OSCON). Note that the effective capacitance of some capacitor types may fall below the minimum at extreme temperatures. Ensure that the capacitor provides more than 1 μF over the entire temperature range.

INPUT BYPASS CAPACITOR

An input bypass capacitor is not strictly required, but is advisable in any application involving long input wires or high source impedance. Connecting a 1 μF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

NOISE REDUCTION

A noise reduction capacitor (C_{NR}) can be used, as shown in Figure 24, to further reduce the noise by 6 dB to 10 dB (Figure 22). Low leakage capacitors in the 100 pF to 1 nF range provide the best performance. Since the noise reduction pin, NR, is internally connected to a high impedance node, any connection to this node should be made carefully to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible, and long PC board traces are not recommended.

When adding a noise reduction capacitor, maintain a minimum load current of 1 mA when not in shutdown.

It is important to note that as C_{NR} increases, the turn-on time will be delayed. With NR values greater than 1 nF, this delay may be on the order of several milliseconds.

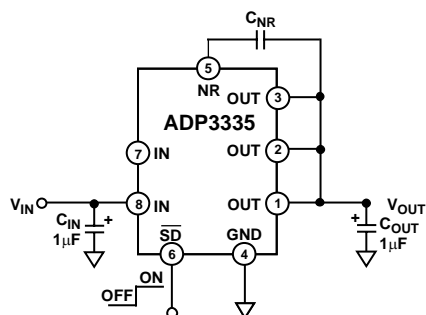


Figure 24. Typical Application Circuit

THERMAL OVERLOAD PROTECTION

The ADP3335 is protected against damage from excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 150°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})I_{LOAD} + (V_{IN})I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, and V_{IN} and V_{OUT} are input and output voltages, respectively.

Assuming $I_{LOAD} = 400$ mA, $I_{GND} = 4$ mA, $V_{IN} = 5.0$ V, and $V_{OUT} = 3.3$ V, device power dissipation is

$$P_D = (5\text{ V} - 3.3\text{ V})400\text{ mA} + 5.0\text{ V}(4\text{ mA}) = 700\text{ mW}$$

The junction temperature can be calculated from the power dissipation, ambient temperature, and package thermal resistance. The thermal resistance is a function not only of the package, but also of the circuit board layout. Standard test conditions are used to determine the values published in this data sheet, but actual performance will vary. For an LFCSP-8 package mounted on a standard 4-layer board, θ_{JA} is 48°C/W. In the above example, where the power dissipation is 700 mW, the temperature rise above ambient will be approximately equal to

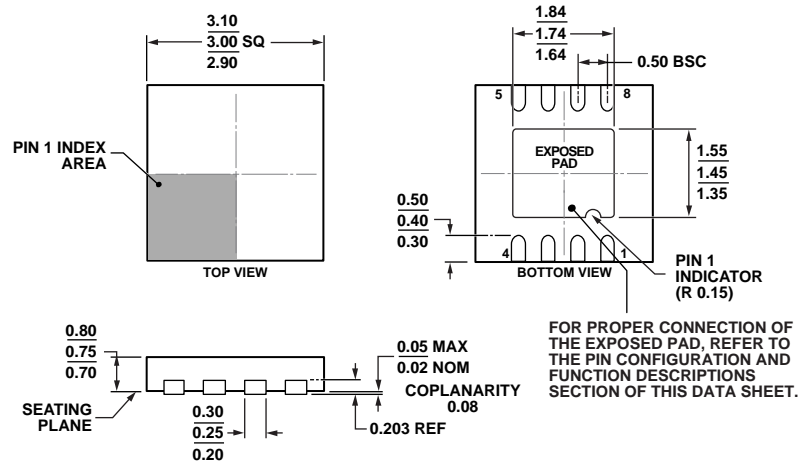
$$\Delta T_{JA} = 0.700\text{ W} \times 48^\circ\text{C/W} = 33.6^\circ\text{C}$$

To limit the maximum junction temperature to 150°C, the maximum allowable ambient temperature will be

$$T_{AMAX} = 150^\circ\text{C} - 33.6^\circ\text{C} = 116.4^\circ\text{C}$$

In this case, the resulting ambient temperature limitation is above the maximum allowable ambient temperature of 85°C.

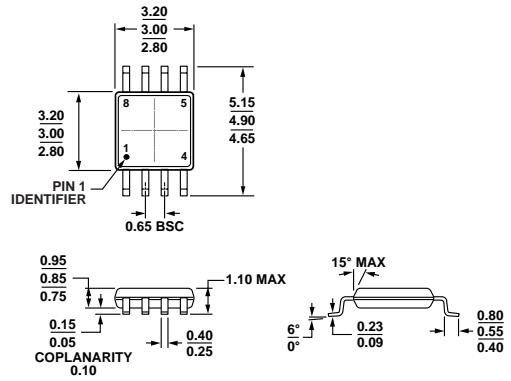
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 26. 8-Lead Lead Frame Chip Scale Package [LFCS_P_WD]
3 mm x 3 mm Body, Very Very Thin, Dual Lead
(CP-8-13)
Dimensions shown in millimeters

12-07-2010-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 27. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

100709-B

ORDERING GUIDE

Model ¹	Output Voltage (V) ²	Temperature Range	Package Description	Package Option	Branding ³
ADP3335ACPZ-1.8-R7	1.8	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1G
ADP3335ACPZ-2.5-R7	2.5	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1H
ADP3335ACPZ-2.85R7	2.85	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1J
ADP3335ACPZ-3.3-R7	3.3	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1K
ADP3335ACPZ-3.3-RL	3.3	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1K
ADP3335ACPZ-5-R7	5	-40°C to +85°C	8-Lead LFCSP_WD	CP-8-13	L1L
ADP3335ARMZ-1.8-R7	1.8	-40°C to +85°C	8-Lead MSOP	RM-8	LFA
ADP3335ARMZ-1.8-RL	1.8	-40°C to +85°C	8-Lead MSOP	RM-8	LFA
ADP3335ARMZ-2.5-RL	2.5	-40°C to +85°C	8-Lead MSOP	RM-8	LFC
ADP3335ARMZ-2.5RL7	2.5	-40°C to +85°C	8-Lead MSOP	RM-8	LFC
ADP3335ARMZ-2.85R7	2.85	-40°C to +85°C	8-Lead MSOP	RM-8	LFD
ADP3335ARMZ-2.85RL	2.85	-40°C to +85°C	8-Lead MSOP	RM-8	LFD
ADP3335ARMZ-3.3-RL	3.3	-40°C to +85°C	8-Lead MSOP	RM-8	LFE
ADP3335ARMZ-3.3RL7	3.3	-40°C to +85°C	8-Lead MSOP	RM-8	LFE
ADP3335ARMZ-5-R7	5	-40°C to +85°C	8-Lead MSOP	RM-8	LFF
ADP3335ARMZ-5-REEL	5	-40°C to +85°C	8-Lead MSOP	RM-8	LFF

¹ Z = RoHS Compliant Part.

² For additional voltage options, contact a local sales or distribution representative.

³ Z = RoHS Compliant Parts have a "#" marked on the device preceding the date code.

NOTES

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NOTES

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- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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