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February 2016



FDMS7658AS

N-Channel PowerTrench® SyncFET™

30 V, 176 A, 1.9 mΩ

Features

- Max $r_{DS(on)}$ = 1.9 mΩ at $V_{GS} = 10$ V, $I_D = 28$ A
- Max $r_{DS(on)}$ = 2.2 mΩ at $V_{GS} = 7$ V, $I_D = 26$ A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- SyncFET™ Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

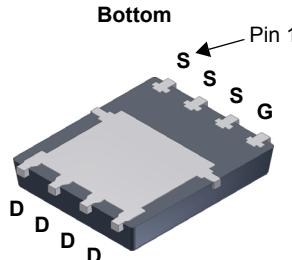
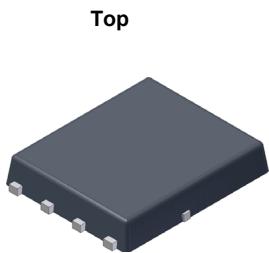


General Description

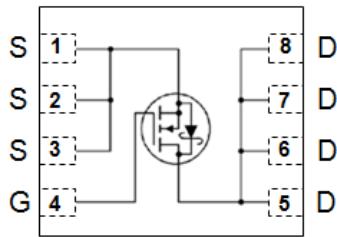
The FDMS7658AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification



Power 56



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	(Note 4)	±20
I_D	Drain Current -Continuous $T_C = 25$ °C	176	A
	-Continuous $T_C = 100$ °C	112	
	-Continuous $T_A = 25$ °C (Note 1a)	29	
	-Pulsed (Note 6)	670	
dv/dt	MOSFET dv/dt	1.5	V/ns
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	mJ
P_D	Power Dissipation $T_C = 25$ °C	89	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7658AS	FDMS7658AS	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	30			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10 \text{ mA}$, referenced to 25°C		23		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

On Characteristics (Note 2)

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	1.2	1.7	3.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10 \text{ mA}$, referenced to 25°C		-5		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 28 \text{ A}$		1.5	1.9	$\text{m}\Omega$
		$V_{GS} = 7 \text{ V}, I_D = 26 \text{ A}$		1.7	2.2	
		$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}$		1.9	2.4	
		$V_{GS} = 10 \text{ V}, I_D = 28 \text{ A}, T_J = 125^\circ\text{C}$		2.0	2.6	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 28 \text{ A}$		181		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		5525	7350	pF
C_{oss}	Output Capacitance			2020	2685	pF
C_{rss}	Reverse Transfer Capacitance			150	230	pF
R_g	Gate Resistance		0.1	0.4	0.9	Ω

Switching Characteristics

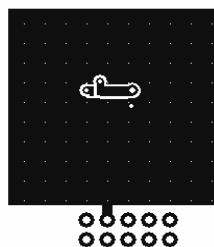
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 28 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		20	36	ns
t_r	Rise Time			8	17	ns
$t_{d(off)}$	Turn-Off Delay Time			43	70	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$		78	109	nC
Q_g	Total Gate Charge		$V_{DD} = 15 \text{ V}, I_D = 28 \text{ A}$	35	49	nC
Q_{gs}	Gate to Source Gate Charge			16.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			6.6		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)		0.38	0.9	V
		$V_{GS} = 0 \text{ V}, I_S = 28 \text{ A}$ (Note 2)		0.74	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 28 \text{ A}, di/dt = 300 \text{ A}/\mu\text{s}$		46	75	ns
				73	117	nC

Notes:

1. R_{QJA} is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5 \text{ in.}$ board of FR-4 material. R_{QCA} is guaranteed by design while R_{QCA} is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty cycle $< 2.0\%$.

3. E_{AS} of 162 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 1 \text{ mH}$, $I_{AS} = 18 \text{ A}$, $V_{DD} = 27 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% test at $L = 0.3 \text{ mH}$, $I_{AS} = 28 \text{ A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

6. Pulsed I_d please refer to Fig 11 SOA graph for more details.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

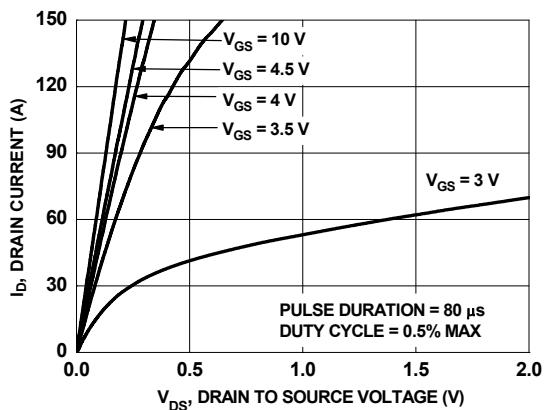


Figure 1. On-Region Characteristics

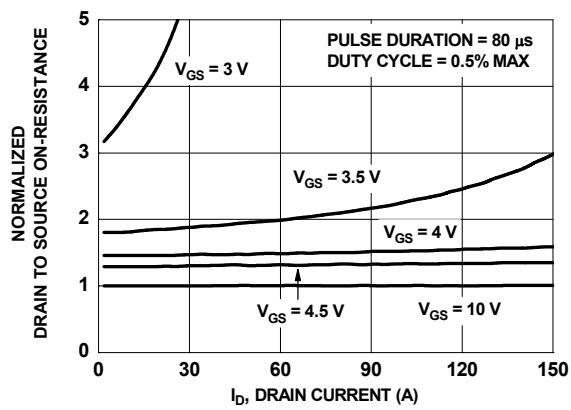


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

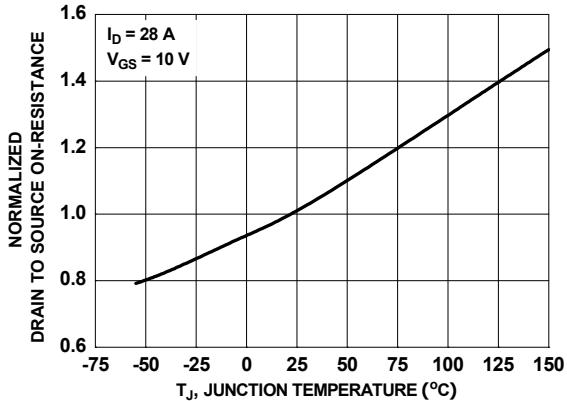


Figure 3. Normalized On-Resistance vs. Junction Temperature

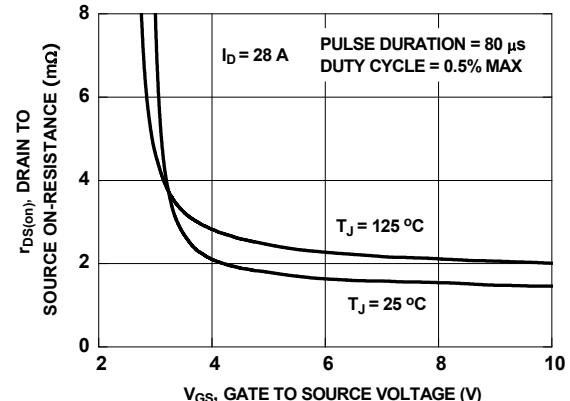


Figure 4. On-Resistance vs. Gate to Source Voltage

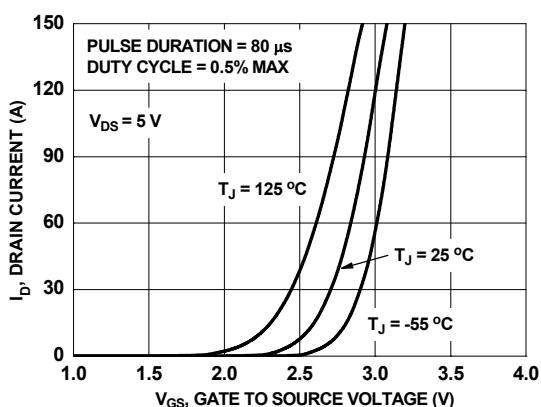


Figure 5. Transfer Characteristics

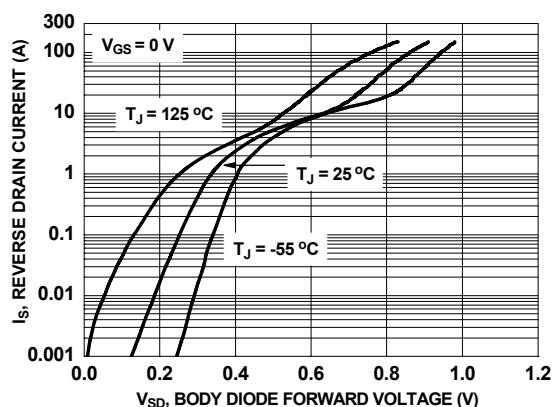


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

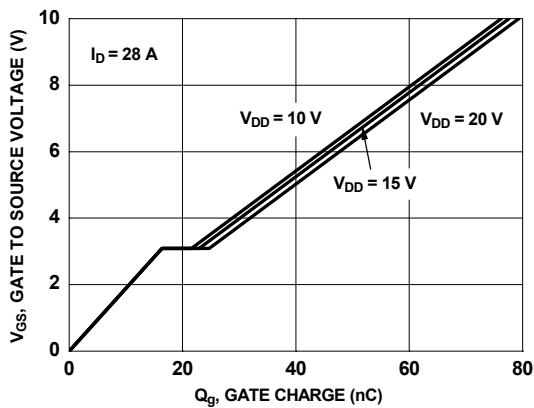


Figure 7. Gate Charge Characteristics

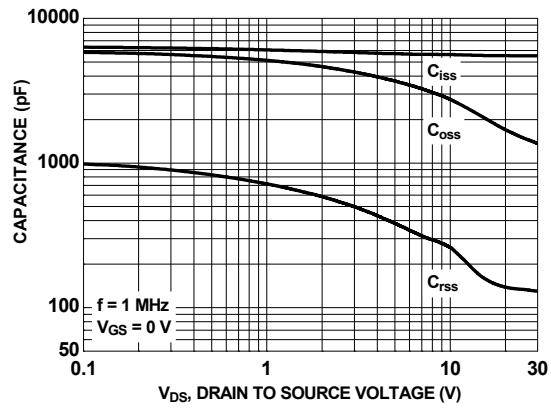


Figure 8. Capacitance vs. Drain to Source Voltage

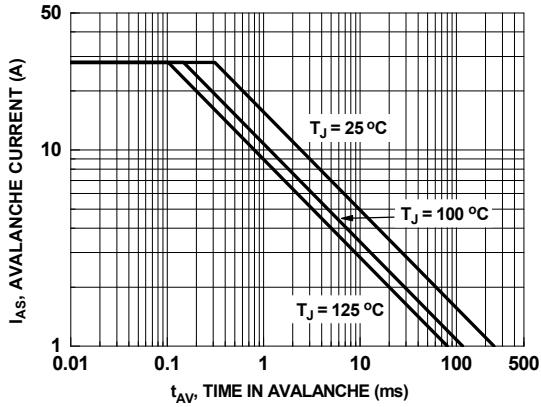


Figure 9. Unclamped Inductive Switching Capability

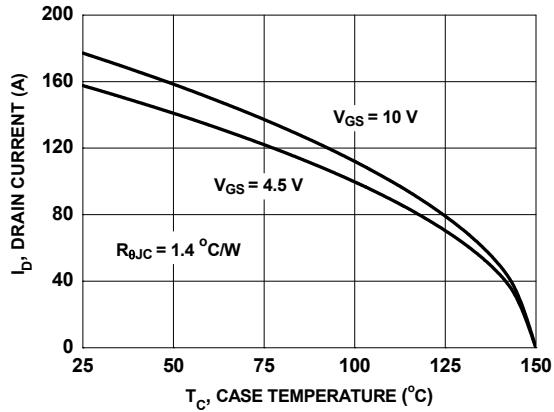


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

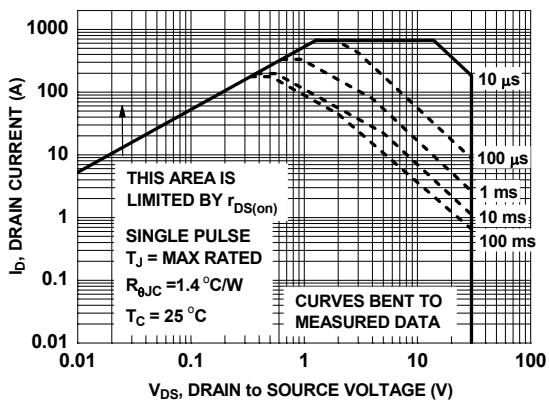


Figure 11. Forward Bias Safe Operating Area

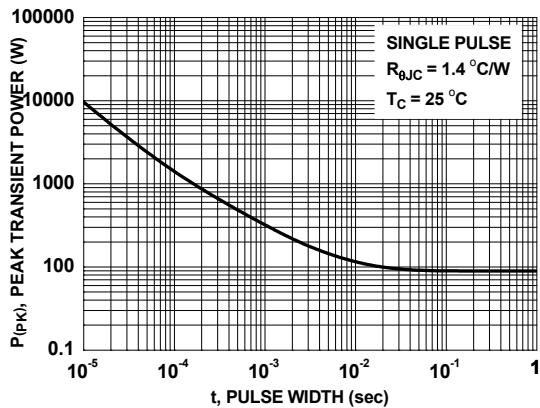


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

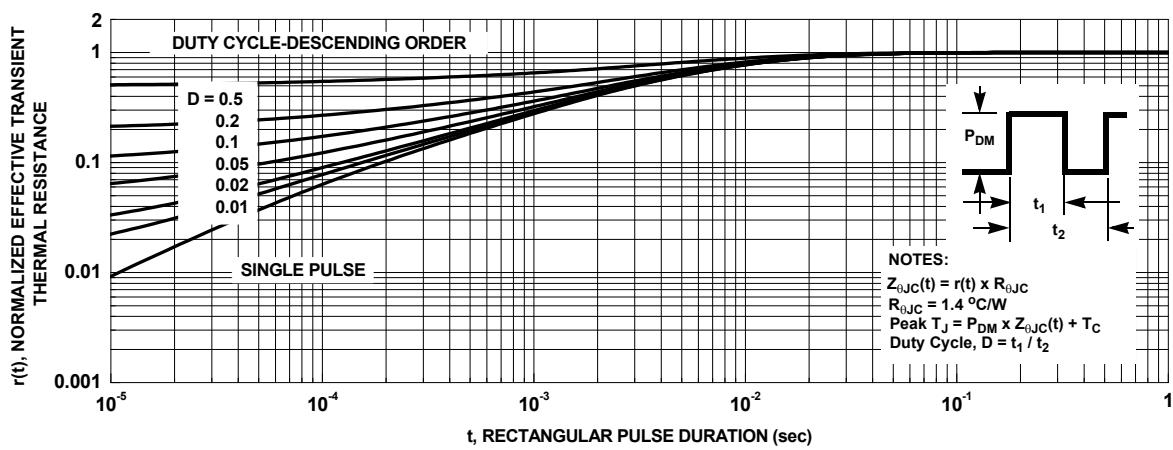


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS7658AS.

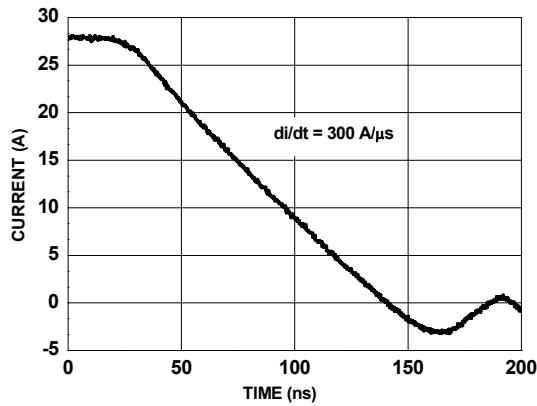


Figure 14. FDMS7658AS SyncFET™ Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

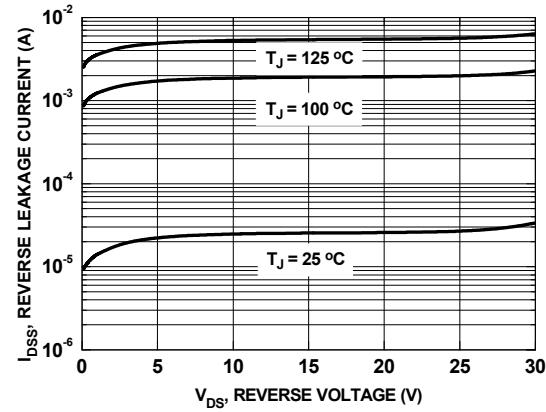
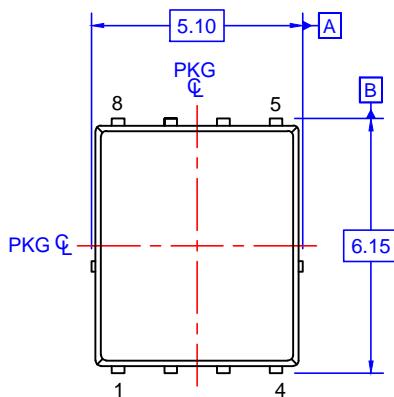
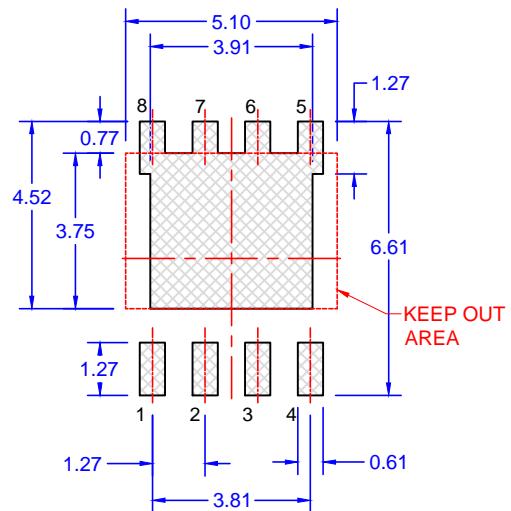
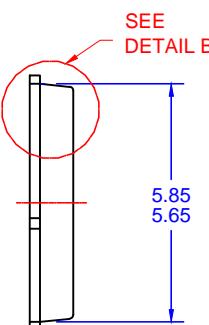


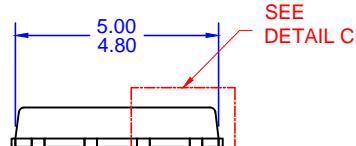
Figure 15. SyncFET™ Body Diode Reverse Leakage vs. Drain-Source Voltage



TOP VIEW

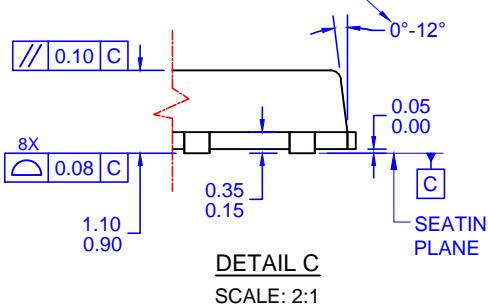


LAND PATTERN
RECOMMENDATION

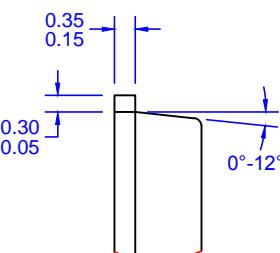


SIDE VIEW

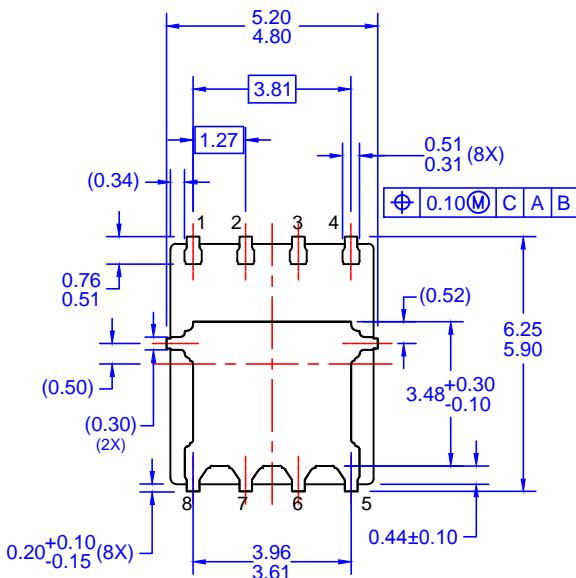
OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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