QPD2195

400 W, 48 V, 1.8-2.2 GHz GaN RF Power Transistor

Product Description

The QPD2195 is a discrete GaN on SiC HEMT which operates from 1.8-2.2 GHz. The device is a single stage pre-matched power amplifier transistor.

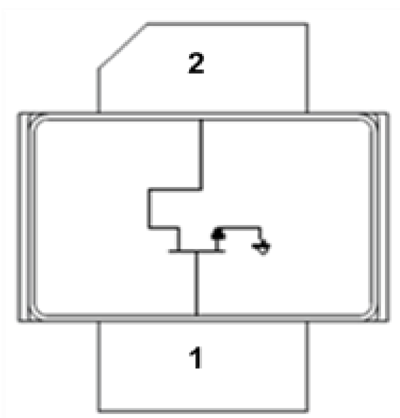
The QPD2195 can be used in Doherty architecture for the final stage of a base station power amplifier for macrocell high efficiency systems.

QPD2195 can deliver P_{3dB} of 400 W at +48 V operation.

RoHS compliant.

2 Lead NI780 Package

Functional Block Diagram



Product Features[1]

- Operating Frequency Range: 1.8-2.2 GHz
- Operating Drain Voltage: +48 V
- Maximum Output Power (P_{3dB}): 400 W (1)
- Maximum Drain Efficiency: 75.4% (1)
- Efficiency-Tuned P3dB Gain: 19.1 dB (1)
- 2-lead, earless, ceramic flange NI780 package

Note 1: Load pull at 2110 MHz

Applications

- W-CDMA / LTE
- Macrocell Base Station, B3-B1
- Active Antenna

Ordering Information

Part Number	Description
QPD2195SR	Reel – 100 Pieces
QPD2195PCB4B01	1805-2170 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Gate Current (I_G)	−67 to 67 mA
Drain Voltage (V_D)	+55 V
Peak RF Input Power	44 dBm
VSWR Mismatch, P1dB Pulse (10 % duty cycle, 100 μ width), T = 25 °C	10:1
Storage Temperature	−65 to +150°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating

Parameter	Min	Typ	Max	Units
Gate Voltage (V_G)		−2.8		V
Drain Voltage (V_D)		48		V
Quiescent Current (I_{DQ})		720		mA

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

RF Characterization

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		1805		2170	MHz
Quiescent Current			720		mA
Linear Gain			20.4		dB
P3dB			56.3		dBm
Drain Efficiency	P3dB		70.1		%

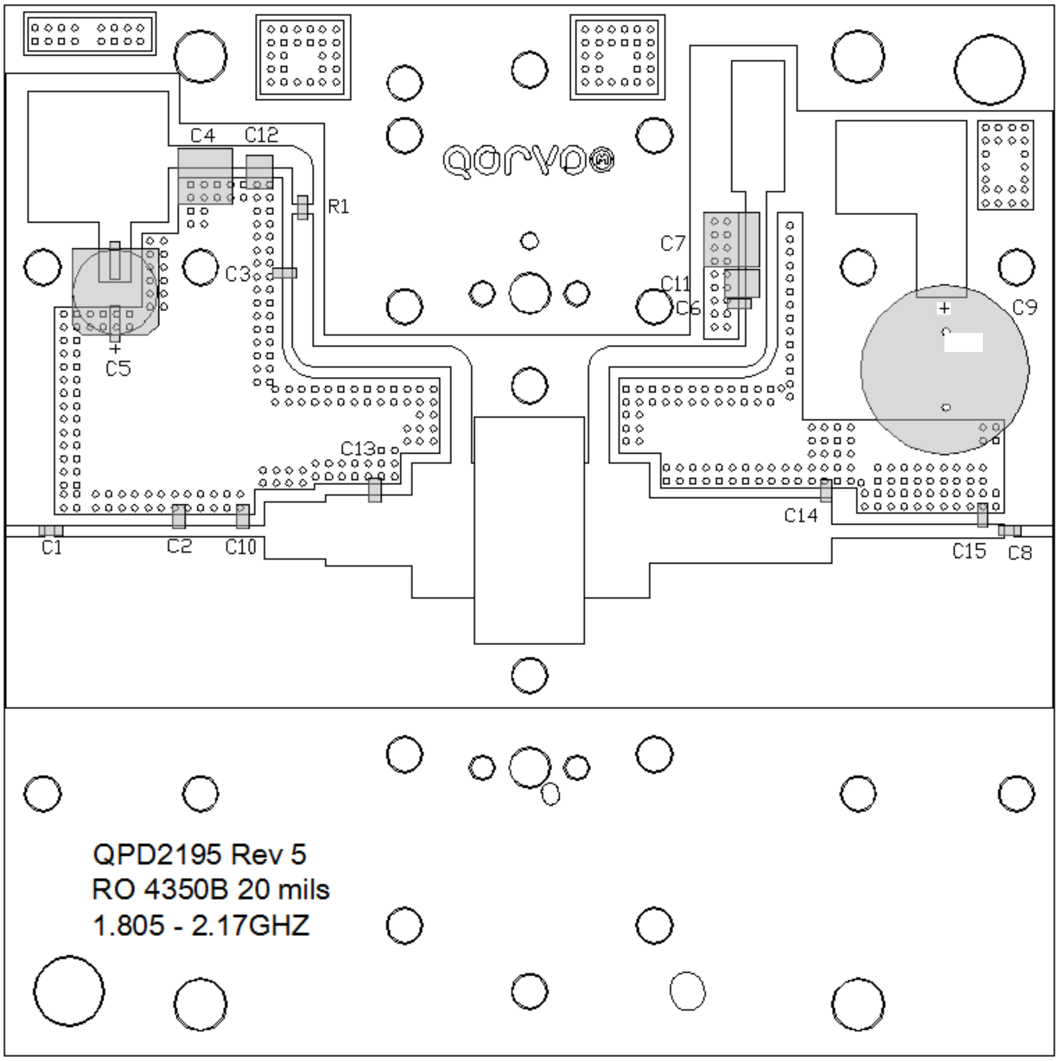
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, Pulsed CW (10% duty cycle, 100 μs width) on Class AB single-ended EVB at 1880 MHz

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = 85°C, T_{CH} = 110°C, CW: P_{DISS} = 60 W, P_{OUT} = 90 W	0.42	°C/W

Notes:
1. Thermal resistance measured to package backside.
2. Based on expected carrier amplifier efficiency of Doherty.
3. P_{OUT} assumes 20% peaking amplifier contribution of total average Doherty rated power.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

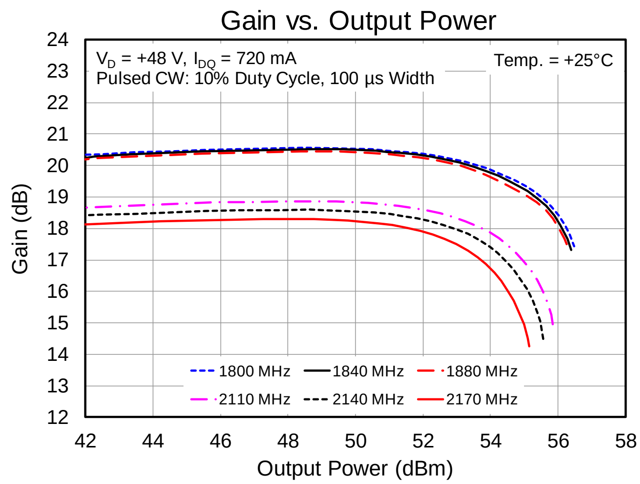
QPD2195PCB4B01 Layout

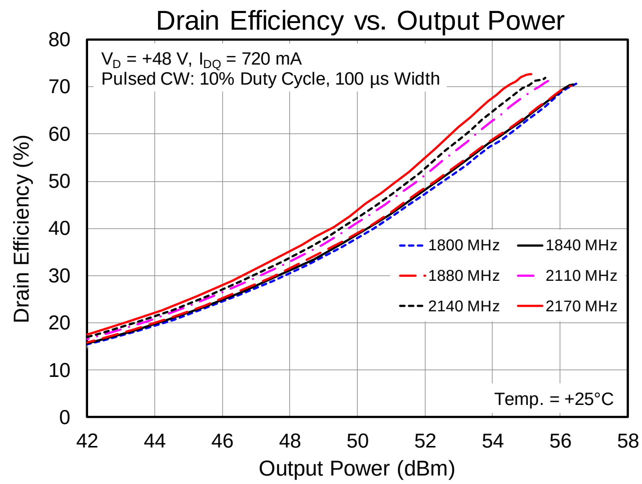


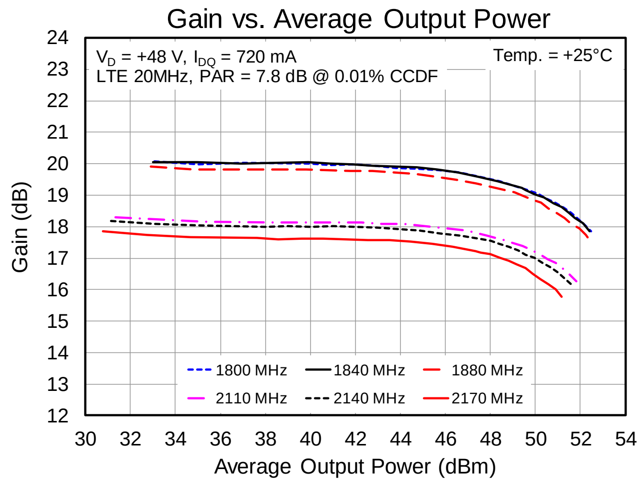
QPD2195PCB4B01 Bill of Materials

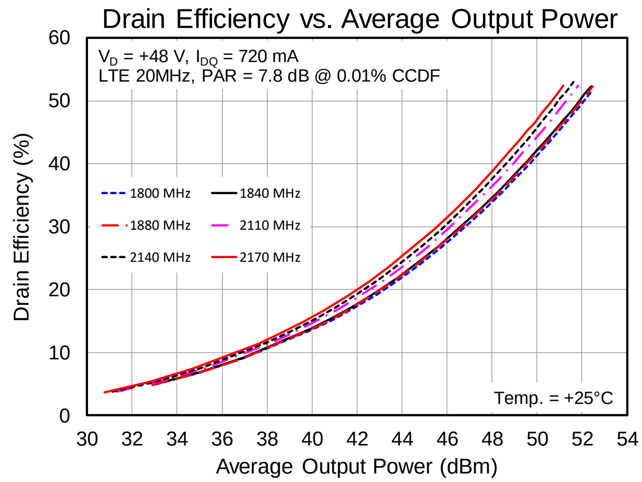
Reference Des.	Value	Description	Manuf.	Part Number
C1, C3, C6, C8	33 pF	Capacitor, 33 pF, 5%, 250V	ATC	ATC800A330JT250X
C2	0.6 pF	Capacitor, 0.6 pF, +/- 0.1pF, 250V	ATC	ATC800A0R6BT250X
C10	0.2 pF	Capacitor, 0.2 pF, +/- 0.1pF, 250V	ATC	ATC800A0R2BT250X
C14, C15	0.4 pF	Capacitor, 0.4 pF, +/- 0.1pF, 250V	ATC	ATC800A0R4BT250X
C13	0.3 pF	Capacitor, 0.3 pF, +/- 0.1pF, 250V	ATC	ATC800A0R3BT250X
C11, C12	1.0 µF	Capacitor, 1 µF, 10%, 100V, X7R	MURATA	GRM32NR72A104KA01L
C4, C7	4.7 µF	Capacitor, 4.7 µF, 10%, 100V, X7R	MURATA	GRM55ER72A475KA01L
C5	100 µF	Capacitor, 100uF, 50V, +/-20%, SMD	Panasonic	EEE-1HA101UAP
C9	220 µF	Capacitor, 220uF, 100V, +/-20%, SMD	Panasonic	AFK227M2AR44T-F
R1	10 Ω	Resistor, 10 Ω, 5%, 0.25W, 1206	Panasonic	ERJ-8ENF10R0V

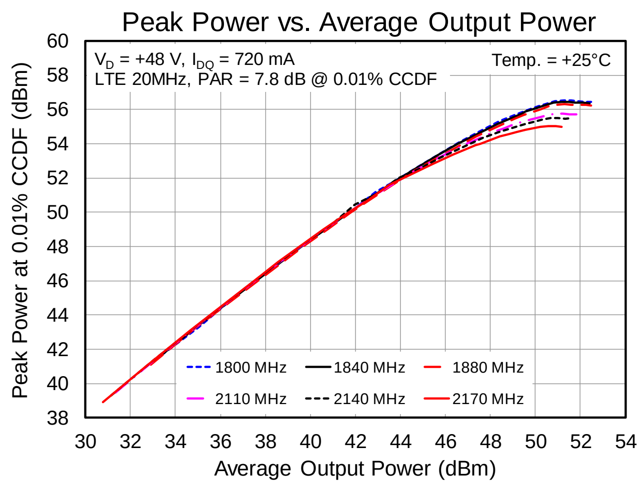
QPD2195PCB4B01 Performance Plots

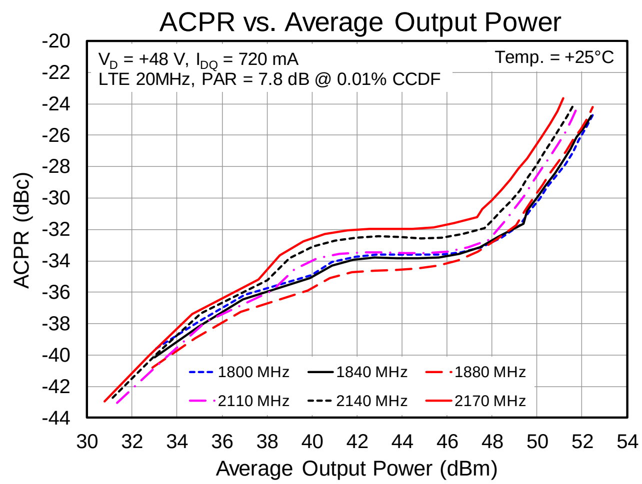






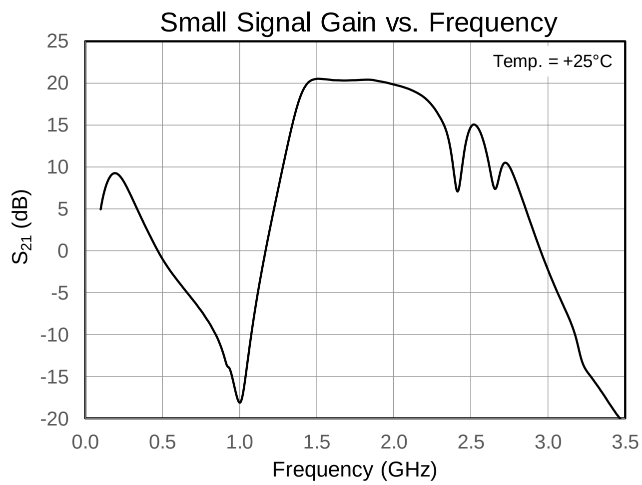


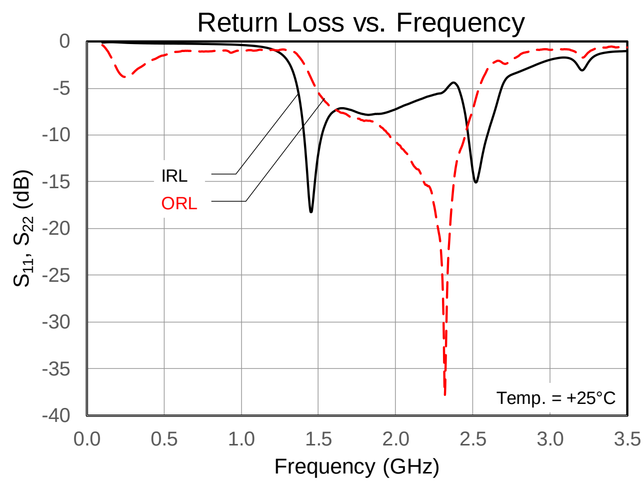




Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, on Class AB single-ended EVB

QPD2195PCB4B01 Performance Plots





Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, on Class AB single-ended EVB

Power-Tuned Load Pull Performance

Frequency (MHz)	Source Impedance	Load Impedance	Gain @ P3dB (dB)	P3dB (dBm)	Drain Efficiency (%)
1800	1.68 – j2.21	5.39 – j1.33	18.2	56.0	60.5
1840	1.34 – j2.45	5.39 – j1.33	18.1	56.1	62.7
1880	1.44 - j2.82	5.54 - j0.11	17.8	56.2	60.9
1990	1.51 – j3.72	5.79 + j1.48	17.4	56.0	60.4
2110	2.00 – j5.57	3.89 + j3.09	17.2	56.0	60.5
2140	2.48 – j6.14	3.67 + j3.42	16.7	56.0	59.5
2170	3.07 - j6.71	3.67 + j3.42	16.6	56.1	61.8
2200	3.38 – j7.21	3.11 + j3.04	16.6	55.9	58.5

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, Pulsed (10% duty cycle, 100 µs width)

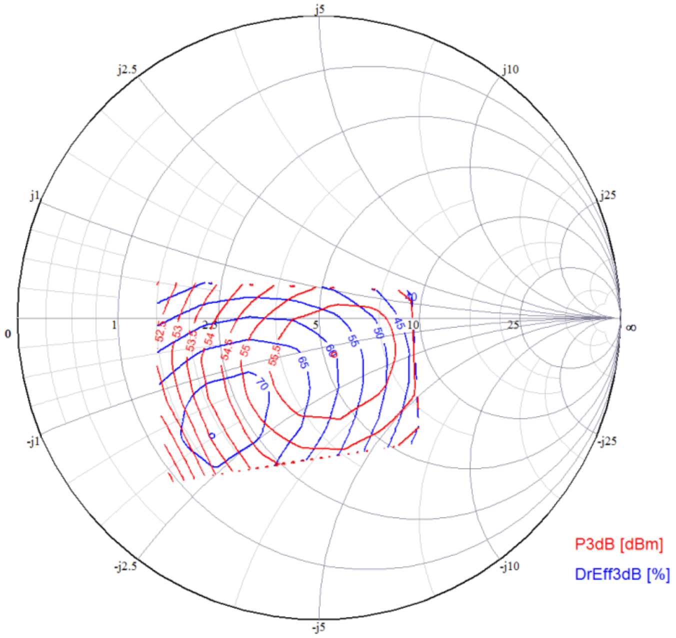
Efficiency-Tuned Load Pull Performance

Frequency (MHz)	Source Impedance	Load Impedance	Gain @ P3dB (dB)	P3dB (dBm)	Drain Efficiency (%)
1800	1.68 – j2.21	1.79 – j1.97	20.3	53.5	72.6
1840	1.34 – j2.45	1.79 – j1.97	20.2	53.2	73.3
1880	1.44 - j2.82	1.79 - j1.97	19.9	53.1	73.9
1990	1.51 – j3.72	3.10 – j1.88	19.4	53.9	74.1
2110	2.00 – j5.57	4.36 – j2.15	19.1	53.2	75.4
2140	2.48 – j6.14	4.40 – j2.03	18.8	53.0	75.5
2170	3.07 - j6.71	5.70 - j2.55	18.4	53.0	77.4
2200	3.38 – j7.21	6.74 – j1.27	18.4	53.6	75.5

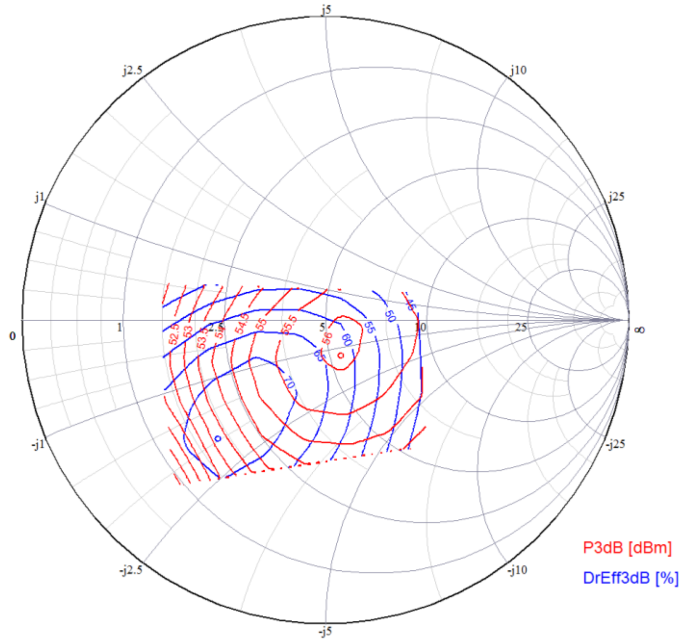
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, Pulsed (10% duty cycle, 100 µs width)

Load Pull Plots

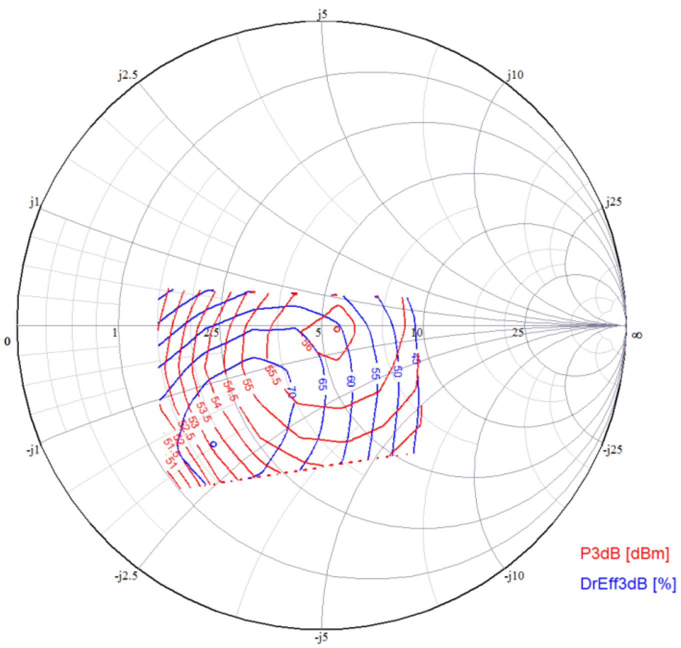
Load Pull at 1.8 GHz



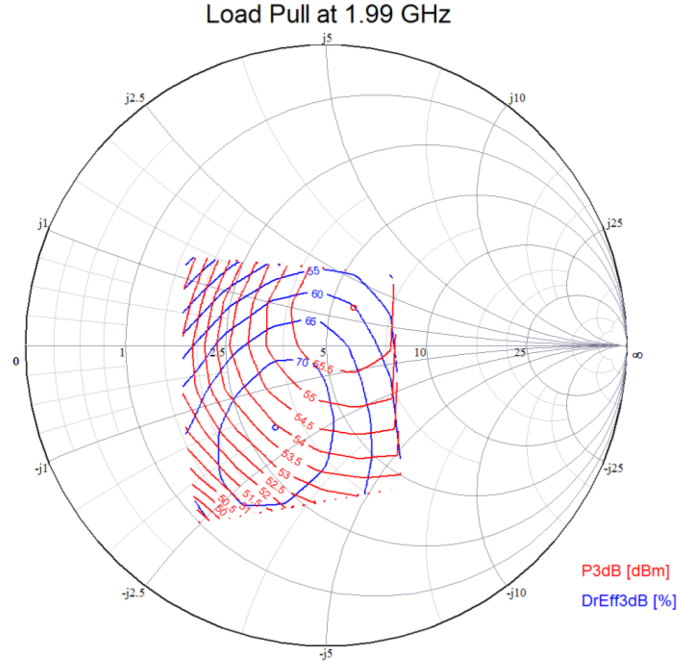
Load Pull at 1.84 GHz



Load Pull at 1.88 GHz

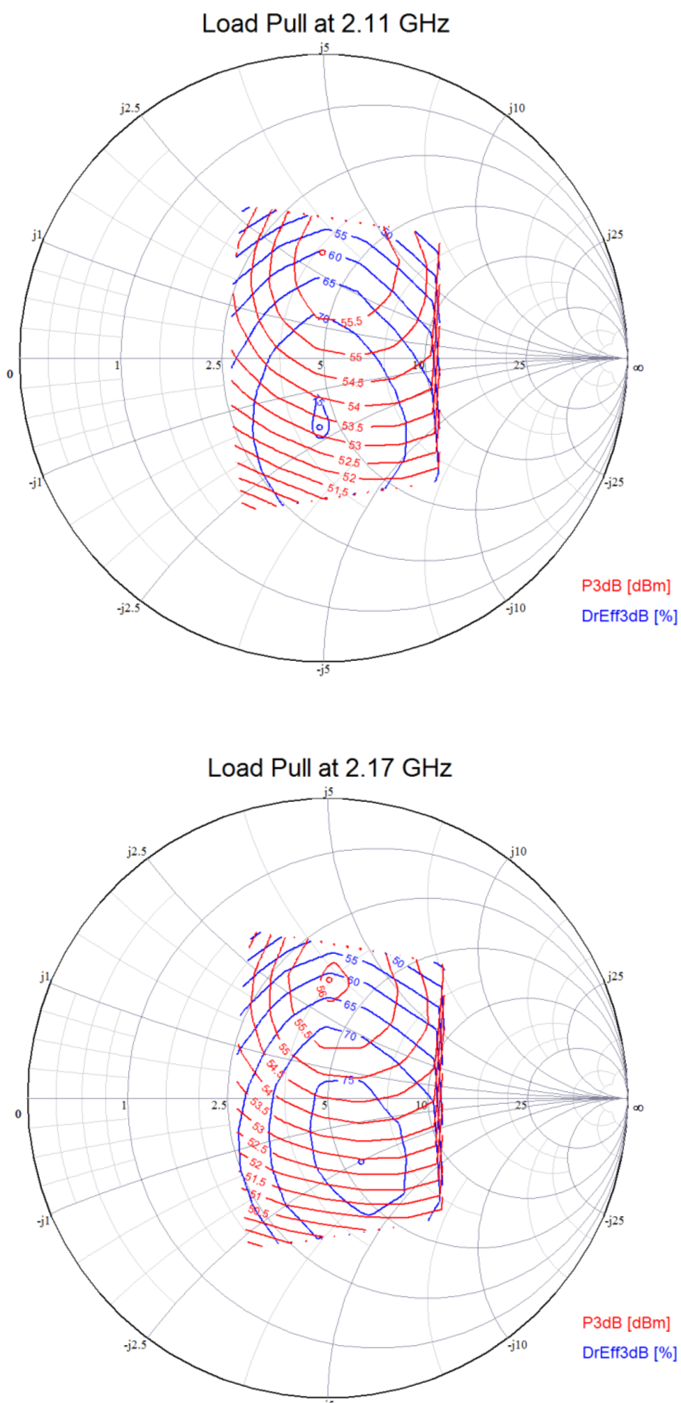


Load Pull at 1.99 GHz



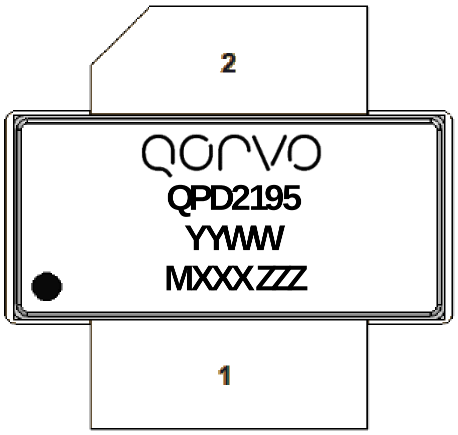
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, Pulsed (10% duty cycle, 100 µs width)

Load Pull Plots

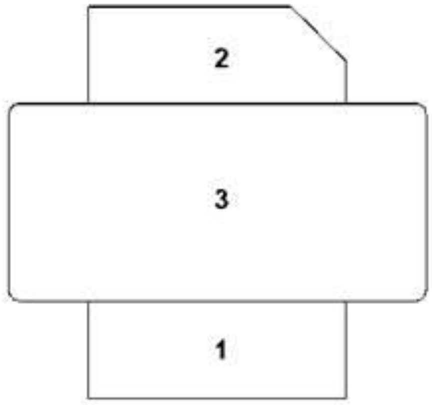


Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 720 mA, T = 25°C, Pulsed (10% duty cycle, 100 µs width)

Pin Configuration



TOP VIEW



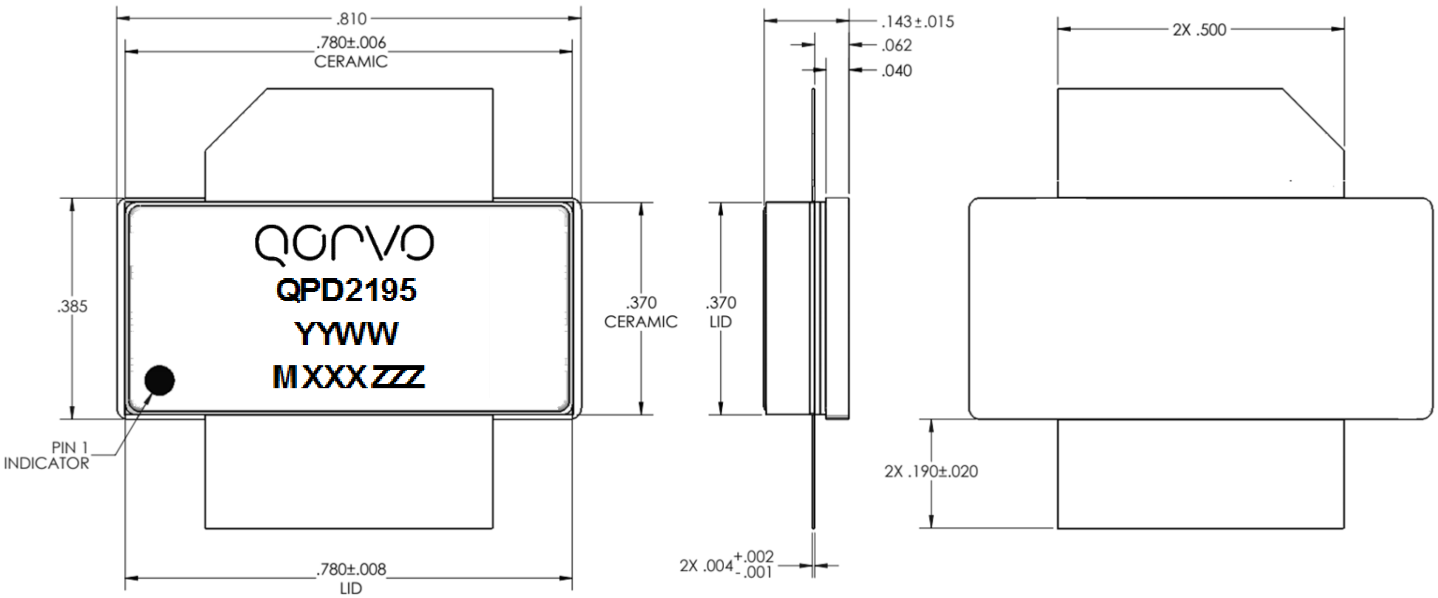
BOTTOM VIEW

Pin Description

Pin No.	Label	Description
1	RF IN, VG	RF Input, Gate Bias
2	RF OUT, VD	RF Output, Drain Bias
3 (Backside Paddle)	RF/DC GND	RF/DC Ground

Package Marking and Dimensions

Marking: Qorvo Logo
Part Number – QPD2195
Date Code – YYWW
Production Lot Number – MXXX
Serial Number – ZZZ



Notes: Unless Otherwise Specified;

1. Material:
   Package Base: Metal/Ceramic
   Package Lid: Ceramic
   Lead: Alloy 42
2. Package exposed metal base and leads are NiAu plated. Au thickness is minimum 60 µin.
3. Part is epoxy sealed.
4. Part meets industry NI780 footprint.
5. Body dimensions do not include lid shift or epoxy run out, which can be up to 0.020 per side.
6. Dimensions are in inches. General tolerance is ±0.005.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESDA/JEDEC Standard JS-002
MSL – 260°C Convection Reflow	Level 3	IPC/JEDEC Standard J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C maximum reflow temperature) soldering processes.
The use of no-clean solder to avoid washing after soldering is recommended.
Contact plating is NiAu. Au thickness is minimum 60 µin.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-II to meet RoHS Compliance requirements
- Halogen Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.qorvo.com **Tel:** 1-844-890-8163
Email: customer.support@qorvo.com

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