PHPT61006NY

100 V, 6 A NPN high power bipolar transistor

26 January 2015 Product data sheet

1. General description

NPN high power bipolar transistor in a SOT669 (LFPAK56) Surface-Mounted Device (SMD) power plastic package.

PNP complement: PHPT61006PY

2. Features and benefits

- High thermal power dissipation capability
- High temperature applications up to 175 °C
- Reduced Printed Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- AEC-Q101 qualified.

3. Applications

- Power management
- Load switch
- Linear mode voltage regulator
- Backlighting applications
- Motor drive
- Relay replacement

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	100	V
I_C	collector current			-	-	6	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-	12	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 6$ A; $I_B = 600$ mA; $t_p \leq 300$ µs; $\delta \leq 0.02$; $T_{amb} = 25$ °C; pulsed		-	35	57	mΩ

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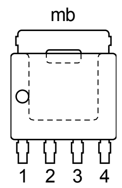
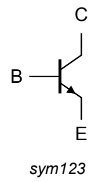
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E	emitter	 **LFPAK56; Power-SO8 (SOT669)**	
2	E	emitter		
3	E	emitter		
4	B	base		
mb	C	collector		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT61006NY	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PHPT61006NY	1006NAB

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

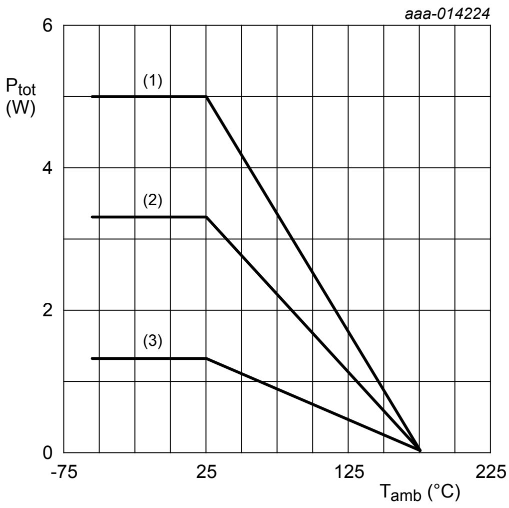
Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	100	V
V_{CEO}	collector-emitter voltage	open base		-	100	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
I_C	collector current			-	6	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	12	A
I_B	base current			-	1	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	1.3	W
			[2]	-	3.3	W
			[3]	-	5	W
			[4]	-	25	W
T_j	junction temperature			-	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB); single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB; single-sided copper; tin-plated and mounting pad for collector 6 cm^2.

[3] Device mounted on an ceramic PCB; Al_2O_3, standard footprint.

[4] Power dissipation from junction to mounting base.



(1) Ceramic PCB, Al_2O_3, standard footprint

(2) FR4 PCB, mounting pad for collector 6 cm^2

(3) FR4 PCB, standard footprint

Fig. 1. Power derating curves

9. Thermal characteristics

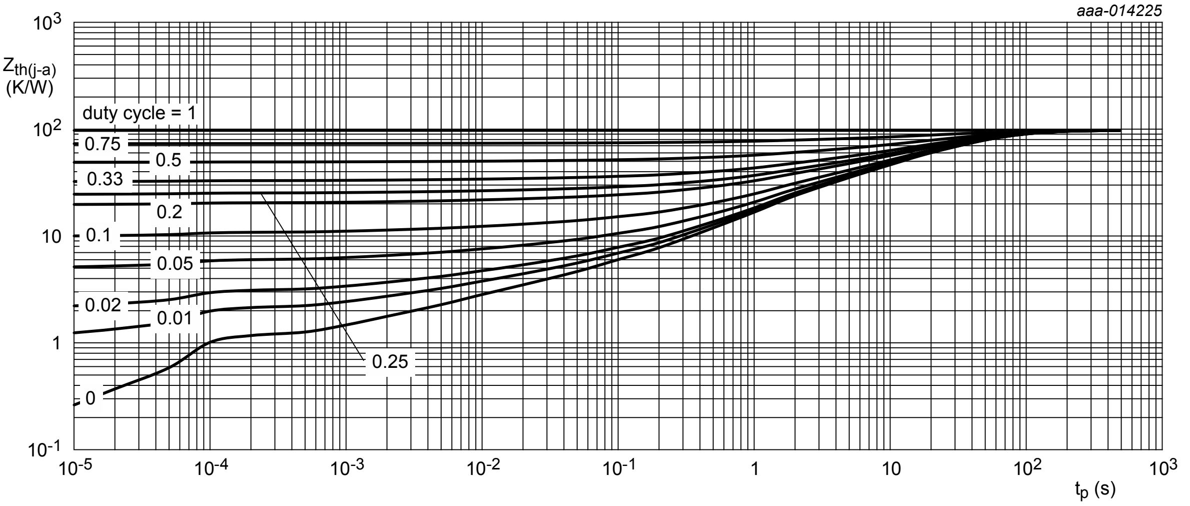
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	115	K/W
			[2]	-	-	45	K/W
			[3]	-	-	30	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	-	6	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

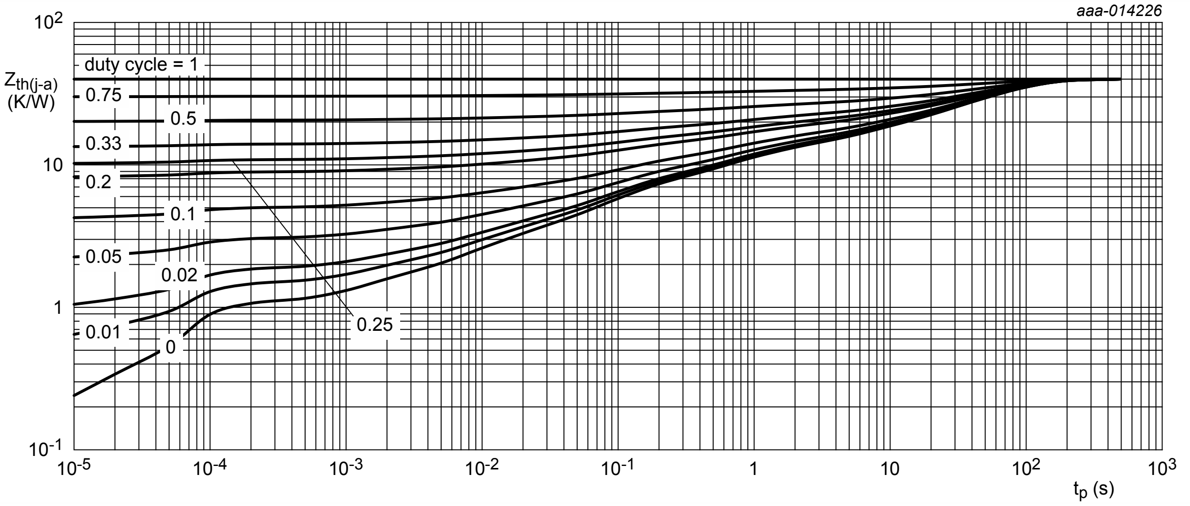
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 6 cm^2.

[3] Device mounted on an ceramic Printed-Circuit Board (PCB), Al_2O_3, standard footprint.



FR4 PCB, standard footprint

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 6 cm^2

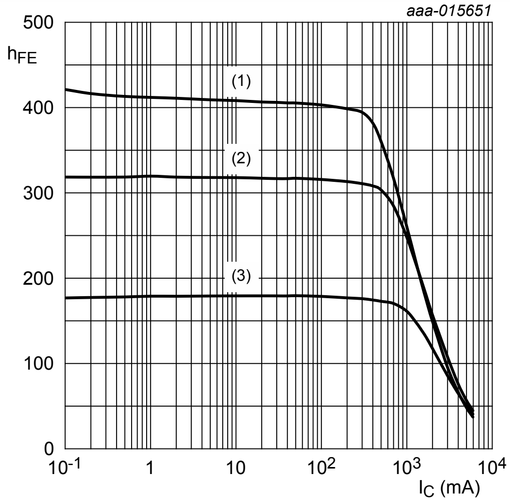
Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = 80 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
		V_{CB} = 80 V; I_E = 0 A; T_j = 150 °C		-	-	50	µA
I_{CES}	collector-emitter cut-off current	V_{CE} = 80 V; V_{BE} = 0 V; T_{amb} = 25 °C		-	-	100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 7 V; I_C = 0 A; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 2 V; I_C = 500 mA; T_{amb} = 25 °C		140	260	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{CE} = 2 V; I_C = 1 A; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		120	210	-	
		V_{CE} = 2 V; I_C = 3 A; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		50	90	-	
		V_{CE} = 2 V; I_C = 6 A; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C; pulsed		25	40	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 50 mA; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C; pulsed		-	45	65	mV
		I_C = 3 A; I_B = 300 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	100	150	mV
		I_C = 6 A; I_B = 600 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	210	340	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = 6 A; I_B = 600 mA; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C; pulsed		-	35	57	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = 1 A; I_B = 50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	0.85	1	V
		I_C = 3 A; I_B = 300 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	1.05	1.3	V
		I_C = 6 A; I_B = 600 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	1.1	1.3	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = 2 V; I_C = 500 mA; T_{amb} = 25 °C		-	0.7	0.9	V
t_d	delay time	V_{CC} = 12.5 V; I_C = 3 A; I_{Bon} = 150 mA; I_{Boff} = -150 mA; T_{amb} = 25 °C		-	10	-	ns
t_r	rise time			-	365	-	ns
t_{on}	turn-on time			-	375	-	ns
t_s	storage time			-	285	-	ns
t_f	fall time			-	385	-	ns
t_{off}	turn-off time			-	670	-	ns
f_T	transition frequency	V_{CE} = 10 V; I_C = 500 mA; f = 100 MHz; T_{amb} = 25 °C		-	170	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	22	-	pF



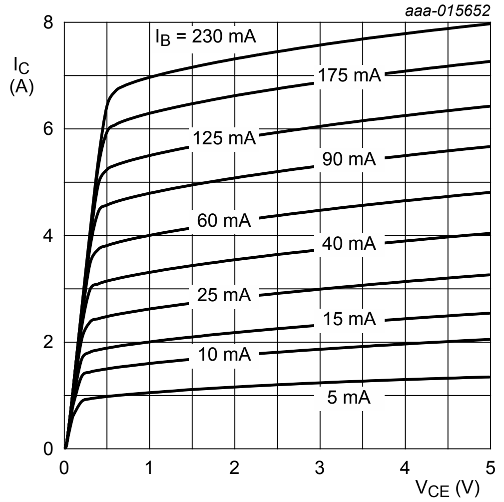
V_{CE} = 2 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

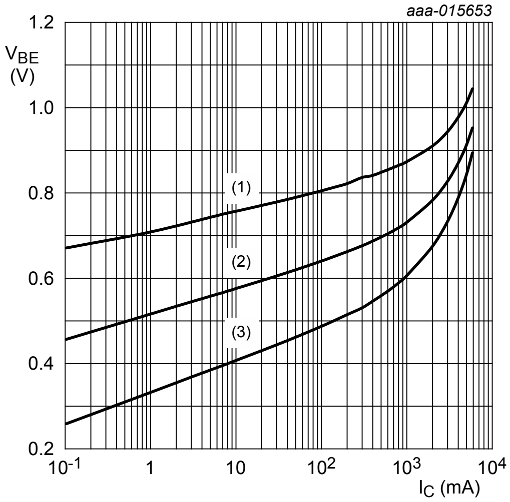
(3) T_{amb} = −55 °C

Fig. 4. DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig. 5. Collector current as a function of collector-emitter voltage; typical values



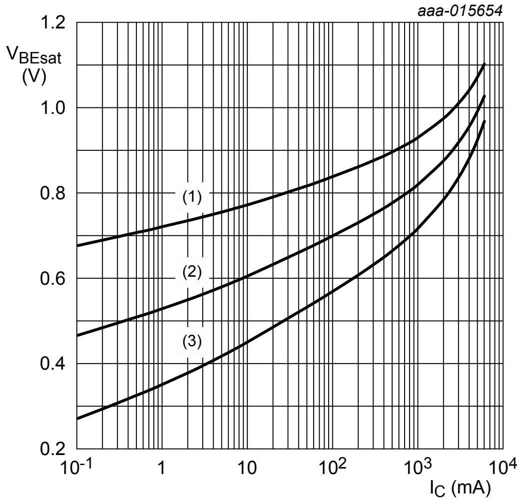
V_{CE} = 2 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig. 6. Base-emitter voltage as a function of collector current; typical values



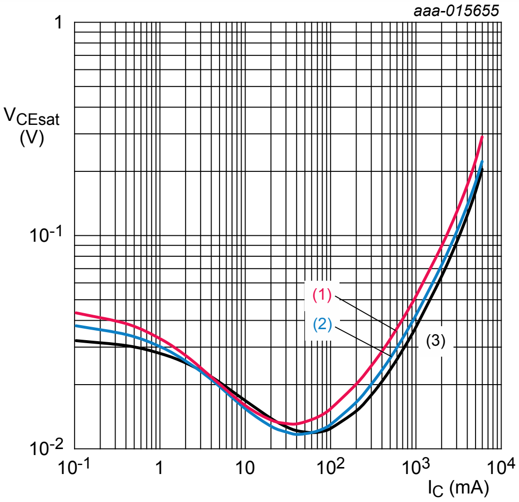
I_C/I_B = 20

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values



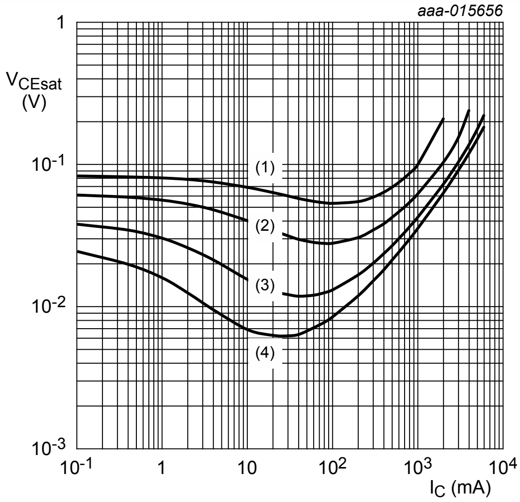
$I_C/I_B = 20$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values



T_{amb} = 25 °C

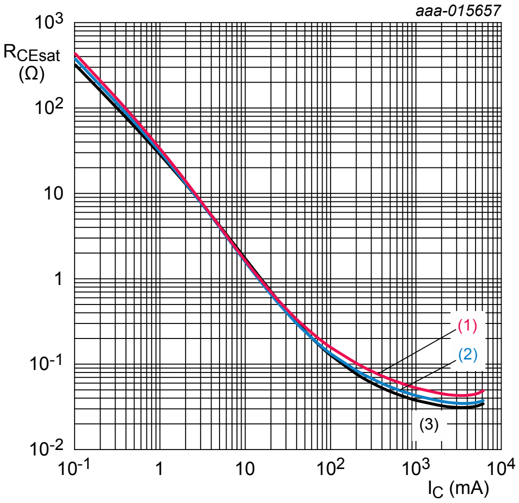
(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 20$

(4) $I_C/I_B = 10$

Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values



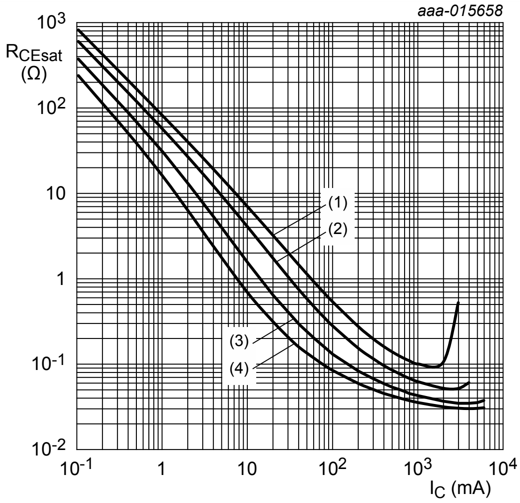
$I_C/I_B = 20$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 10. Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 20$

(4) $I_C/I_B = 10$

Fig. 11. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

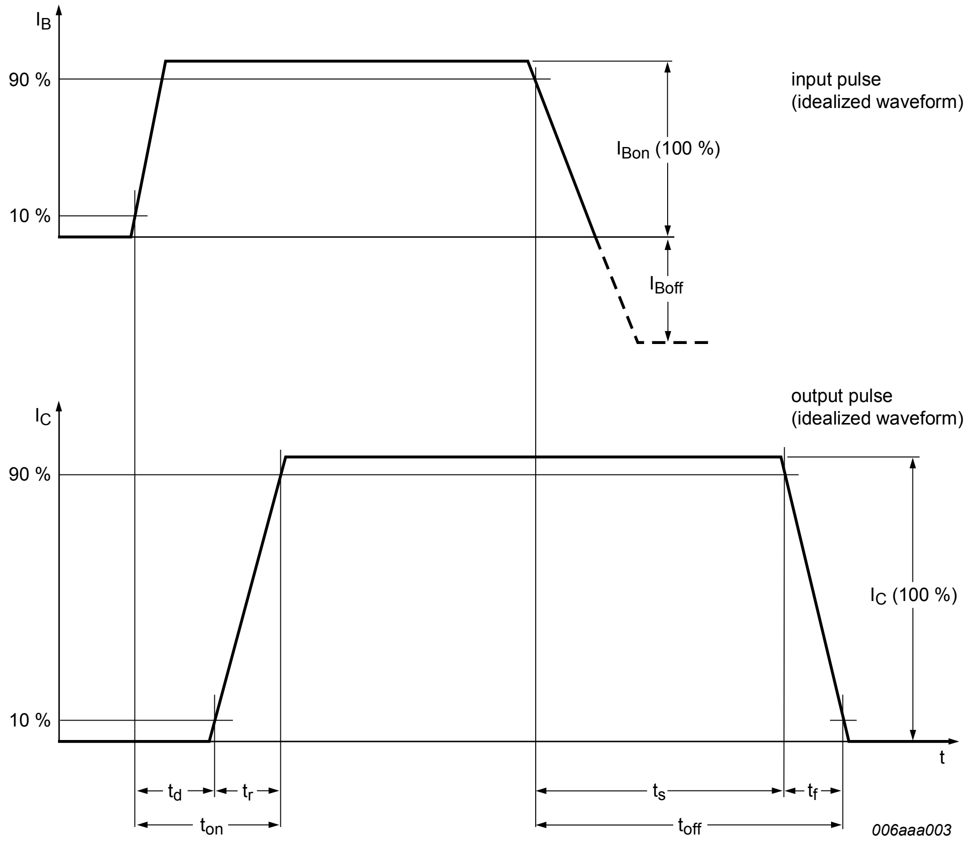


Fig. 12. BISS transistor switching time definition

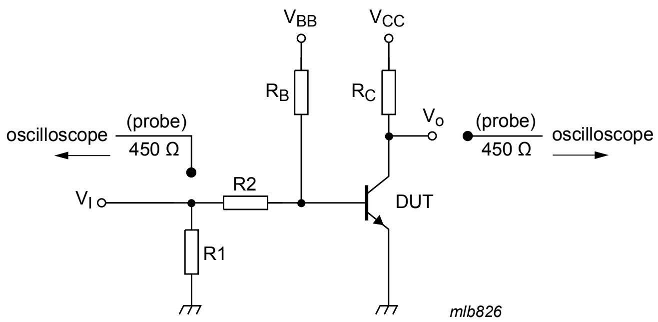


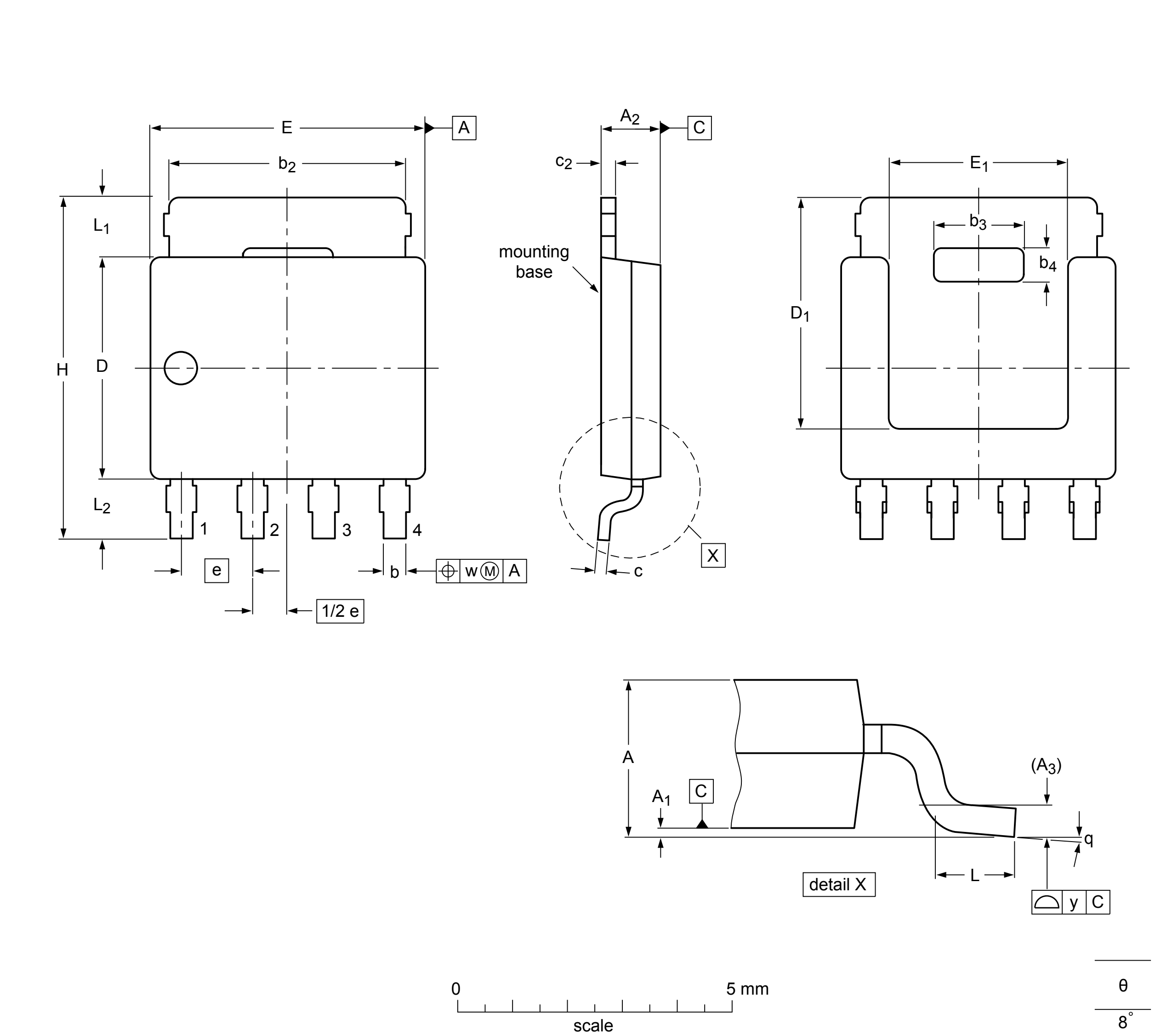
Fig. 13. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 14. Package outline LFPAK56; Power-SO8 (SOT669)

13. Soldering

Footprint information for reflow soldering **SOT669**

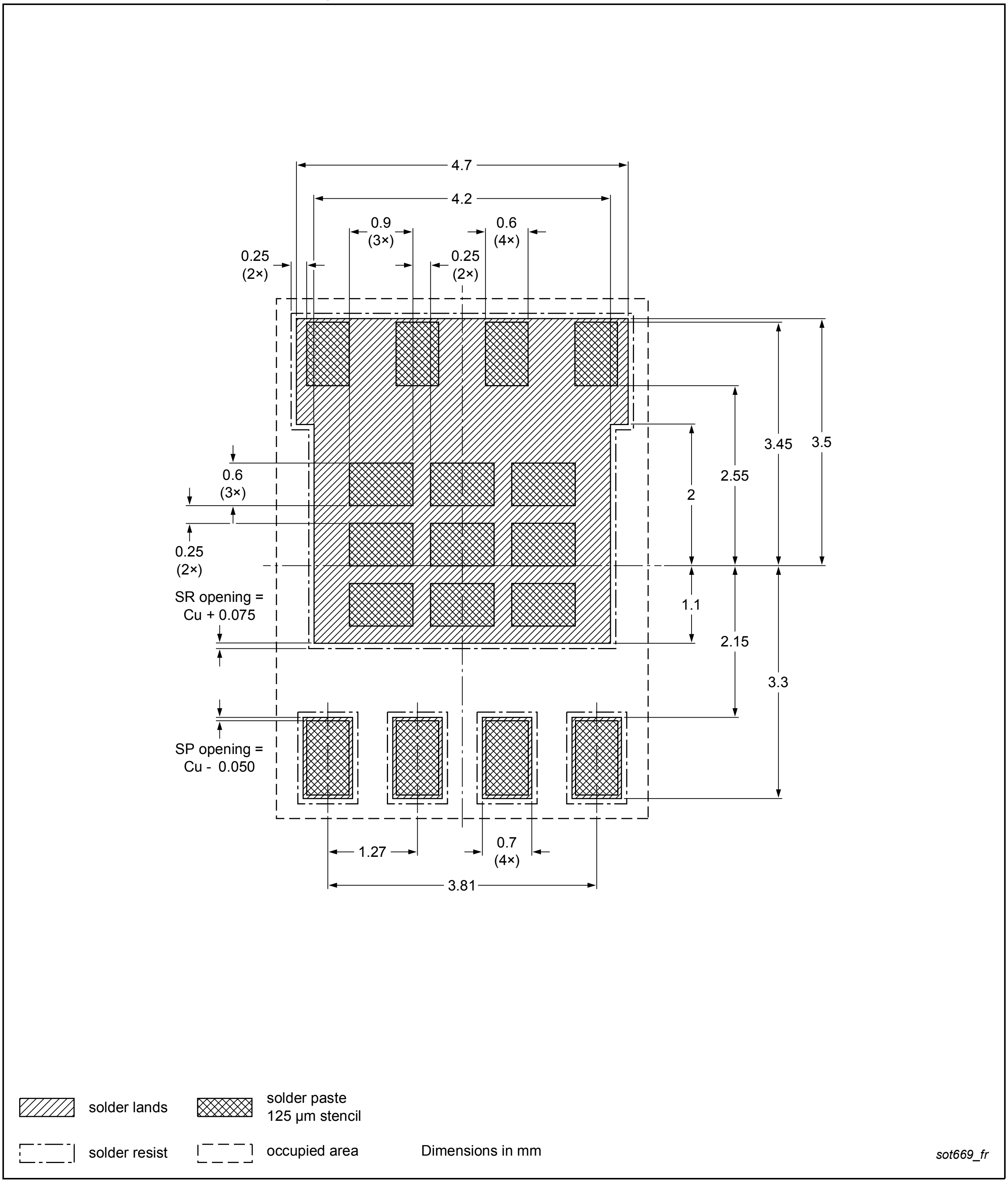


Fig. 15. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT61006NY v.1	20150126	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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16. Contents

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Date of release: 26 January 2015

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