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**FDMC86160**

# N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 43 A, 14 mΩ

## Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 14 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 9 \text{ A}$
- Max  $r_{DS(on)} = 23 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 7 \text{ A}$
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant



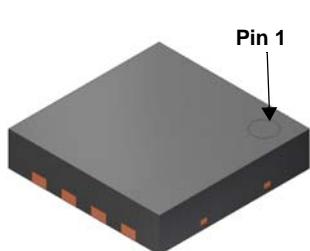
September 2014

## General Description

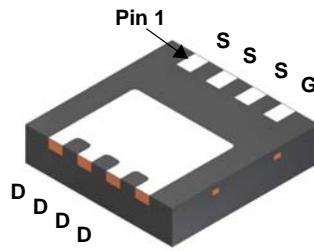
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance. This device is well suited for applications where ultra low  $R_{DS(on)}$  is required in small spaces such as High performance VRM, POL and orring functions.

## Applications

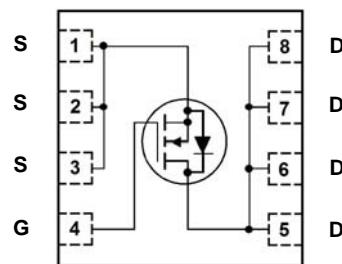
- Bridge Topologies
- Synchronous Rectifier



Top



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**MOSFET Maximum Ratings**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter			Ratings	Units	
$V_{DS}$	Drain to Source Voltage			100	V	
$V_{GS}$	Gate to Source Voltage			$\pm 20$	V	
$I_D$	Drain Current	-Continuous	$T_C = 25 \text{ }^\circ\text{C}$	43	A	
		-Continuous	$T_A = 25 \text{ }^\circ\text{C}$	(Note 1a)		
		-Pulsed		(Note 4)		
$E_{AS}$	Single Pulse Avalanche Energy			(Note 3)	181	
$P_D$	Power Dissipation			$T_C = 25 \text{ }^\circ\text{C}$	54	
	Power Dissipation			$T_A = 25 \text{ }^\circ\text{C}$	(Note 1a)	2.3
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range			-55 to +150	$^\circ\text{C}$	

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86160	FDMC86160	Power33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\Delta \text{BV}_{\text{DSS}}$ $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		73		$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2	2.9	4	V
$\Delta V_{GS(\text{th})}$ $\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-9		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 9 \text{ A}$		11.2	14	$\text{m}\Omega$
		$V_{GS} = 6 \text{ V}, I_D = 7 \text{ A}$		16	23	
		$V_{GS} = 10 \text{ V}, I_D = 9 \text{ A}, T_J = 125^\circ\text{C}$		21	26	
$g_{\text{FS}}$	Forward Transconductance	$V_{DD} = 10 \text{ V}, I_D = 9 \text{ A}$		43		S

### Dynamic Characteristics

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		968	1290	pF
$C_{\text{oss}}$	Output Capacitance			241	320	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			11	20	pF
$R_g$	Gate Resistance		0.1	0.6	2.5	$\Omega$

### Switching Characteristics

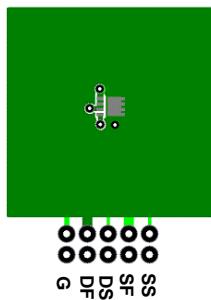
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 9 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		9.7	19	ns
$t_r$	Rise Time			3.6	10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time			16	30	ns
$t_f$	Fall Time			3.4	10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$		15	22	nC
	Total Gate Charge		$V_{DD} = 50 \text{ V}, I_D = 9 \text{ A}$	9.8	15	nC
$Q_{gs}$	Total Gate Charge			4.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.5		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 9 \text{ A}$	(Note 2)		0.79	1.3	V
		$V_{GS} = 0 \text{ V}, I_S = 1.9 \text{ A}$	(Note 2)		0.72	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$			47	75	ns
					45	73	nC
$Q_{rr}$	Reverse Recovery Charge						

Notes:

1.  $R_{\text{QJA}}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\text{QJC}}$  is guaranteed by design while  $R_{\text{QCA}}$  is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 181 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = 11 \text{ A}$ ,  $V_{DD} = 100 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ . 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 35 \text{ A}$ .

4. Pulse  $I_d$  refers to Figure 11 Forward Bias Safe Operation Area.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

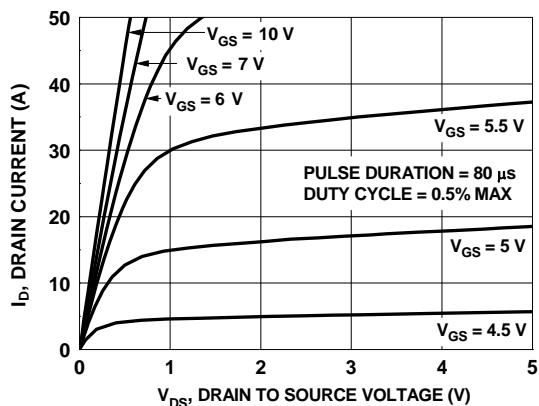


Figure 1. On-Region Characteristics

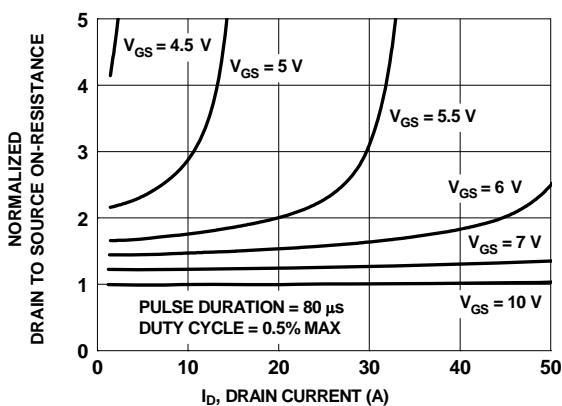


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

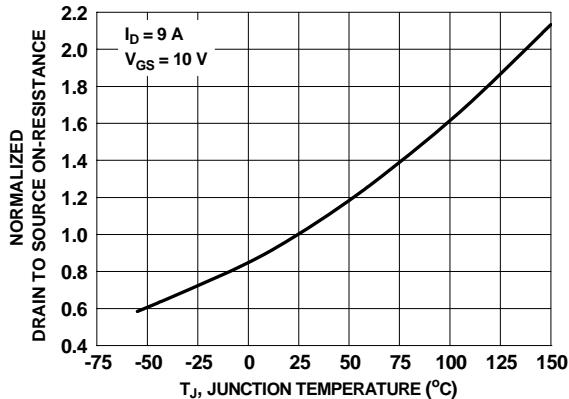


Figure 3. Normalized On-Resistance vs Junction Temperature

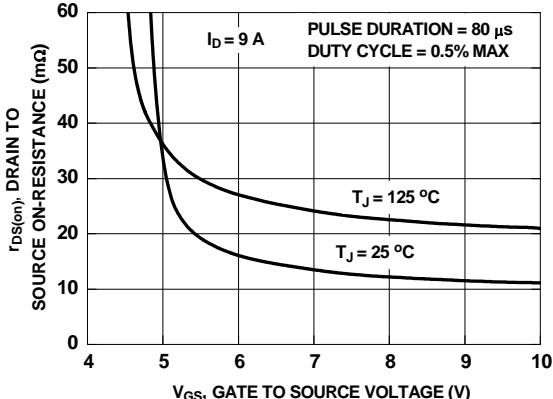


Figure 4. On-Resistance vs Gate to Source Voltage

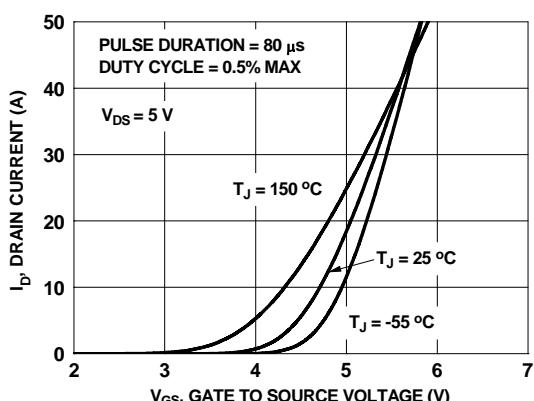


Figure 5. Transfer Characteristics

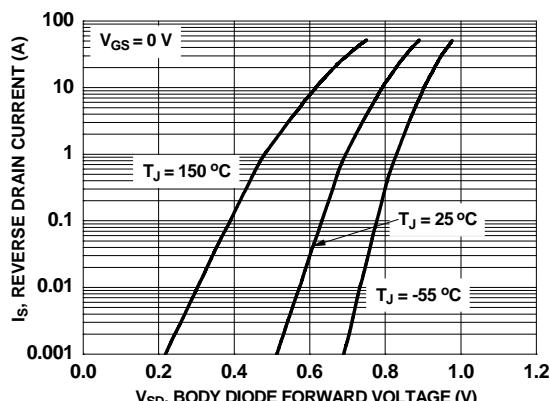


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

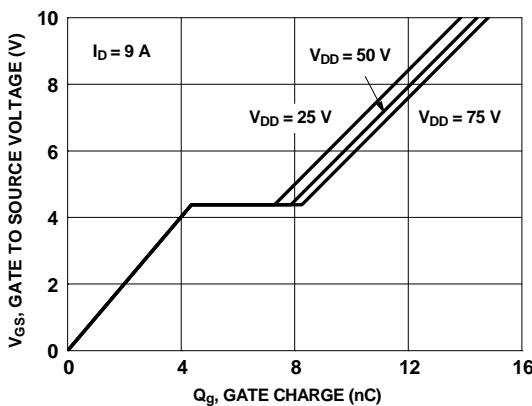


Figure 7. Gate Charge Characteristics

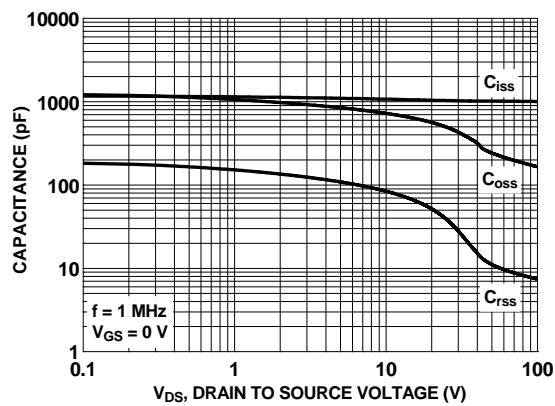


Figure 8. Capacitance vs Drain to Source Voltage

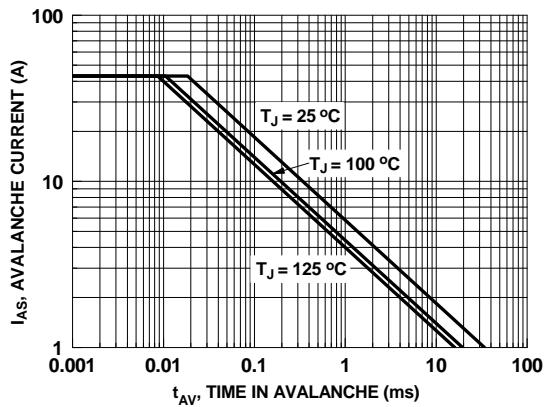


Figure 9. Unclamped Inductive Switching Capability

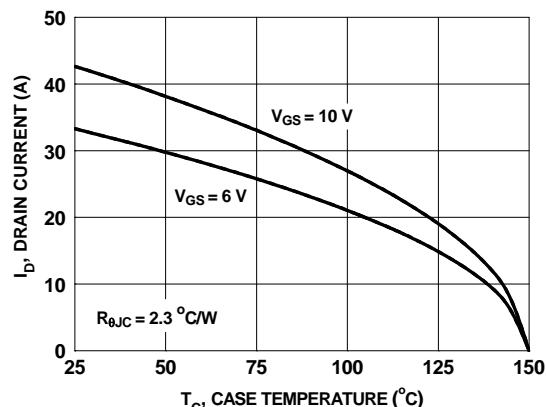


Figure 10. Maximum Continuous Drain Current vs Case Temperature

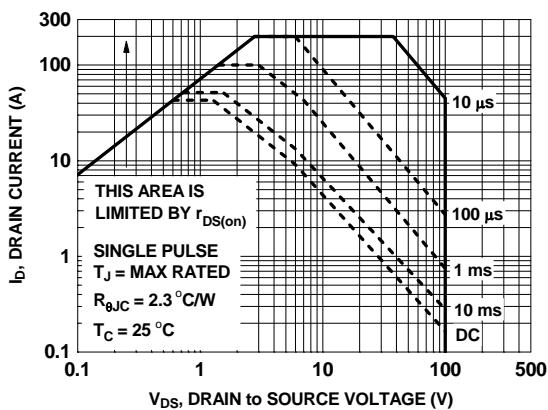


Figure 11. Forward Bias Safe Operating Area

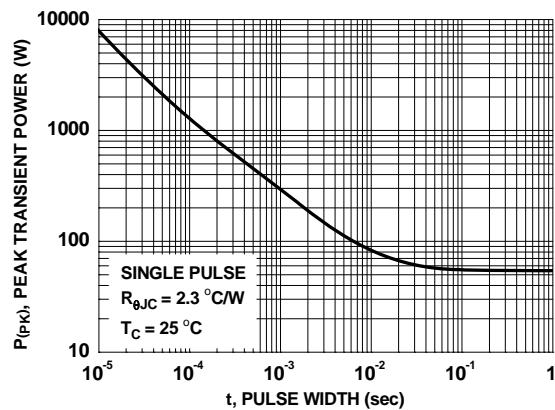


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

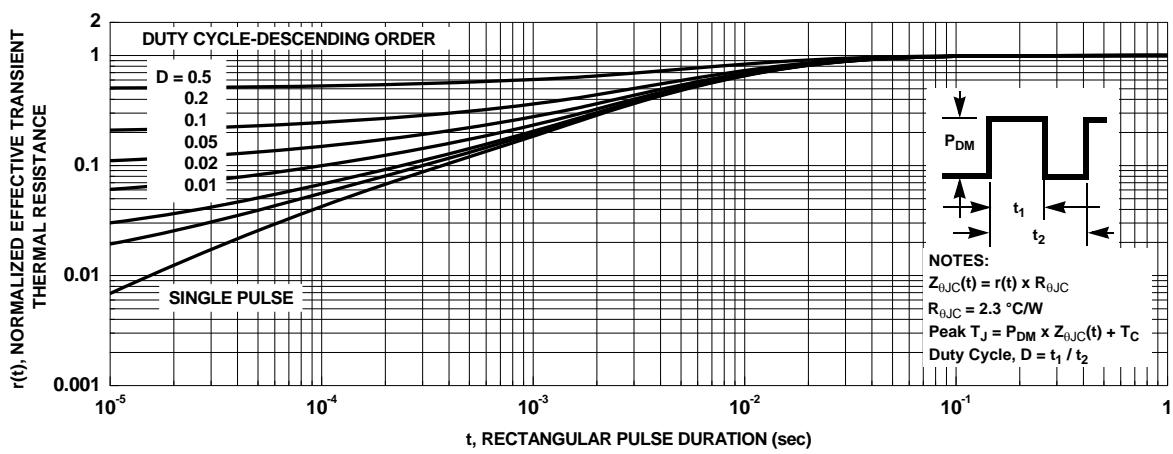


Figure 13. Junction-to-Case Transient Thermal Response Curve

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