

Devices Connected/Referenced	
ADN4663	Dual Channel LVDS Driver
ADN4664	Dual Channel LVDS Receiver
ADuM3442	Quad Channel Digital Isolator
ADuM5000	Isolated DC-to-DC Converter

Isolated LVDS Interface Circuit

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[CN-0256 Circuit Evaluation Board \(EVAL-CN0256-EBZ\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

Low voltage differential signaling (LVDS) is an established standard (TIA/EIA-644) for low power, high speed, point-to-point communication. It is used in instrumentation and control applications to send high volumes of data across backplanes or short cable links, or to distribute high speed clocks to different parts of an application circuit.

The circuit shown in Figure 1 demonstrates isolation of an LVDS interface. Advantages of isolating LVDS interfaces include protection against fault conditions (safety isolation) and improving robustness (functional isolation).

The [ADuM3442](#) provides digital isolation of the logic inputs to the [ADN4663](#) LVDS driver and the logic outputs from the [ADN4664](#) LVDS receiver. Together with provision of isolated power using the [ADuM5000](#), a number of challenges to isolating

LVDS links in industrial and instrumentation applications are met that include the following:

- Isolation of the logic signals to/from the LVDS drivers/receivers, ensuring standard LVDS communication on the bus side of the circuit.
- Highly integrated isolation using just two additional wide-body SOIC devices, the [ADuM3442](#) and [ADuM5000](#), to isolate the standard LVDS devices, the [ADN4663](#) and [ADN4664](#).
- Low power consumption compared to traditional isolation (opto-couplers). Low power operation is a feature of LVDS applications.
- Multiple channels of isolation. In LVDS applications, parallel channels are used to maximize data throughput. This circuit demonstrates quad-channel isolation (in this case, two transmit and two receive channels).
- High speed operation; the isolation can operate at up to 150 Mbps, facilitating basic LVDS speed requirements.

The circuit shown in Figure 1 isolates a dual-channel LVDS line driver and a dual-channel LVDS receiver. This allows demonstration of two complete transmit and receive paths on a single board.

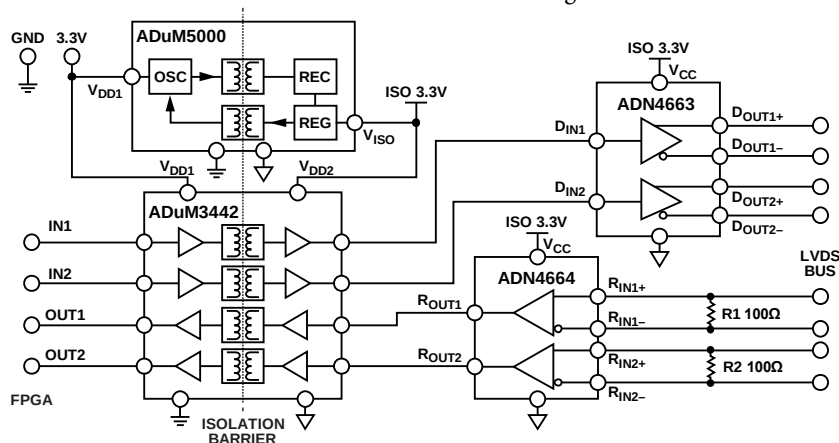


Figure 1. Isolated LVDS Interface Circuit (Simplified Schematic, All Connections Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

Applications of isolated LVDS are safety isolation and/or functional isolation of board-to-board, backplane, and printed circuit board (PCB) communication links. An example of safety isolation is a system with an LVDS backplane where one or more plug-in cards are at risk from high voltage transients. Isolating the LVDS interface ensures that such fault conditions do not affect other circuits in the system. An example of an application where functional isolation is beneficial is measurement equipment. Isolating LVDS links, for example, between an ADC and FPGA, can provide a floating ground plane to boost the integrity of measurement data, minimizing interference from the rest of the application.

Figure 2 shows a photo of the isolated LVDS interface circuit shown isolating two transmit communication channels (CMOS/TTL to LVDS) and two receive channels (LVDS to CMOS/TTL). The signals can be isolated at data rates up to 150 Mbps while maintaining the [ADuM3442](#) specification for maximum pulse width distortion.

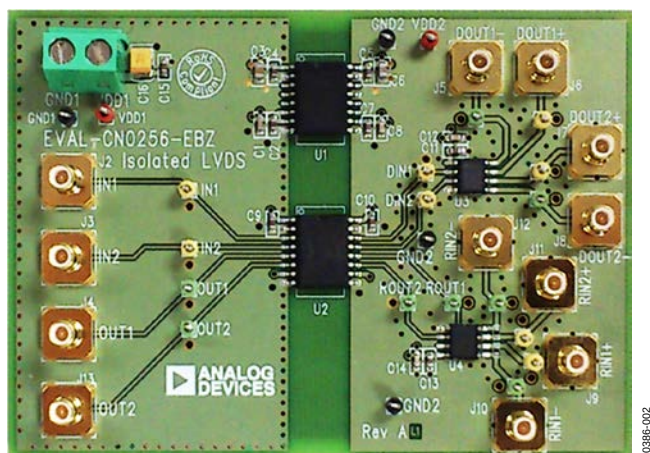


Figure 2. Isolated LVDS Interface Circuit

Logic signals can be applied to IN1 and IN2 and are isolated by the [ADuM3442](#). The corresponding outputs of the [ADuM3442](#) (the DIN1 and DIN2 test points) are connected to the [ADN4663](#) LVDS driver to create LVDS signals on DOUT1+, DOUT1– and DOUT2+, DOUT2–.

The [ADN4664](#) LVDS receiver can receive LVDS signals on RIN1+, RIN1– and RIN2+, RIN2–. The receiver outputs (the ROUT1, ROUT2 test points) are connected to the [ADuM3442](#) to isolate the signals. The corresponding logic outputs from the [ADuM3442](#) are OUT1 and OUT2.

The circuit is powered on the logic side by a connection to VDD1. This supply can be 3.3 V or 5 V and powers the logic side of the [ADuM3442](#) (the signal isolation for the circuit) and provides power to the [ADuM5000](#), which provides an isolated supply for the bus side of the circuit.

The V_{ISO} output of the [ADuM5000](#) provides the 3.3 V supply required for the LVDS driver ([ADN4663](#)) and LVDS receiver ([ADN4664](#)) as well as the bus side of the [ADuM3442](#).

Guidelines described in the [AN-0971](#) Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*, were used to generate the circuit layout. Additionally, the layout has been optimized for high speed differential signaling. The LVDS input/output traces are of matched length and have 50 Ω impedance to ground (100 Ω between differential pairs). Test points on each pair are also a matched distance from the driver/receiver. Multiple vias to ground are placed alongside the traces to improve signal integrity at high speeds.

Termination resistors (R1, R2) of 100 Ω are fitted on the LVDS inputs RIN1+, RIN1– and RIN2+, RIN2–. Terminate the receiving end of any bus connected to DOUT1+, DOUT1– and DOUT2+, DOUT1–.

Power and ground are connected via a screw-wire connector (VDD1 and GND1). Logic inputs (IN1, IN2)/outputs (OUT1, OUT2) are connected via four SMB connectors. The bus signals are similarly connected via eight SMB connectors. These connect to the LVDS driver ([ADN4663](#)) and receiver ([ADN4664](#)) on traces with impedances of 50 Ω to ground.

CIRCUIT EVALUATION AND TEST

To power the isolated LVDS interface circuit board, apply a 3.3 V or 5 V supply to VDD1. To test that the circuit is powered correctly, check the voltage level at the VDD2 test point. This test point is the isolated supply from the [ADuM5000](#) and should be 3.3 V or 5 V nominally.

A complete transmit and receive path can be tested by connecting the LVDS outputs for a channel to the LVDS inputs for a channel. As an example, to test Channel 1, connect DOUT1+ to RIN1+ and DOUT1– to RIN1– using SMB-to-SMB leads.

A signal or pattern generator can be connected to IN1, and the output at the OUT1 test point (or the OUT1 connector) must match the input. The test setup is shown in Figure 3.

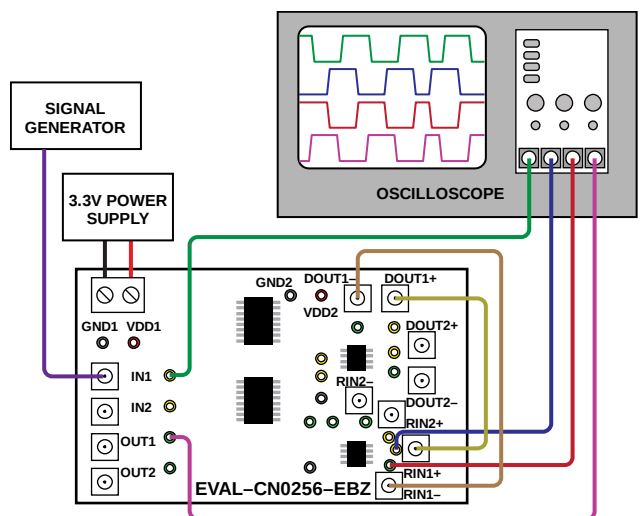


Figure 3. Transmit and Receive Channel 1 Test Setup

The oscilloscope plot in Figure 4 shows the waveforms for IN1, RIN1+, RIN1–, and OUT1 when this test is performed with a 50 Mbps clock signal on IN1 and 90 cm shielded leads between DIN1+ and RIN1+, and DIN1– and RIN1–.

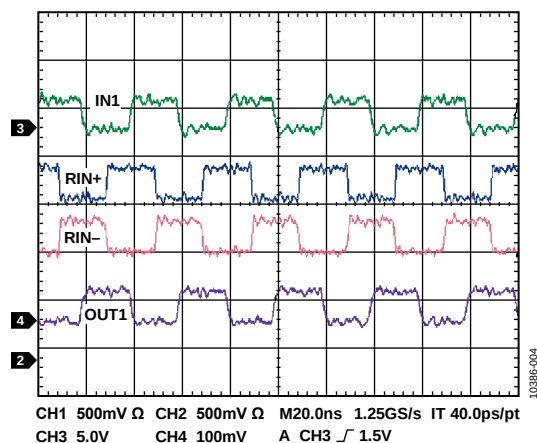


Figure 4. Oscilloscope Plot of IN1, RIN1+, RIN1– and OUT1 for 50 Mbps Signal

These measurements were taken with low capacitance probes on the LVDS bus (<1 pF). For higher data rates, use shorter wires between the LVDS outputs and inputs.

LEARN MORE

CN0256 Design Support Package:

<http://www.analog.com/CN0256-DesignSupport>.

Cantrell, Mark. Application Note AN-0971. Recommendations for Control of Radiated Emissions with isoPower Devices. Analog Devices.

Chen, Baoxing. iCoupler® Products with isoPower™ Technology: Signal and Power Transfer Across Isolation Barrier Using Microtransformers. Analog Devices, 2006.

Data Sheets and Evaluation Boards

[ADN4663 Data Sheet](#)

[ADN4664 Data Sheet](#)

[ADuM3442 Data Sheet](#)

[ADuM5000 Data Sheet](#)

REVISION HISTORY

7/12—Revision 0: Initial Version

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