



10 GHz LATCHED COMPARATOR WITH RSPECL OUTPUT STAGE

Typical Applications

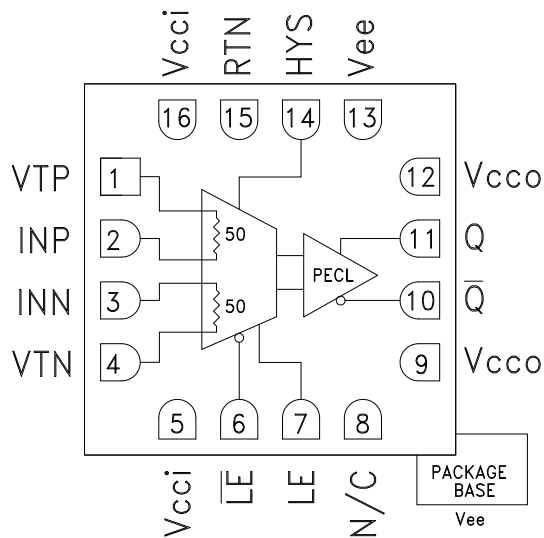
The HMC674LC3C is ideal for:

- ATE Applications
- High Speed Instrumentation
- Digital Receiver Systems
- Pulse Spectroscopy
- High Speed Trigger Circuits
- Clock & Data Restoration

Features

- Equivalent Input Bandwidth: 10 GHz
- Propagation Delay: 85 ps
- Overdrive & Slew Rate Dispersion: 10 ps
- Minimum Pulse Width: 60 ps
- Resistor Programmable Hysteresis
- Differential Latch Control
- Power Dissipation: 140 mW
- RSCML and RSECL Versions Available
- 16 Lead 3 x 3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC674LC3C is a SiGe monolithic, ultra fast comparator that features reduced swing (RS) PECL output drivers and latch inputs. The comparator supports 10 Gbps operation while providing 85 ps propagation delay and 60 ps minimum pulse width with 0.2 ps rms random jitter (RJ). Overdrive and slew rate dispersion are typically 10 ps, making the device ideal for a wide range of applications from ATE to broadband communications. The reduced swing PECL output stages are designed to directly drive 400 mV into 50 Ohms terminated to +1.3 V while maintaining compatibility with other PECL logic families. The HMC674LC3C features high speed latch and programmable hysteresis and may be configured to operate in either latch mode or as a tracking comparator.

Electrical Specifications, $T_A = +25\text{ }^\circ\text{C}$, $V_{ccI} = +3.3\text{ V}$, $V_{ccO} = +3.3\text{ V}$, $V_{ee} = -3\text{ V}$, $V_{TERM} = +1.3\text{ V}$

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|--------------------|-------|------|------|---------|
| Input Voltage Range | | -2 | | +2 | V |
| Input Differential Voltage | | -1.75 | | 1.75 | V |
| Input Offset Voltage | | | ±5 | | mV |
| Input Offset Voltage, Temperature Coefficient | | | 15 | | µV / °C |
| Input Bias Current | | | 15 | | µA |
| Input Bias Current Temperature Coefficient | | | 50 | | nA / °C |
| Input Offset Current | | | 4 | | µA |
| Input Impedance | | | 50 | | Ω |
| Common Mode Input Impedance | | | 350 | | KΩ |
| Differential Input Impedance | | | 15 | | KΩ |
| Active Gain | | | 48 | | dB |
| Common Mode Rejection Ratio | | | 80 | | dB |
| Hysteresis | $R_{hys} = \infty$ | | ±1 | | mV |

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824

Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com

Application Support: Phone: 978-250-3343 or apps@hittite.com


**10 GHz LATCHED COMPARATOR
WITH RSPECL OUTPUT STAGE**

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Latch Enable Characteristics

| Parameter | Conditions | Min. | Typ. | Max | Units |
|--|--------------|------|------|-----|------------|
| Latch Enable Input Impedance | Each Pin | | 8 | | K Ω |
| Latch to Output Delay, $t_{P\text{LOL}}$, $t_{P\text{LOH}}$ | VOD = 200 mV | | 85 | | ps |
| Latch Minimum Pulse Width, t_{PL} | VOD = 200 mV | | 20 | | ps |
| Latch Enable Input Range | VOD = 200 mV | 1.6 | | 2.4 | V |
| Latch Setup Time, t_{S} | VOD = 200 mV | | 45 | | ps |
| Latch Hold Time, t_{H} | | | -42 | | ps |

DC Output Characteristics, with 50 Ω to Vcco - 2 V

| Parameter | Conditions | Min. | Typ. | Max | Units |
|-----------------------------------|------------|------|------|------|-------|
| Output Voltage High Level, Voh | | 2.33 | 2.39 | 2.44 | V |
| Output Voltage Low Level, Vol | | 1.95 | 2.01 | 2.11 | V |
| Output Voltage Differential Swing | | 380 | 380 | 330 | mV |

AC Performance

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|--|------|------|-----|------------------------------|
| Propagation Delay - t_{PD} , t_{PDL} , t_{PDH} | VOD = 500 mV | 80 | 85 | 110 | ps |
| Propagation Delay, Temperature Coefficient | | | 0.45 | | ps / $^{\circ}\text{C}$ |
| Propagation Delay Skew (Rising to Falling Transition) | VOD = 500 mV | | 10 | | ps |
| VOD Dispersion | 50 mV < VOD < 1 V | | 10 | | ps |
| t_{PD} vs. Common Mode Dispersion, -1.75 V < Vcm < 1.75 V | VOD = 500 mV | | 8 | | ps |
| Noise (RTI) | | | 5.9 | | nV/ $\sqrt{(\text{Hz})}$ RTI |
| Equivalent Input Bandwidth ^[1] | | 8.6 | 9.3 | 12 | GHz |
| Deterministic Jitter (pp) | Deterministic Jitter at 10 Gbps with ± 100 mV Overdrive | | 2 | | ps |
| Random Jitter (rms) | Random Jitter at 10 Gbps with ± 100 mV Overdrive | | 0.2 | | ps rms |
| Input Signal Minimum Pulse Width | $V_{\text{CM}} = 0$; ± 100 mV Overdrive | | 60 | | ps |
| Q / QB Rise Time | From 20% to 80% | | 24 | | ps |
| Q / QB Fall Time | From 20% to 80% | | 15 | | ps |

Power Supply Requirements

| Parameter | Conditions | Min. | Typ. | Max | Units |
|-----------------------------|------------|------|------|-----|-------|
| Input Supply Current, IccI | | | 9 | | mA |
| Output Supply Current, Icco | | | 45 | | mA |
| Vee Current, Iee | | | 19 | | mA |
| Power Dissipation, Pd | | | 140 | | mW |
| PSRR, Vcci | | | 38 | | dB |
| PSRR, Vee | | | 38 | | dB |

Note 1: Equivalent Input Bandwidth is calculated with the following formula: $B_{\text{weq}} = 0.22/f$ (TRCOMP2-TRIN2) where TRIN is the 20%/80% transition time of a quasi-Gaussian signal applied to the comparator input, and TRCOMP is the effective transition time digitized by the comparator.

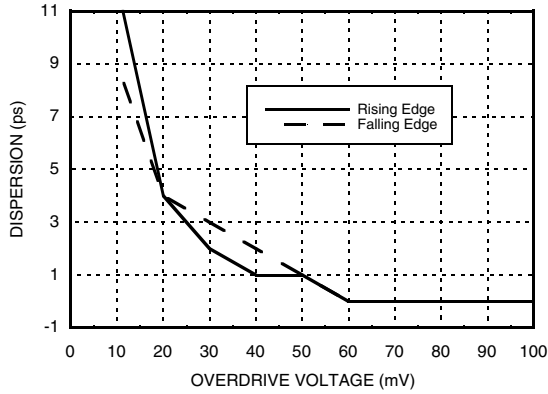


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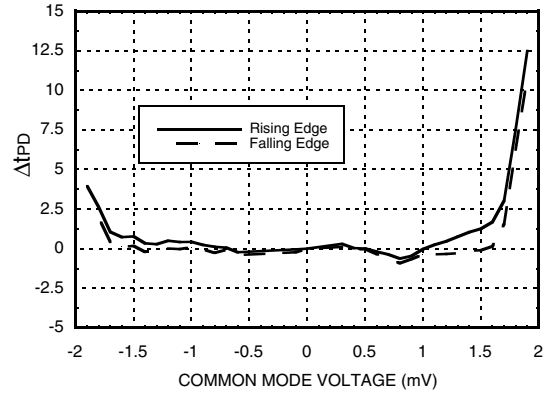
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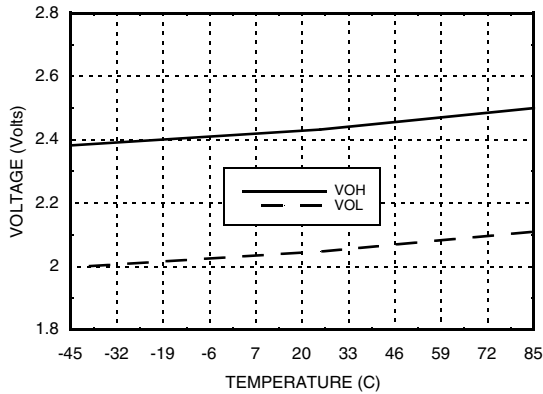
Dispersion vs. Overdrive Voltage



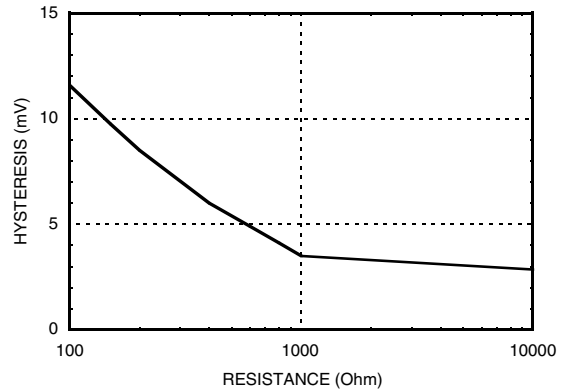
Propagation Delay vs. Common Mode



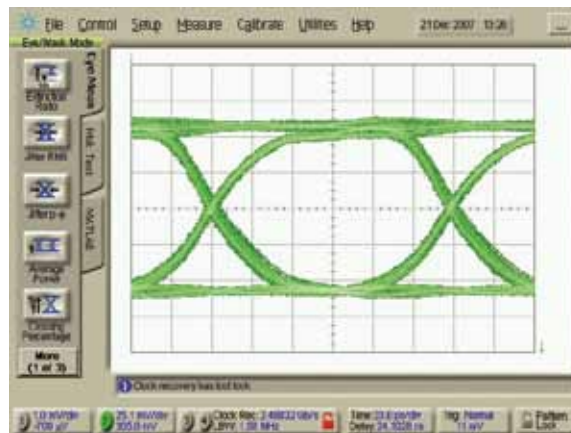
Output Voltage vs. Temperature



Comparator Hysteresis vs. Rhys Control Resistor

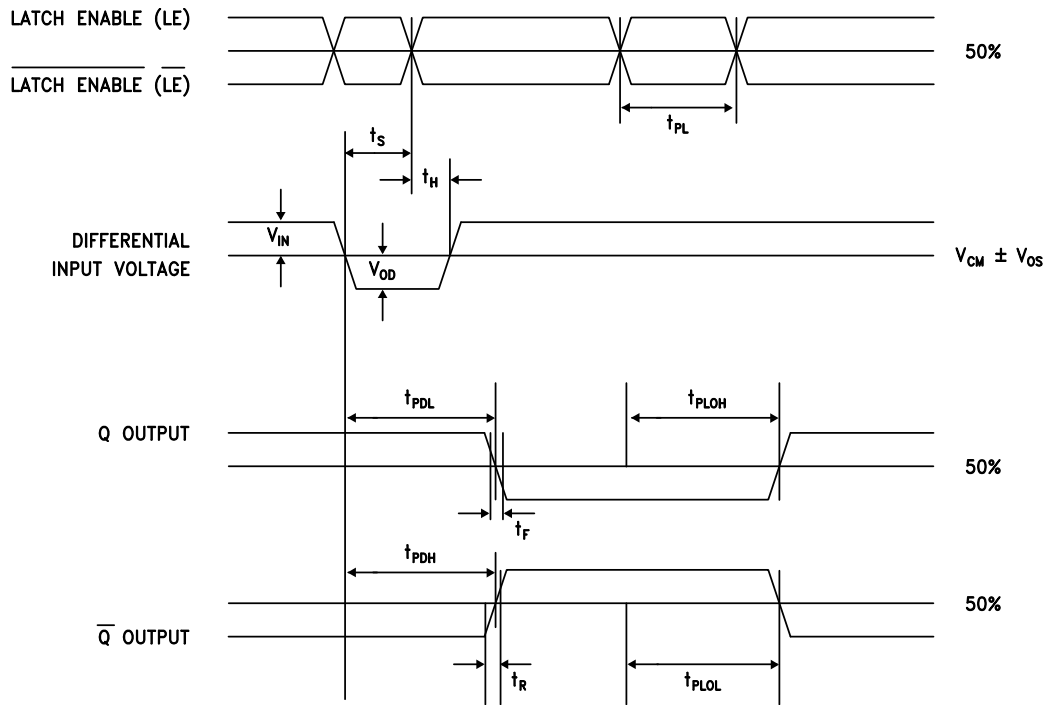


Eye Diagram



10 GHz LATCHED COMPARATOR WITH RSPECL OUTPUT STAGE

Timing Diagram



Timing Descriptions

| Symbol | Timing | Description |
|------------|-----------------------------------|---|
| t_{PDH} | Input to output high delay | Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output low-to-high transition. |
| t_{PDL} | Input to output low delay | Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output high-to-low transition. |
| t_{PLOH} | Latch enable to output high delay | Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition. |
| t_{PLOL} | Latch enable to output low delay | Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition. |
| t_H | Minimum hold time | Minimum time after the positive transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs. |
| t_{PL} | Minimum latch enable pulse width | Minimum time that the latch enable signal must be high to acquire an input signal change. |
| t_s | Minimum setup time | Minimum time before the positive transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs. |
| t_R | Output rise time | Amount of time required to transition from a low to a high output as measured at the 20% and 80% points. |
| t_F | Output fall time | Amount of time required to transition from a high to a low output as measured at the 20% and 80% points. |
| V_{OD} | Voltage overdrive | Difference between the input voltages V_{INP} and V_{INN} . |

**10 GHz LATCHED COMPARATOR
WITH RSPECL OUTPUT STAGE****1****COMPARATORS - SMT****Operational Description**

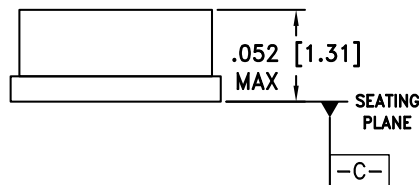
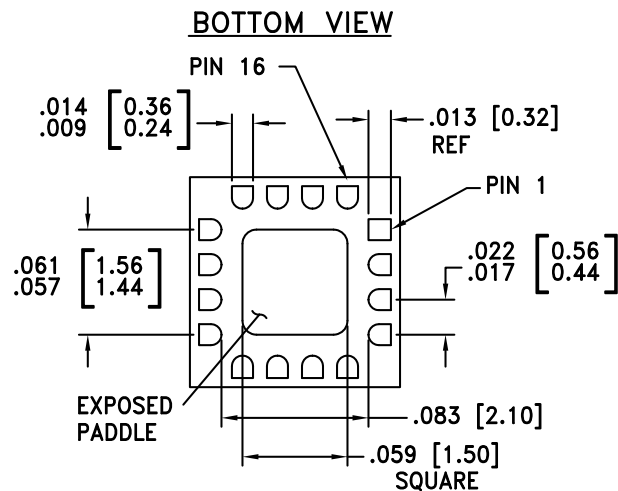
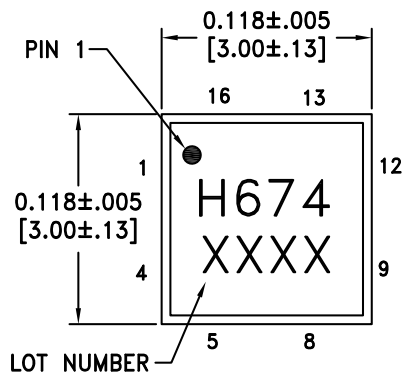
The HMC674LC3C is a Latched Comparator with 10 GHz equivalent input bandwidth. The device is comprised of three blocks: 1) An input amplifier, 2) A latch, and 3) An RSPECL Output Buffer. The latching circuit is level sensitive, and consists of a single high-speed latch. The HMC674LC3C comparator supports 10 Gb/s operation. The minimum input data latching pulse width is 60 ps.

The HMC674LC3C operates in either Track (Transparent) Mode, where the output follows the logical value of the input, or the Latch (Hold) Mode, where the output value is held to the logical value of the comparison result of the input just prior to (LE - LE_bar) going HI. Track Mode operation is selected by either 1) (LE - LE_bar) LO, or 2) LE and LE_bar inputs floating. Latch Mode is selected by (LE - LE_bar) HI. The input impedance of the LE and LE_bar inputs is 8 k ohms, but these inputs can be terminated with 50 ohm external resistors if desired.

When DC coupled, the clock inputs operate at an input common mode voltage of 2 V. In this case, any termination resistors would ideally be returned to 2 V. If the clock is AC coupled to the device, the input termination resistors can be returned to ground.


**10 GHz LATCHED COMPARATOR
WITH RSPECL OUTPUT STAGE**
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Absolute Maximum Ratings

| | |
|---|-----------------------------------|
| Input Supply Voltage (V _{cci} to GND) | -0.5 V to +4 V |
| Output Supply Voltage (V _{cco} to GND) | -0.5 V to +4 V |
| Positive Supply Voltage Differential (V _{cci} - V _{cco}) | -0.5 V to +3.3 V |
| Input Voltage | -2 V to +2 V |
| Differential Input Voltage | -2 V to +2 V |
| Input Voltage, Latch Enable | -0.5 V to V _{cci} +0.5 V |
| Applied Voltage (HYS) | V _{ee} to GND |
| Maximum Input Current | ±1 mA |
| Output Current | 40 mA |
| Junction Temperature | 125 °C |
| Continuous P _{diss} (T = 85°C) (Derate 20.4 mW/°C above 85°C) | 0.816 W |
| Thermal Resistance (R _{th}) (Junction to Lead) | 49 °C/W |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 °C to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**
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Outline Drawing

NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO V_{ee}.

10 GHz LATCHED COMPARATOR WITH RSPECL OUTPUT STAGE



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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|------------|-----------------|--|---------------------|
| 1 | VTP | Termination resistor return pin for Vp Input. | |
| 2 | INP | Non-Inverting analog input | |
| 3 | INN | Inverting analog input | |
| 4 | VTN | Termination resistor return pin for Vn input | |
| 5, 16 | Vcci | Positive supply voltage input stage. | |
| 6 | \overline{LE} | Latch enable bar input pin, inverting side. Refer to the Operational Description for more details. | |
| 7 | LE | Latch enable input pin, non-inverting side. Refer to the Operational Description for more details. | |
| 8 | N/C | Pin is not connected inside the package. Connect package pin to GND for improved noise. | |
| 9, 12 | Vcco | Positive supply voltage for the RSPECL output stage. | |
| 10 | \overline{Q} | Inverting output. Q bar is at logic low if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in compare mode. Refer to the Operational Description for more details. | |
| 11 | Q | Non-inverting output. Q is at logic high if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in compare mode. Refer to the Operational Description for more details.. | |
| 14 | HYS | Hysteresis Control pin. This pin should be left disconnected for zero hysteresis. Connect to vee with a resistor to add the desired amount of hysteresis. Refer to hysteresis graph to determine the correct sizing of Rhys hysteresis control resistor. | |
| 13 | Vee | Negative power supply, -3 V. | |
| 15 | RTN | Return for ESD protection. | |
| | Package Base | Exposed paddle must be connected to Vee. | |

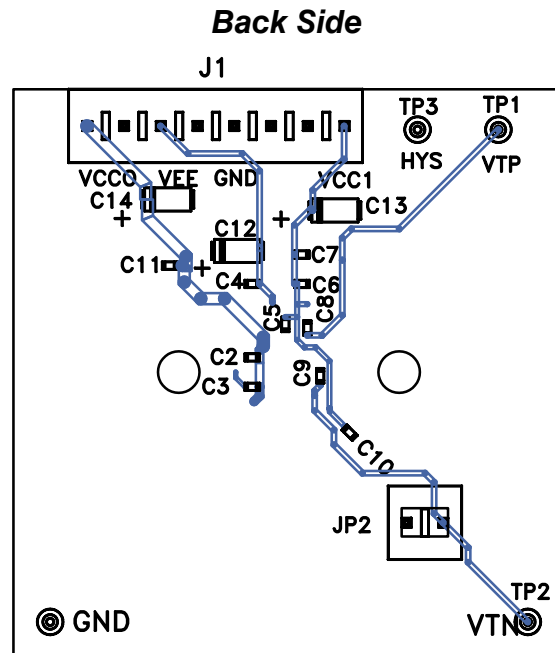
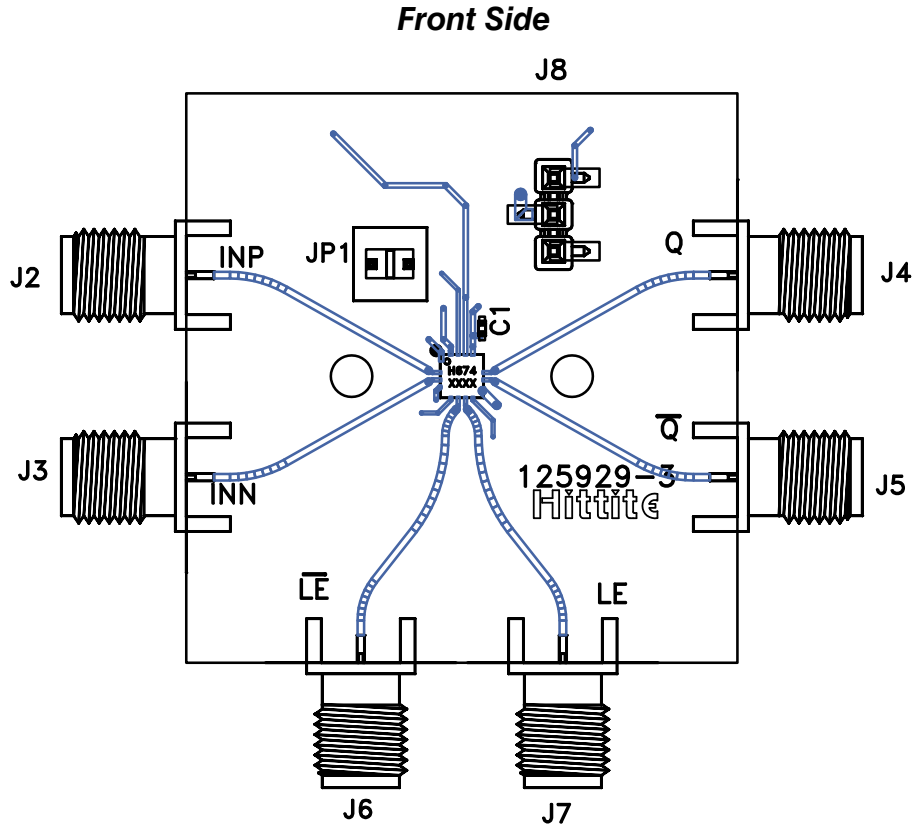
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Evaluation PCB

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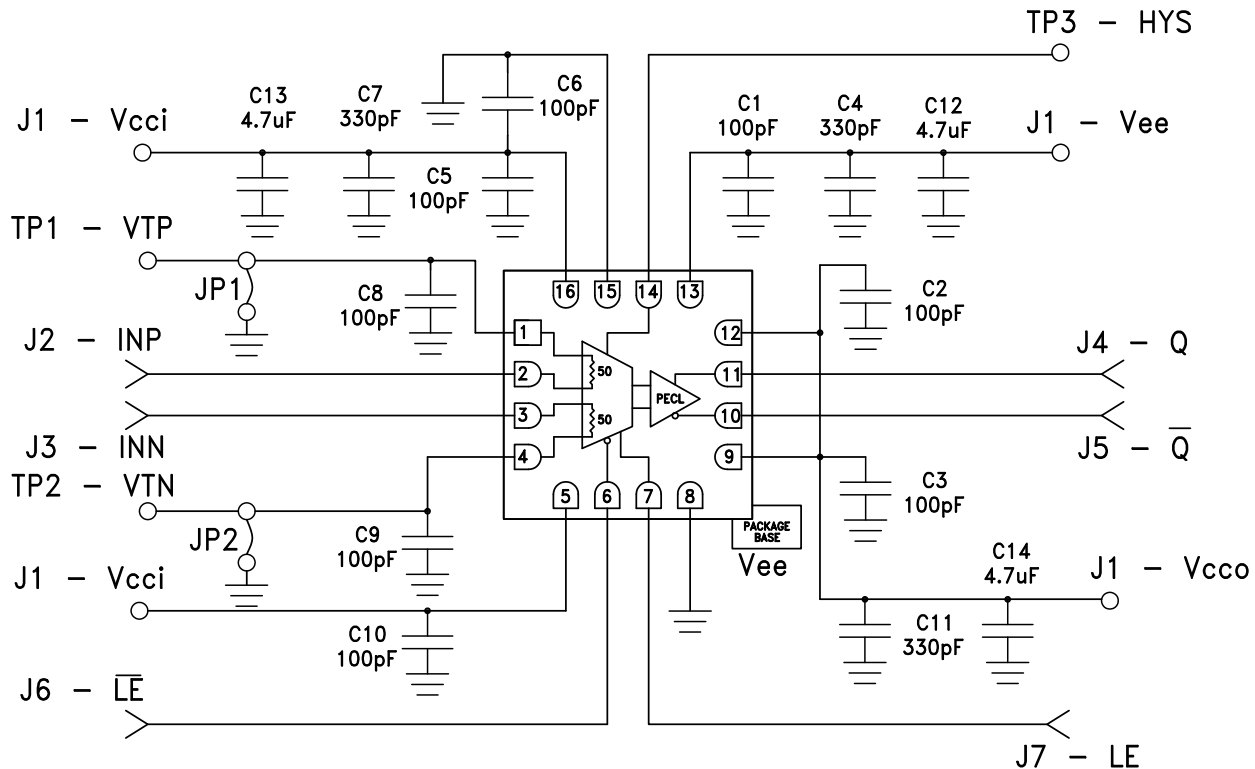
**10 GHz LATCHED COMPARATOR
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List of Materials for Evaluation PCB 125932 [1]

| Item | Description |
|---------------------------|--------------------------------------|
| J1 | 8 Pos. Vertical TIN |
| J2 - J7 | 2.92 mm 40 GHz Jack |
| J8 | Terminal Strip, Single Row 3 Pin SMT |
| JP1, JP2 | 2 Pos. Vertical TIN |
| C1 - C3, C5, C6, C8 - C10 | 100 pF Capacitor, 0402 Pkg. |
| C4, C7, C11 | 330 pF Capacitor, 0402 Pkg. |
| C11 - C13 | 4.7 uF Tantalum |
| TP1 - TP4 | DC Pin, Swage Mount |
| U1 | HMC674LC3C Comparator |
| PCB | 125929 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 10 GHz. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit




10 GHz LATCHED COMPARATOR WITH RSPECL OUTPUT STAGE

Notes:

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JONHON

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