Click here for production status of specific part numbers.

MAX5717/MAX5719

16 and 20-Bit Voltage DACs

General Description

The MAX5717 and MAX5719 are serial-input, unbuffered 16 and 20-bit voltage-output unipolar digital-to-analog converters (DACs) with integrated feedback resistors that allow bipolar operation when used with an external operational amplifier. These DACs provide low glitch energy, low noise, tight bipolar resistor matching, and high accuracy. The DACs feature 1LSB INL (max, MAX5717A) over the temperature range of -40°C to +105°C. Integrated precision setting resistors make the DACs easy to use. The MAX5717 and MAX5719 feature a 50MHz, 3-wire SPI™, QSPI™, MICROWIRE™, and DSP-compatible serial interface.

On power-up, the output resets to zero-scale, providing additional safety for applications which drive valves or other transducers that need to be off on power-up. The DAC output settles in 750ns and has a low offset and gain drift of ±0.1 ppm/°C of FSR.

The MAX5717 is functionally similar to the MAX542, but with significantly faster settling time. The MAX5719 provides a similar speed improvement as well as an increase in resolution to 20 bits.

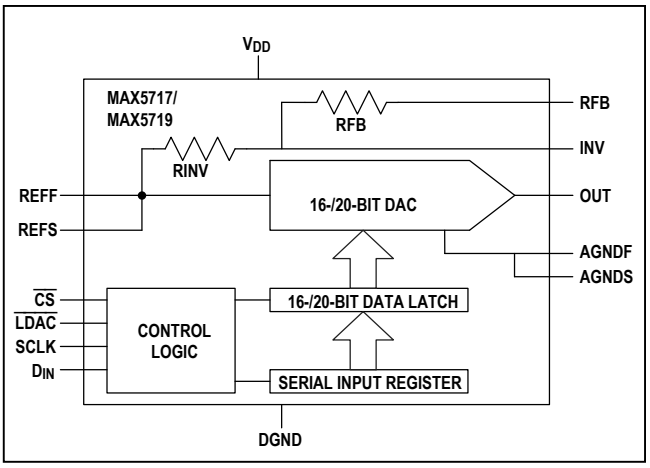
Applications

- Test and Measurement Equipment
- Automatic Test Equipment
- Gain and Offset Adjustment
- Data-Acquisition Systems
- Process Control and Servo Loops
- Portable Instrumentation
- Programmable Voltage and Current sources
- Automatic Tuning
- Communication Systems

Benefits and Features

- 16 and 20-bit Resolution
- 1LSB INL (Max, 16-bit)
- ±0.5 LSB DNL (Max, MAX5717A)
- 750ns Settling Time (Typ)
- 0.05 nV-sec Glitch Energy
- 6 nv/√Hz Output Noise Density
- Integrated ±0.025% (max) Bipolar Setting Resistors
- 4.5V to 5.5V Supply Range
- 4.0V to V_{DD} Reference Input Range
- Safe Power-Up Reset-to-Zero-Scale DAC Output (Unipolar)
- 50MHz 3-Wire SPI Interface
- -40°C to +105°C Operating Temperature Range.
- SO-14 Package

Simplified Block Diagram



***Ordering Information* appears at end of data sheet.**

maxim integrated™

Absolute Maximum Ratings

V_{DD} to DGND .....-0.3V to +6V
$\overline{CS}$, SCLK, D_{IN}, $\overline{LDAC}$
to DGND ..... -0.3V to Lesser of V_{DD} + 0.3 and 6V
REFF, REFS to AGND .....-0.3V to Lesser of V_{DD}+0.3 and 6V
AGNDF, AGNDS to DGND .....-0.3V to +0.3V
OUT, INV, to AGND,
DGND .....-0.3V to Lesser of V_{DD}+0.3 and 6V
RFB to AGND, DGND .....-6V to +6V
Maximum Current into Any Pin..... -100mA to +100mA
Continuous Power Dissipation
(T_A = +70°C, derate 8.33mW/°C above +70°C.).....667mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Thermal Resistance, Single-Layer Board
Junction-to-Ambient (θ_{JA}).....120°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W
Thermal Resistance, Four-Layer Board
Junction-to-Ambient (θ_{JA}).....84°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....34°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.5V to 5.5V, AGND, DGND, AGNDF, AGNDS = 0V, V_{REF} = V_{REFF} = V_{REFS} = 4.096V, $\overline{LDAC}$ = 0V, C_L=10pF, R_L= No Load, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE – ANALOG						
Resolution	N	MAX5717	16			Bits
		MAX5719	20			
Integral Nonlinearity	INL	MAX5717. Measured by a line passing through D_{IN} = 0 and (2^{16} – 1).	-4	±0.25	+4	LSB (16-bit)
		MAX5717A. Measured by a line passing through DIN = 0 and (2^{16} - 1).	-1	±0.25	+1	LSB (16-bit)
		MAX5719. Measured by a line passing through D_{IN} = 0 and (2^{20} – 1).	-64.0	±1	+64.0	LSB (20-bit)
		MAX5719A. Measured by a line passing through DIN = 0 and (2^{20} - 1).	-20	±1	+20	LSB (20-bit)
Differential Nonlinearity	DNL	MAX5717	-0.5	±0.125	+0.5	LSB (16-bit)
		MAX5719	-2.0	±1	+2.0	LSB (20-bit)
Zero-Code Offset Error		Code = 0, MAX5717	-2	±0.125	+2	LSB (16-bit)
		Code = 0, MAX5719	-32	±2	+32	LSB (20-bit)
Zero-Code Temperature Coefficient				±0.2		µV/°C
Gain Error		Code = full scale	-0.003		+0.003	%

Electrical Characteristics (continued)

(V_{DD} = 4.5V to 5.5V, AGND, DGND, AGNDF, AGNDS = 0V, V_{REF} = V_{REFF} = V_{REFS} = 4.096V, $\overline{LDAC}$ = 0V, C_L=10pF, R_L= No Load, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Error Temperature Coefficient				±0.1		ppm/°C
Output Voltage Range		No load	AGND		V_{REF}	V
Output Resistance	R_{OUT}			2		kΩ
Bipolar Resistor Ratio		R_{FB}/R_{INV}		1		Ω/Ω
Bipolar Resistor Ratio Error		R_{FB}/R_{INV} - 1	-0.025		+0.025	%
Bipolar Zero Offset Error		MAX5717		±5		LSB (16-bit)
		MAX5719		±80		LSB (20-bit)
Bipolar Zero Temperature Coefficient				±4		µV/°C
REFERENCE INPUT						
Reference Input Voltage Range			4		V_{DD}	V
Reference Input Resistance	RREF		2	3.9	6	kΩ
Reference Input Capacitance		Code = 0		75		pF
		Code = full scale		120		
DYNAMIC PERFORMANCE - ANALOG						
Voltage Output Slew-Rate	SR	C_L = 10pF		100		V/µs
Settling Time		To ±1.0 LSB of FS step (16-bit), ±16 LSB (20-bit) from $\overline{CS}$ low to high, C_L = 10pF.		1.5		µs
		To ±1.0 LSB of FS step (16-bit), ±16 LSB (20-bit) from $\overline{LDAC}$ high to low, C_L = 10pF.		0.75		
DAC Glitch Impulse		Worst-case transition		0.05		nV-s
Digital Feedthrough		Code = 0000h; $\overline{CS}$ = V_{DD}, $\overline{LDAC}$ = 0; SCLK, DIN = 0 to V_{DD} levels.		1.0		nV-s
Output Voltage Spectral Noise Density		f_{SW} = 1kHz, code = midscale		6		nV/(Hz)$^{1/2}$
Output Voltage Noise LF		0.1Hz to 10Hz		1		μV_{p-p}
DYNAMIC PERFORMANCE - REFERENCE INPUT						
Reference -3 dB Bandwidth		Code = 3FFFFh		1		MHz
Reference Feedthrough		Code = 0000h, Ref = 100mV_{p-p} at 100kHz		1		mV p-p

Electrical Characteristics (continued)

(V_{DD} = 4.5V to 5.5V, AGND, DGND, AGNDF, AGNDS = 0V, V_{REF} = V_{REFF} = V_{REFS} = 4.096V, $\overline{LDAC}$ = 0V, C_L=10pF, R_L= No Load, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 5V.)

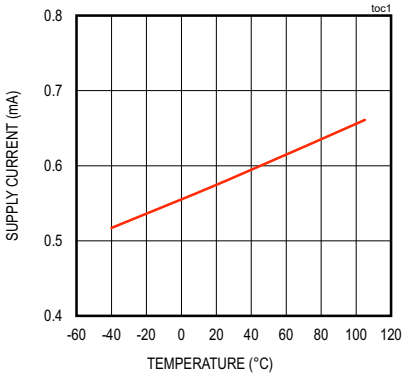
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	DIN = SCLK = $\overline{CS}$ = $\overline{LDAC}$ = V_{DD}		750	1050	µA
		When updating DAC, f_{SCLK} = 50MHz		7		mA
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7			V_{DD}
Input Low Voltage	V_{IL}				0.3	V_{DD}
Input Hysteresis				150		mV
Input Current	I_{IN}		-1	±0.1	+1	µA
Input Capacitance	C_{IN}			10		pF
TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCLK}		0		50	MHz
SCLK Period			20			ns
SCLK Pulse-Width High	t_{CH}	40% duty cycle.	8			ns
SCLK Pulse-Width Low	t_{CL}	40% duty cycle.	8			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSSO}	To first SCLK rising edge	8			ns
$\overline{CS}$ Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE	0			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 24th rising edge (MAX5719) or 16th rising edge (MAX5717).	8			ns
D_{IN} to SCLK Rise Setup Time	t_{DS}		5			ns
D_{IN} to SCLK Rise Hold Time	t_{DH}		4.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSPW}		20			ns
$\overline{LDAC}$ Pulse Width	t_{LDPW}		20			ns
$\overline{CS}$ High to $\overline{LDAC}$ Setup Time	t_{LDH}		20			ns
Last Active Clock Edge to Ready for DAC Output Update				1210	1500	ns

Note 1: Limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

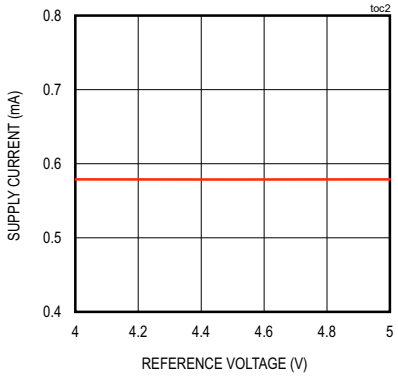
Typical Operating Characteristics

V_{DD} = 5V, V_{REF} = 4.096V, T_A = 25°C unless otherwise noted.

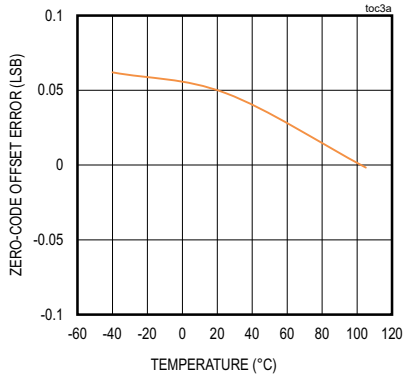
SUPPLY CURRENT vs. TEMPERATURE



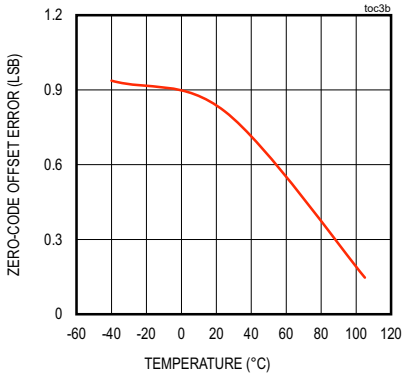
SUPPLY CURRENT vs. REFERENCE VOLTAGE



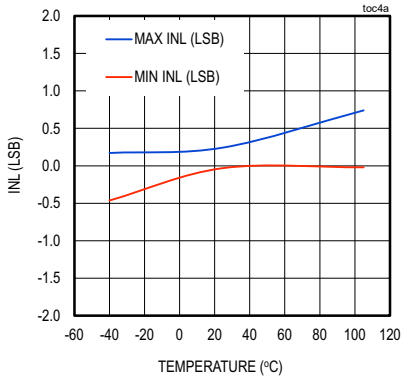
ZERO-CODE OFFSET ERROR vs. TEMPERATURE (MAX5717)



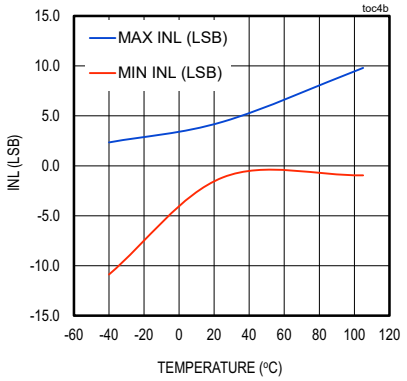
ZERO-CODE OFFSET ERROR vs. TEMPERATURE (MAX5719)



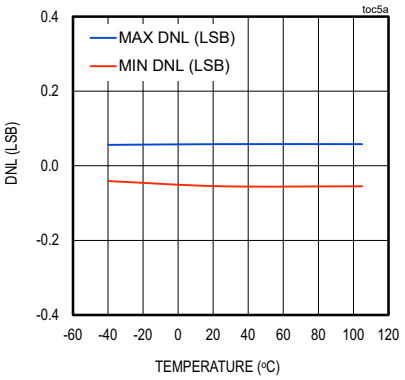
INL vs. TEMPERATURE (MAX5717)



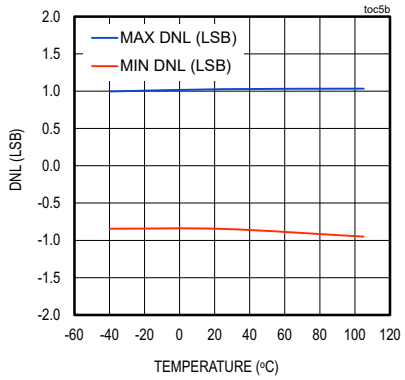
INL vs. TEMPERATURE (MAX5719)



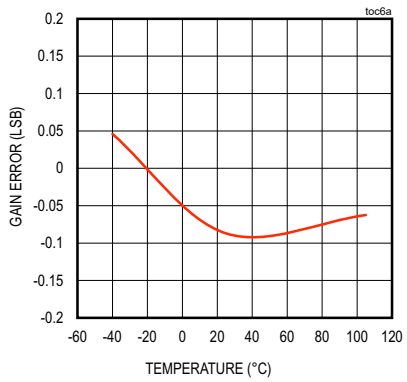
DNL vs. TEMPERATURE (MAX5717)



DNL vs. TEMPERATURE (MAX5719)



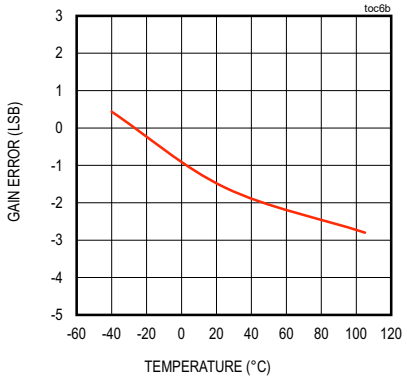
GAIN ERROR vs. TEMPERATURE (MAX5717)



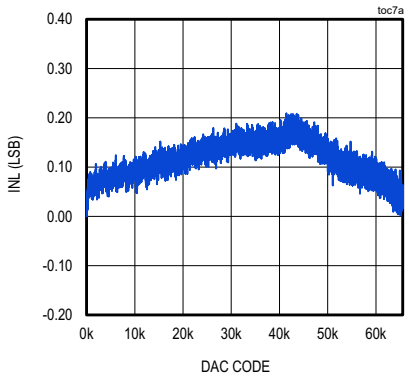
Typical Operating Characteristics (continued)

V_{DD} = 5V, V_{REF} = 4.096V, T_A = 25°C unless otherwise noted.

GAIN ERROR vs. TEMPERATURE (MAX5719)



INL vs. CODE (MAX5717)



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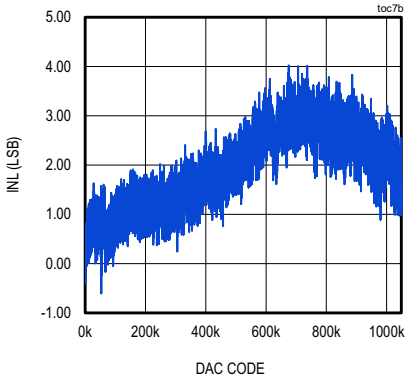
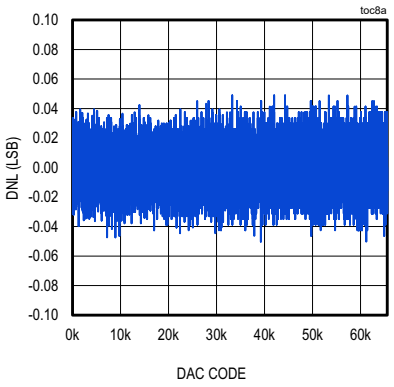
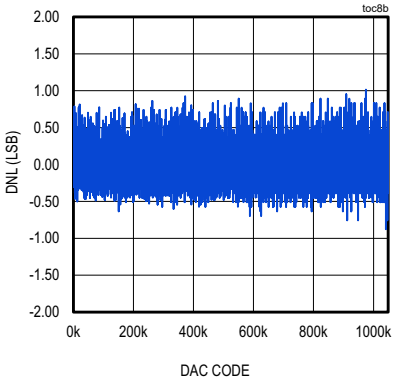


DNL vs. CODE (MAX5717)



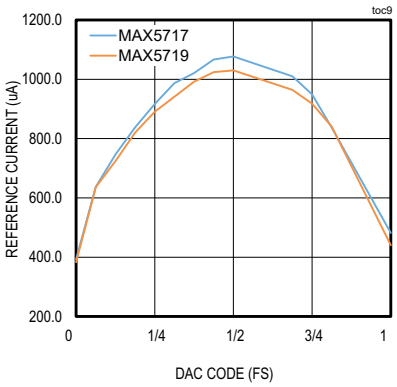
DNL vs. CODE (MAX5719)



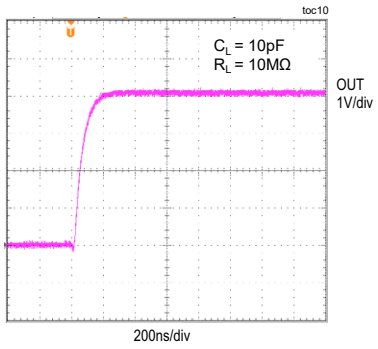
Typical Operating Characteristics (continued)

V_{DD} = 5V, V_{REF} = 4.096V, T_A = 25°C unless otherwise noted.

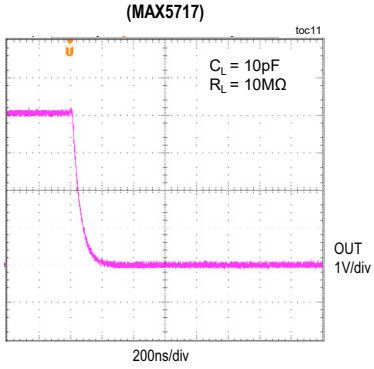
REFERENCE CURRENT vs. CODE



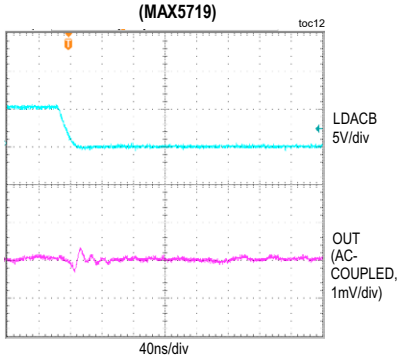
FULL-SCALE STEP RESPONSE (MAX5719)



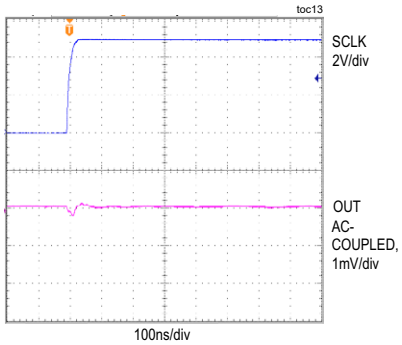
FULL-SCALE STEP RESPONSE (MAX5717)



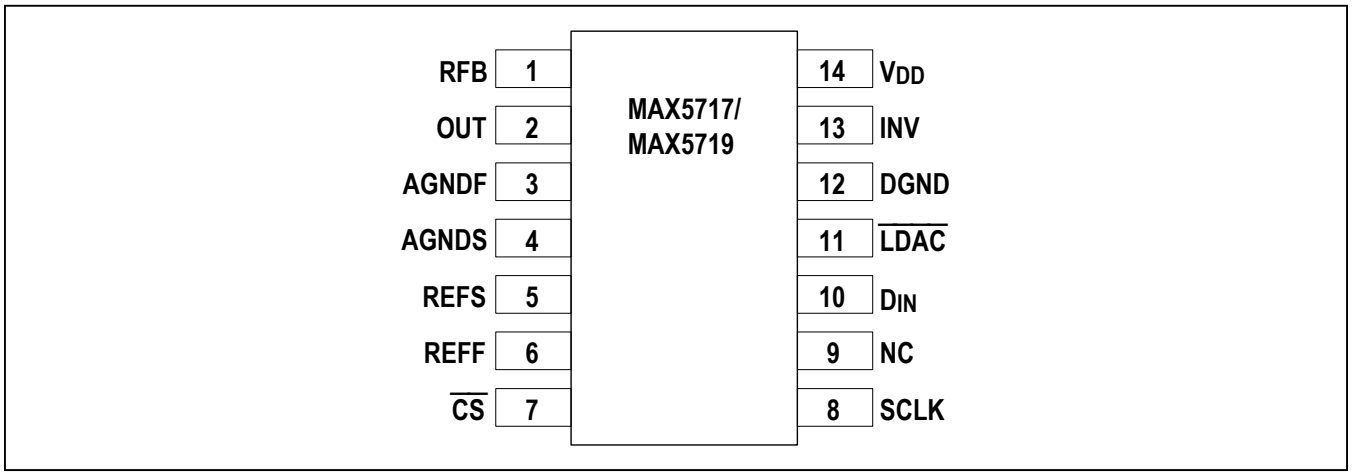
MAJOR CARRY OUTPUT GLITCH (MAX5719)



DIGITAL FEEDTHROUGH (MAX5719)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	TYPE
1	RFB	Feedback Resistor. Connect to external op amp's output in bipolar mode.	Analog
2	OUT	DAC Voltage Output	Analog
3	AGNDF	Analog Ground (Force)	Analog
4	AGNDS	Analog Ground (Sense)	Analog
5	REFS	Reference Input (Sense). Connect to external 4.096V reference sense.	Analog
6	REFF	Reference Input (Force). Connect to external +4.096V reference force output.	Analog
7	$\overline{CS}$	Active-Low Chip-Select Input	Digital
8	SCLK	Serial Clock Input. Rising edge triggered. Duty cycle must between 40% and 60%.	Digital
9	NC	Not Connected	
10	D_{IN}	SPI Bus Serial Data Input	Digital
11	$\overline{LDAC}$	LDAC Input. A falling edge updates the internal DAC latch.	Digital
12	DGND	Digital Ground	Power
13	INV	Junction of Internal Resistors. Connect to the inverting input of the external op amp in bipolar mode.	Analog
14	V_{DD}	Power Supply Input. Connect to a 5V supply.	Power

Detailed Description

The MAX5717 and MAX5719 are serial-input, unbuffered voltage output unipolar/bipolar digital-to-analog converters (DACs). These DACs provide low glitch energy, low noise, tight bipolar resistor matching, and high accuracy. The DACs feature 1LSB INL (max, MAX5717A) accuracy and are guaranteed monotonic over the temperature range of -40°C to +105°C. The offset and gai,n drift are low: ±0.1 ppm /°C of FSR. Integrated precision setting resistors make the DACs easy to use in bipolar-output configurations.

The low-resistance DAC resistor network provides two important advantages over DACs that have higher-resistance networks. First, the DAC's thermal noise, which is proportional to the square root of resistance, is lower than for higher-resistance DACs. Second, the DAC's settling time, which is directly proportional to the resistance, is lower than for other DACs. The DAC output settles in 750nS.

On power-up, the output resets to zero-scale (unipolar mode) providing additional safety for applications which drive valves or other transducers that need to be off on power-up. The MAX5717 and MAX5719 feature a 50MHz 3-wire SPI™, QSPI™, MICROWIRE™, and DSP-compatible serial interface.

Digital Inputs and Interface Logic

The digital interface is based on a 3-wire standard that is compatible with SPI, QSPI, and MICROWIRE interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC. $\overline{LDAC}$ updates the DAC output asynchronously. All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the DACs without additional external logic. The digital inputs are compatible with CMOS-logic levels.

SPI Interface

16-Bit Interface (MAX5717)

The 16-Bit Serial Interface Timing Diagram shows the operation of the SPI interface. SCLK rising edges clock in the data on the DIN input. The $\overline{CS}$ low interval frames the 16-cycle SPI instruction. Qualified operations will be executed in response to the rising edge of $\overline{CS}$. Operations consisting of less than 16 SCLK cycles will not be executed. Operations consisting of more than 16 SCLK cycles will be executed using the first two bytes of data available. In order to abort a command sequence, the rise of $\overline{CS}$ must precede the 16th rising edge of SCLK. $\overline{LDAC}$ allows the DACD latch to update asynchronously, by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high. Hold $\overline{LDAC}$ high during the data loading sequence.

Table 1. 16-Bit SPI Data Register

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DAC Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB

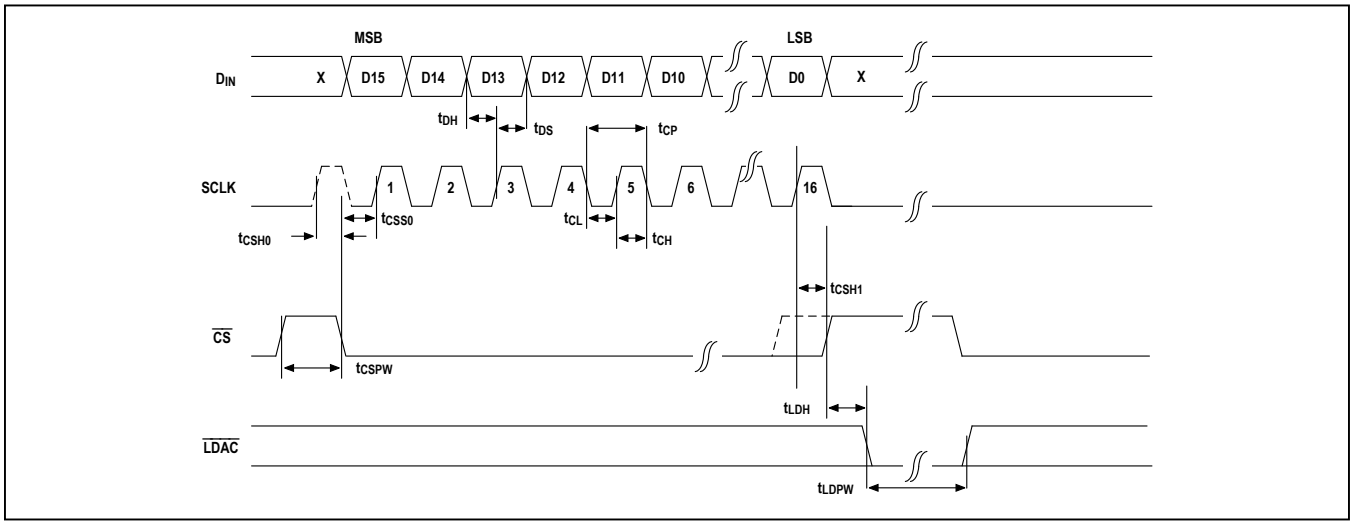


Figure 1. 16-Bit Serial Interface Timing Diagram

20-Bit Interface (MAX5719)

The 20-Bit Serial Interface Timing Diagram shows the operation of the SPI interface. SCLK rising edges clock in the data on the DIN input. The $\overline{CS}$ low interval frames the 24-cycle SPI instruction. Qualified operations will be executed in response to the rising edge of $\overline{CS}$. Operations consisting of less than 24 SCLK cycles will not be executed. Operations consisting of more than 24 SCLK cycles will be executed using the first 20 bits of data available. In order to abort a command sequence, the rise of $\overline{CS}$ must precede the 24th rising edge of SCLK. $\overline{LDAC}$ allows the DACD latch to update asynchronously, by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high. Hold $\overline{LDAC}$ high during the data loading sequence.

Throughput Rate

The throughput rate is dominated by the time required to load the DAC data and the time required for the internal calibration circuitry to operate (referred to as "digital latency"). At a 50MHz serial clock frequency, clocking the DAC data into the input register requires 20ns times the number of bits of resolution. Therefore, for a 20-bit DAC, the data is clocked into the register in 400ns. The digital latency is nominally 1210ns, with a maximum value of 1500ns. An additional 20ns is required for the $\overline{CS}$ minimum pulse width, for a total throughput period of 1.92µs, as shown in the figure below.

Table 2. 20-Bit SPI DAC Register Table

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
DAC Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC Data	D19 MSB	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB	X	X	X	X

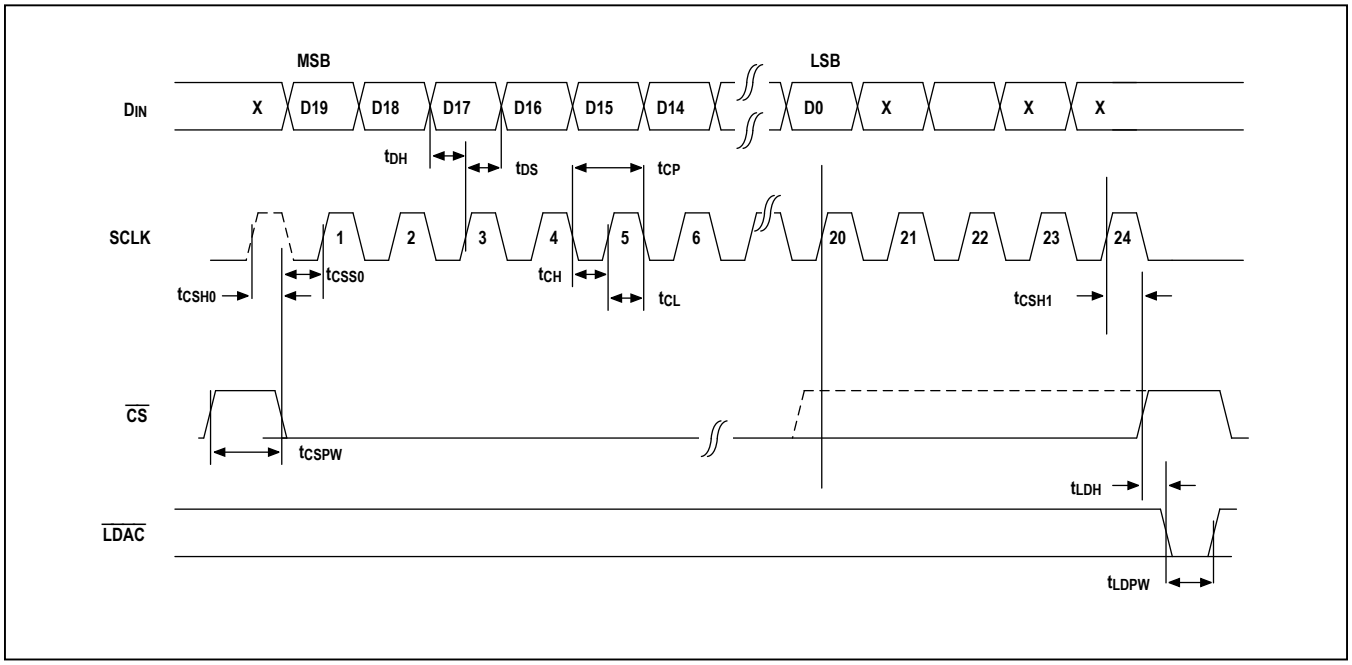


Figure 2. 20-Bit Serial Interface Timing Diagram

When the falling-edge of $\overline{LDAC}$ occurs after the digital latency period, the DAC output begins to change on the falling-edge of $\overline{LDAC}$. When the falling-edge of $\overline{LDAC}$ occurs before the end of the digital latency period, the DAC output begins to change at the end of the digital latency period. Settling time is approximately 750ns, which means that the DAC will settle to value (N - 1) at some point during the digital latency period for data (N). The DAC will begin to settle to value (N) on either the next falling-edge of $\overline{LDAC}$ (if $\overline{LDAC}$ goes low after the end of the digital latency period) or at the end of the next digital latency period (if $\overline{LDAC}$ goes low before the end of the digital latency period).

Power-On Reset

The internal power-on reset circuit sets the DAC's output to 0V in unipolar mode and $-V_{REF}$ in bipolar mode when V_{DD} is first applied. This ensures that unexpected DAC output voltages will not occur immediately following a system power-up, such as after a loss of power.

Applications Information

Reference And Analog Ground Inputs

Apply an external voltage reference between the 4.0V and V_{DD} to the reference inputs. The reference voltage determines the DAC's full-scale output voltage. Kelvin connections are provided for optimum performance.

Since these converters are designed as inverted R-2R voltage-mode DACs, the input resistance seen by the voltage reference is code-dependent. The worst-case input resistance variation is from 2KΩ to 15KΩ. The maximum change in load current for a 4.096V reference is approximately 2mA. Therefore, when using a voltage reference with 10ppm/mA load regulation, the reference voltage may change by around 20ppm across the full range of input codes. Therefore, a buffer amplifier should be used when the best INL performance is needed. In addition, the impedance of the path must be kept low because it contributes directly to the load regulation error. If separate force and sense lines are not used, tie the appropriate force and sense pins together, close to the package.

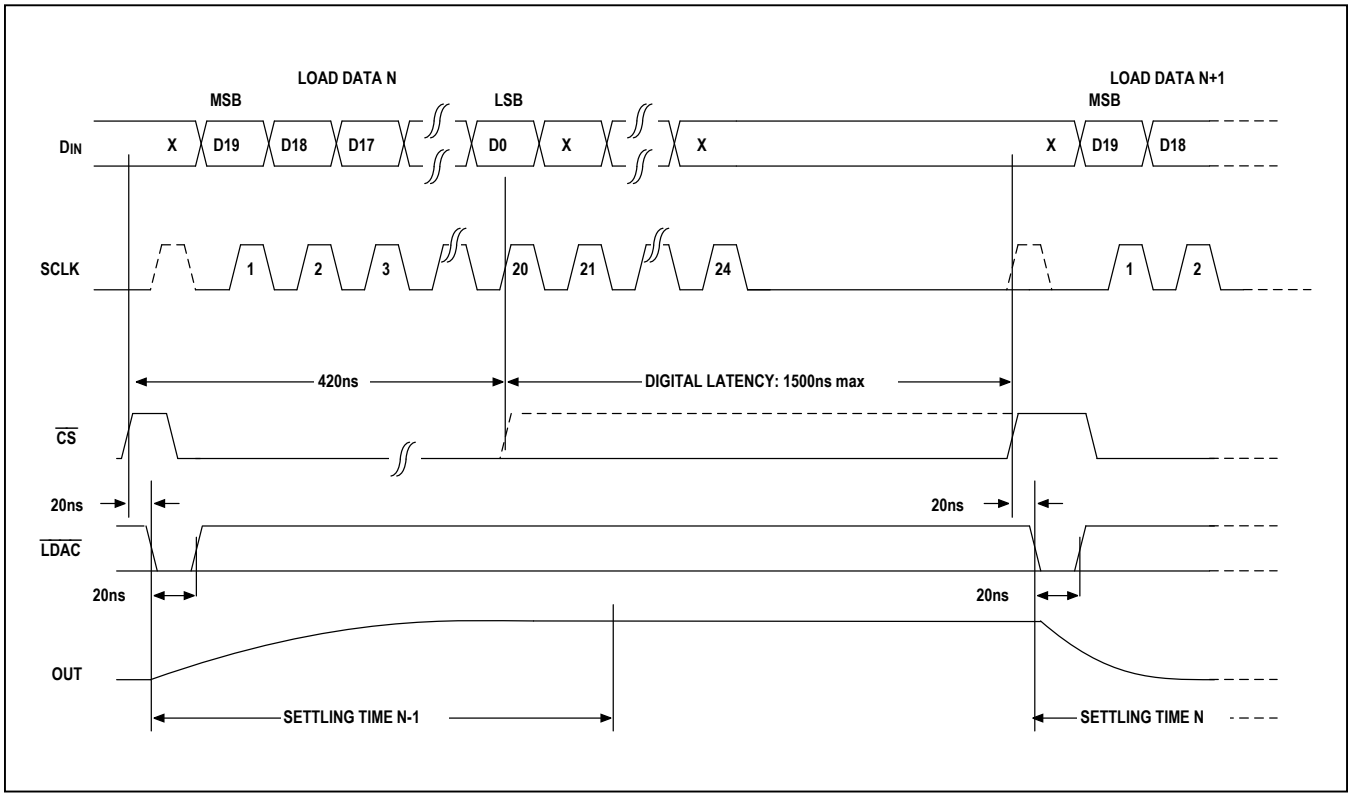


Figure 3. Throughput Timing (20-Bit Resolution Shown)

Use appropriate capacitor bypassing between the reference inputs and ground. A 0.1µF ceramic capacitor with short leads between REFF and AGNDF provides high-frequency bypassing. A 10µF low-ESR tantalum, film, or organic semiconductor capacitor works well for low-frequency bypassing. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading.

To maintain the excellent accuracy of these high-performance DACs, the analog ground connection must be low impedance. Connect AGNDF and AGNDS to a star ground very close to the pins and with the lowest impedance possible. The effect of ground trace resistance may be eliminated by using a precision operational amplifier to drive AGNDF and force AGNDS to ground. A voltage reference with a ground sense pin can also be used to control the DAC's reference voltage, provided that measurements are referred to AGNDS.

As in all high-resolution, high-accuracy applications, separate analog and digital ground planes yield the best results. Tie DGND to AGND at the AGND pin to form the “star” ground for the DAC system. Always refer remote DAC loads to this system ground for the best possible performance.

External Output Buffer Amplifier

The requirements on the external output buffer amplifier change whether the DAC is used in the unipolar or bipolar modes of operation. In unipolar mode, the output amplifier is used in a voltage-follower configuration. In bipolar mode, the amplifier operates with the internal scaling resistors (see Typical Application Circuits). In each mode, the DAC’s output impedance is constant and is independent of input code; however, the output amplifier’s input impedance should still be as high as possible to minimize gain errors. The DAC’s output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In bipolar mode, a precision amplifier operating with dual power supplies (such as the MAX9632) provides the $\pm V_{REF}$ output range. In single-supply applications, precision amplifiers with input common-mode ranges including AGND are available. However, their output swings do not normally include the negative rail (AGND) without significant degradation of performance. A single-supply amplifier may be suitable if the application does not use codes near zero.

Since the LSBs for high-resolution DACs are extremely small, pay close attention to the external amplifier’s input specifications. The input offset voltage can degrade the zero scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than ½ LSB. Similarly, the input bias current, multiplied by the DAC output resistance (2KΩ, typ), contributes to the zero-scale error. Temperature drift of offset voltage and input bias current must also be taken into account.

The settling time is affected by the buffer input capacitance, the DAC’s output capacitance, and the PC board capacitance. The typical DAC output voltage settling time to ±1ppm is 750ns for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time constant exponential settling response, a full scale step takes about 13.8 time constants to settle to within ±1ppm of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. Any additional output capacitance, such as the buffer's input capacitance, will increase the settling time.

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time constant response, is approximately the square root of the sum of the two time constants. The DAC output's time constant (due to internal resistance and capacitance) is about 50ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 10MHz bandwidth is

$$1/(2\pi \times 10MHz) = 15.9ns,$$

then the effective time constant of the combined system is:

$$[50ns^2 + 15.9ns^2]^{1/2} \approx 52.5ns$$

This suggests that the settling time to within ±1ppm of the final output voltage, including the external buffer amplifier, will be approximately

$$13.8 \times 52.5ns = 724ns.$$

Unipolar Configuration

Figure 4 shows the MAX5717/MAX5719 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and the tables below list the codes and corresponding output voltages for this circuit when using the 16-bit MAX5717 or the 20-bit MAX5719. At power-up, the default output in unipolar mode is zero-scale.

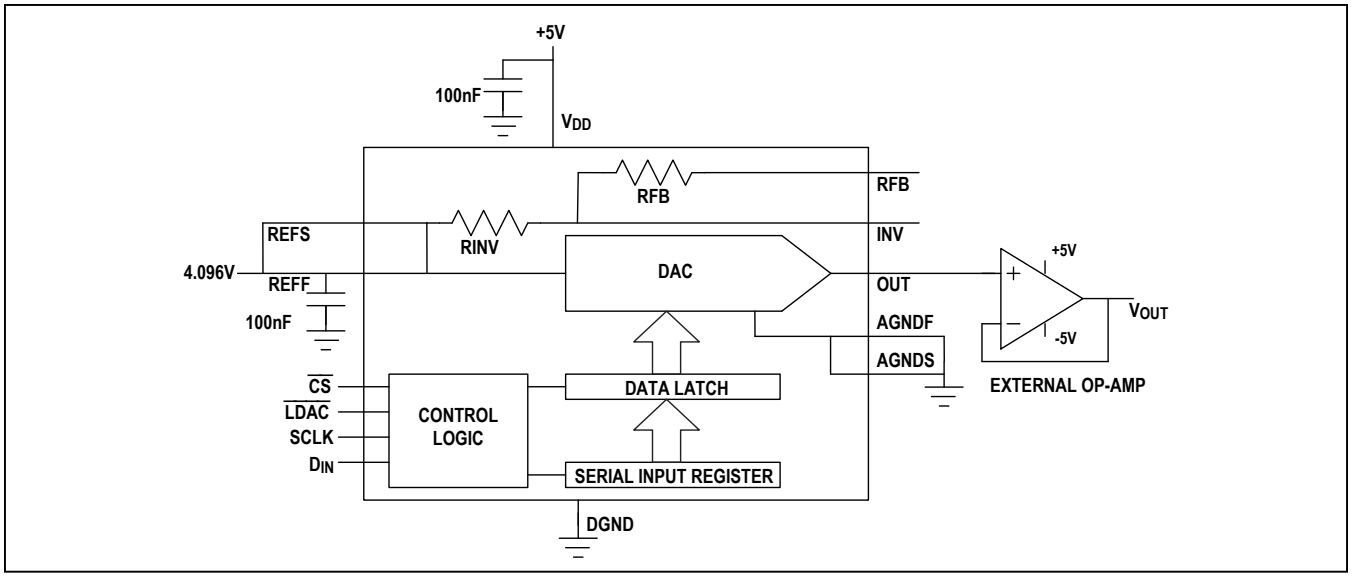


Figure 4. MAX5717/MAX5719 in Unipolar Mode. The Internal Bipolar Setting Resistors are Not Used in Unipolar Mode. The Force and Sense Pins for AGND and Reference Input May Be Used in This Mode, But Are Shown Connected Together in The Figure.

Table 3. MAX5717 Unipolar V_{OUT} vs. DAC Code

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535/65,536)
1000 0000 0000 0000	V_{REF} x (32,768/65,536) = ½ V_{REF}
0000 0000 0000 0001	V_{REF} x (1/65,536)
0000 0000 0000 0000	0V

Table 4. MAX5719 Unipolar V_{OUT} vs. DAC Code

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111 1111 xxxx	V_{REF} x (1,048,575/1,048,576)
1000 0000 0000 0000 0000 xxxx	V_{REF} x (524,288/262,144) = ½ V_{REF}
0000 0000 0000 0000 0001 xxxx	V_{REF} x (1/1,048,576)
0000 0000 0000 0000 0000 xxxx	0V

Bipolar Configuration

The Typical Application Circuits show the DAC configured for bipolar operation with an external op amp. Table 5 and Table 6 list the offset binary codes for this circuit when using the 16-bit MAX5717 and the 20-bit MAX5719. Ideal values (ignoring offset and gain errors) are shown in the tables. At power-up, the default output in bipolar mode is negative full-scale ($-V_{REF}$).

Power-Supply Bypassing and Ground Management

For optimum system performance, use PC boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC.

Table 5. MAX5717 Bipolar V_{OUT} vs. DAC Code

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	$+V_{REF}$ x (32,767/32,768)
1000 0000 0000 0001	$+V_{REF}$ x (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ x (1/32,768)
0000 0000 0000 0000	$-V_{REF}$ x (32,768/32,768) = $-V_{REF}$

The best ground connection can be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

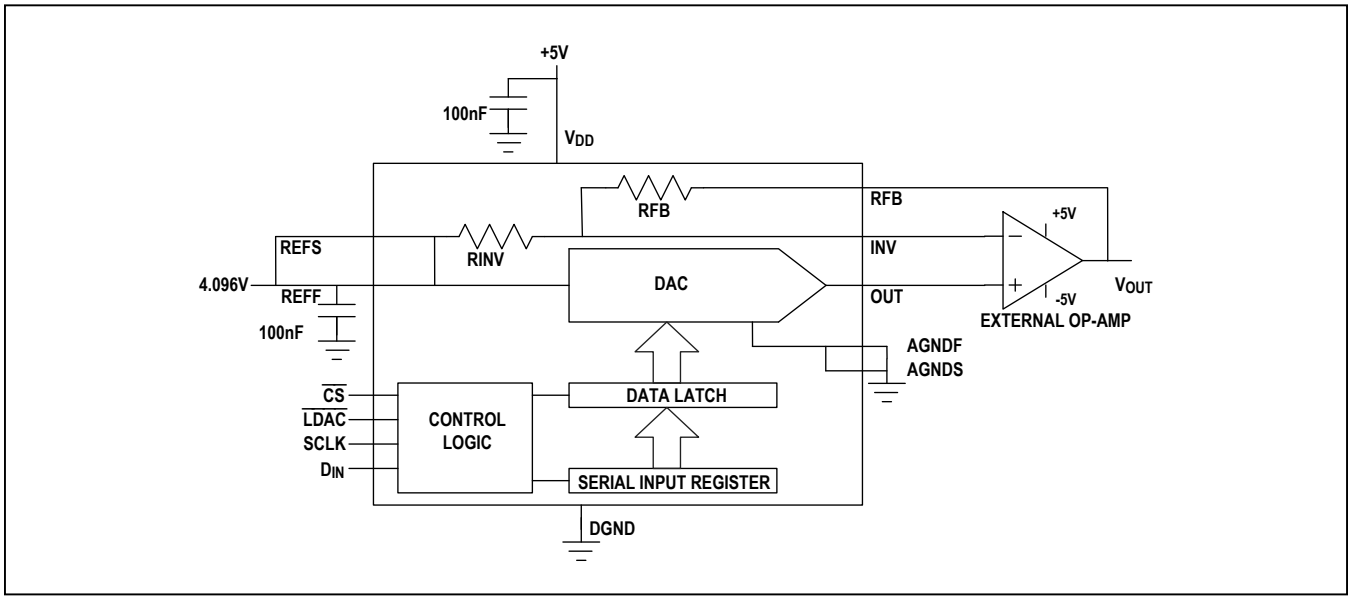
Bypass V_{DD} with a 0.1µF ceramic capacitor connected between V_{DD} and AGND. Mount it with short leads close to the device. Ferrite beads can also be used to further isolate the analog and digital power supplies.

Table 6. MAX5719 Bipolar V_{OUT} vs. DAC Code

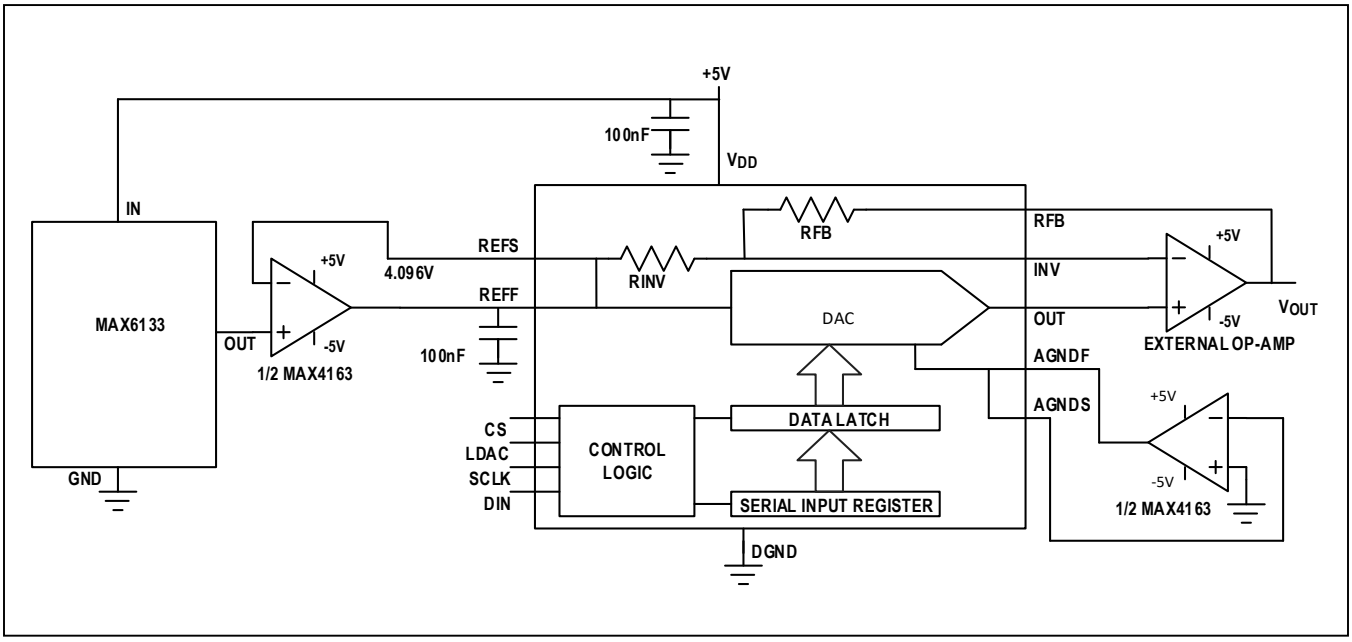
DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111 1111 xxxx	$+V_{REF}$ x (524,287/524,288)
1000 0000 0000 0000 0001 xxxx	$+V_{REF}$ x (1/524,288)
1000 0000 0000 0000 0000 xxxx	0V
0111 1111 1111 1111 1111 xxxx	$-V_{REF}$ x (1/524,288)
0000 0000 0000 0000 0000 xxxx	$-V_{REF}$ x (524,288/524,288) = $-V_{REF}$

Typical Application Circuits

Simple Bipolar Output (Force and Sense Pins Connected Together Close to IC)

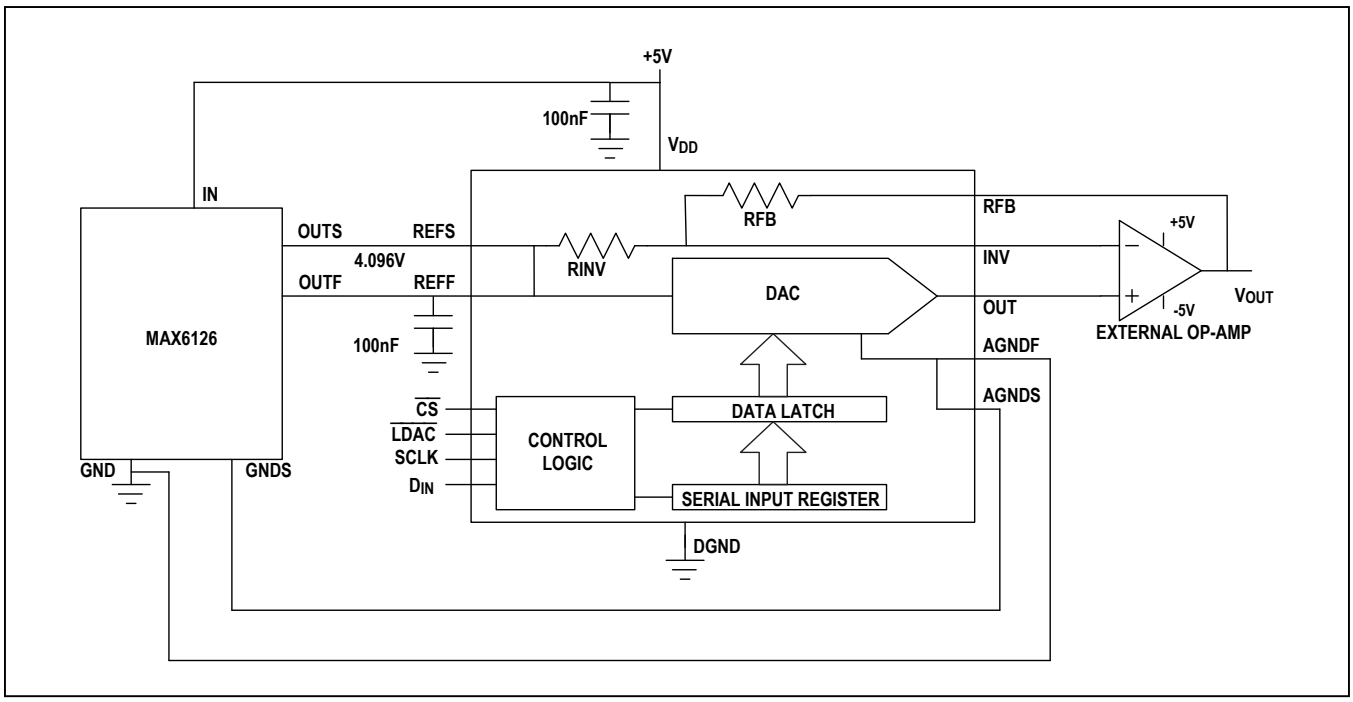


Bipolar Output with Force and Sense Reference and Ground Connections Using Operational Amplifiers



Typical Application Circuits (continued)

Bipolar Output Using Voltage Reference with Force and Sense on Output and Ground



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX5717GSD+	-40°C to +105°C	14 SO
MAX5717GSD+T	-40°C to +105°C	14 SO
MAX5717AGSD+	-40°C to +105°C	14 SO
MAX5717AGSD+T	-40°C to +105°C	14 SO
MAX5719GSD+	-40°C to +105°C	14 SO
MAX5719GSD+T	-40°C to +105°C	14 SO
MAX5719AGSD+	-40°C to +105°C	14 SO
MAX5719AGSD+T	-40°C to +105°C	14 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NUMBER	LAND PATTERNNUMBER
SOIC (N)	S14+4	21-0041	90-0112

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/16	Initial release	—
1	1/17	Added MAX5717A and MAX5719A versions to data sheet	1, 2, 9, 16
2	7/19	Updated *Typical Application Circuit*	15

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