Title	***Reference Design Report for a Dual Output 20 W Power Supply Using InnoSwitch™-EP INN2605K***
Specification	85 VAC – 264 VAC Input; 12 V, 1.5 A and 5 V, 0.5 A Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	RDR-469
Date	February 4, 2016
Revision	1.3

Summary and Features

- InnoSwitch-EP - industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built in synchronous rectification for >87% efficiency
- All the benefits of secondary side control with the simplicity of primary side regulation
    - Insensitive to transformer variation
    - Extremely fast transient response independent of load timing
- Meets output cross regulation requirements without linear regulators
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 1.5 A, 12 V and 0.5 A, 5 V dual output embedded power supply utilizing INN2605K from the InnoSwitch-EP family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

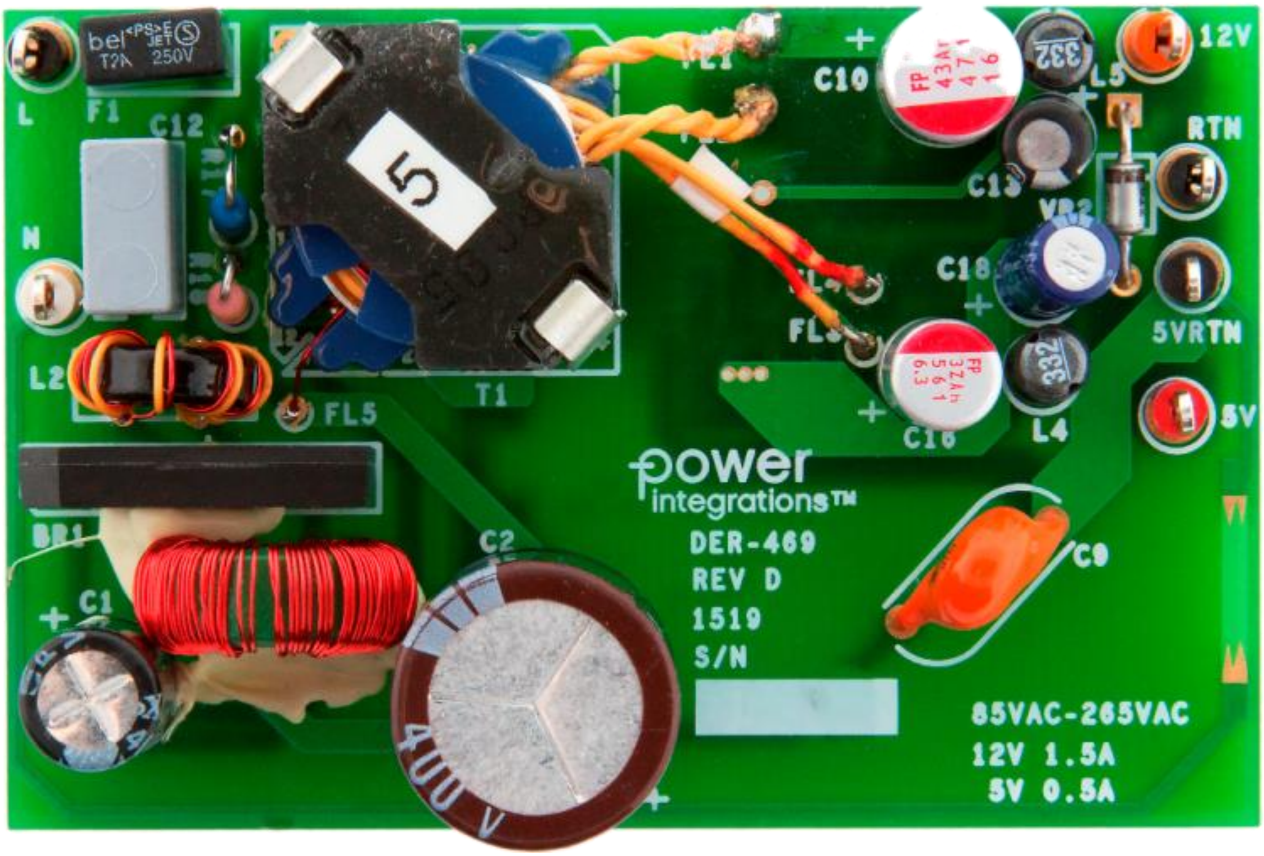

Figure 1 – Populated Circuit Board Photograph, Top.

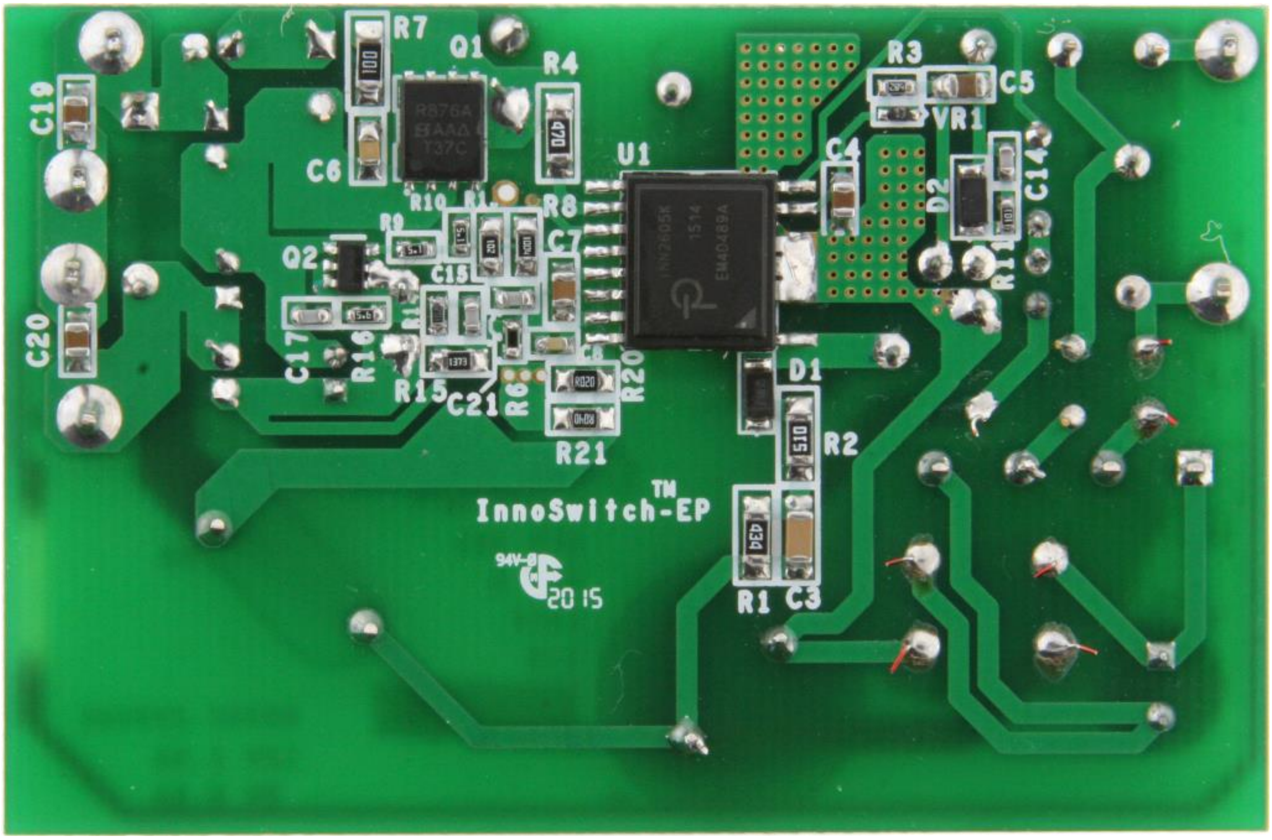

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	3 Wire Input
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5 %
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0		0.5	A	
Output Voltage 2	V_{OUT2}	10.2	12	13.8	V	±15 %, (±10 % with 0.1 A Min Load on 12 V)
Output Ripple Voltage 2	$V_{RIPPLE2}$			150	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}	0		1.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		21		W	
Efficiency						
Full Load	η	88			%	Measured at 110 / 230 VAC, P_{OUT} 25 °C
No Load Input Power				30	mW	V_{IN} at 230 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Differential		1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Surge Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level

3 Schematic

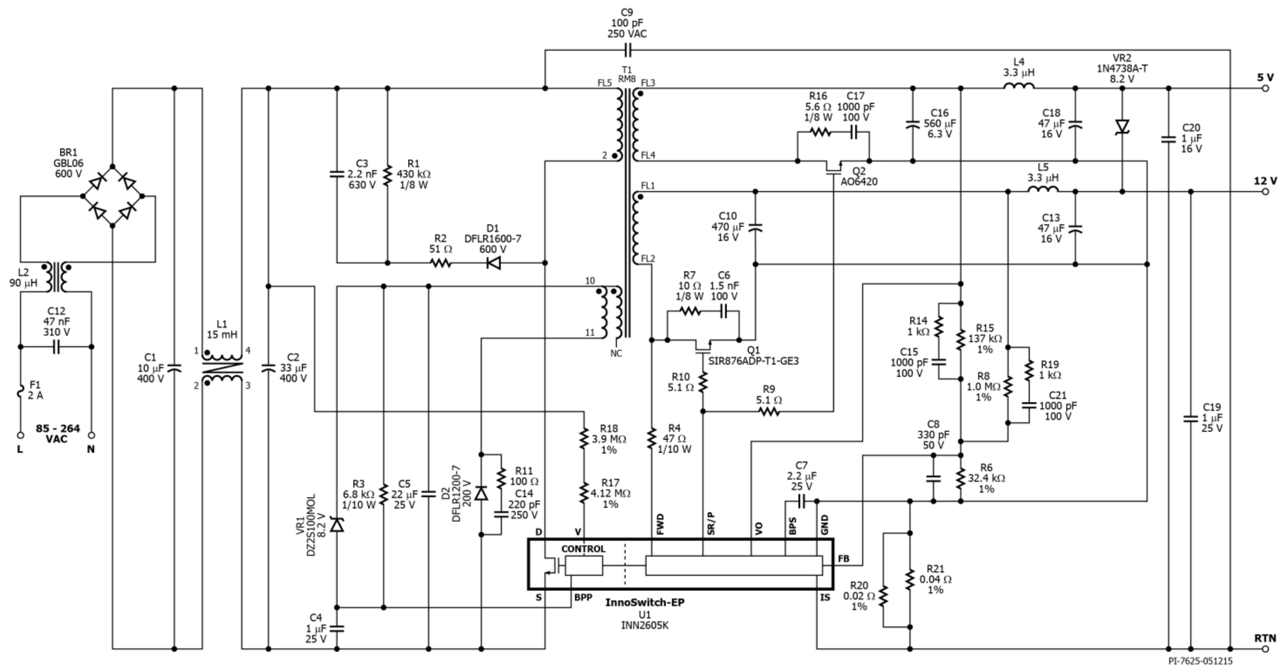

Figure 3 – Schematic.

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4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and the common mode chokes L1 and L2 with capacitors, C9 and C12, provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1 and C2. There is no need to use an inrush current limiter in the circuit with the high peak forward surge current rated bridge rectifier, GBL06. The differential inductance of common mode choke L1 with capacitors C1 and C2 provide differential noise filtering.

4.2 *InnoSwitch-EP Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the InnoSwitch-EP IC (U1).

A low cost RCD clamp formed by D1, R1, R2, and C3 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C5, and fed in the BPP pin via a current limiting resistor R3. Radiated EMI caused by resonant ringing across diode D2 is reduced via snubber components R11 and C14. The primary side overvoltage protection is obtained using Zener diode VR1. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR1 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch-EP IC.

Resistor R17 and R18 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C2. At approximately 100 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 460 V DC, the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1.

4.3 *InnoSwitch-EP IC Secondary*

The secondary side of the InnoSwitch-EP provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q2. Very low ESR capacitor C16 provides filtering, and inductor L4 and capacitor C18 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 12 V output is provided by SR FET Q1. Very low ESR capacitors C10 provides filtering, and Inductor L5 and capacitor C13 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 12 V output. C19 and C20 capacitors reduce the radiation EMI noise.

RC snubber networks comprising R16 and C17 for Q2, R7 and C6 for Q1 damp high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R4 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C7 via R4 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Resistor R8, R15 and R6 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. Zener diode VR2 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification. The InnoSwitch-EP IC has an internal reference of 1.265 V. Feedback compensation networks comprising capacitors C15, C21 and resistors R14, R19 reduce the output ripple voltage. Capacitor C8 provides decoupling from high frequency noise affecting power supply operation. Total output current is sensed by R20 and R21 with a threshold of approximately 33 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current

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5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

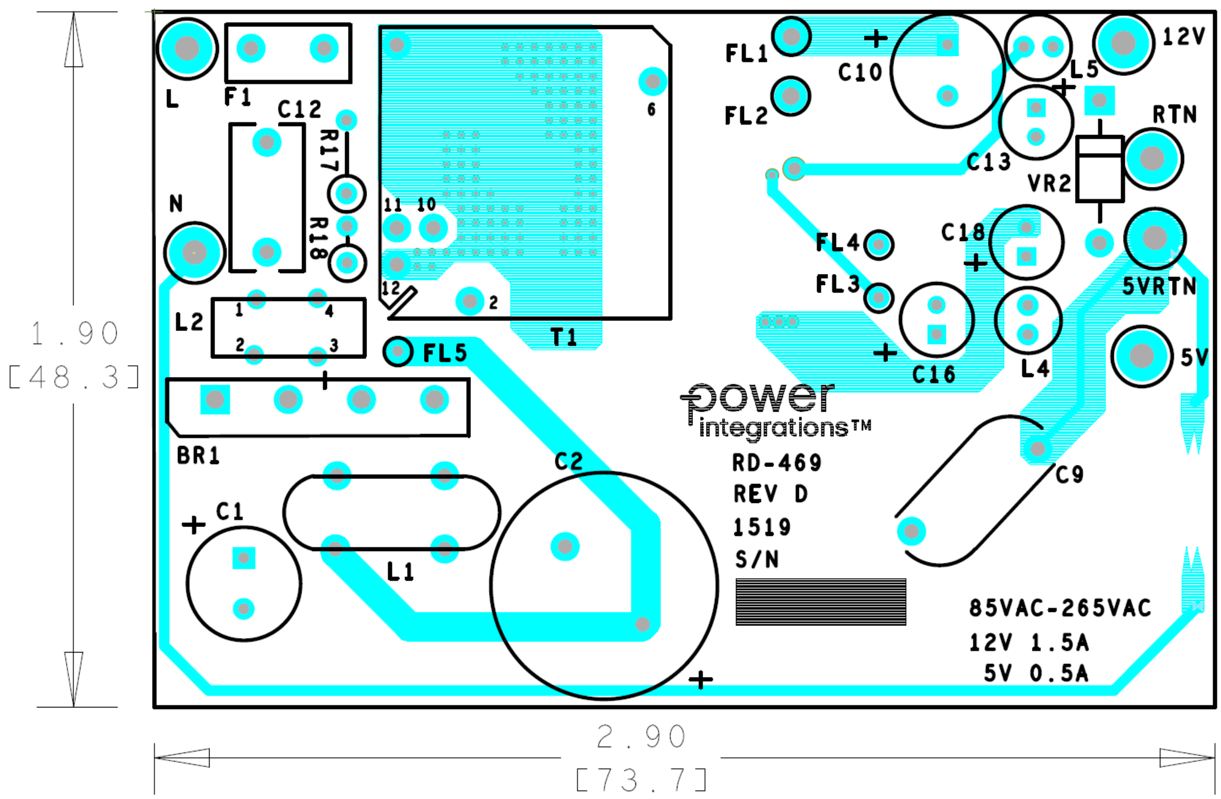

Figure 4 – Printed Circuit Layout, Top.

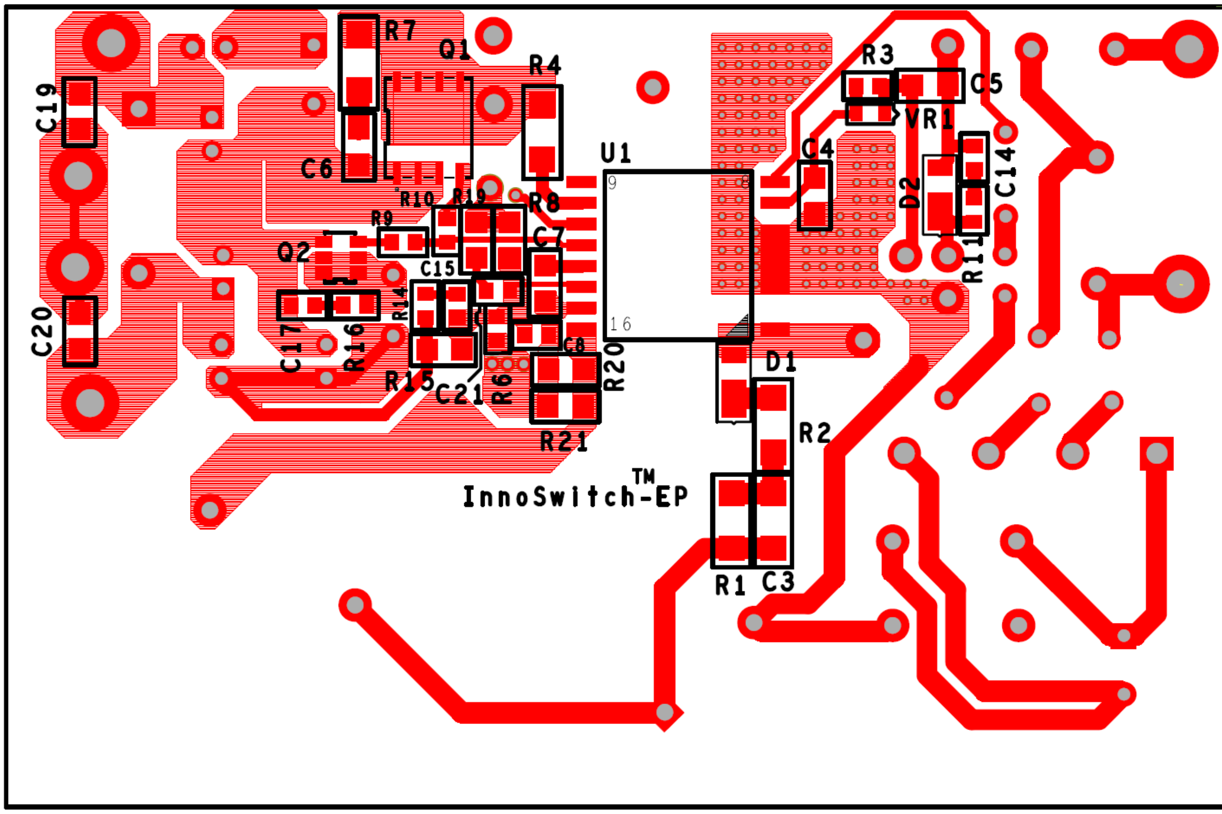

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	12V	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
2	1	5V	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
3	3	5VRTN L RTN	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
4	1	BR1	DIODE BRIDGE 600V 4A GB	GBL06	Genesic Semi
5	1	C1	10 μF, 400 V, Electrolytic, (8 x 14)	EWH2GM100F14OT	Aishi
6	1	C2	33 μF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	EKMX401ELL330ML20S	Nippon Chemi-Con
7	1	C3	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
8	3	C4 C19 C20	1 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
9	1	C5	22 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E226M125AC	TDK
10	1	C6	1.5 nF, 200 V, 10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
11	1	C7	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
12	1	C8	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
13	1	C9	100 pF, Ceramic, Y1	440LT10-R	Vishay
14	1	C10	470 μF, 16 V, Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
15	1	C12	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
16	1	C13	47 μF, 16 V, Electrolytic, Gen Purpose, (5 x 11.5)	ECA-1CHG470	Panasonic
17	1	C14	220 pF, 250 V, Ceramic, COG, 0603	C1608C0G2E221J	TDK
18	3	C15 C17 C21	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
19	1	C16	560 μF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
20	1	C18	47 μF, 16 V, Electrolytic, Low ESR, 500 mΩ, (5 x 11.5)	ELXZ160ELL470MEB5D	Nippon Chemi-Con
21	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
22	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
23	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
24	1	L1	15 mH, Common Mode Choke	SNX-R1789 TSD-3641	Santronics Premier Magnetics
25	1	L2	Custom, 90 μH, constructed on Core 35T0375-10H from PI# 30-00275-00	SNX-R1790 TSD-3640	Santronics Premier Magnetics
26	2	L4 L5	3.3 μH, 1.5 A	11R332C	Murata
27	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
28	1	Q1	100 V, 40 A, N-Channel, PowerPAK SO-8	SIR876ADP-T1-GE3	Vishay
29	1	Q2	MOSFET, N-CH, 60 V, 4.2 A, 6TSOP	AO6420	Alpha & Omega Semi
30	1	R1	430 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ434V	Panasonic
31	1	R2	51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
32	1	R3	6.8 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ682V	Panasonic
33	1	R4	47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
34	1	R6	32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
35	1	R7	10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
36	1	R8	1 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1004V	Panasonic
37	2	R9 R10	5.1 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ5R1V	Panasonic
38	1	R11	100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
39	1	R14	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
40	1	R15	137 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1373V	Panasonic
41	1	R16	5.6 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ5R6V	Panasonic
42	1	R17	4.12 MΩ, 1%, 1/4 W, Metal Film	RNF14FTC4M12	Stackpole

43	1	R18	3.9 MΩ, 1%, 1/4 W, Metal Film	HHV-25FR-52-3M9	Yageo
44	1	R19	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
45	1	R20	0.02 Ω, 1%, 1/4 W, Thick Film, 0805	RL0805FR-7W0R02L	Yageo
46	1	R21	0.04 Ω1/8 W, 1%, Thick Film, 0805	RL0805FR-070R04L	Yageo
47	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer Transformer	RM8/12/1 SNX-R1788 POL-INN010	Schwartzpunkt Santroincs Premier Magnetics
48	1	U1	InnoSwitch-EP, Off-Line CV/CC Flyback Switcher, ReSOP-16B	INN2605K	Power Integrations
49	1	VR1	8.2 V, 5%, 150 mW, SSMINI-2	DZ2S08200L	Panasonic
50	1	VR2	8.2 V, 5%, 1 W, DO-41	1N4738A,113	NXP Semi

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7 Transformer (T1) Specification

7.1 *Electrical Diagram*

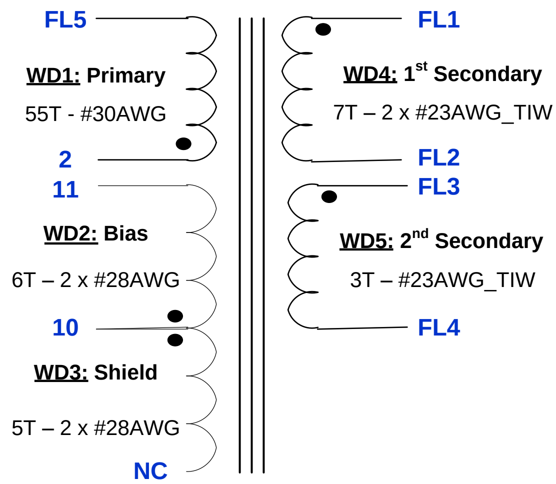

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 2 and FL5, with all other windings open.	545 μH ±10%
Resonant Frequency	Between pin 2 and FL5, other windings open.	1100 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and FL5, with FL1, FL2, FL3, FL4 shorted.	20 μH (Max).

7.3 *Material List*

Item	Description
[1]	Core: RM8, PC95 TDK or DMR95 from DMEGC magnetics.
[2]	Bobbin: RM8, Vertical, 12 pins (6/6-circular) (PI P/N: 25-1022-00).
[3]	Core Clip: Allstar Magnetic, P/N: CLI/P-RM8/I.
[4]	Magnet wire: #30 AWG, double coated.
[5]	Magnet wire: #28 AWG, double coated.
[6]	Magnet wire: #23 AWG, Triple Insulated Wire.
[7]	Barrier Tape: 3M 1298 Polyester Film, 1 mil thickness, 9.0 mm wide.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

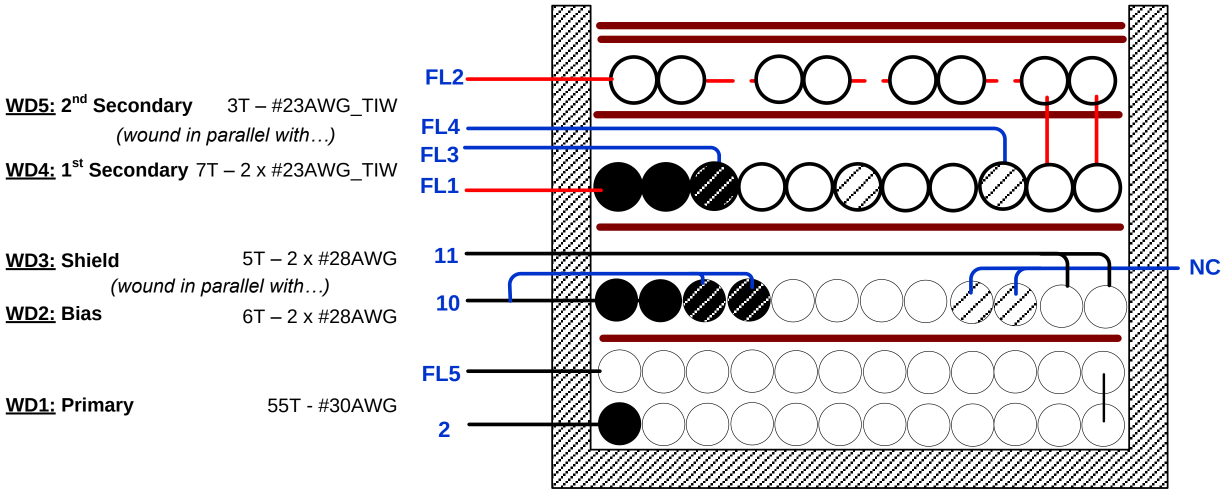

Figure 7 – Transformer Build Diagram.

7.5 *Winding Instructions*

Winding Preparation	For the purpose of these instructions, bobbin item [1] is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 2, wind 55 turns of wire item [4] from left to right then right to left in 2 layers and finish as FL5 floating.
Insulation	1 layer of tape item [7] for insulation.
WD2 Bias & WD3 Shield	Take 4 wires item [5], start at pin 10, wind 5 turns, cut 2 wires and leave no-connect for WD3-Shield. Continue winding 1 more turn for other 2 wires and bring thses wire to the left to finish at pin 11 for WD2-Bias.
Insulation	1 layer of tape item [7] for insulation.
WD4 1st Secondary & WD5 2nd Secondary	Take 3 wires item [6], (WD4-1st Secondary needs 2 wires, WD5-2nd Secondary needs single wire), designate start leads FL1 for WD4 and FL3 for WD5.Wind 3 turns, at the 3rd turn, bring the single wire to the left, and leave floating as FL4 for WD5. Place 1 layer of tape to secure the winding, then continue winding 4 more turns of other 2 wires from right to left and leave floating as FL2 for WD4.
Insulation	2 layers of tape item [7] for insulation and secure the windings.
Finish	Cut short FL1, FL2 to ~20.0 mm, and FL4, FL4 to ~30.0 mm. Gap the core halves to get 545 μH. Assemble the core halves with clip item [3]. Cut short leg of bottom clip (see picture below). Remove pins: 1,3,4,5,7,8, and 9. Varnish with item [8].

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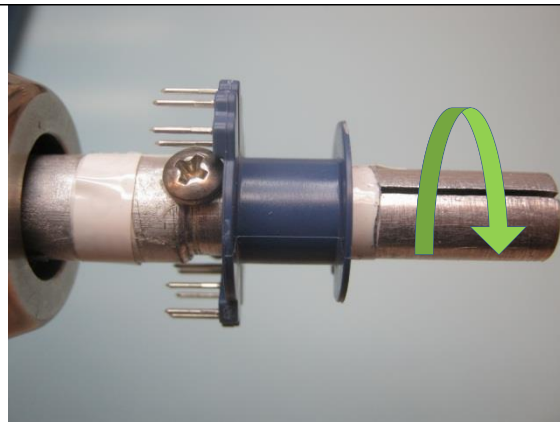
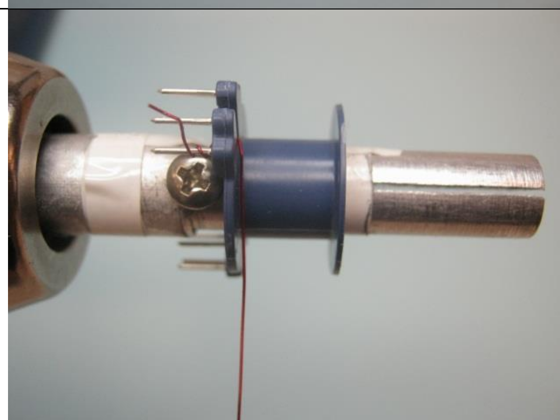
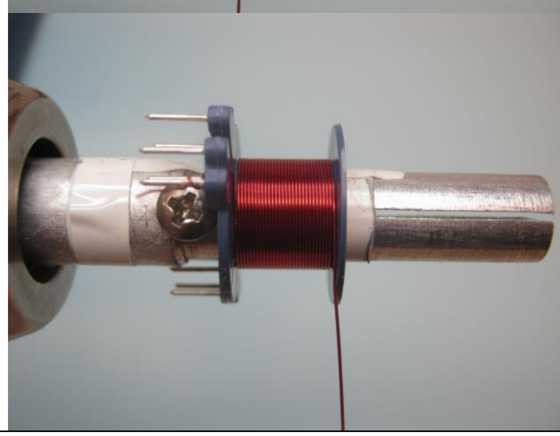
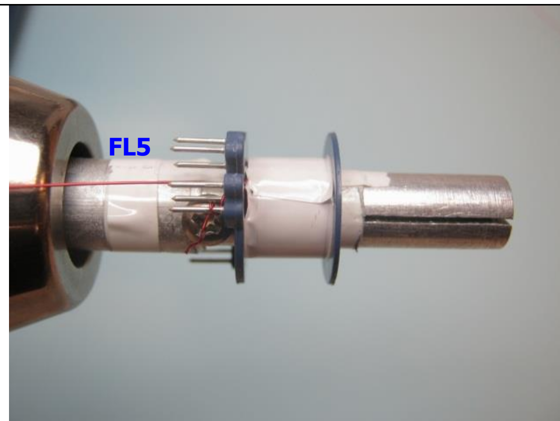
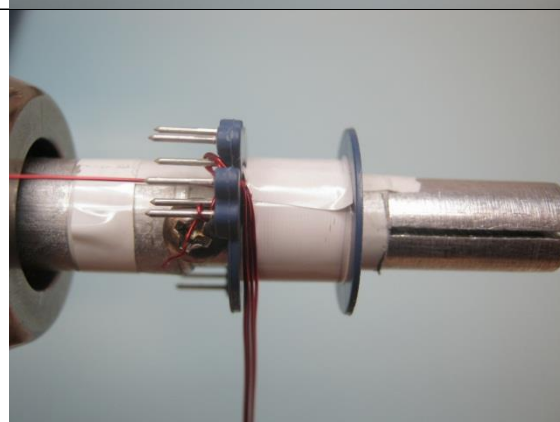
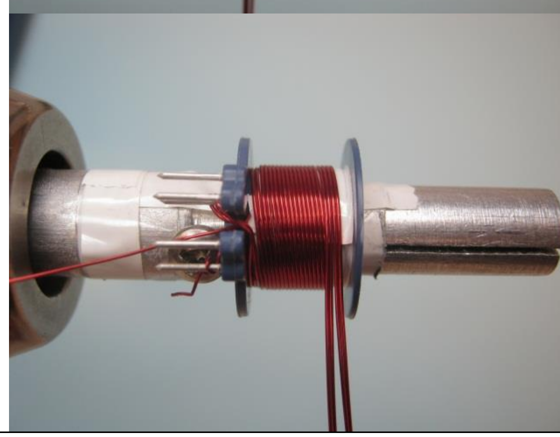
7.6 *Winding Illustrations*

Winding Preparation		For the purpose of these instructions, bobbin item [1] is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**	 	Start at pin 2, wind FL5 55 turns of wire item [4] from left to right then right to left in 2 layers and finish as FL5 floating.

Insulation		1 layer of tape item [7] for insulation.
WD2 Bias & WD3 Shield	 	Take 4 wires item [5], start at pin 10, wind 5 turns.

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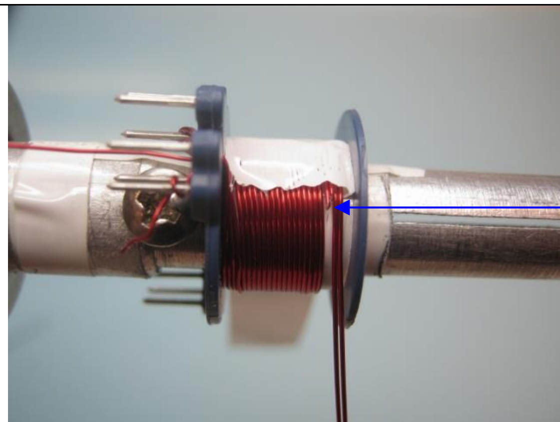
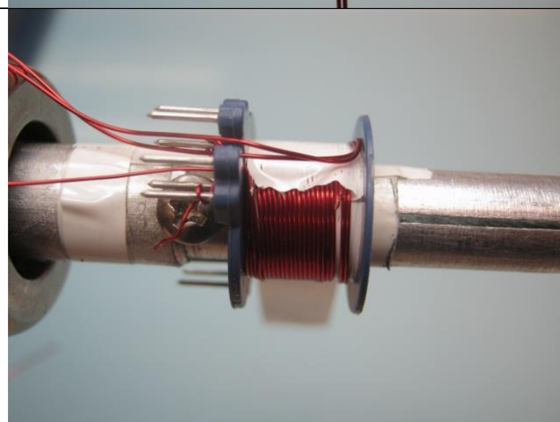
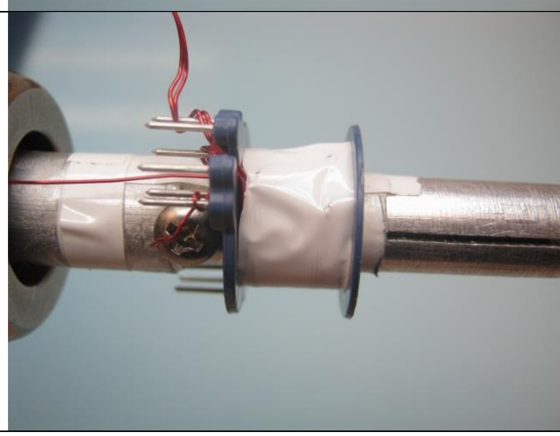
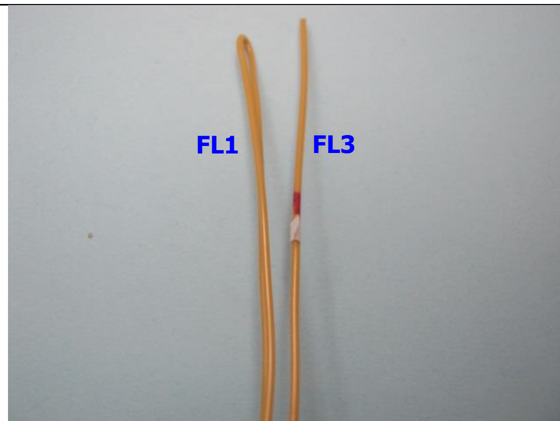
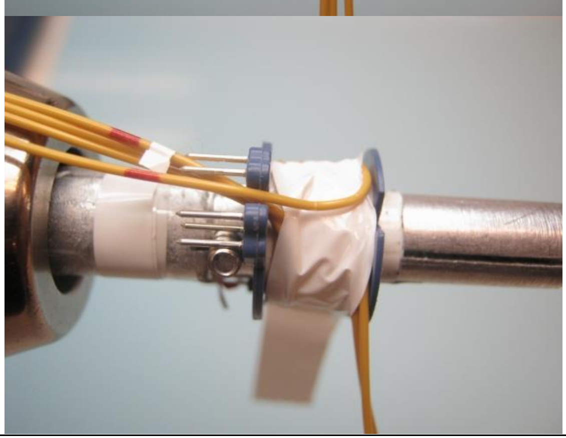
		Cut 2 wires and leave no-connect for WD3-Shield.
		Continue winding 1 more turn for other 2 wires and bring theses wire to the left to finish at pin 11 for WD2-Bias.
Insulation		1 layer of tape item [7] for insulation.

WD4 1st Secondary & WD5 2nd Secondary	 	Take 3 wires item [6], (WD4-1st Secondary needs 2 wires, WD5-2nd Secondary needs single wire), designate start leads FL1 for WD4 and FL3 for WD5.
	 	Wind 3 turns, at the 3rd turn, bring the single wire to the left, and leave floating as FL4 for WD5. Place 1 layer of tape to secure the winding, then continue winding 4 more turns of other 2 wires from right to left and leave floating as FL2 for WD4.

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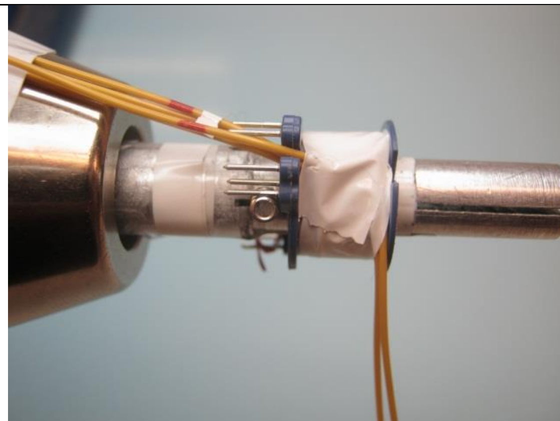
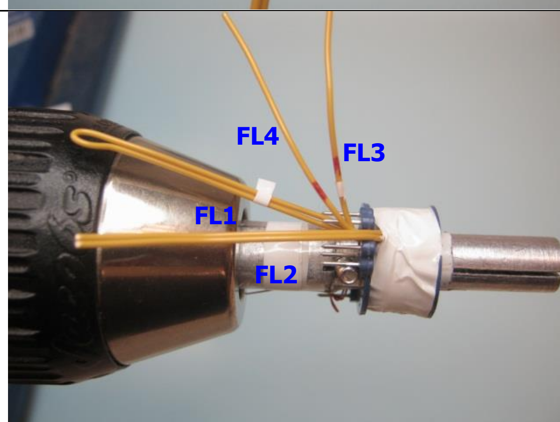
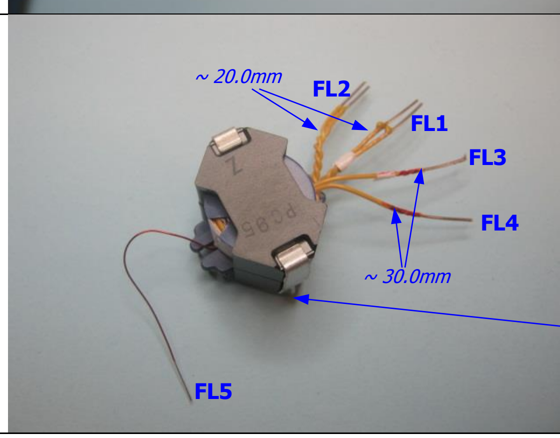
	 	
	 	2 layers of tape item [7] for insulation and secure the windings.
Finish	 	Cut short FL1, FL2 to ~20.0 mm, and FL4, FL4 to ~30.0 mm. Gap the core halves to get 545 μH. Assemble the core halves with clip item [3]. Remove pins: 1, 3, 4, 5, 7, 8, and 9. <u>Cut short leg of bottom clip</u>. Varnish with item [8].

8 15 mH Common Mode Choke (L1) Specification

8.1 *Electrical Diagram*

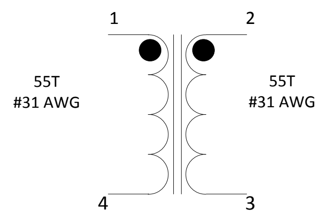


Figure 8 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS	13 mH ±25%
Core Effective Inductance		4960 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted	80 µH

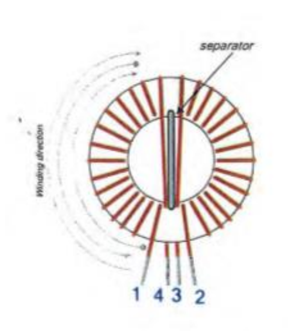
8.3 *Material List*

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID, PI Part number: #32-00286-00 1) JLW Electronics (Hong Kong), T14 x 8 x 5. 5C-JL10 2) TDK, B64290L0658 x 038 material
	Divider -- Fish paper, insulating cotton rag, 0.010" thick, PI #: 66-00042-00. Cut to size 8 mm x 5.5 mm.
[2]	Magnet Wire: #31 AWG Heavy Nyleze.

8.4 *Winding Instructions*

- Use 4 ft of item [2], start at pin 1 wind 55 turns end at pin 4.
- Do the same for another half of Toroid, start at pin 2 and end at pin 3.

8.5 *Illustrations*



Top View.

Front View.

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9 90 μH Common Mode Choke (L2) Specification

9.1 *Electrical Diagram*

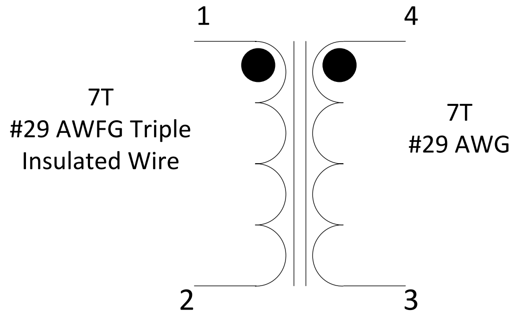


Figure 9 – Inductor Electrical Diagram.

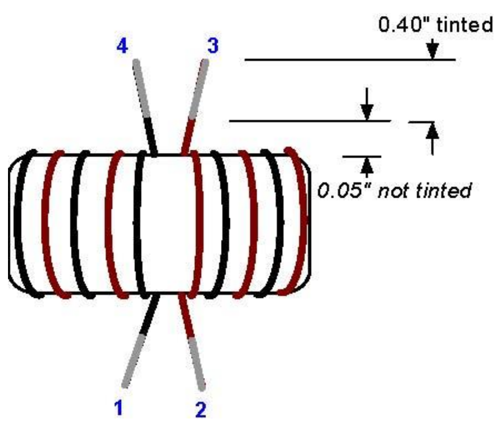
9.2 *Electrical Specifications*

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	90 μH ±25%
Resonant Frequency	Pins 1-2, all other windings open.	
Primary Leakage Inductance	Pins 1-2, with 3-4 shorted.	0.5 μH

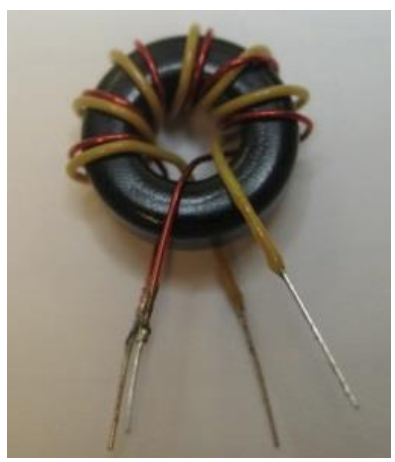
9.3 *Material List*

Item	Description
[1]	1) Toroid: FERRITE INDUCTR TOROID .415" OD ;Mfg Part number: 35T0375-10H Dim: 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L, PI Part number: 32-00275-00. 2) Toroid: Ferrite core, TDK, B64290L38x30,PI Part number : 32-00329-00.
[2]	Magnet Wire: #29 AWG.
[3]	Triple Insulated wire #29 AWG.

9.4 *Illustrations*



Top View.



Front View.

10 Transformer Design Spreadsheet

ACDC_InnoSwitch-CH_102014; Rev.2.0; Copyright Power Integrations 2014	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**ACDC_InnoSwitch-CH_101714_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet**
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	12.00		12.00	V	Output Voltage (continuous power at the end of the cable)
IO	1.75		1.75	A	Power Supply Output Current (corresponding to peak power)
Power		**Info**	21	W	Specified Output Power exceeds the value specified on the datasheet for universal input adapter. Please verify performance on bench
n	0.87		0.87		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	44.00		44.00	uFarad	Input Capacitance
ENTER InnoSwitch-CH VARIABLES					
InnoSwitch-CH	**INN20x5**		**INN20x5**		User defined InnoSwitch
Cable drop compensation	**0%**		**0%**		Select Cable Drop Compensation option
Complete Part Number			**INN2005K**		Final part number including package
Chose Configuration	**INC**		**Increased Current Limit**		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.955	A	Minimum Current Limit
ILIMITTYP			1.050	A	Typical Current Limit
ILIMITMAX			1.145	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			92.61	A^2kHz	Worst case I2F parameter across the temperature range
VOR	100		100	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.92		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.54		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			5.79	V	Bias Winding Number of Turns
PIVB			64.34	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM8**		**RM8**		Enter Transformer Core
Core			PC47RM8Z-12		Enter core part number, if necessary
Bobbin			BRM8-718CPFR		Enter bobbin part number, if necessary
AE			0.640	cm^2	Core Effective Cross Sectional Area
LE			3.80	cm	Core Effective Path Length
AL			1950	nH/T^2	Ungapped Core Effective Inductance
BW			9.05	mm	Bobbin Physical Winding Width
M	0.00		0.00	mm	Safety Margin Width (Half the Primary to

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					Secondary Creepage Distance)
L	2		2		Number of Primary Layers
NS	7		7		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			82	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.56		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.29	A	Average Primary Current
IP			0.955	A	Peak Primary Current assuming ILIMITMIN
IR			0.875	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.43	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			545	uHenry	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 490 uH
LP_TOLERANCE	10.0		10.0	%	Primary inductance tolerance
NP			58		Primary Winding Number of Turns
ALG			162	nH/T^2	Gapped Core Effective Inductance
BM			1999	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			915	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			921		Relative Permeability of Ungapped Core
LG			0.45	mm	Gap Length (Lg > 0.1 mm)
BWE			18.1	mm	Effective Bobbin Width
OD			0.31	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.26	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			235	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			7.91	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			3.15	A	Secondary RMS Current
IRIPPLE			2.62	A	Output Capacitor RMS Ripple Current
CMS			630	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			22	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			605	V	Maximum Drain Voltage Estimate
PIVS			76	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			12.00	V	Main Output Voltage directly after output rectifier
IO1			1.75	A	Output DC Current
PO1			21.00	W	Output Power
VD1			0.10	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			7.00	Turns	Output Winding Number of Turns

ISRMS1			3.15	A	Output Winding RMS Current
IRIPPLE1			2.62	A	Output Capacitor RMS Ripple Current
PIVS1			76	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			**Si7456**		Recommended SR FET for this output
RDSON_HOT			0.042	Ohm	RDSon at 100C
VRATED			100	V	Rated voltage of selected SR FET
CMS1			630	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			22	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.65	mm	Minimum Bare Conductor Diameter
ODS1			1.29	mm	Maximum Outside Diameter for Triple Insulated Wire

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11 Performance Data

11.1 *Full Load Efficiency vs. Line*

Two SR FETS (SIR876 & AO6420) vs. One SR FET + one Schottky diode (SIR876 and SS24). (Need to have 60 Ω load on the 5 V output to be comparable with two SR FETs in cross regulation with SS24.)

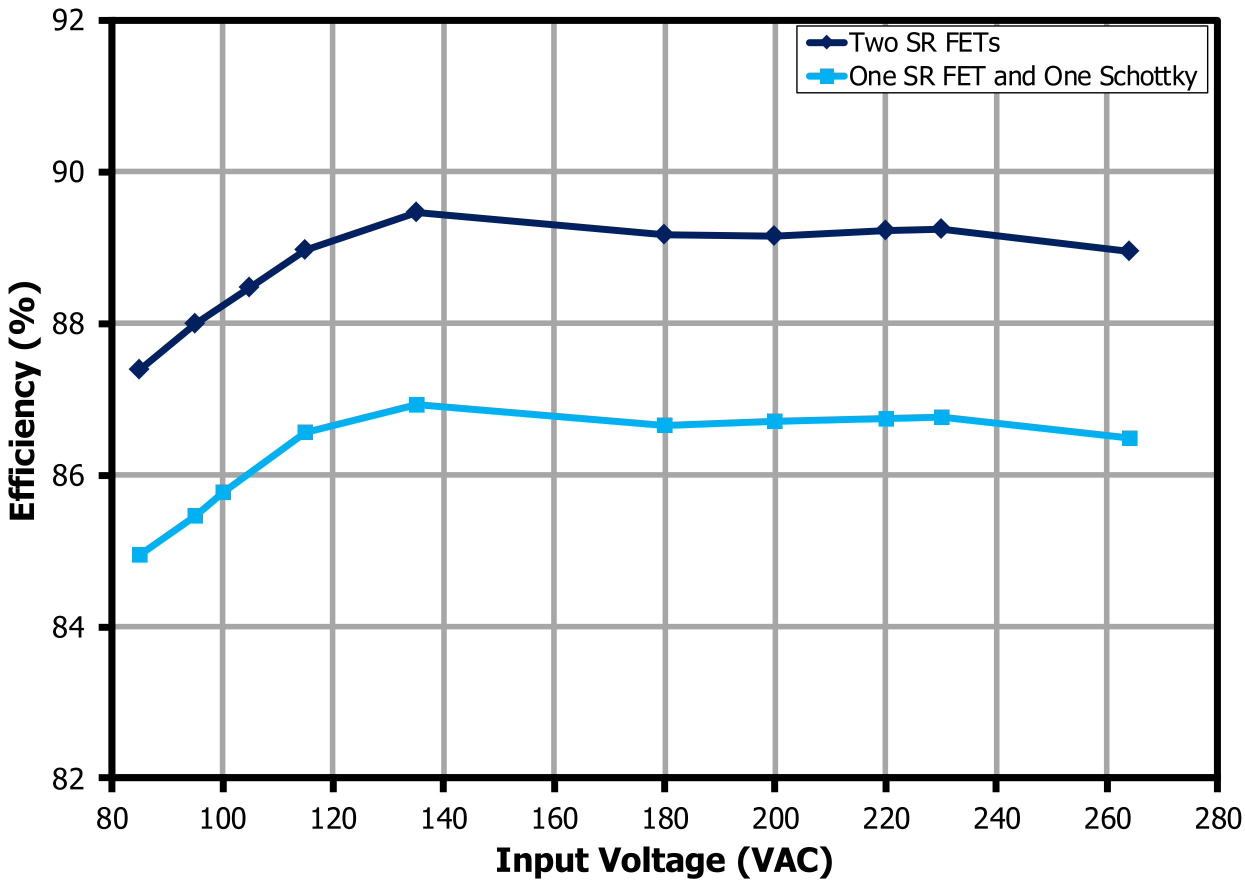

Figure 10 – Full load Efficiency vs. Line Voltage, Room Temperature.

11.2 *Efficiency vs. Load (0 A – 1.5 A on 12 V, Full Load on 5 V)*

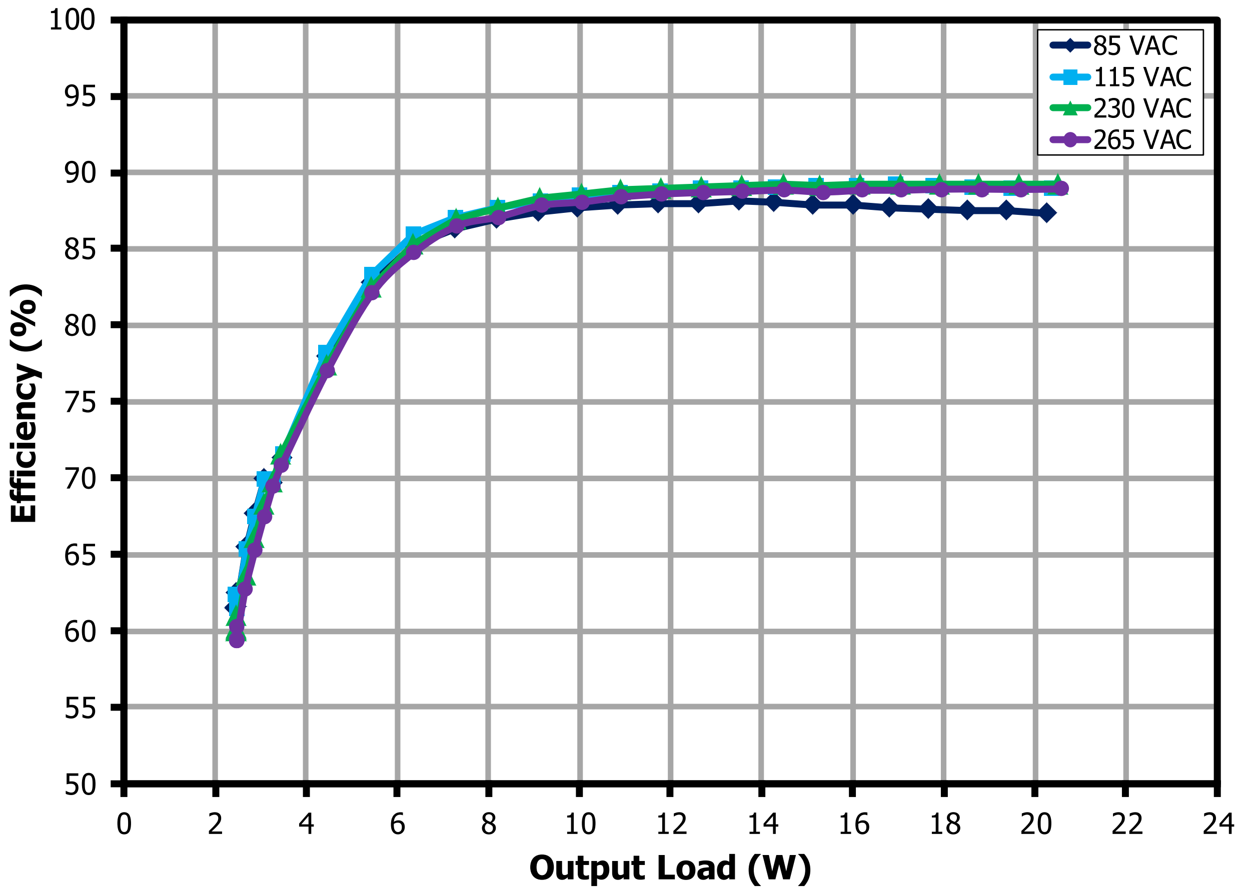

Figure 11 – Efficiency vs. Load, Room Ambient.

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11.3 *Efficiency vs. Load (0 A – 1.5 A on 12 V, No-Load on 5 V)*

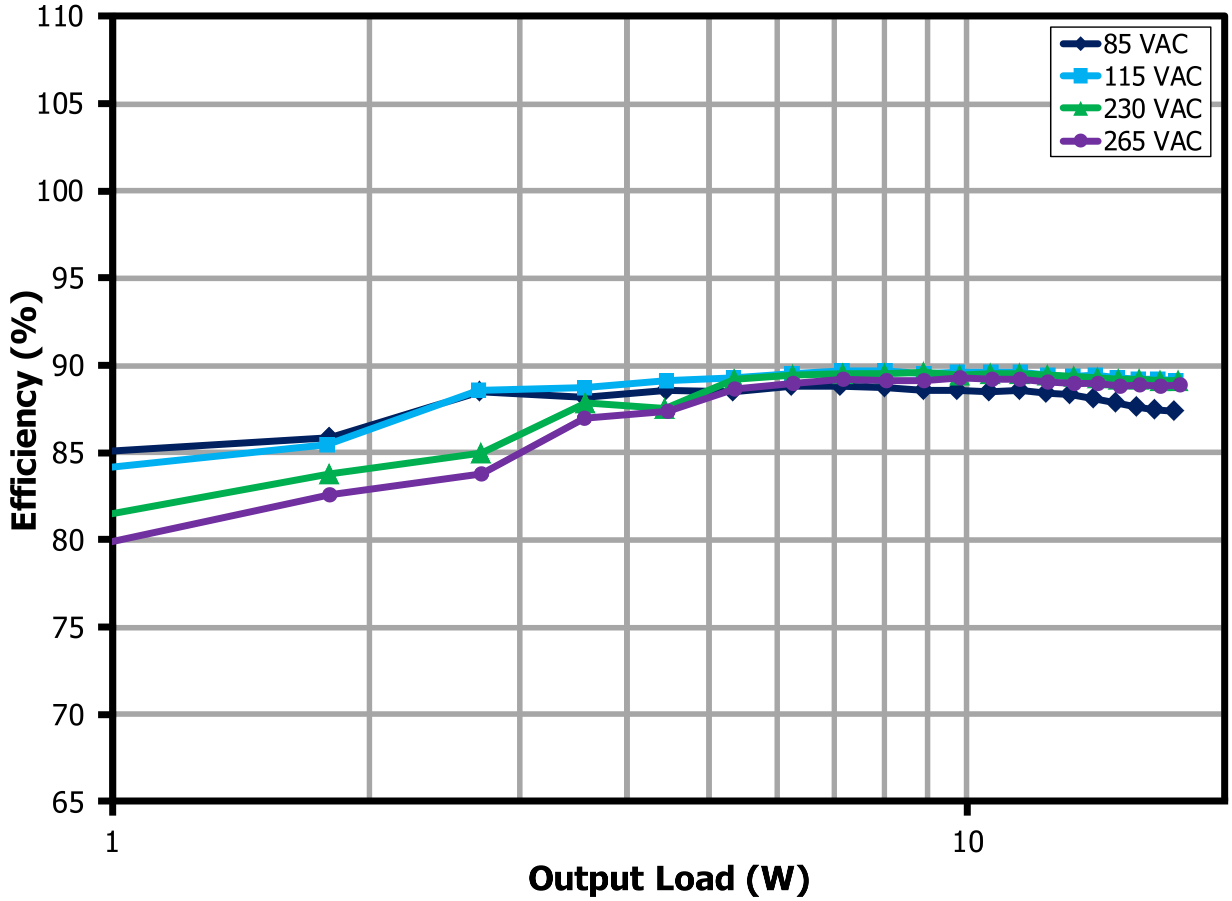

Figure 12 – Efficiency vs. Load (Log Scale to Demonstrate Light Load Performance).

11.4 *No-Load Input Power*

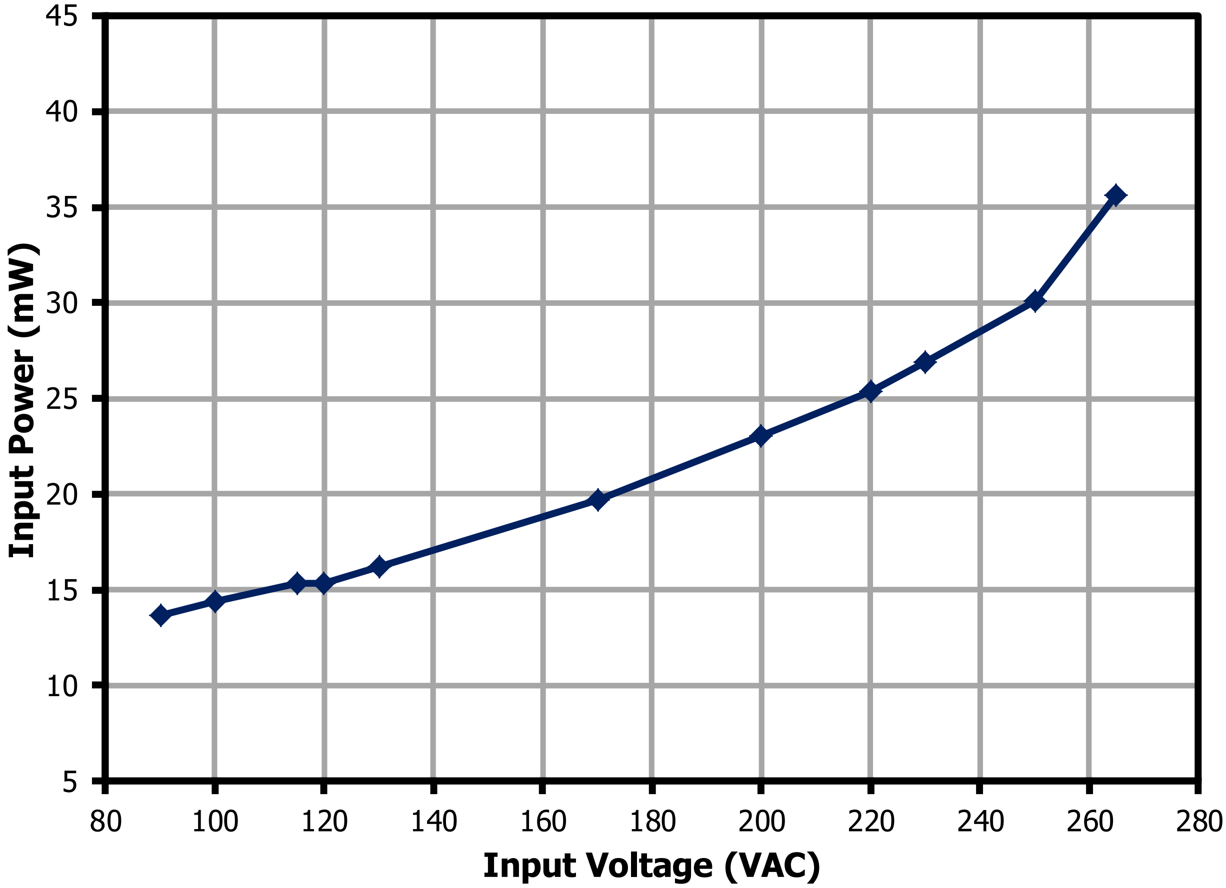

Figure 13 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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11.5 ***5 V Output Power with Low Input Power (No-Load on 12 V)***

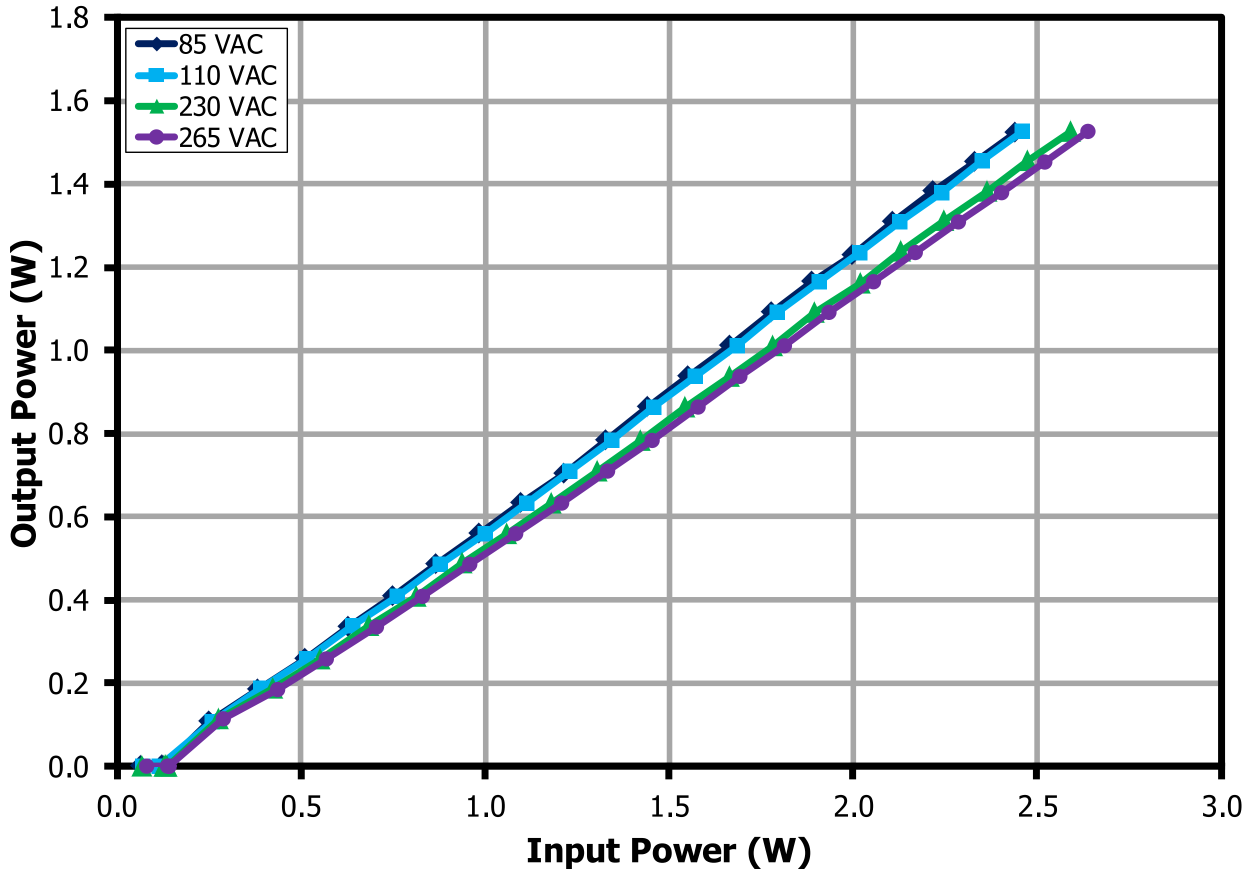

Figure 14 – 5 V Output Power vs. 12 V No-Load Input Power.

11.6 *Line and Load Regulation*

11.6.1 Line Regulation (Full load)

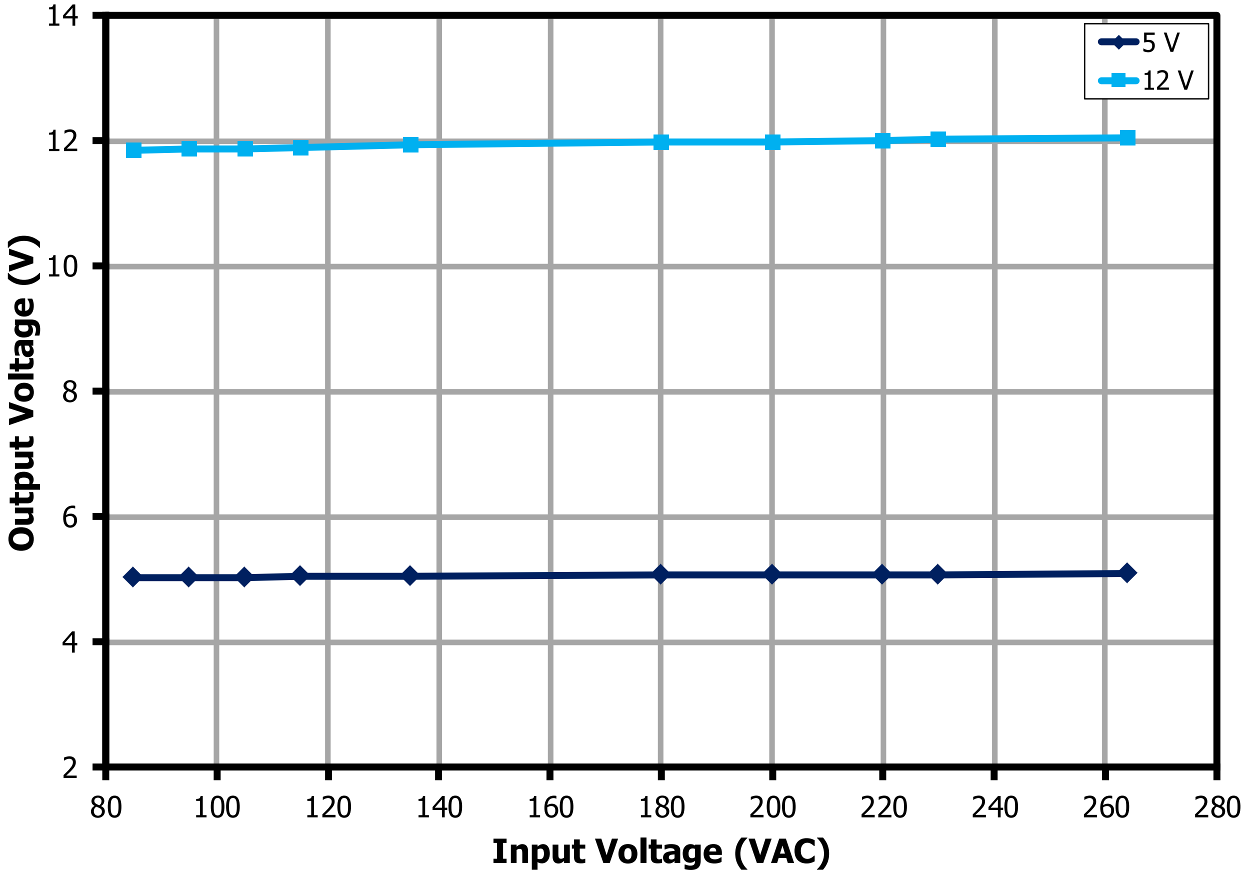

Figure 15 – Output Voltage vs. Input Line Voltage, Room Temperature.

	5 V	**12 V**
Min.	5.03 V	11.87 V
Max.	5.09 V	12.04 V

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11.6.2 Cross Load Regulation

11.6.2.1 12 V Load Change with Full Load on 5 V

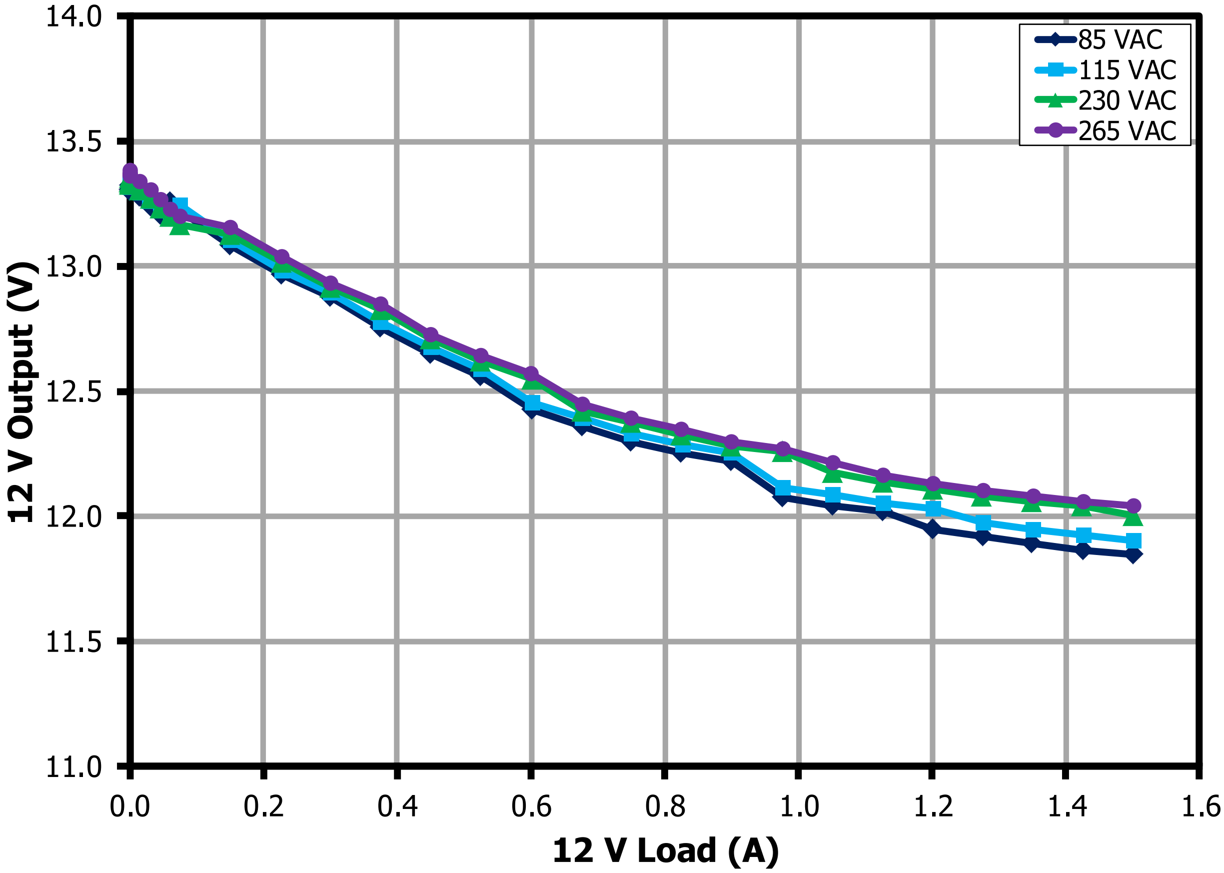

Figure 16 – 12 V Output Voltage vs. Output Load, Room Temperature.

	5 V	**12 V**
Min.	4.93 V	11.85 V
Max.	5.04 V	13.39 V

11.6.2.2 12 V Load Change with No Load on 5 V

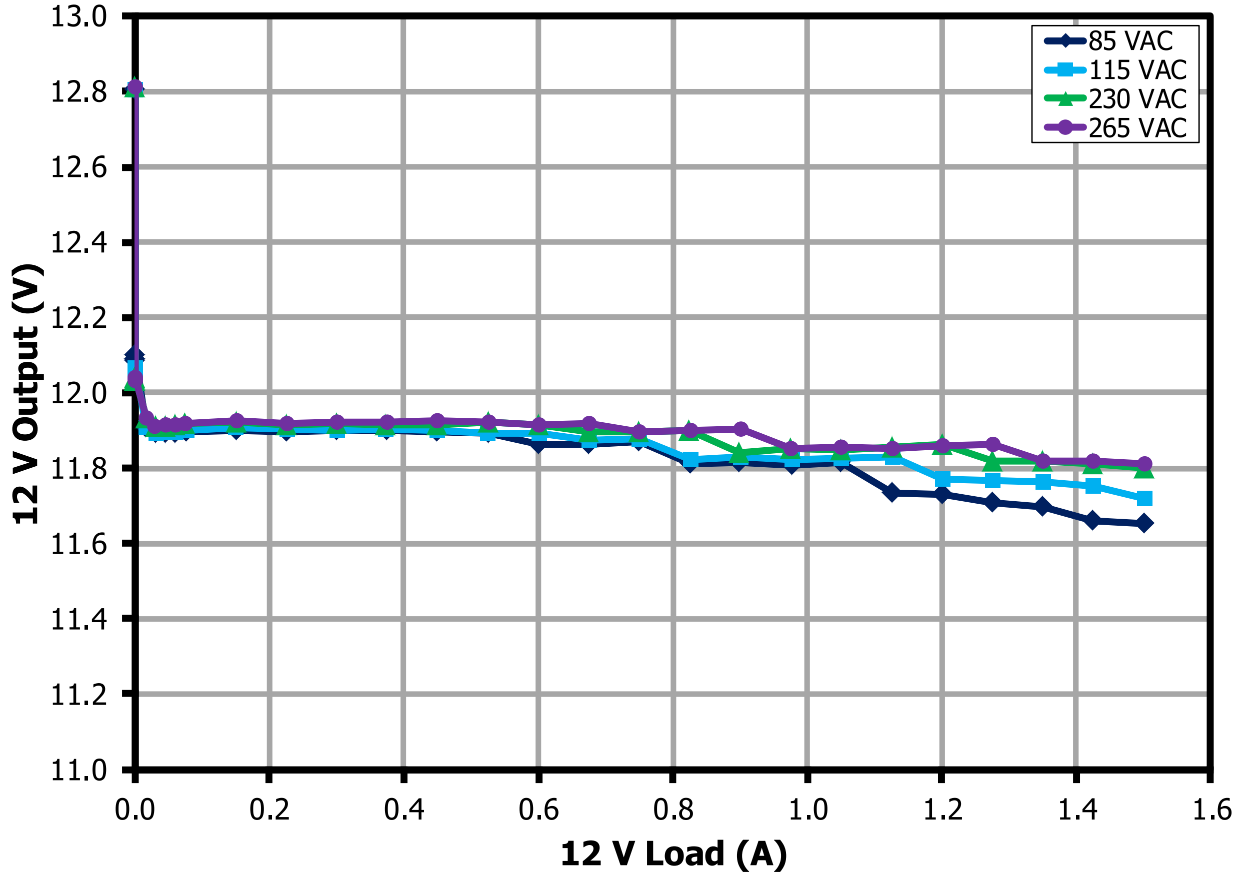

Figure 17 – 12 V Output Voltage vs. Output Load, Room Temperature.

	5 V	**12 V**
Min.	5.05 V	11.65 V
Max.	5.20 V	12.81 V

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11.6.2.3 5 V Load Change with Full Load on 12 V

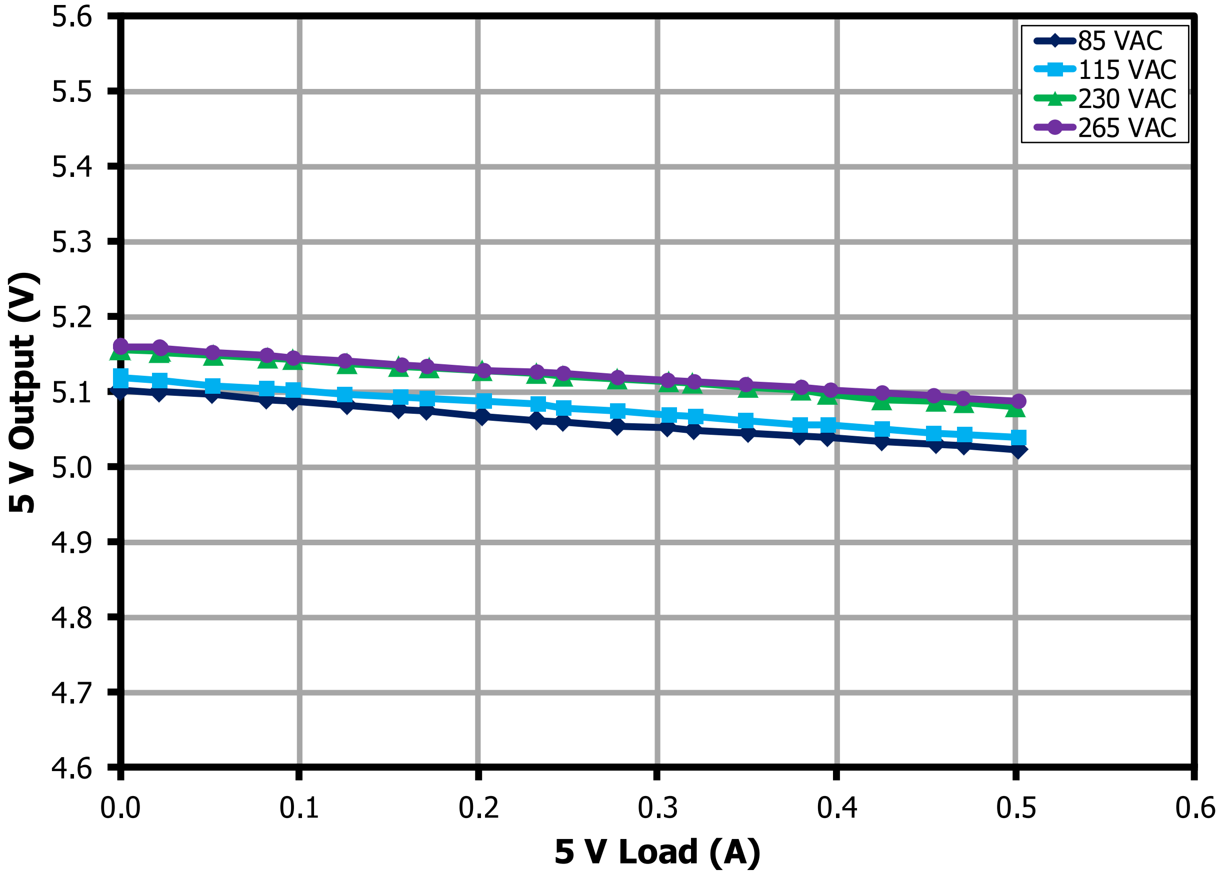

Figure 18 – 5 V Output Voltage vs. Output Load, Room Temperature.

	5 V	12 V
Min.	5.02 V	11.66 V
Max.	5.16 V	11.86 V

11.6.2.4 5 V Load Change with No Load on 12 V

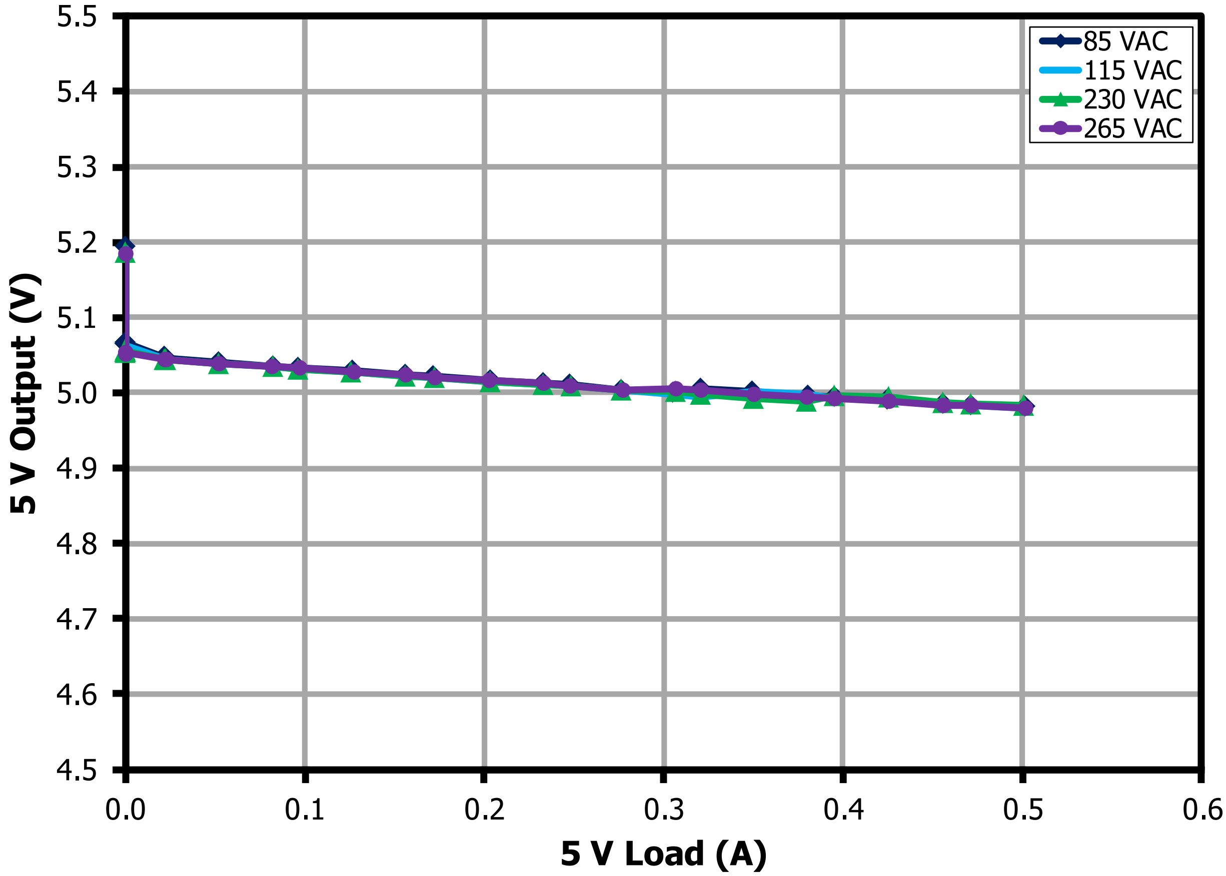

Figure 19 – 5 V Output Voltage vs. Output Load, Room Temperature**.**

	5 V	**12 V**
Min.	4.98 V	11.77 V
Max.	5.19 V	13.33 V

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12 Thermal Performance

12.1 *85 VAC*

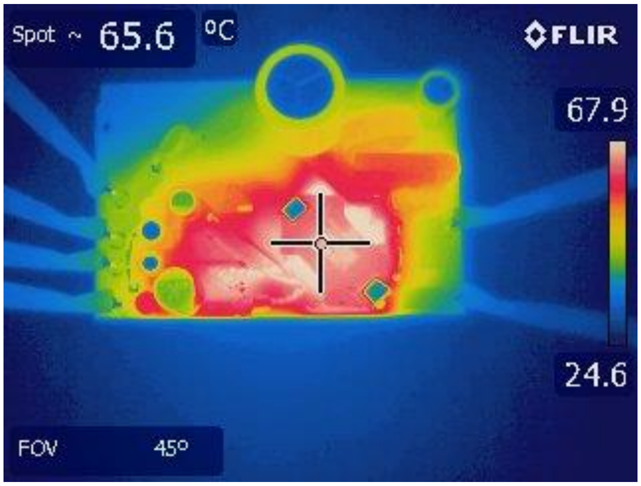

Figure 20 – Transformer Side. 85 VAC, Full Load.

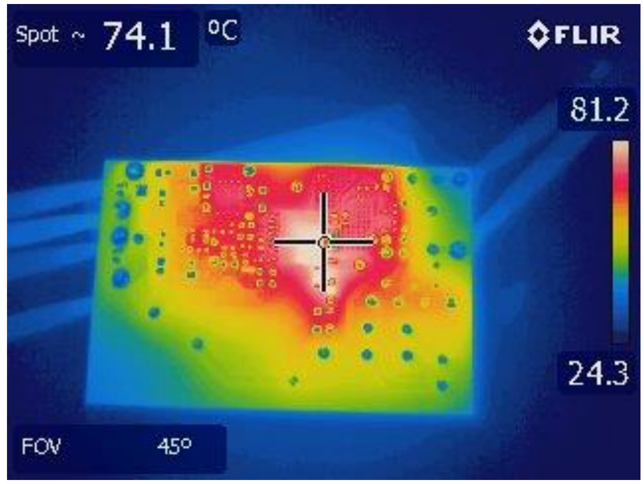

Figure 21 – InnoSwitch-EP Side. 85 VAC, Full Load.

	Reference	ºC
Ambient		25.5
Transformer	T1	67
Input Capacitor	C2	45.5
Bridge Rectifier	BR1	62.6
CMC	L1	55.3
12 V Choke	L5	59.2
12 V Capacitor	C10	40.8
5 V Choke	L4	48.4

	Reference	ºC
Ambient		26.9
InnoSwitch-EP	U1	83
SR FET Q1	Q1	68
SR FET Q2	Q2	64
Snubber Resistor	R7	65
Clamp Resistor	R2	84

12.2 ***110 VAC***

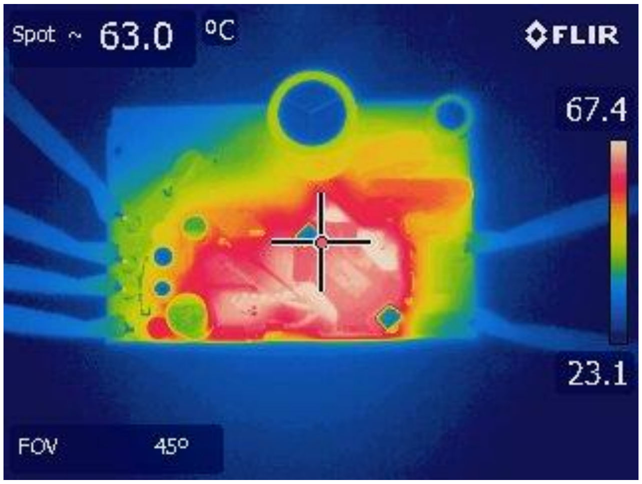

Figure 22 – Transformer Side. 110 VAC, Full Load.

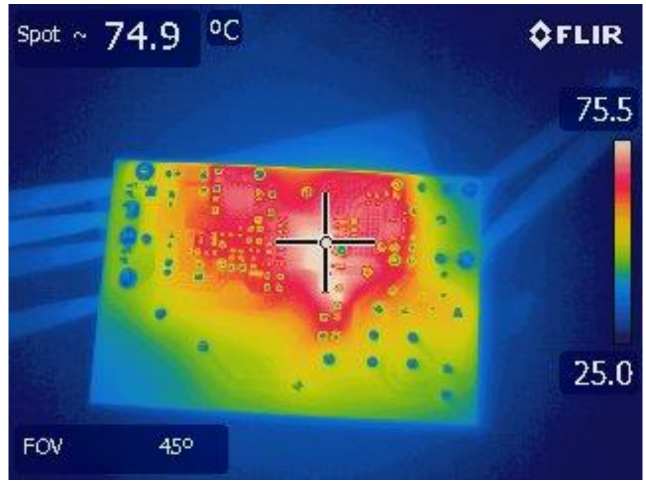

Figure 23– InnoSwitch-EP Side. 110 VAC, Full Load.

	Reference	ºC
Ambient		25.7
Transformer	T1	65.8
Input Capacitor	C2	42.6
Bridge Rectifier	BR1	57.8
CMC	L1	49.9
12 V Choke	L5	57.3
12 V Capacitor	C10	40.8
5 V Choke	L4	50

	Reference	ºC
Ambient		26.8
InnoSwitch-EP	U1	76
SR FET Q1	Q1	67
SR FET Q2	Q2	63
Snubber Resistor	R7	64
Clamp Resistor	R2	78

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12.3 ***230 VAC***

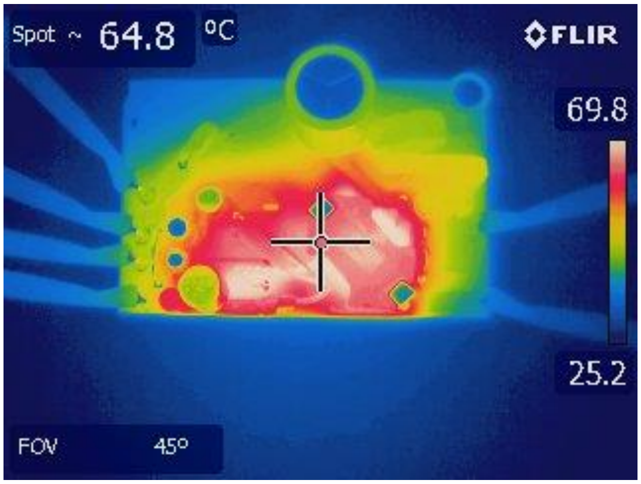

Figure 24 – Transformer Side. 230 VAC, Full Load.

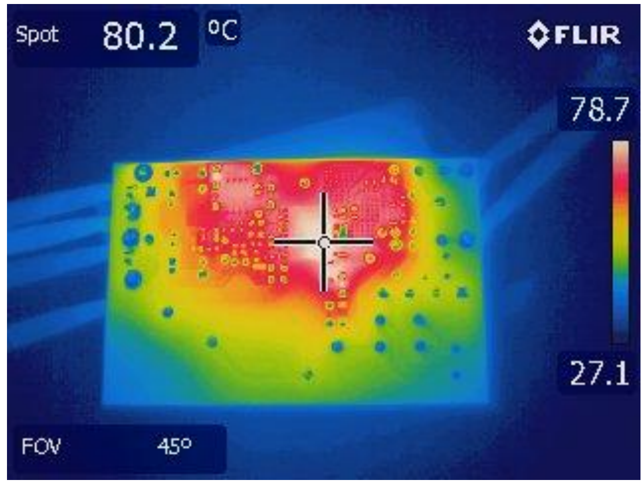

Figure 25 – InnoSwitch-EP Side. 230 VAC, Full Load.

	Reference	**ºC**
Ambient		26.3
Transformer	T1	66.4
Input Capacitor	C2	41
Bridge Rectifier	BR1	46.2
CMC	L1	41.1
12 V Choke	L5	61.2
12 V Capacitor	C10	42.4
5 V Choke	L4	51.6

	Reference	**ºC**
Ambient		26.6
InnoSwitch-EP	U1	80.5
SR FET Q1	Q1	72.9
SR FET Q2	Q2	66.9
Snubber Resistor	R7	71.2
Clamp Resistor	R2	77.8

12.4 ***265 VAC***

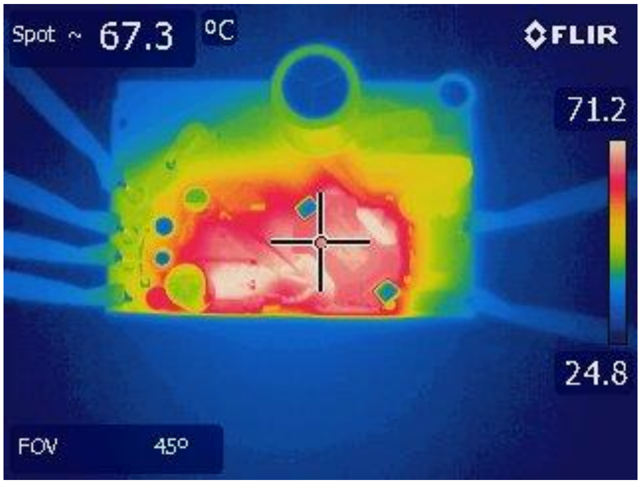

Figure 26 – Transformer Side. 265 VAC, Full Load.

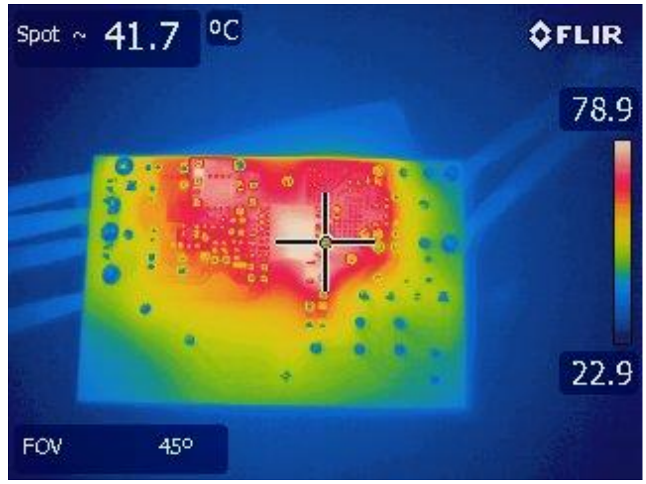

Figure 27 – InnoSwitch-EP Side. 265 VAC, Full Load.

	Reference	ºC
Ambient		26.3
Transformer	T1	67.3
Input Capacitor	C2	39.8
Bridge Rectifier	BR1	45.5
CMC	L1	40
12 V Choke	L5	61.2
12 V Capacitor	C10	43.3
5 V Choke	L4	49.5

	Reference	ºC
Ambient		26.5
InnoSwitch-EP	U1	81.4
SR FET Q1	Q1	74.3
SR FET Q2	Q2	64.3
Snubber Resistor	R7	70.2
Clamp Resistor	R2	78

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13 Waveforms

13.1 ***Load Transient Response***

13.1.1 50% 12 V Load Transient

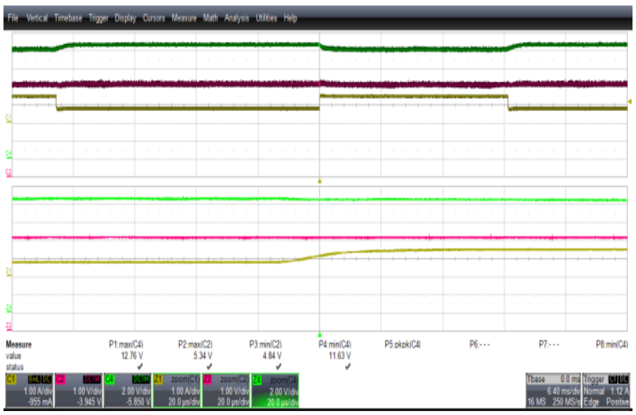

Figure 28 – 0.75 A – 1.5 A, 12 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 4.85 V.
5 V_{MAX}: 5.34 V.
12 V_{MIN}: 11.63 V.
12 V_{MAX}: 12.76 V.
Upper: 12 V_{OUT}, 2 V / div.
Middle: 5 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 6.4 ms, 20 μs / div.

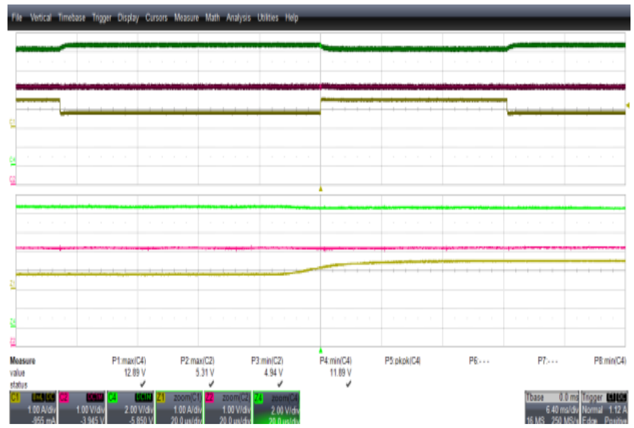

Figure 29 – 0.75 A – 1.5 A, 12 V Load Step Transient Response. 265 VAC.
5 V_{MIN}: 4.94 V.
5 V_{MAX}: 5.31 V.
12 V_{MIN}: 11.89 V.
12 V_{MAX}: 12.89 V.
Upper: 12 V_{OUT}, 2 V / div.
Middle: 5 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 6.4 ms, 20 μs / div.

13.2 *Switching Waveforms*

13.2.1 InnoSwitch-EP Waveforms

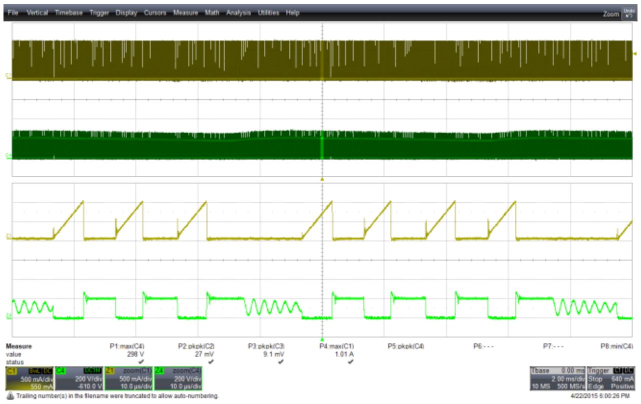

Figure 30 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 2 ms, 10 µs / div.

Figure 31 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (537 V_{MAX}).
Lower: I_{DRAIN}, 500 mA / div.
Upper: V_{DRAIN}, 200 V, 2 ms, 10 µs / div.

13.2.2 InnoSwitch-EP Drain Voltage and Current Waveforms During Start-up and Shorted Output

Start-Up

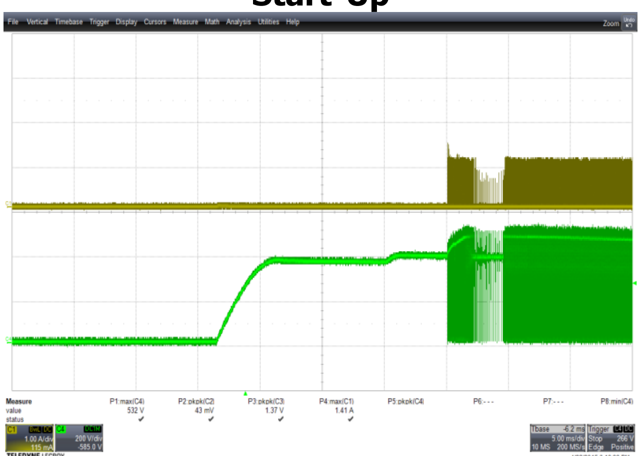

Figure 32 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (532 V_{MAX}).
Lower: I_{DRAIN}, 1 A / div.
Upper: V_{DRAIN}, 200 V, 5 ms / div.

Shorted Output

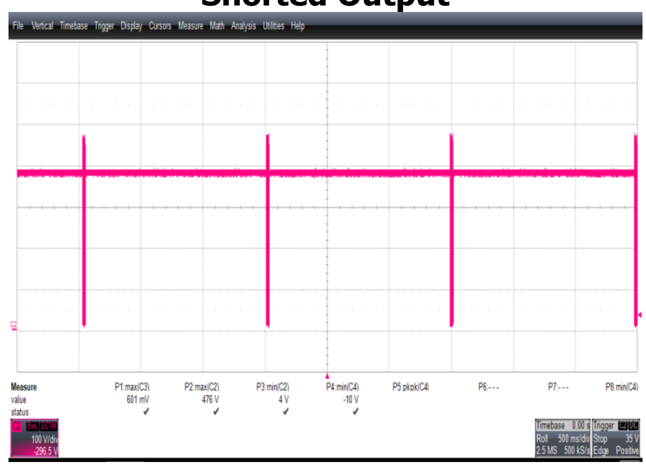

Figure 33 – Drain Voltage and Current Waveforms.
265 VAC Input, (476 V_{MAX}).
V_{DRAIN}, 100 V, 500 ms / div.

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13.2.3 SR FET Waveforms

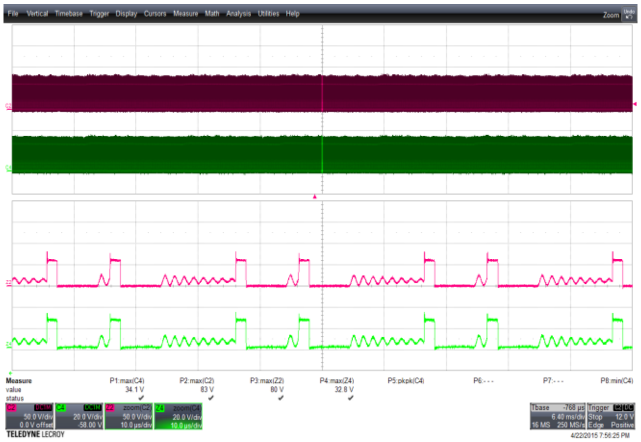

Figure 34 – SR FET Voltage Waveforms.
265 VAC Input, Full Load.
(83 V_{MAX} for 12 V, 34 V_{MAX} for 5 V.)
Lower: 12 V, 50 V / div.
Upper: 5 V, 20 V /, 6.4 ms, 10 μs / div.

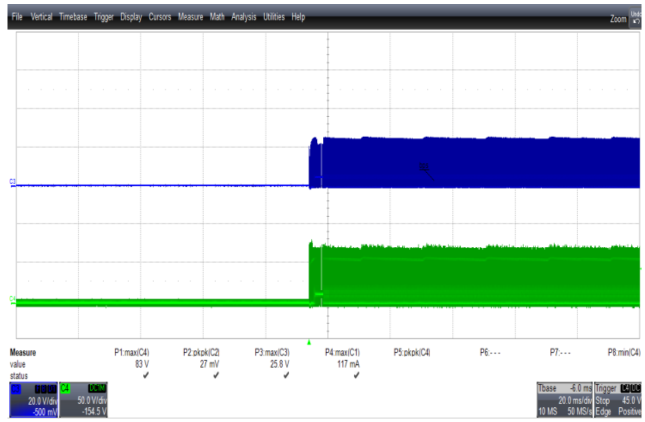

Figure 35 – SR FET Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
Lower: 12 V, 50 V / div.
Upper: 5 V, 20 V /, 6.4 ms, 10 μs / div.

13.2.4 Output Voltage and Current Waveforms During Start-Up

13.2.4.1 Full load

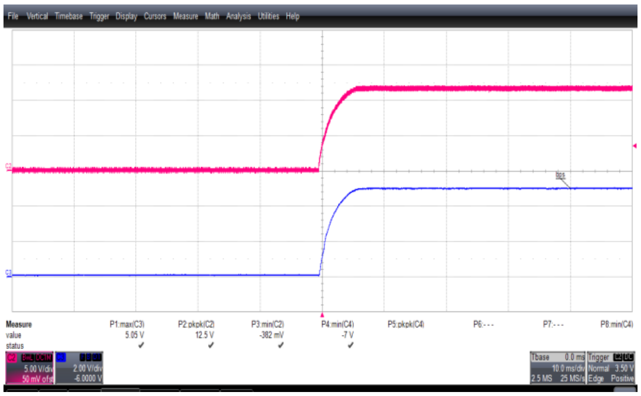

Figure 36 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 5 V, 2 V / div.
Middle: I_{OUT}, 1 A / div.
Lower: 12 V, 5 V, 1.6 ms / div.

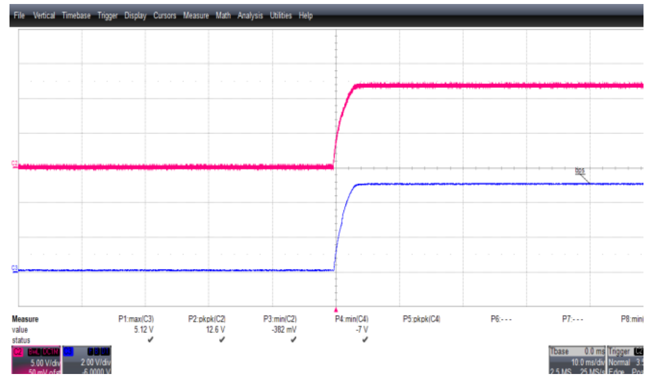

Figure 37 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V, 2 V / div.
Middle: I_{OUT}, 1 A / div.
Lower: 12 V, 5 V, 1.6 ms / div.

13.2.4.2 No-Load

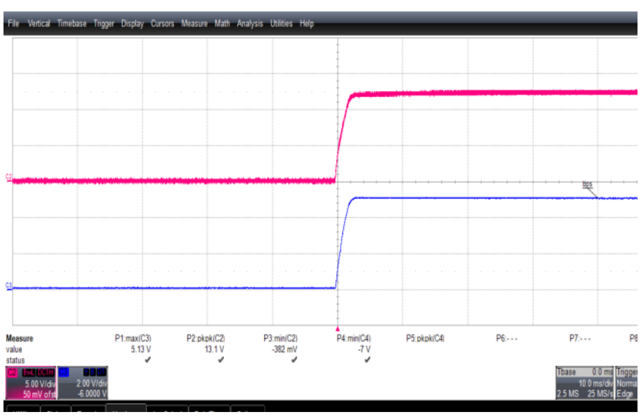

Figure 38 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 5 V, 2 V / div.
Middle: I_{OUT}, 1 A / div.
Lower: 12 V, 5 V, 1.6 ms / div.

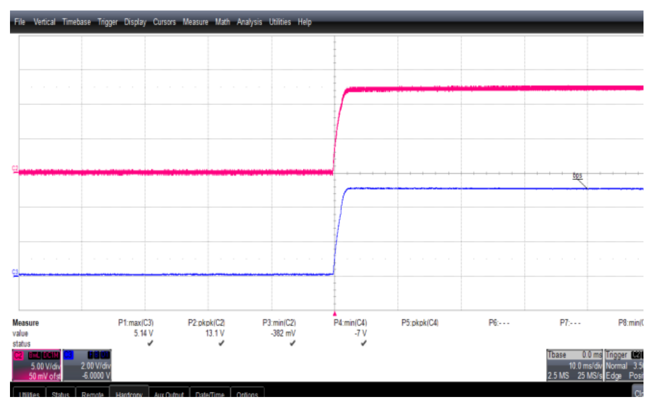

Figure 39 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V, 2 V / div.
Middle: I_{OUT}, 1 A / div.
Lower: 12 V, 5 V, 1.6 ms / div.

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13.2.5 Output Voltage and Current Waveform with Shorted Output (12 V)

Figure 40 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: I_{OUT}, 2 A / div.
Middle: 12 V, 2 V / div.
Lower: 5 V, 1 V, 2 s / div.

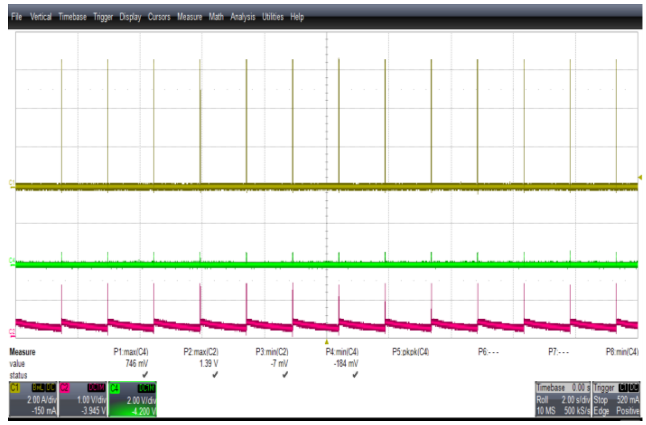

Figure 41 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: I_{OUT}, 2 A / div.
Middle: 12 V, 2 V / div.
Lower: 5 V, 1 V, 2 s / div.

13.2.6 Output Voltage and Current Waveform with Open Feedback Loop

Latched off for overvoltage protection (Loop opened while power supply was in operation)

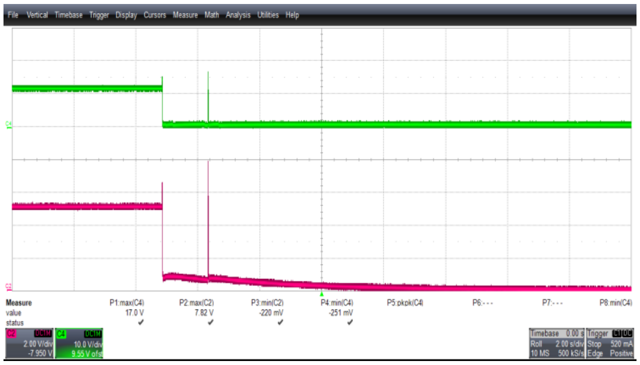

Figure 42 – Output Voltage Waveform.
85 VAC Input.
Upper: 12 V, 10 V / div.
Lower: 5 V, 2 V /, 2 s / div.

Figure 43 – Output Voltage Waveform.
265 VAC Input.
Upper: 12 V, 10 V / div.
Lower: 5 V, 2 V /, 2 s / div.

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13.3 *Output Ripple Measurements*

13.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

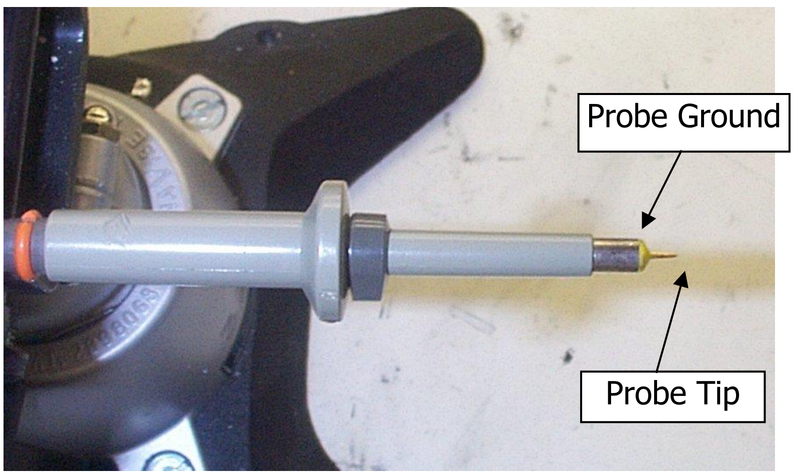

Figure 44 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

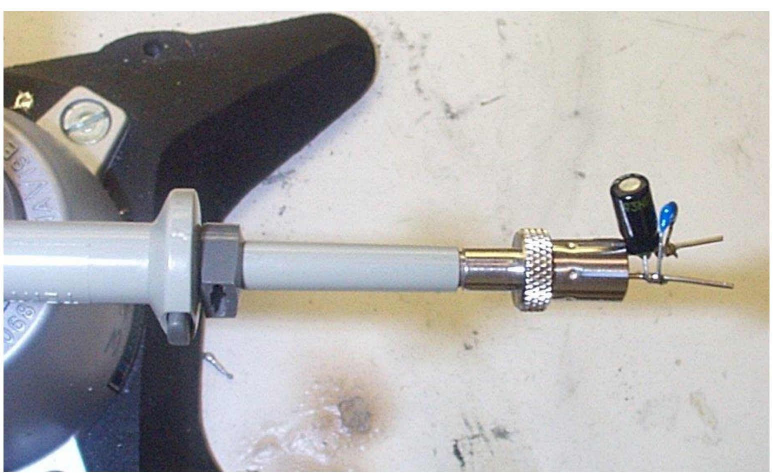

Figure 45 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.3.2 Ripple Voltage Waveforms

13.3.2.1 0.5 A Load on 5 V

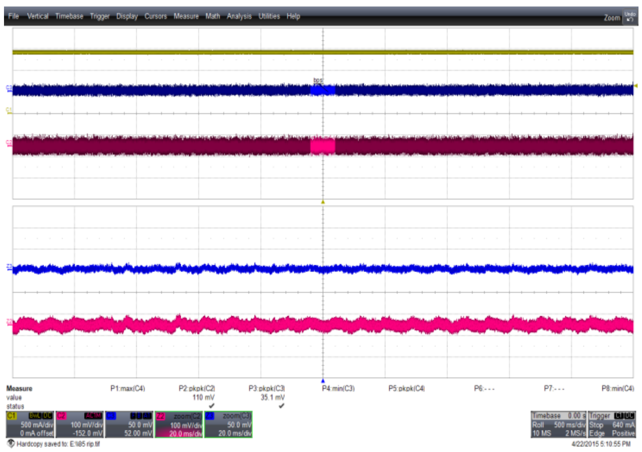

Figure 46 – Output Voltage ripple Waveforms.
85 VAC Input. **1.5 A on 12 V.**
5 V_{PK}: 35 mV, 12 V_{PK}: 110 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

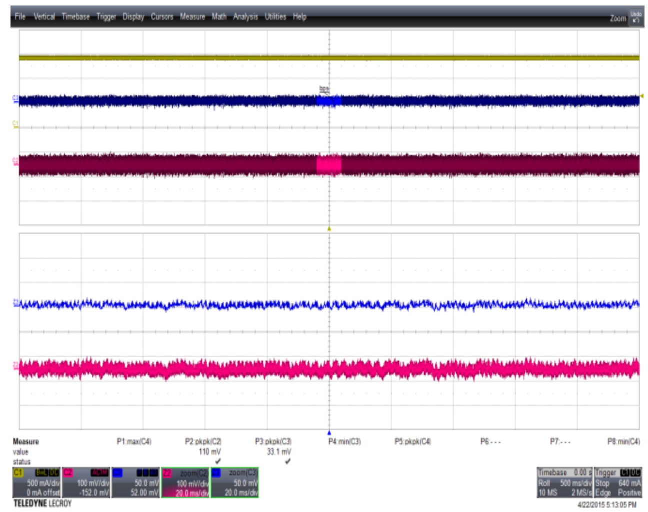

Figure 47 – Output Ripple Voltage Waveforms**.**
265 VAC Input. **1.5 A on 12 V.**
5 V_{PK}: 33 mV, 12 V_{PK}: 110 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

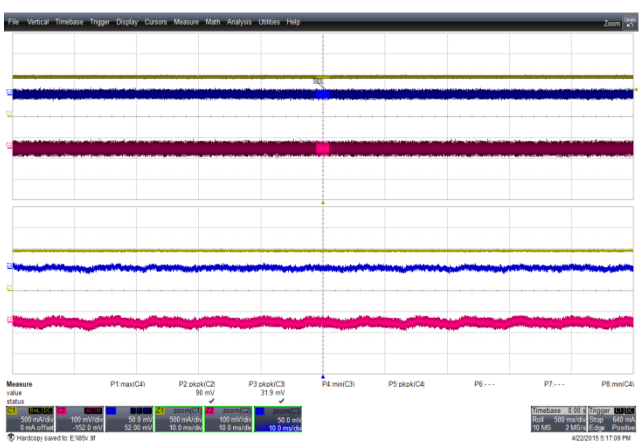

Figure 48 – Output Ripple Voltage Waveforms.
85 VAC Input. **1.0 A on 12 V.**
5 V_{PK}: 32 mV, 12 V_{PK}: 90 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

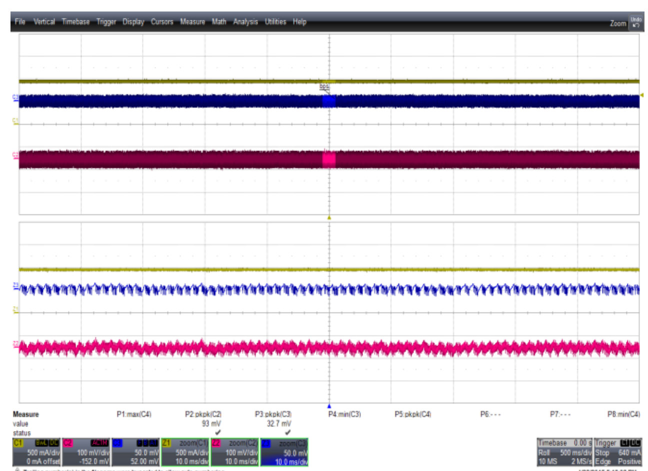

Figure 49 – Output Ripple Voltage Waveforms.
265 VAC Input**. 1.0 A on 12 V.**
5 V_{PK}: 33 mV, 12 V_{PK}: 93 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

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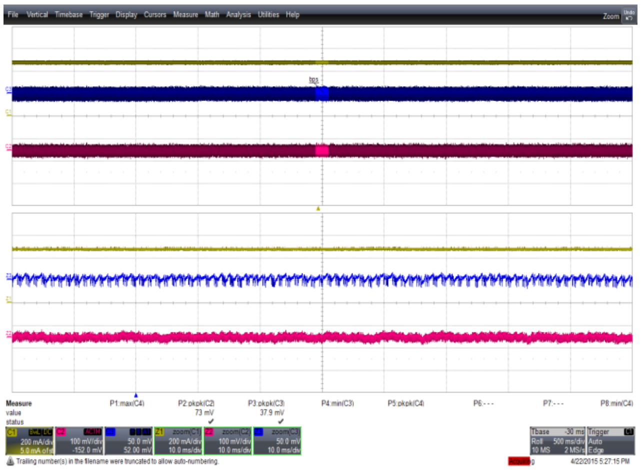


Figure 50 – Output Ripple Voltage Waveforms.
85 VAC Input, **0.5 A on 12 V.**
5 V_{PK}: 38 mV, 12 V_{PK}: 73 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

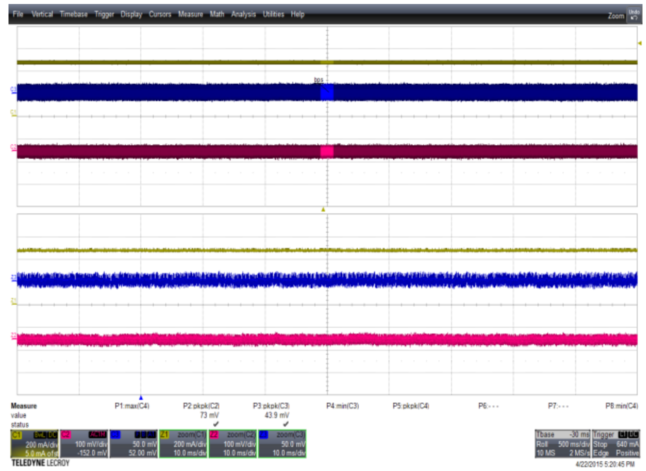


Figure 51 – Output Ripple Voltage Waveforms.
265 VAC Input, **0.5 A on 12 V.**
5 V_{PK}: 44 mV, 12 V_{PK}: 73 mV.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 100 mV /, 500 ms, 20 ms / div.

13.4 *Line Undervoltage and Overvoltage (DC Input)*

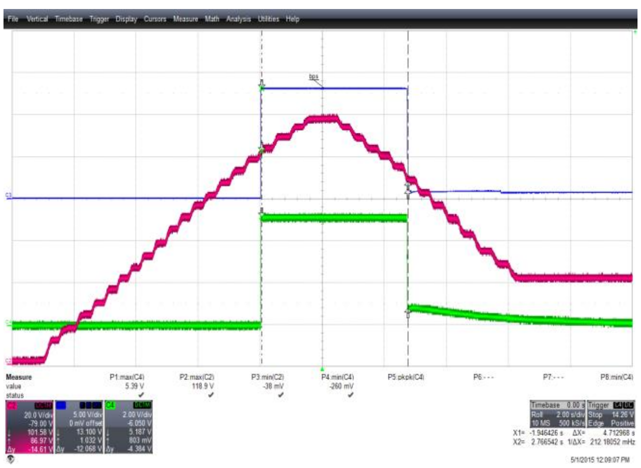


Figure 52 – Line Undervoltage.
DC Input, No-Load.
V_{UV+}: 101.6 V, V_{UV-}: 87 V
Upper: 12 V , 5 V / div.
Middle: 5 V, 2 V / div.
Lower: Input, 20 V /, 2 s / div.

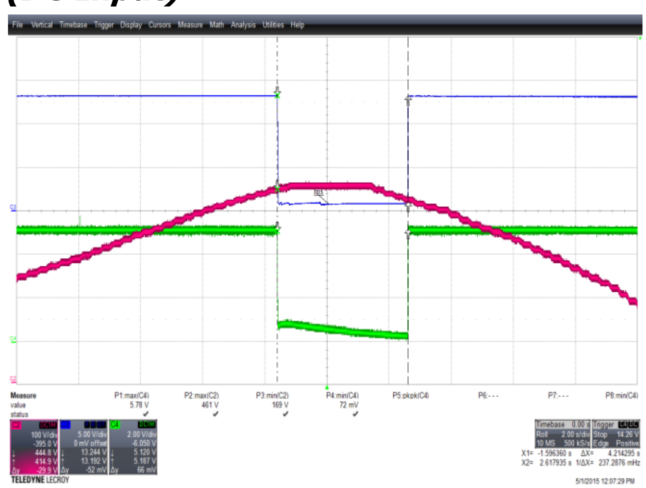


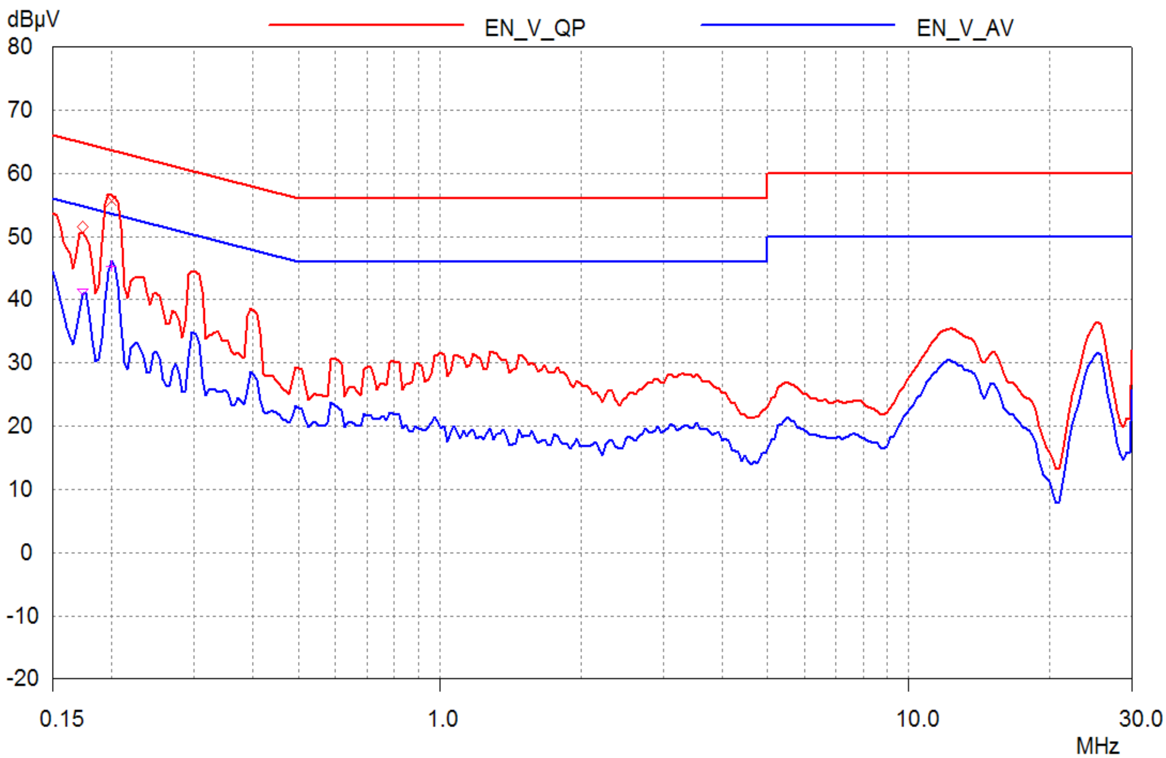
Figure 53 – Line Overvoltage.
DC Input, No-Load.
V_{OV+}: 445 V, V_{OV-}: 415 V
Upper: 12 V , 5 V / div.
Middle: 5 V, 2 V / div.
Lower: Input, 100 V /, 2 s / div.

14 EMI

14.1 *Conductive EMI*

14.1.1 Floating Output (QP / AV)

14.1.1.1 110 VAC Input



Frequency (MHz)	QP	Limit	Margin
0.20	55.43	63.63	8.2

Figure 54 – Floating Ground at 110 VAC.

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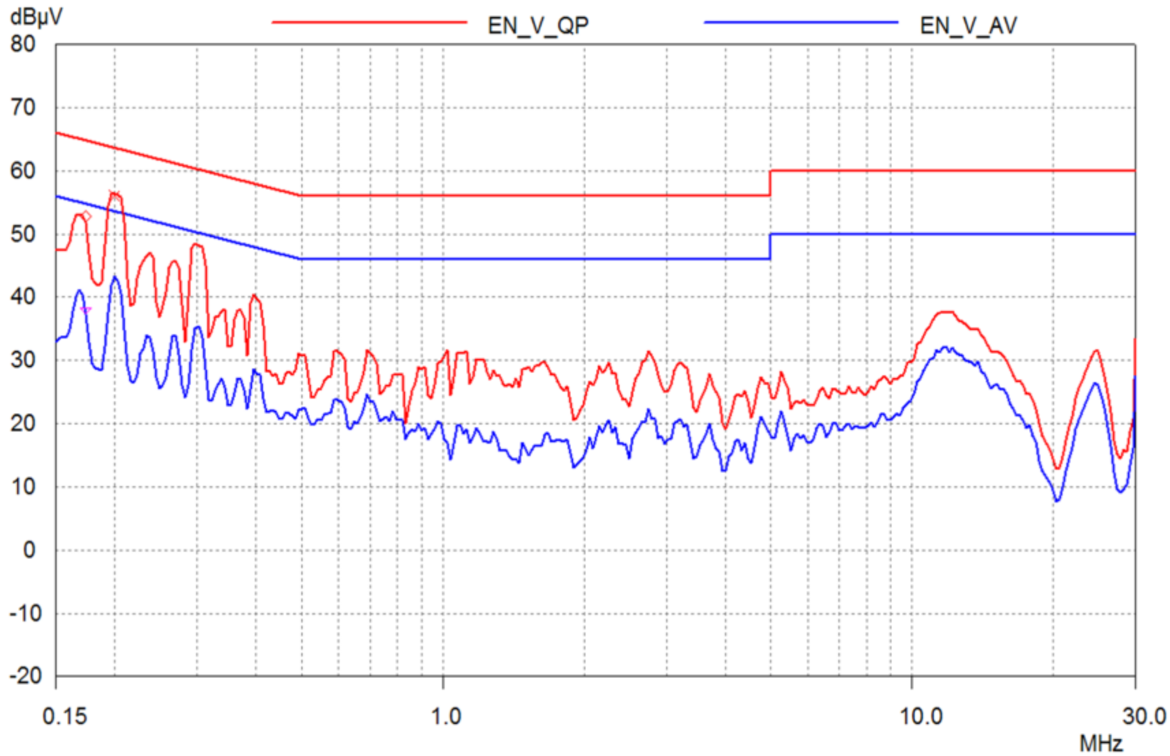
14.1.1.2 230 VAC Input

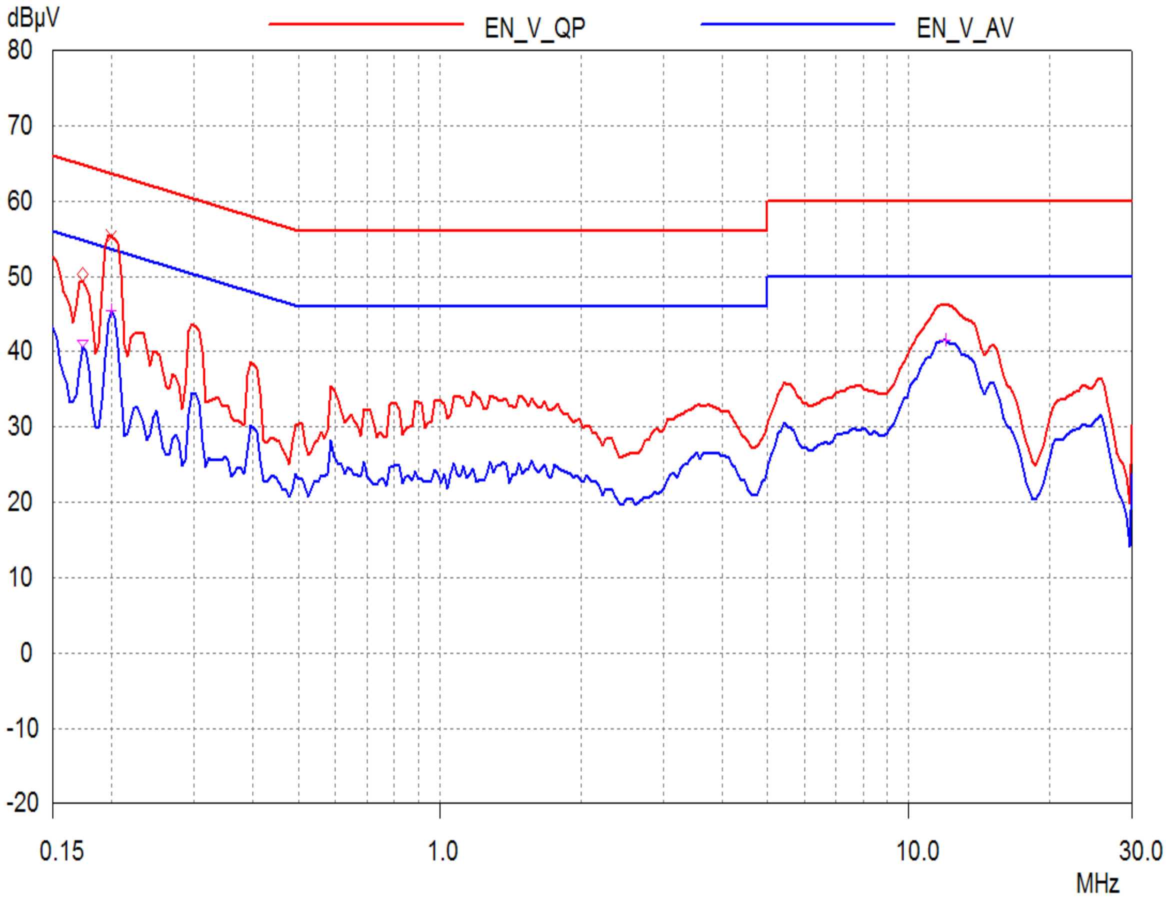


Frequency (MHz)	QP	Limit	Margin
0.20	56.07	63.63	7.56

Figure 55 – Floating Ground at 230 VAC.

14.1.2 Earth Grounded Output (QP / AV)

14.1.2.1 110 VAC Input



Frequency (MHz)	QP	Limit	Margin
0.20	55.36	63.63	8.27
Frequency (MHz)	**AV**	**Limit**	**Margin**
0.20	45.44	53.63	8.19
11.99	41.44	50	8.56

Figure 56 – Earth Ground at 110 VC.

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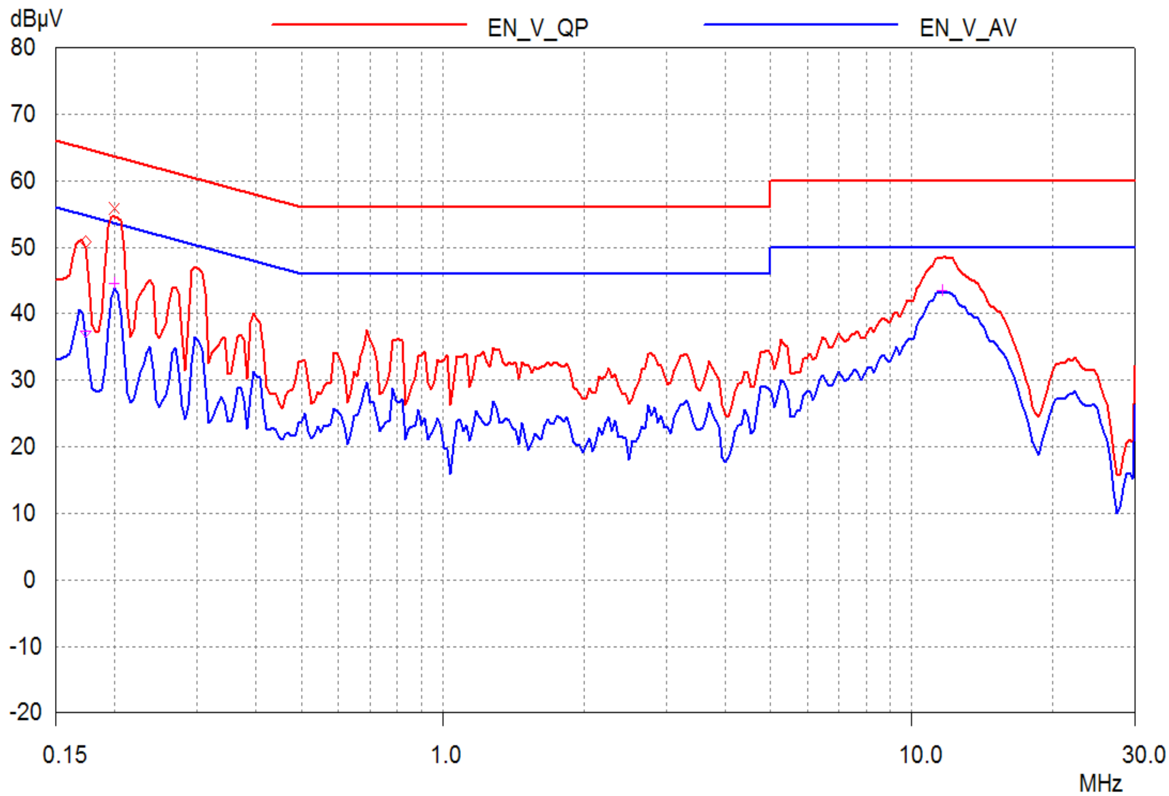
14.1.2.2 230 VAC Input



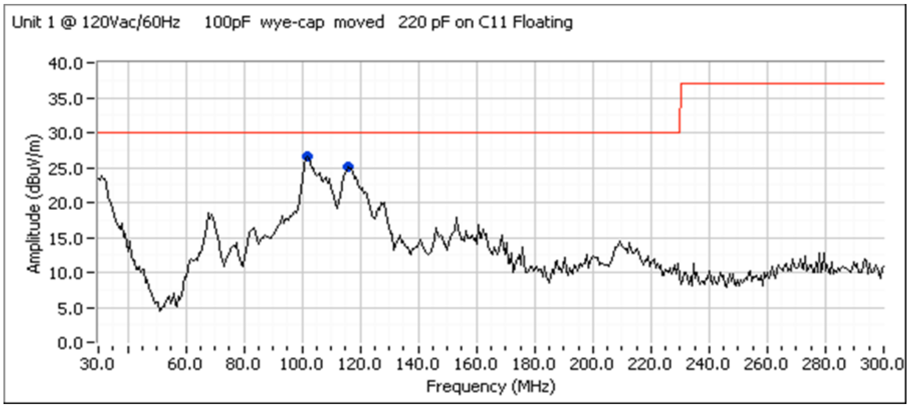
Frequency (MHz)	QP	Limit	Margin
0.20	55.81	63.63	7.82
Frequency (MHz)	**AV**	**Limit**	**Margin**
0.20	44.55	53.63	9.08
11.61	43.52	50	6.48

Figure 57 – Earth Ground at 230 VAC.

14.2 ***Radiated EMI***

14.2.1 Floating Output

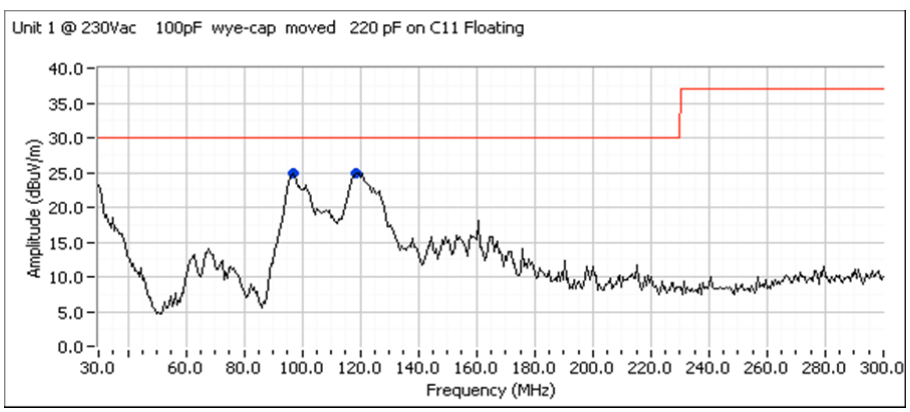
14.2.1.1 110 VAC Input



MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
116.032	**22.5**	V	30.0	**-7.5**	QP	34	1.0
101.964	19.1	V	30.0	-10.9	QP	238	1.0
101.964	***26.6***	*V*	*30.0*	***-3.4***	*Peak*	*224*	*1.0*

Figure 58 – Floating Ground at 110 VAC.

14.2.1.2 230 VAC Input



MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
118.634	**21.6**	V	30.0	**-8.4**	QP	280	1.0
96.602	21.3	V	30.0	-8.7	QP	49	1.0
97.094	*24.8*	*V*	*30.0*	*-5.2*	*Peak*	*61*	*1.0*
118.737	*25.0*	*V*	*30.0*	*-5.0*	*Peak*	*273*	*1.0*

Figure 59 – Floating Ground at 230 VAC.

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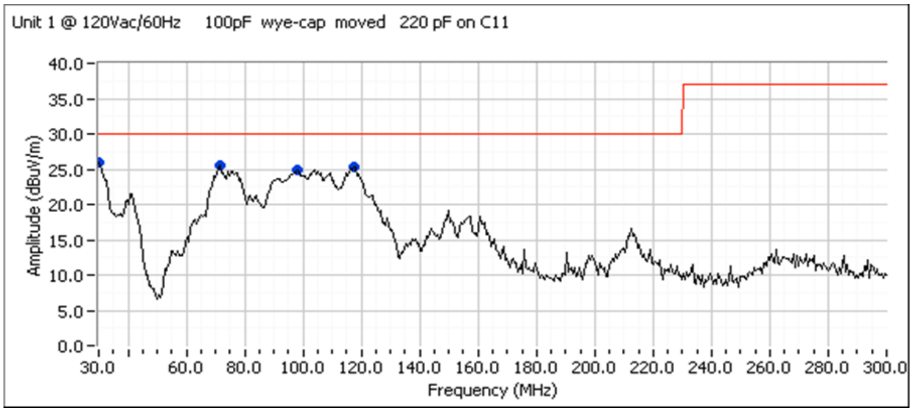
14.2.2 Earth Grounded Output

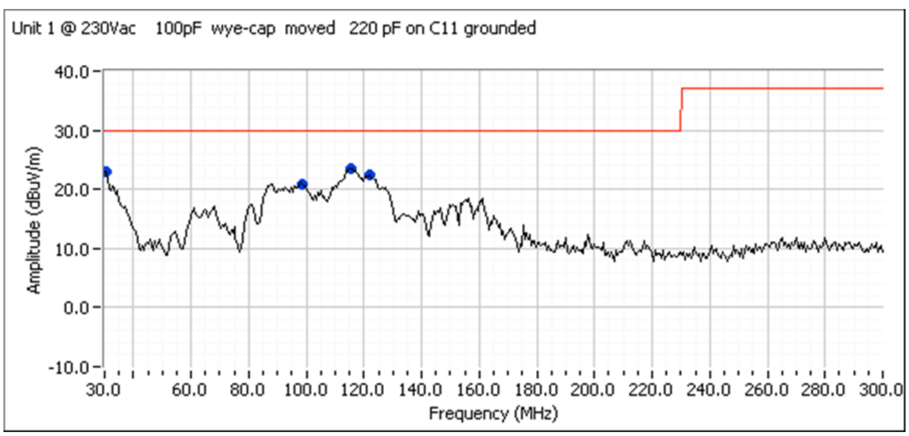
14.2.2.1 110 VAC Input



MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
71.663	***25.5***	*V*	*30.0*	***-4.5***	*Peak*	*256*	*1.0*
118.196	*25.3*	*V*	*30.0*	*-4.7*	*Peak*	*31*	*1.0*
98.176	*24.9*	*V*	*30.0*	*-5.1*	*Peak*	*126*	*1.0*

Figure 60 – Earth Ground at 110 VAC.

14.2.2.2 230 VAC Input



MHz	dBµV/m	v/h	Limit	Margin	Pk/QP/Avg	degrees	meters
71.663	***25.5***	*V*	*30.0*	***-4.5***	*Peak*	*256*	*1.0*
118.196	*25.3*	*V*	*30.0*	*-4.7*	*Peak*	*31*	*1.0*
98.176	*24.9*	*V*	*30.0*	*-5.1*	*Peak*	*126*	*1.0*

Figure 61 – Earth Ground at 230 VAC**.**

15 Lighting Surge Test

15.1 *Differential Mode Test*

Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
1	90	2	10	PASS
1	270	2	10	PASS

15.2 *Common Mode Test*

Passed ±6 kV, 500 A ring wave test

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
6	90	12	10	PASS
-6	90	12	10	PASS
6	270	12	10	PASS
-6	270	12	10	PASS

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16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
15-Sep-15	DK	1.0	Initial Release	Apps & Mktg
30-Oct-15	DK	1.1	Updated No-Load Graph and Photographs of Assembled Boards. Added Magnetics Source.	
22-Dec-15	DK	1.2	Updated Transformer Information and Figure 13.	
04-Feb-16	KM	1.3	Updated Figure 53 Caption	

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