74LV74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 1 — 23 September 2013

Product data sheet

1. General description

The 74LV74-Q100 is a dual positive edge triggered, D-type flip-flop. It has individual data (nD) inputs, clock (nCP) inputs, set (nSD) and (nRD) inputs, and complementary nQ and nQ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-833, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

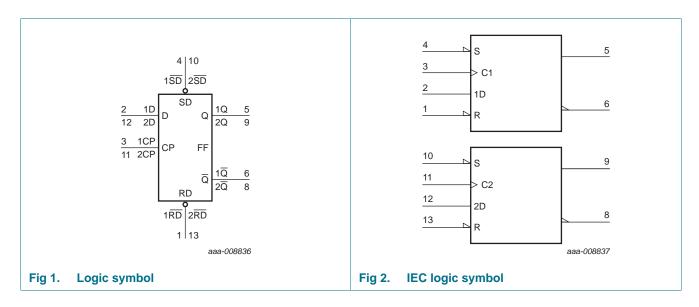
3. Ordering information

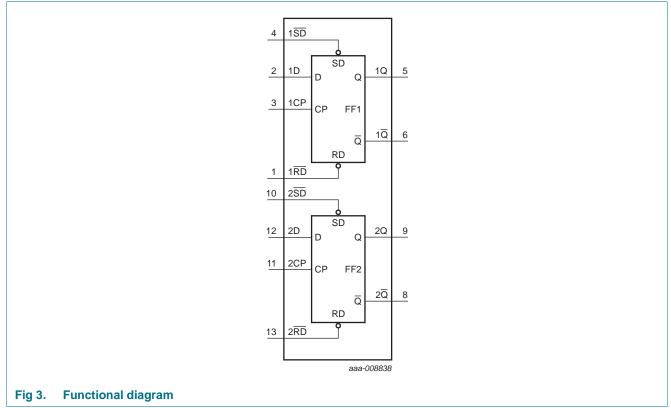
Table 1. Ordering information

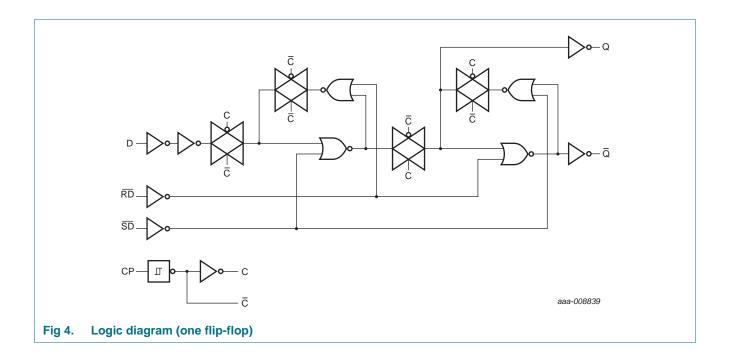
Type number	Package										
	Temperature range	Name	Description	Version							
74LV74D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1							
74LV74PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							



4. Functional diagram

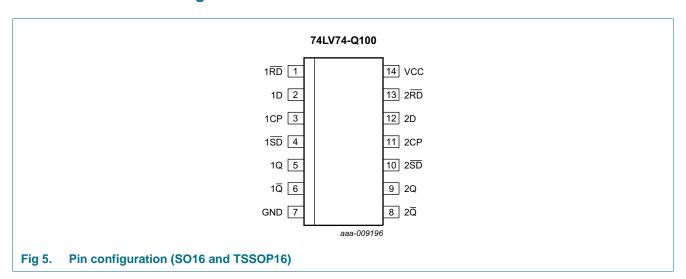






5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active-LOW)
1D	2	data inputs
1CP	3	clock input (LOW-to-HIGH), edge-triggered)
1SD	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop outputs
1Q	6	complement flip-flop outputs
GND	7	ground (0 V)
2Q	8	complement flip-flop outputs
2Q	9	true flip-flop outputs
2SD	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered)
2D	12	data inputs
2RD	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input				Output	Output							
nSD	nRD	nCP	nD	nQ	nQ	Q _{n+1}	nQ _{n+1}					
L	Н	X	X	Н	L	-	-					
Н	L	Х	X	L	Н	-	-					
L	L	Х	X	Н	Н	-	-					
Н	Н	↑	L	-	-	L	Н					
Н	Н	↑	Н	-	-	Н	L					

^[1] H = HIGH voltage level;

L = LOW voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		<u>[1]</u>	-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$		-	20	mA
VI	input voltage		<u>[1]</u>	-0.5	+7	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$		-	±50	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I _{CC}	supply current			-	±50	mA
I _{GND}	ground current			-	±50	mA
T _{stg}	storage temperature			- 65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$				
		SO16 package	<u>[</u>	2] _	500	mW
		TSSOP16 package	<u>[</u>	3] _	400	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

X = don't care;

^{↑ =} LOW-to-HIGH clock transition;

 Q_{n+1} = state after the next LOW-to-HIGH CP transition

^[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

^[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage	<u>[1]</u>	1.0	3.3	5.5	V
VI	input voltage		0	-	V_{CC}	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 1.0 \text{ V to } 2.0 \text{ V}$	0	-	500	ns/V
		$V_{CC} = 2.0 \text{ V to } 2.7 \text{ V}$	0	-	200	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	100	ns/V
		$V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$	0	-	50	ns/V

^[1] LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}). DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions	-40	°C to +8	35 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-	V
V_{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	-	$0.3 \times V_{CC}$	
V _{OH} HIGH-level		$V_I = V_{IH}$ or V_{IL} ; $I_O = -100 \mu A$						
	output voltage	V _{CC} = 1.2 V	-	1.2		-		
		V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		$V_{CC} = 3.0 \text{ V}; I_{O} = -6 \text{ mA}$	2.40	2.82	-	2.20	-	V
		$V_{CC} = 4.5 \text{ V}; I_O = -12 \text{ mA}$	3.60	4.20	-	3.50	-	V
V_{OL}	LOW-level	$V_I = V_{IH} \text{ or } V_{IL}; \ I_O = 100 \ \mu A$						
	output voltage	$V_{CC} = 1.2 \text{ V}$	-	0	-	-	-	
		$V_{CC} = 2.0 \text{ V}$	-	0	0.2		0.2	V
		$V_{CC} = 2.7 \text{ V}$	-	0	0.2		0.2	V
		$V_{CC} = 3.0 \text{ V}$	-	0	0.2		0.2	V
		$V_{CC} = 4.5 \text{ V}$	-	0	0.2		0.2	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		$V_{CC} = 3.0 \text{ V}; I_O = 6 \text{ mA}$	-	0.25	0.40	-	0.50	V
		$V_{CC} = 4.5 \text{ V}; I_{O} = 12 \text{ mA}$	-	0.35	0.55	-	0.65	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	20	-	80	μΑ
ΔI_{CC}	additional supply current	$VI = V_{CC} - 0.6 \text{ V};$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	500	-	850	μΑ
C _I	input capacitance		-	3.5	-			pF

^[1] Typical values are measured at T_{amb} = 25 $^{\circ}C.$

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see Figure 8

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C t	o +125 °C	Uni
				Min	Typ[1]	Max	Min	Max	
pd	propagation	nCP to nQ, $n\overline{Q}$; see Figure 6	[2]						
	delay	V _{CC} = 1.2 V		-	70	-	-	-	ns
		V _{CC} = 2.0 V		-	24	44	-	56	ns
		V _{CC} = 2.7 V		-	18	28	-	41	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	13	26	-	33	ns
		$V_{CC} = 3.3 \text{ V}; C_L = 15 \text{ pF}$		-	11	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	<u>[4]</u>	-	9.5	17	-	23	ns
		nSD to nQ, nQ; see Figure 7							
		V _{CC} = 1.2 V		-	90	-	-	-	ns
		V _{CC} = 2.0 V		-	31	46	-	58	ns
		V _{CC} = 2.7 V		-	23	34	-	43	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	<u>[4]</u>	-	12	19	-	24	ns
		nRD to nQ, nQ; see Figure 7							
		V _{CC} = 1.2 V		-	90	-	-	-	ns
		V _{CC} = 2.0 V		-	31	46	-	58	ns
		V _{CC} = 2.7 V		-	23	34	-	43	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3 \text{ V}; C_L = 15 \text{ pF}$		-	14	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	<u>[4]</u>	-	12	19	-	24	ns
W	pulse width	nCP input HIGH to LOW; see Figure 6							
		V _{CC} = 2.0 V		34	10	-	41	-	ns
		V _{CC} = 2.7 V		25	8	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V _{CC} = 4.5 V to 5.5 V	<u>[4]</u>	15	6	-	18	-	ns
		nSD or nRD pulse width LOW; see Figure 7							
		V _{CC} = 2.0 V		34	10	-	41	-	ns
		V _{CC} = 2.7 V		25	8	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V _{CC} = 4.5 V to 5.5 V	[4]	15	6	-	18	_	ns

Table 7. Dynamic characteristics ...continued GND (ground = 0 V): for test circuit, see <u>Figure 8</u>

Symbol	Parameter	Conditions		-40	0 °C to +8	5 °C	-40 °C t	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{rec}	recovery time	nRD; see Figure 7			'		1		
		V _{CC} = 1.2 V		-	5	-	-	-	ns
		V _{CC} = 2.0 V		14	2	-	15	-	ns
		$V_{CC} = 2.7 \text{ V}$		10	1	-	11	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	<u>[3]</u>	8	1	-	9	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[4]	6	1	-	7	-	ns
t _{su}	set-up time	nD to nCP; see Figure 6							
		V _{CC} = 1.2 V		-	10	-	-	-	ns
		V _{CC} = 2.0 V		22	4	-	26	-	ns
		$V_{CC} = 2.7 \text{ V}$		12	3	-	15	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	<u>[3]</u>	8	2	-	10	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[4]	6	1	-	8	-	ns
t _h	hold time	nD to nCP; see Figure 6							
		V _{CC} = 1.2 V		-	-10	-	-	-	ns
		$V_{CC} = 2.0 \text{ V}$		3	-2	-	3	-	ns
		$V_{CC} = 2.7 \text{ V}$		3	-2	-	3	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		3	-2	-	3	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		3	-2	-	3	-	ns
f _{max}	maximum	nCP; see Figure 6							
	frequency	V _{CC} = 2.0 V		14	40	-	12	-	MHz
		$V_{CC} = 2.7 \text{ V}$		50	90	-	40	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	<u>[3]</u>	60	100	-	48	-	MHz
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	<u>[4]</u>	70	110	-	56	-	MHz
C _{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	<u>[5]</u>	-	24	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C.

f_o = output frequency in MHz;

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs};$

 C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

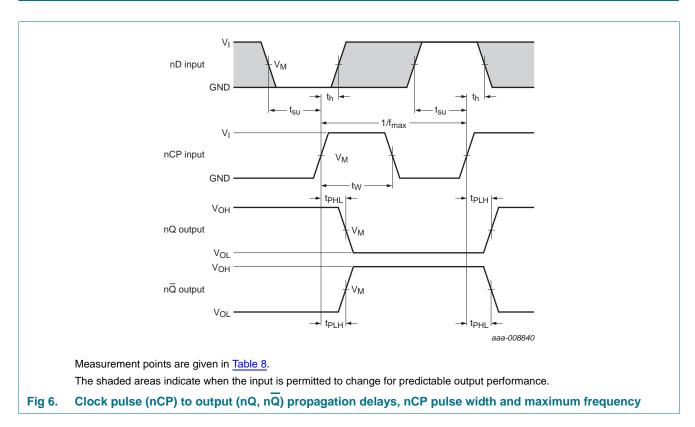
^[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

^[3] Typical value measured at V_{CC} = 3.3 V.

^[4] Typical values are measured at V_{CC} = 5.0 V.

^[5] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) (P_D \text{ in } \mu \text{W})$, where: $f_i = \text{input frequency in MHz}$;

11. Waveforms



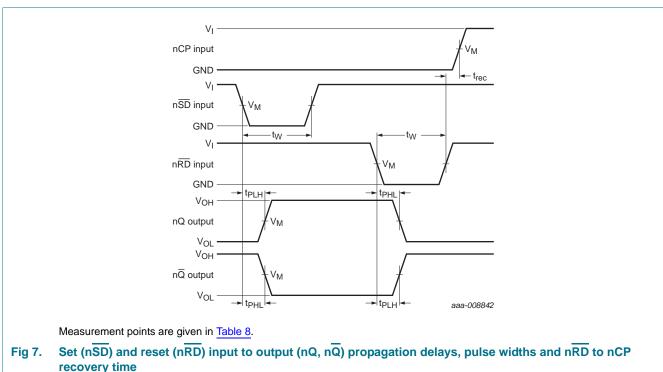
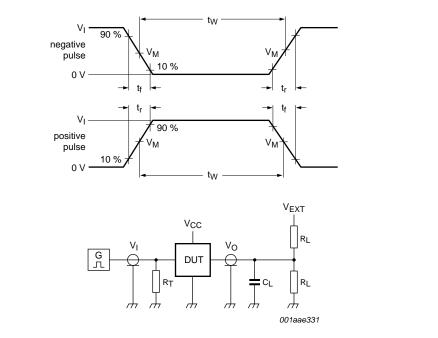


Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
< 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V _{CC}	0.5V _{CC}



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

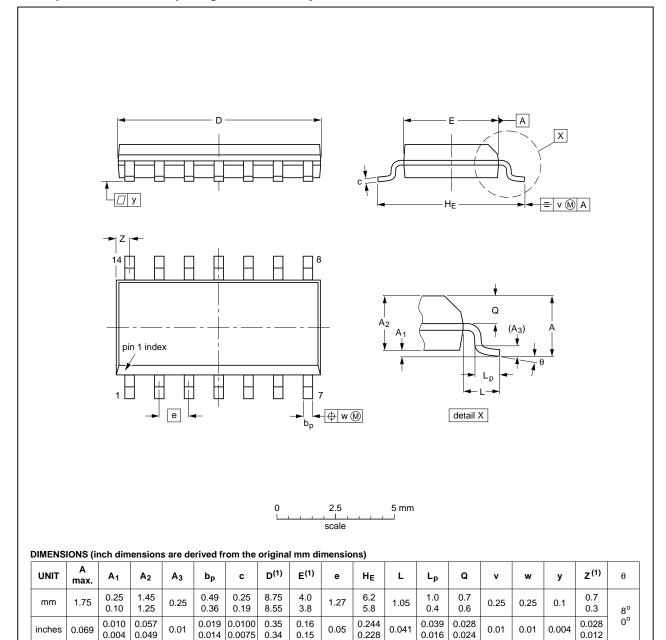
Table 9. Test data

Supply voltage	Input		Load	Load				
	VI	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}			
< 2.7 V	V _{CC} 2.5 ns		50 pF	1 kΩ	open			
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open			
≥ 4.5 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open			

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

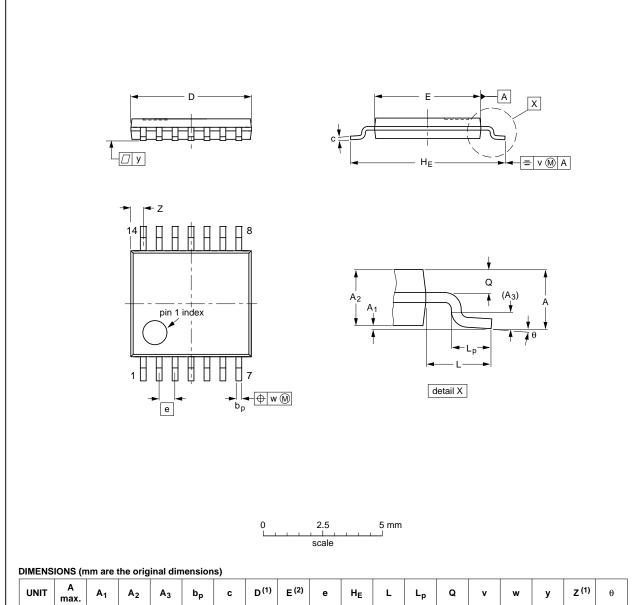
74LV74_Q100

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



_					,		-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

74LV74_Q100

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description	
CMOS	Complementary Metal-Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
НВМ	Human Body Model	
MM	Machine Model	
TTL	Transistor-Transistor Logic	

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74_Q100 v.1	20130923	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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Nexperia 74LV74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А