

PRELIMINARY DATA SHEET

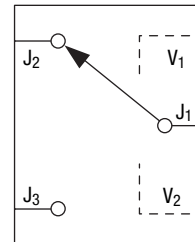
SKY13270-92LF: GaAs SPDT Switch

100 MHz–2.5 GHz

Features

- Broadband: 100 MHz–2.5 GHz
- Very low insertion loss: 0.35 dB typical @ 900 MHz
- High isolation: 24 dB typical @ 900 MHz
- $P_{0.1\text{ dB}}$: 37 dBm typical @ 3 V
- Low current consumption: <100 μA @ 3 V
- Miniature SC-70 6-lead package
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

Functional Block Diagram



Description

The SKY13270-92LF is a PHEMT GaAs FET IC high-linearity SPDT switch. This wideband switch has been designed for use from 100 MHz to 2.5 GHz, where extremely high linearity, low control voltage, high isolation, low insertion loss, and ultraminiature package size are required. It can be controlled with positive, negative, or a combination of both voltages. The RF signal paths within the SKY13270-92 are fully bilateral.


Some standard implementations include T/R switching and diversity switching over 3 W. The SKY13270-92LF switch can be used in many analog and digital wireless communication systems including cellular, GSM and UMTS applications.

Switching is controlled via two control voltage inputs. Depending upon the voltage level applied to the control voltage pins, the common RF port (J_1) is connected to one of two RF ports (J_2 or J_3) via a low insertion loss path, while the path between J_1 and the other RF port is in its isolation state. When the control voltages are toggled, the states between J_1 and J_2 , as well as J_1 and J_3 , are also toggled.

This part is available in a lead (Pb)-free, 6-lead SC-70 package which is RoHS-compliant.

An evaluation board is available upon request.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



Electrical Specifications

V_{CTL} = 0 V/3 V, T = 25 °C, P_{INPUT} = 0 dBm, Z₀ = 50 Ω, unless otherwise noted

| Parameter | Frequency | Min. | Typ. | Max. | Unit |
|----------------|-------------|------|-------|------|------|
| Insertion loss | 0.1–0.5 GHz | | 0.30 | 0.4 | dB |
| | 0.5–1.0 GHz | | 0.35 | 0.5 | dB |
| | 1.0–2.0 GHz | | 0.45 | 0.6 | dB |
| | 2.0–2.5 GHz | | 0.55 | 0.7 | dB |
| Isolation | 0.1–0.5 GHz | 28 | 30 | | dB |
| | 0.5–1.0 GHz | 22 | 24 | | dB |
| | 1.0–2.0 GHz | 17 | 19 | | dB |
| | 2.0–2.5 GHz | 15 | 17 | | dB |
| VSWR | 0.1–1.0 GHz | | 1.2:1 | | |
| | 1.0–2.5 GHz | | 1.3:1 | | |

Operating Characteristics

V_{CTL} = 0 V/3 V, T = 25 °C, P_{INPUT} = 0 dBm, Z₀ = 50 Ω, unless otherwise noted

| Parameter | Condition | Frequency | Min. | Typ. | Max. | Unit |
|-------------------------------------|---|-----------|------|------|------|------|
| Switching characteristics | | | | | | |
| Rise, fall | 0/90% or 90/10% RF | | | 60 | | ns |
| On, off | 50% CTL to 90/10% RF | | | 100 | | ns |
| Video feedthru | T _{RISE} = 1 ns, BW = 500 MHz | | | 50 | | mV |
| Input power for -0.1 dB compression | | 900 MHz | | 37 | | dBm |
| Second, third harmonics | P _{IN} = 34.5 dBm, f _{IN} = 900 MHz | | | -65 | | dBc |
| Thermal resistance | | | | 25 | | °C/W |
| Control voltages | V _{LOW} = 0 @ 20 μA max. V _{HIGH} = 2.5 V @ 100 μA max. to 5 V @ 200 μA max. | | | | | |

Absolute Maximum Ratings

| Characteristic | Value |
|------------------------|-----------------------------|
| Control voltage range | -0.2 ≤ V _C ≤ 8 V |
| RF input power @ 0/5 V | 6 W, f > 900 MHz |
| Operating temperature | -40 °C to +85 °C |
| Storage temperature | -65 °C to +150 °C |

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

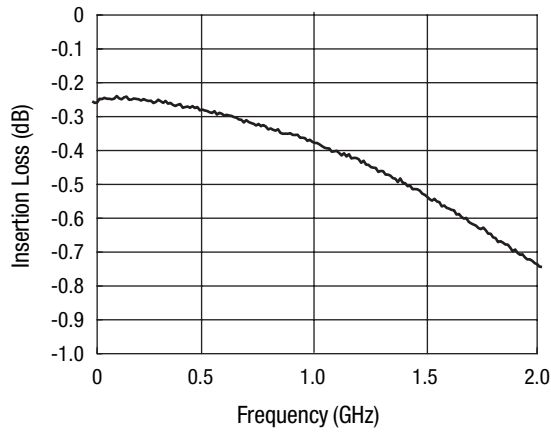
Truth Table

| V ₁ | V ₂ | J ₁ -J ₂ | J ₁ -J ₃ |
|-------------------|-------------------|--------------------------------|--------------------------------|
| V _{LOW} | V _{HIGH} | Isolation | Insertion loss |
| V _{HIGH} | V _{LOW} | Insertion loss | Isolation |

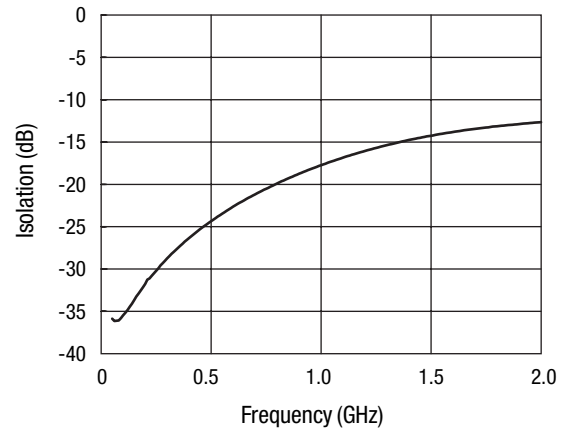
2.5 V ≤ V_{HIGH} ≤ 5 V, 0 ≤ V_{LOW} ≤ 0.2 V.
All other conditions not recommended.

Typical Performance Data

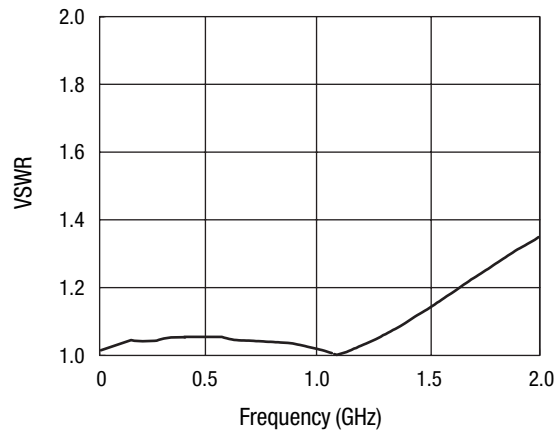
T = 25 °C, Z₀ = 50 Ω, unless otherwise noted



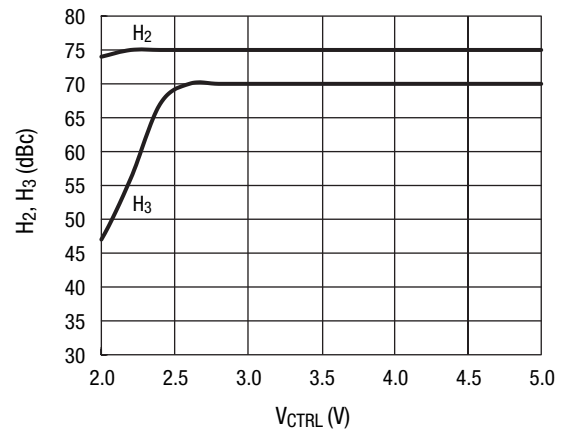
Insertion Loss vs. Frequency



Isolation vs. Frequency

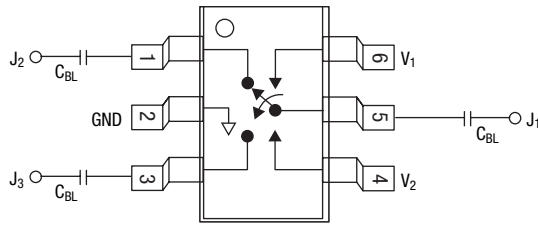


VSWR vs. Frequency



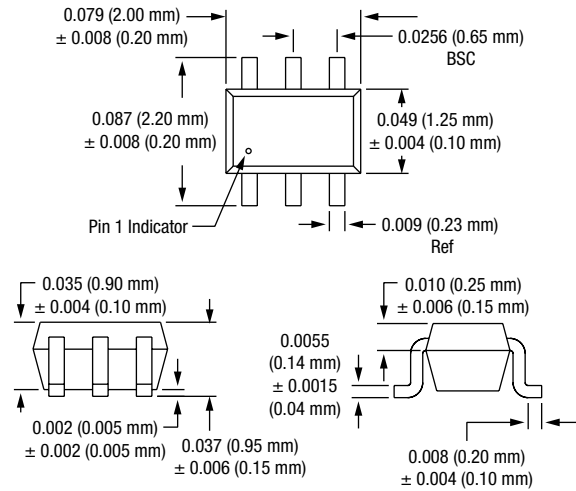
Second and Third Harmonics vs. Control Voltage
 f_{IN} = 900 MHz, P_{IN} = 34.5 dBm, GSM Signal

Pin Out



DC blocking capacitors (C_{BL}) must be supplied externally.
 C_{BL} = 100 pF for operating frequency >500 MHz.

SC-70 Package Outline



Pin Descriptions

| Pin Number | Pin Name | Description |
|------------|----------------|--|
| 1 | J ₂ | RF Input/Output – RF input/output port which is either connected to J ₁ via a low insertion loss path or isolated from J ₁ , according to the logic voltage levels applied to V ₁ and V ₂ |
| 2 | GND | Equipotential Point – Internal circuit common, which must be connected to the pcb ground or common via the lowest possible impedance |
| 3 | J ₃ | RF Input/Output – RF input/output port which is either connected to J ₁ via a low insertion loss path or isolated from J ₁ , according to the logic voltage levels applied to V ₁ and V ₂ |
| 4 | V ₂ | Control Voltage 2 – Control voltage input #2. The logic voltage level applied to this pin, along with the voltage level applied to V ₁ (pin 6), determines the states of the RF paths between J ₁ –J ₂ and J ₁ –J ₃ |
| 5 | J ₁ | RF Common Input/Output – RF common input/output port which is either connected to J ₂ or to J ₃ via a low insertion loss and isolated from the other RF port, according to the logic voltage levels applied to V ₁ and V ₂ |
| 6 | V ₁ | Control Voltage 1 – Control voltage input #1. The logic voltage level applied to this pin, along with the voltage level applied to V ₂ (pin 4), determines the states of the RF paths between J ₁ –J ₂ and J ₁ –J ₃ |

Recommended Solder Reflow Profiles

Refer to the [“Recommended Solder Reflow Profile”](#) Application Note.

Tape and Reel Information

Refer to the [“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”](#) Application Note.

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А