32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

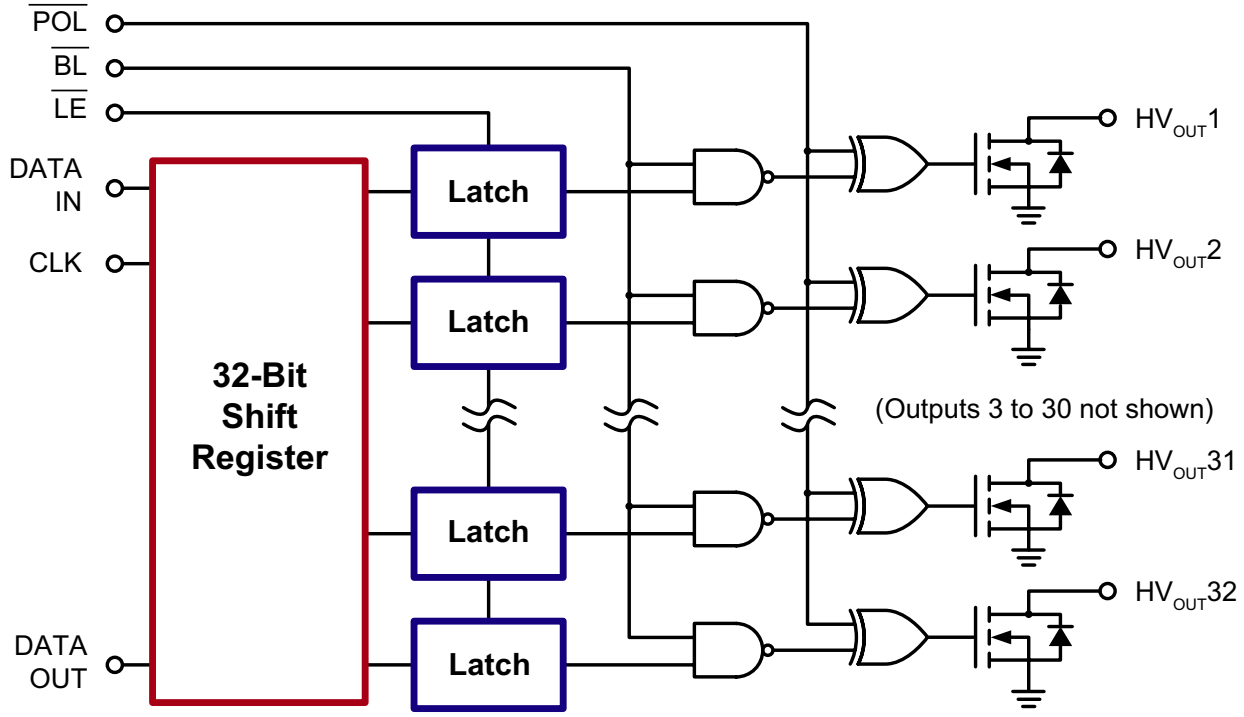
- Processed with HVCMOS® technology
- Sink current minimum 100mA
- Shift register speed 8.0MHz
- Polarity and Blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to VPP allows efficient power recovery

General Description

The HV5522 is a low-voltage serial to high-voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV5522 shifts in the counter clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Functional Block Diagram



Ordering Information

Device	Package Options	
	44-Lead Quad Plastic Gullwing *10.00x10.00mm body 2.45mm height (max) 0.80mm pitch*	44-Lead Quad Plastic Chip Carrier *.653x.653in body .180in height (max) .050in pitch*
HV5522	HV5522PG-G	HV5522PJ-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	
Supply voltage, V_{DD} [1]	-0.5V to +15V
Output voltage, V_{PP} [1]	-0.5V to +230V
Logic input levels [1]	-0.5V to V_{DD} +0.5V
Ground current [2]	1.5A
Continuous total power dissipation [3]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

1. *All voltages are referenced to V_{SS}*
2. *Duty cycle is limited by the total power dissipated in the package*
3. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic voltage supply	10.8	13.2	V
HV_{OUT}	High voltage output	-0.3	+220	V
V_{IH}	Input high voltage	V_{DD} -2.0	V_{DD}	V
V_{IL}	Input low voltage	0	2.0	V
f_{CLK}	Clock frequency	-	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

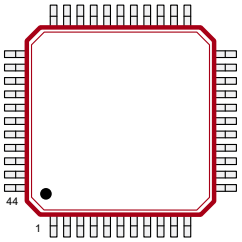
Power-Up Sequence

Power-up sequence should be the following:

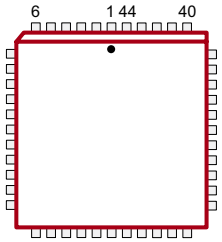
1. Connect ground
2. Apply V_{DD}
3. Set all inputs to a known state

Power-down sequence should be the reverse of the above.

Pin Configurations



44-Lead PQFP (PG)
(top view)

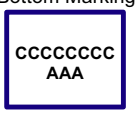


44-Lead PLCC (PJ)
(top view)

Product Marking

Top Marking

Bottom Marking



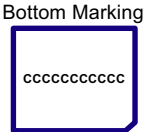
YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PQFP (PG)

Top Marking

Bottom Marking



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Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Electrical Characteristics *(over recommended operating conditions unless otherwise noted)*

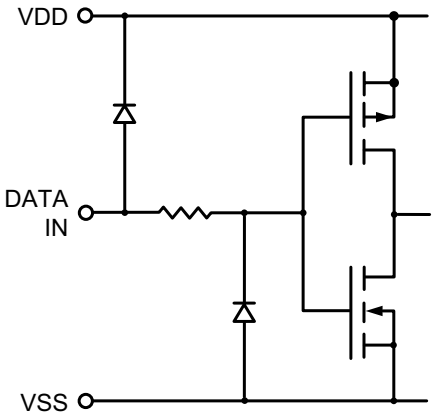
DC Characteristics

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz
I_{DDQ}	V_{DD} supply current (quiescent)		-	100	µA	V_{IN} = 0V
$I_{O(OFF)}$	Off state output current		-	10	µA	All outputs high, all SWS parallel
I_{IH}	High-level logic input current		-	1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V
V_{OH}	High-level output data out		V_{DD} -1.0V	-	V	I_{DOUT} = -100µA
V_{OL}	Low-level output voltage	HV_{OUT}	-	15	V	I_{HVOUT} = +100mA
		Data out	-	1.0	V	I_{DOUT} = +100µA
V_{OC}	HV_{OUT} clamp voltage		-	-1.5	V	I_{OL} = -100mA

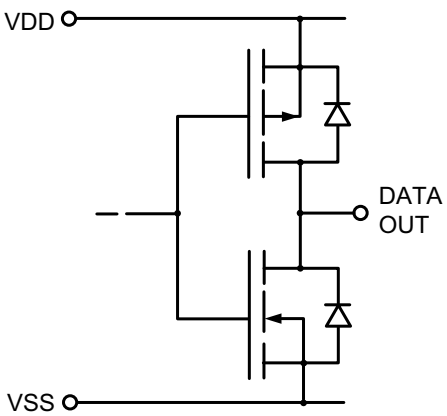
AC Characteristics *(V_{DD} = 12V, T_C = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_W	Clock width, high or low	62	-	ns	---
t_{SU}	Data set-up time before CLK falls	25	-	ns	---
t_H	Data hold time after CLK falls	10	-	ns	---
t_{ON}	Turn-on time, HV_{OUT} from enable	-	500	ns	R_L = 2.0KΩ to V_{PP} max.
t_{DHL}	Delay time clock to data high to low	-	100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50	-	ns	---
t_{WLE}	Width of $\overline{LE}$ pulse	50	-	ns	---
t_{SLE}	$\overline{LE}$ setup time before clock falls	50	-	ns	---

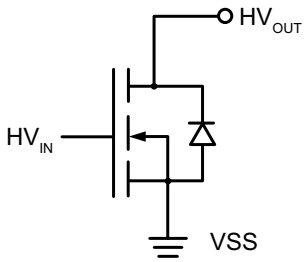
Input and Output Equivalent Circuits



Logic Inputs

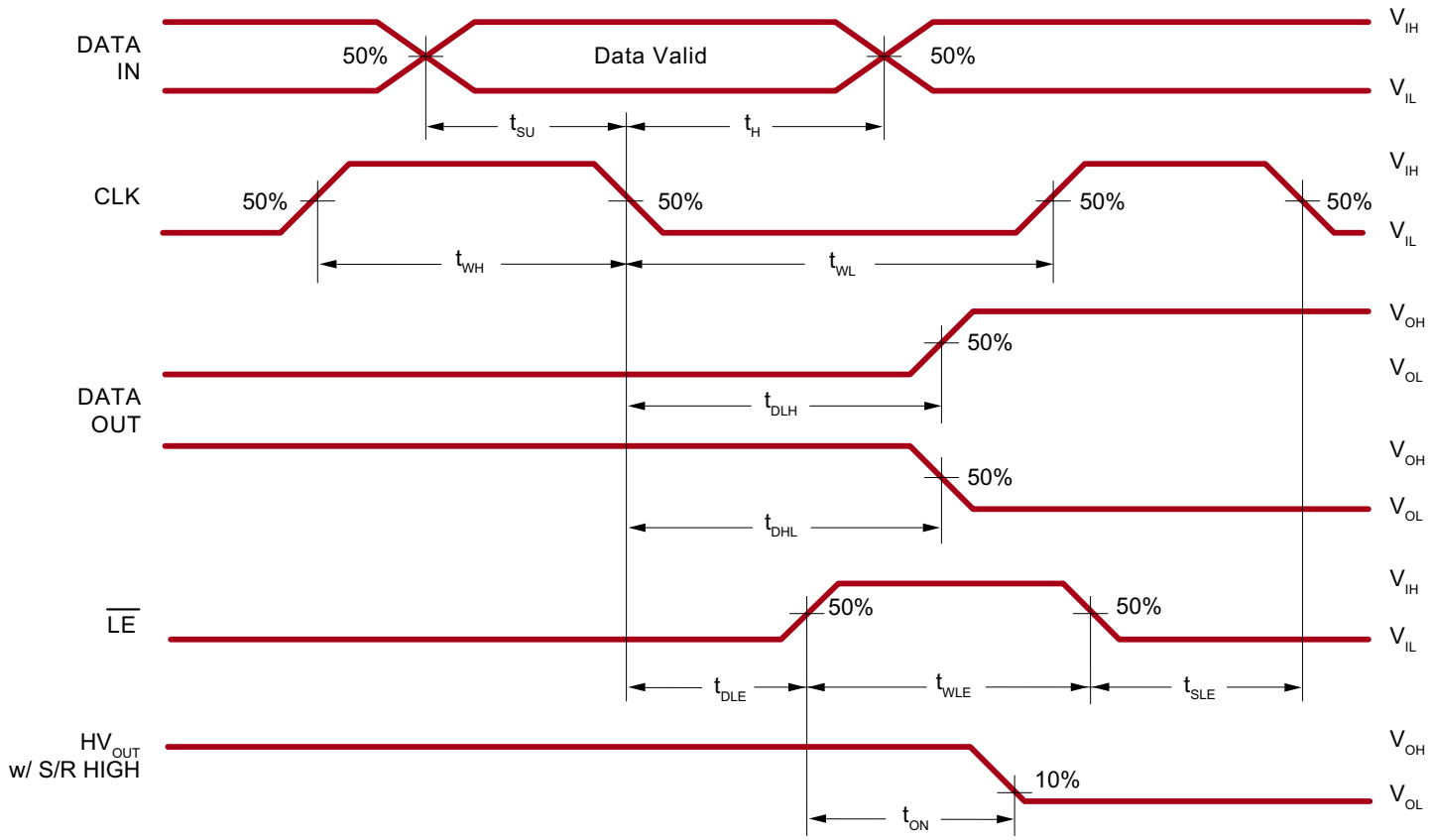


Logic Data Output



High Voltage Outputs

Switching Waveforms



Functional Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	On	On...On	*
All off	X	X	X	L	H	*	*...*	Off	Off...Off	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L	*...*	Off	*...*	*
	H	↓	H	H	H	H	*...*	On	*...*	*

Notes:

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transistion.

* *dependent on previous stage's state before the last CLK ↓ or last $\overline{LE}$ high.*

44-Lead PQFP Pin Assignment (PG)

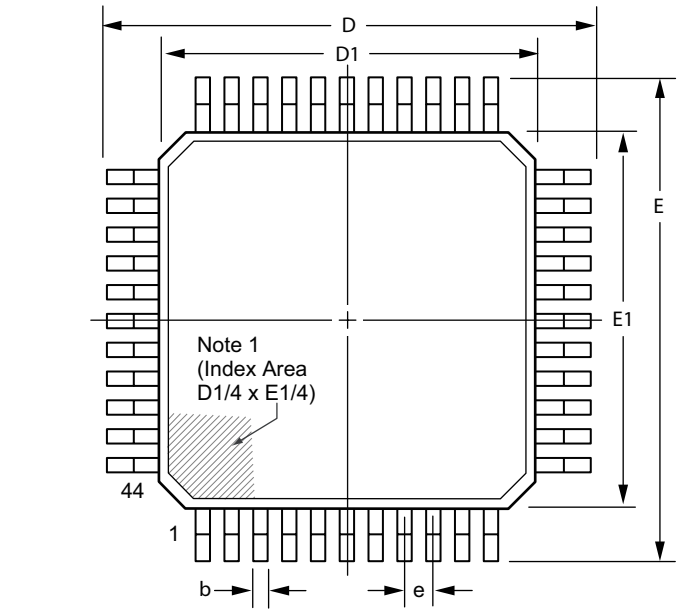
Pin #	Function	Description
1	$HV_{OUT}11$	High voltage outputs.
2	$HV_{OUT}12$	
3	$HV_{OUT}13$	
4	$HV_{OUT}14$	
5	$HV_{OUT}15$	
6	$HV_{OUT}16$	
7	$HV_{OUT}17$	
8	$HV_{OUT}18$	
9	$HV_{OUT}19$	
10	$HV_{OUT}20$	
11	$HV_{OUT}21$	
12	$HV_{OUT}22$	
13	$HV_{OUT}23$	
14	$HV_{OUT}24$	
15	$HV_{OUT}25$	
16	$HV_{OUT}26$	
17	$HV_{OUT}27$	
18	$HV_{OUT}28$	
19	$HV_{OUT}29$	
20	$HV_{OUT}30$	
21	$HV_{OUT}31$	
22	$HV_{OUT}32$	
23	DATA OUT	Data output pin.
24	N/C	No internal connection.
25	N/C	
26	N/C	
27	$\overline{POL}$	Inverts the polarity of the HV_{OUT} pins
28	CLK	Clock pin, shift registers shifts data on falling edge of input clock.
29	VSS	Reference voltage, usually ground.
30	VDD	Logic supply voltage.
31	$\overline{LE}$	Latch enable pin, data is shifted from shift register to latches on logic input high.
32	DATA IN	Data input pin.
33	$\overline{BL}$	Blanking pin sets all HV_{OUT} pins low or high depending upon state of polarity. See function table.
34	N/C	No internal connection.
35	$HV_{OUT}1$	High voltage outputs.
36	$HV_{OUT}2$	
37	$HV_{OUT}3$	
38	$HV_{OUT}4$	
39	$HV_{OUT}5$	
40	$HV_{OUT}6$	
41	$HV_{OUT}7$	
42	$HV_{OUT}8$	
43	$HV_{OUT}9$	
44	$HV_{OUT}10$	

44-Lead PLCC Pin Assignment (PJ)

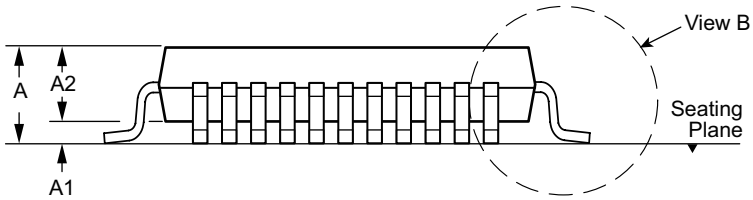
Pin #	Function	Description
1	$HV_{OUT}16$	High voltage outputs.
2	$HV_{OUT}17$	
3	$HV_{OUT}18$	
4	$HV_{OUT}19$	
5	$HV_{OUT}20$	
6	$HV_{OUT}21$	
7	$HV_{OUT}22$	
8	$HV_{OUT}23$	
9	$HV_{OUT}24$	
10	$HV_{OUT}25$	
11	$HV_{OUT}26$	
12	$HV_{OUT}27$	
13	$HV_{OUT}28$	
14	$HV_{OUT}29$	
15	$HV_{OUT}30$	
16	$HV_{OUT}31$	
17	$HV_{OUT}32$	
18	DATA OUT	Data output pin.
19	N/C	No internal connection.
20	N/C	
21	N/C	
22	$\overline{POL}$	Inverts the polarity of the HV_{OUT} pins
23	CLK	Clock pin, shift registers shifts data on falling edge of input clock.
24	VSS	Reference voltage, usually ground.
25	VDD	Logic supply voltage.
26	$\overline{LE}$	Latch enable pin, data is shifted from shift register to latches on logic input high.
27	DATA IN	Data input pin.
28	$\overline{BL}$	Blanking pin sets all HV_{OUT} pins low or high depending upon state of polarity. See function table.
29	N/C	No internal connection.
30	$HV_{OUT}1$	High voltage outputs.
31	$HV_{OUT}2$	
32	$HV_{OUT}3$	
33	$HV_{OUT}4$	
34	$HV_{OUT}5$	
35	$HV_{OUT}6$	
36	$HV_{OUT}7$	
37	$HV_{OUT}8$	
38	$HV_{OUT}9$	
39	$HV_{OUT}10$	
40	$HV_{OUT}11$	
41	$HV_{OUT}12$	
42	$HV_{OUT}13$	
43	$HV_{OUT}14$	
44	$HV_{OUT}15$	

44-Lead PQFP Package Outline (PG)

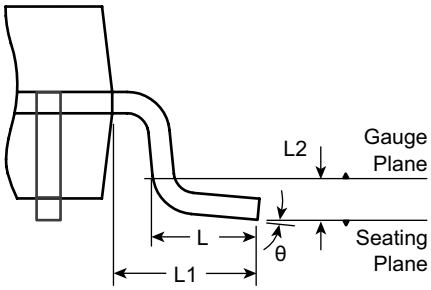
10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Top View



Side View



View B

Note:

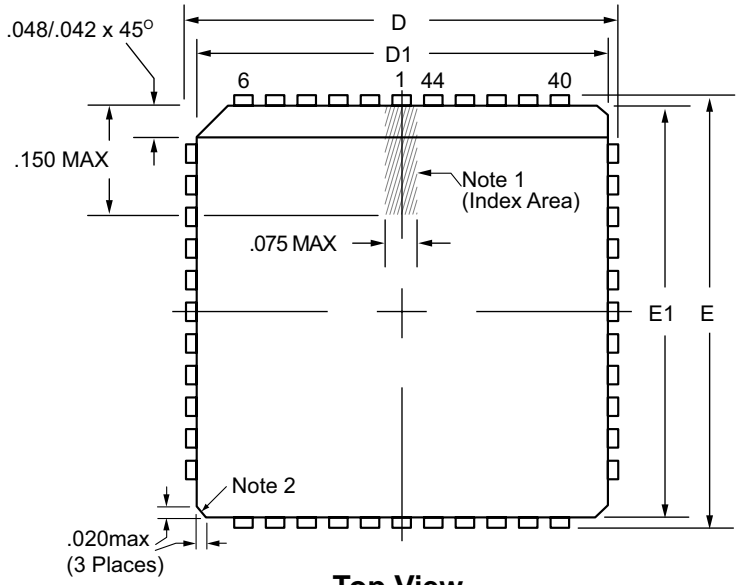
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

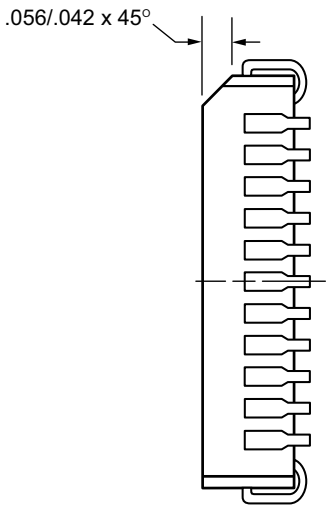
JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex** Doc. #: DSPD-44PQFPPG, Version C041309.*

44-Lead PLCC Package Outline (PJ)

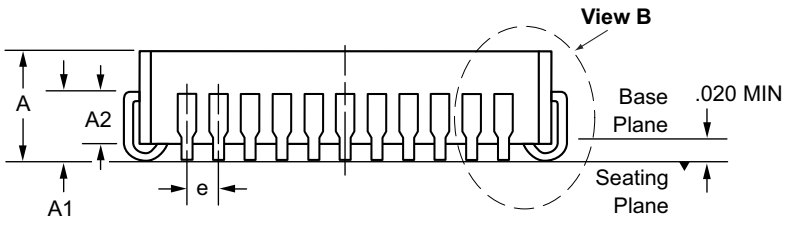
.653x.653in body, .180in height (max), .050in pitch



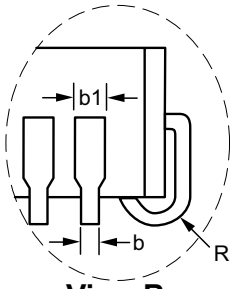
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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FORSTAR®

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