

NB6L239

2.5V / 3.3V Any Differential Clock IN to Differential LVPECL OUT $\div 1/2/4/8$, $\div 2/4/8/16$ Clock Divider

Description

The NB6L239 is a high-speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios; $\div 1/2/4/8$ and $\div 2/4/8/16$. Both divider circuits drive a pair of differential LVPECL outputs. (More device information on page 8). The NB6L239 is a member of the ECLinPS MAX™ Family of the high performance clock products.

Features

- Maximum Clock Input Frequency, 3.0 GHz
- CLOCK Inputs Compatible with LVDS/LVPECL/CML/HSTL
- \overline{EN} , \overline{MR} , and SEL Inputs Compatible with LVTTTL/LVCMOS
- Rise/Fall Time 65 ps Typical
- < 10 ps Typical Output-to-Output Skew
- Example: 622.08 MHz Input Generates 38.88 MHz to 622.08 MHz Outputs
- Internal 50 Ω Termination Provided
- Random Clock Jitter < 1 ps RMS
- QA $\div 1$ Edge Aligned to QB $\div n$ Edge
- Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- Master Reset for Synchronization of Multiple Chips
- V_{BBAC} Reference Output
- Synchronous Output Enable/Disable
- Pb-Free Packages are Available



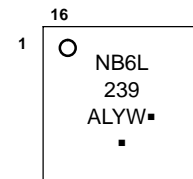
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



QFN-16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NB6L239

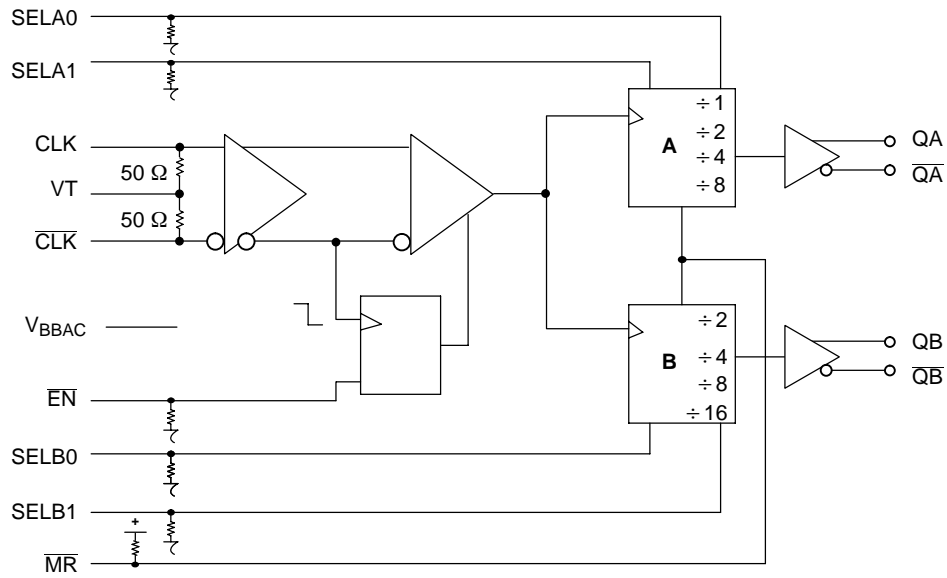


Figure 1. Simplified Logic Diagram

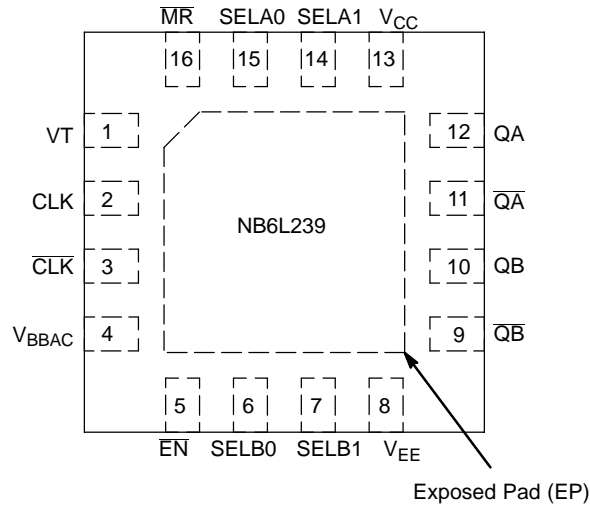


Figure 2. Pinout: QFN-16 (Top View)

NB6L239

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|-----------------------------|-------------------------------|---|
| 1 | VT | | Internal 100 Ω Center-Tapped Termination Pin for CLK and $\overline{\text{CLK}}$. |
| 2 | CLK | LVPECL, CML, LVDS, HSTL Input | Noninverted Differential CLOCK Input. |
| 3 | $\overline{\text{CLK}}$ | LVPECL, CML, LVDS, HSTL Input | Inverted Differential CLOCK Input. |
| 4 | V_{BBAC} | | Output Voltage Reference for Capacitor Coupled Inputs, Only. |
| 5 | $\overline{\text{EN}}^*$ | LVC MOS/LVTTL Input | Synchronous Output Enable |
| 6 | SELB0* | LVC MOS/LVTTL Input | Clock Divide Select Pin |
| 7 | SELB1* | LVC MOS/LVTTL Input | Clock Divide Select Pin |
| 8 | V_{EE} | Power Supply | Negative Supply Voltage |
| 9 | $\overline{\text{QB}}$ | LVPECL Output | Inverted Differential Output. Typically terminated with 50 Ω resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 10 | QB | LVPECL Output | Noninverted Differential Output. Typically terminated with 50 Ω resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 11 | $\overline{\text{QA}}$ | LVPECL Output | Inverted Differential Output. Typically terminated with 50 Ω resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 12 | QA | LVPECL Output | Noninverted Differential Output. Typically terminated with 50 Ω resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 13 | V_{CC} | Power Supply | Positive Supply Voltage. |
| 14 | SELA1* | LVC MOS/LVTTL Input | Clock Divide Select Pin |
| 15 | SELA0* | LVC MOS/LVTTL Input | Clock Divide Select Pin |
| 16 | $\overline{\text{MR}}^{**}$ | LVC MOS/LVTTL Input | Master Reset Asynchronous, Default Open High, Asserted LOW |
| | EP | Power Supply (OPT) | The Exposed Pad on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V_{EE} on the PC board. |

*Pins will default LOW when left OPEN.

**Pins will default HIGH when left OPEN.

NB6L239

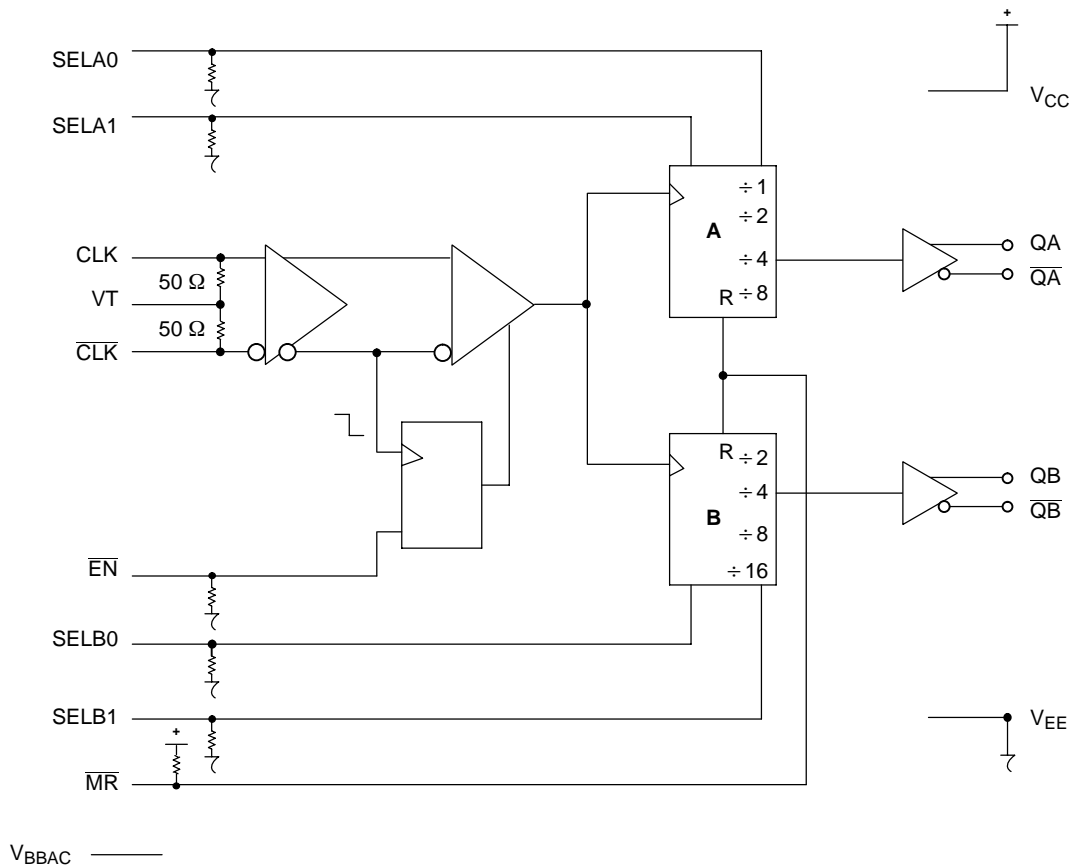


Figure 3. Logic Diagram

Table 2. FUNCTION TABLE

| CLK | EN* | MR** | FUNCTION |
|-----|-----|------|----------|
| ⌋ | L | H | Divide |
| ⌋ | H | H | Hold Q |
| X | X | L | Reset Q |

Table 3. CLOCK DIVIDE SELECT, QA OUTPUTS

| SELA1* | SELA0* | QA Outputs |
|--------|--------|-------------|
| L | L | Divide by 1 |
| L | H | Divide by 2 |
| H | L | Divide by 4 |
| H | H | Divide by 8 |

Table 4. CLOCK DIVIDE SELECT, QB OUTPUTS

| SELB1* | SELB0* | QB Outputs |
|--------|--------|--------------|
| L | L | Divide by 2 |
| L | H | Divide by 4 |
| H | L | Divide by 8 |
| H | H | Divide by 16 |

⌋ = Low-to-High Transition

⌋ = High-to-Low Transition

X = Don't Care

*Pins will default LOW when left OPEN.

**Pins will default HIGH when left OPEN.

NB6L239

Table 5. ATTRIBUTES

| Characteristics | | Value | |
|---|---|---------------------------------|-------------|
| Internal Input Pulldown Resistor | | 75 kΩ | |
| Internal Input Pullup Resistor | | 75 kΩ | |
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 1500 V > 150 V > 1000 V | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb-Free Pkg |
| QFN-16 | | Level 1 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 367 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|-----------------------|--|--------------|--------------|
| V _{CC} | Positive Mode Power Supply | V _{EE} = 0 V | | 3.6 | V |
| V _I | Input Voltage | V _{EE} = 0 V | V _{EE} ≤ V _I ≤ V _{CC} | 3.6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I _{BB} | V _{BBAC} Sink/Source Current | | | ± 0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | | 41.6 35.2 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | | 4.0 | °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NB6L239

Table 6. DC CHARACTERISTICS, CLOCK INPUTS, LVPECL OUTPUTS

($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|--|-------------------------------|-------------------------------|------------------------------|-------------------------------|-------------------------------|--------------------------------|-------------------------------|------------------------------|--------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 30 | 40 | 50 | 30 | 40 | 50 | 30 | 40 | 50 | mA |
| V_{OH} | Output HIGH Voltage (Notes 2, 3) $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$ | $V_{CC}-1150$ 2150 1350 | $V_{CC}-1060$ 2240 1440 | $V_{CC}-950$ 2350 1550 | $V_{CC}-1100$ 2200 1400 | $V_{CC}-1015$ 2285 1485 | $V_{CC} - 900$ 2400 1600 | $V_{CC}-1050$ 2250 1450 | $V_{CC}-980$ 2320 1520 | $V_{CC} - 850$ 2450 1650 | mV |
| V_{OL} | Output LOW Voltage (Notes 2, 3) $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$ | $V_{CC}-1935$ 1365 565 | $V_{CC}-1775$ 1525 725 | $V_{CC}-1630$ 1670 870 | $V_{CC}-1875$ 1430 630 | $V_{CC}-1735$ 1565 765 | $V_{CC}-1580$ 1720 920 | $V_{CC}-1810$ 1490 690 | $V_{CC}-1675$ 1625 825 | $V_{CC}-1530$ 1770 970 | mV |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 7, 10)

| | | | | | | | | | | | |
|------------|---|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|----|
| V_{th} | Input Threshold Reference Voltage (Note 4) | 100 | | $V_{CC} - 100$ | 100 | | $V_{CC} - 100$ | 100 | | $V_{CC} - 100$ | mV |
| V_{IH} | Single-ended Input HIGH Voltage | $V_{th} + 100$ | | V_{CC} | $V_{th} + 100$ | | V_{CC} | $V_{th} + 100$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage | V_{EE} | | $V_{th} - 100$ | V_{EE} | | $V_{th} - 100$ | V_{EE} | | $V_{th} - 100$ | mV |
| V_{BBAC} | Output Voltage Reference @ 100 μA (Note 7) $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$ | $V_{CC}-1460$ 1840 1040 | $V_{CC}-1330$ 1970 1170 | $V_{CC}-1200$ 2100 1300 | $V_{CC}-1460$ 1840 1040 | $V_{CC}-1340$ 1960 1160 | $V_{CC}-1200$ 2100 1300 | $V_{CC}-1460$ 1840 1040 | $V_{CC}-1350$ 1950 1150 | $V_{CC}-1200$ 2100 1300 | mV |

DIFFERENTIAL INPUT DRIVEN DIFFERENTIALLY (Figures 8, 9, 11) (Note 6)

| | | | | | | | | | | | |
|-----------|--|----------|----|-------------------|----------|----|-------------------|----------|----|-------------------|----------|
| V_{IHD} | Differential Input HIGH Voltage | 100 | | V_{CC} | 100 | | V_{CC} | 100 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | V_{EE} | | $V_{CC} - 100$ | V_{EE} | | $V_{CC} - 100$ | V_{EE} | | $V_{CC} - 100$ | mV |
| V_{CMR} | Input Common Mode Range (Differential Cross-point Voltage) (Note 5) | 50 | | $V_{CC} - 50$ | 50 | | $V_{CC} - 50$ | 50 | | $V_{CC} - 50$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD(CLK)} - V_{ILD(CLK)}$) and ($V_{IHD(CLK)} - V_{ILD(CLK)}$) | 100 | | $V_{CC} - V_{EE}$ | 100 | | $V_{CC} - V_{EE}$ | 100 | | $V_{CC} - V_{EE}$ | mV |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} .
3. Outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$ for proper operation.
4. V_{th} is applied to the complementary input when operating in single-ended mode.
5. $V_{CMR_{MIN}}$ varies 1:1 with V_{EE} , $V_{CMR_{MAX}}$ varies 1:1 with V_{CC} .
6. Input and output voltage swing is a single-ended measurement operating in differential mode.
7. V_{BBAC} used to rebias capacitor-coupled inputs only (see Figures 16 and 17).

NB6L239

Table 7. DC CHARACTERISTICS, LVTTTL/LVCMOS INPUTS ($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|----------|------------------------------------|----------|-----|----------|---------------|
| V_{IH} | Input HIGH Voltage (LVCMOS/LVTTTL) | 2.0 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (LVCMOS/LVTTTL) | V_{EE} | | 0.8 | V |
| I_{IH} | Input HIGH Current | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | 150 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 8. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.465\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 8)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|---|-------------------------------------|---------------|-----------------------|------------|---------------|-----------------------|------------|---------------|-----------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{inMAX} | Maximum Input CLOCK Frequency | 3.0 | | | 3.0 | | | 3.0 | | | GHz |
| V_{OUTPP} | Output Voltage Amplitude (Notes 10, 11) QA(÷2, 4, 8), QB(÷n) QA(÷1), QB(÷n) QA(÷1), QB(÷n) 2.5 GHz < $f_{in} \leq 3.0\text{ GHz}$ | $f_{in} \leq 3.0\text{ GHz}$ 450 | 650 | | 450 | 650 | | 450 | 650 | | mV |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential @ 50 MHz CLK, Qn MR, Qn | 370 330 | 470 370 | 570 430 | 370 330 | 470 380 | 570 430 | 400 330 | 500 400 | 600 480 | ps |
| t_{RR} | Reset Recovery | 0 | -90 | | 0 | -90 | | 0 | -90 | | ps |
| t_s | Setup Time @ 50 MHz EN, CLK SELA/B, CLK | 0 0 | -60 -300 | | 0 0 | -60 -300 | | 0 0 | -60 -300 | | ps |
| t_h | Hold Time @ 50 MHz CLK, EN CLK, SELA/B | 150 700 | 65 200 | | 150 700 | 65 200 | | 150 700 | 65 200 | | ps |
| t_{skew} | Within-Device Skew @ 50 MHz Device-to-Device Skew Duty Cycle Skew (Note 9) (Note 9) (Note 9) | | 5 25 25 | 30 80 40 | | 5 30 30 | 30 90 45 | | 6 30 30 | 35 90 45 | ps |
| t_{PW} | Minimum Pulse Width MR | 550 | | | 550 | | | 550 | | | ps |
| t_{JITTER} | RMS Random Clock Jitter (See Figure 20. $F_{max}/JITTER$) | | | < 1 | | | < 1 | | | < 1 | ps |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 10) | 100 | | V_{CC} $-V_{EE}$ | 100 | | V_{CC} $-V_{EE}$ | 100 | | V_{CC} $-V_{EE}$ | mV |
| t_r t_f | Output Rise/Fall Times @ 50 MHz (20% – 80%) Qn, Qn | 30 | 60 | 120 | 30 | 65 | 120 | 30 | 70 | 120 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 750 mV, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
9. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
10. Input and output voltage swing is a single-ended measurement operating in differential mode.
11. Output Voltage Amplitude ($V_{OHCLK} - V_{OLCLK}$) at input CLOCK frequency, f_{in} . The output frequency, f_{out} , is the input CLOCK frequency divided by n, $f_{out} = f_{in} \div n$. Input CLOCK frequency is $\leq 3.0\text{ GHz}$.

Application Information

The NB6L239 is a high-speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios; $\div 1/2/4/8$ and $\div 2/4/8/16$. Both divider circuits drive a pair of differential LVPECL outputs. The internal dividers are synchronous to each other. Therefore, the common output edges are precisely aligned.

The NB6L239 clock inputs can be driven by a variety of differential signal level technologies including LVDS, LVPECL, HSTL, or CML. The differential clock input buffer employs a pair of internal 50 Ω termination resistors in a 100 Ω center-tapped configuration and accessible via the VT pin. This feature provides transmission line termination on-chip, at the receiver end, eliminating external components. The V_{BBAC} reference output can be used to rebias capacitor-coupled differential or

single-ended input CLOCK signals. For the capacitor-coupled CLK and/or \overline{CLK} inputs, V_{BBAC} should be connected to the V_T pin and bypassed to ground with a 0.01 μF capacitor. Inputs CLK and \overline{CLK} must be signal driven or auto oscillation may result.

The common enable (\overline{EN}) is synchronous so that the internal divider flip-flops will only be enabled/disabled when the internal clock is in the LOW state. This avoids any chance of generating a runt pulse on the internal clock when the device is enabled/disabled, as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

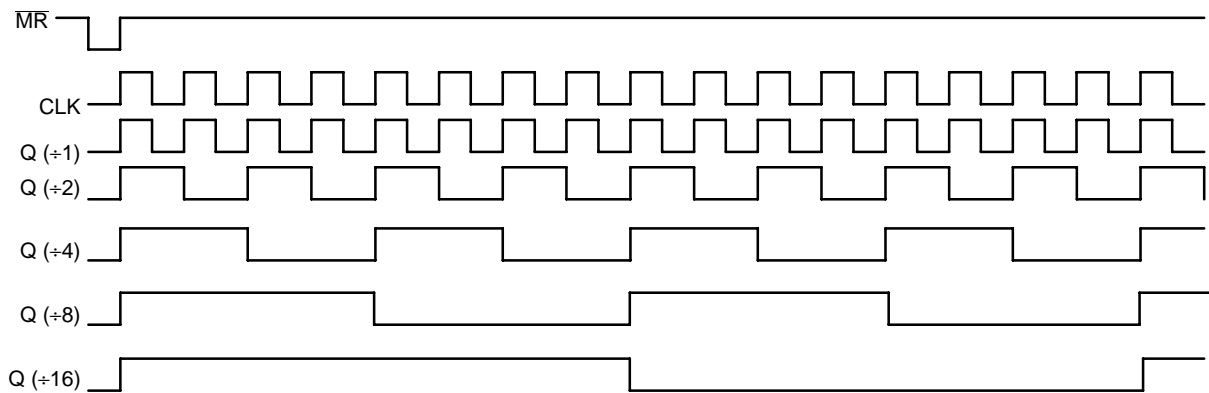


Figure 4. Timing Diagram

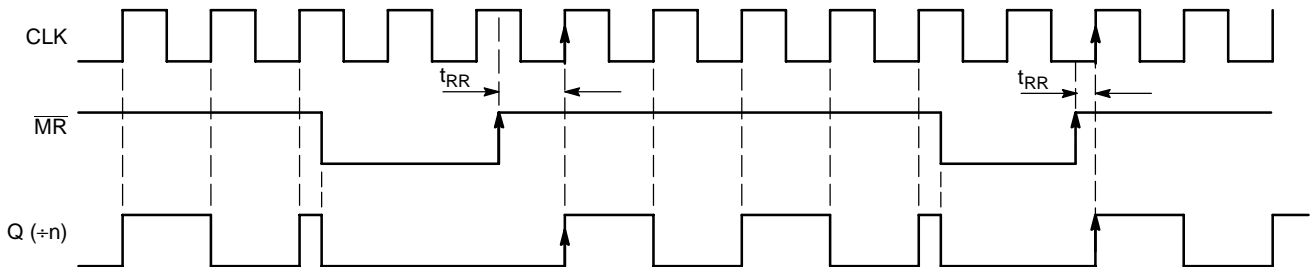


Figure 5. Master Reset Timing Diagram

NOTE: On the rising edge of \overline{MR} , Q goes HIGH after the first rising edge of CLK.

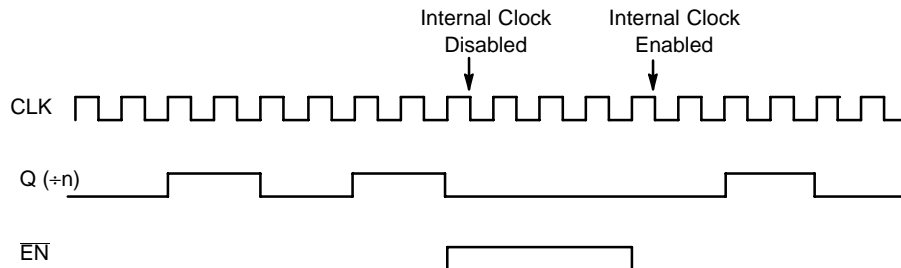


Figure 6. Output Enable Timing Diagrams

The \overline{EN} signal will “freeze” the internal divider flip-flops on the first falling edge of CLK after its assertion. The internal divider flip-flops will maintain their state during the freeze. When \overline{EN} is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip-flops will “unfreeze” and continue to their next state count with proper phase relationships.

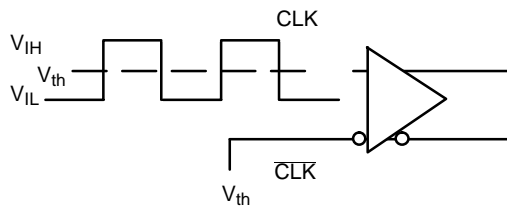


Figure 7. Differential Input Driven Single-Ended

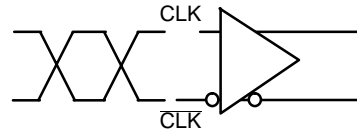


Figure 8. Differential Inputs Driven Differentially

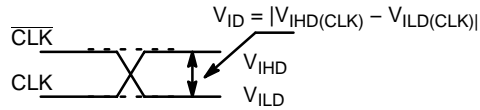


Figure 9. Differential Inputs Driven Differentially

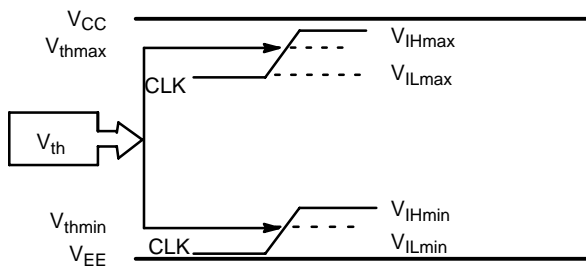


Figure 10. V_{th} Diagram

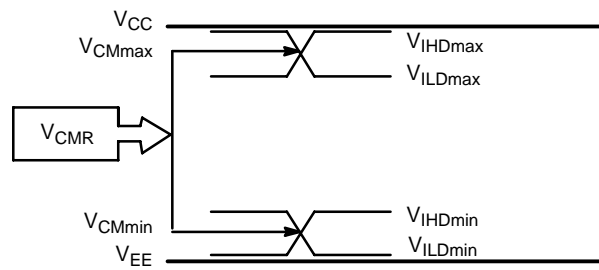


Figure 11. V_{CM} Diagram

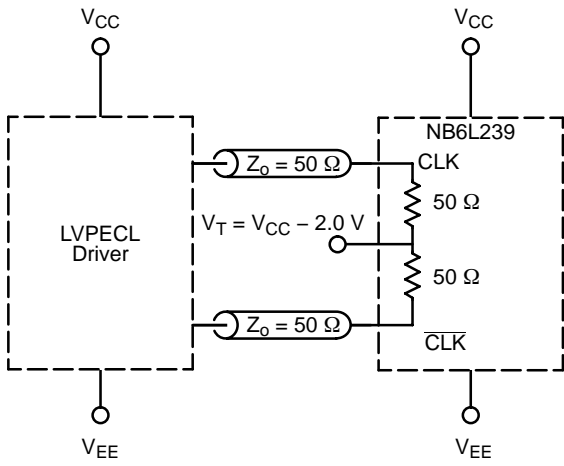


Figure 12. LVPECL Interface

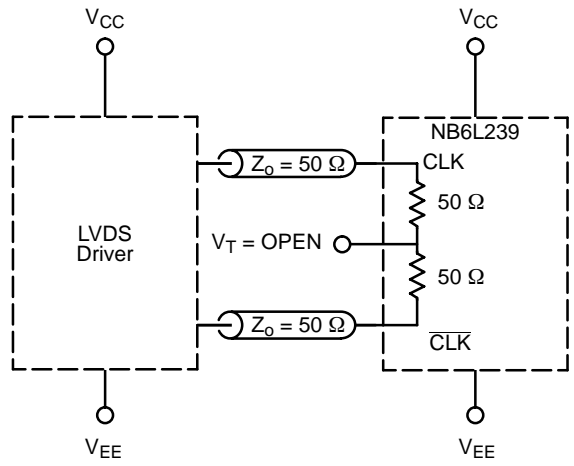


Figure 13. LVDS Interface

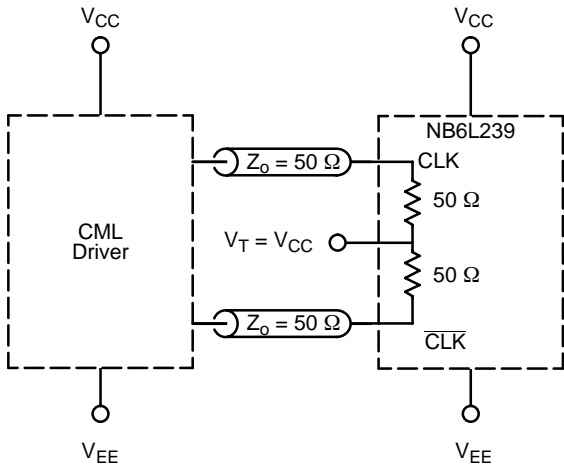


Figure 14. Standard 50 Ω Load CML Interface

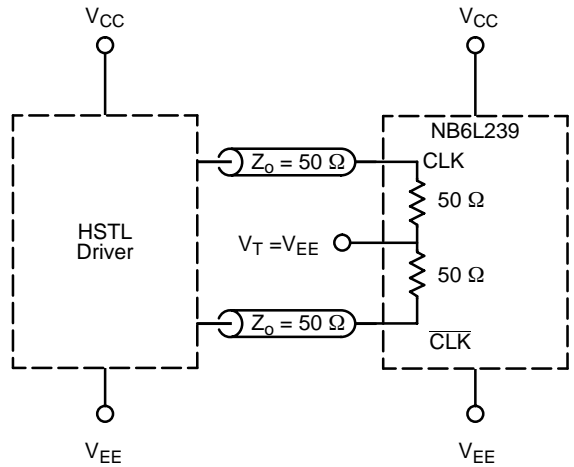


Figure 15. Standard 50 Ω Load HSTL Interface

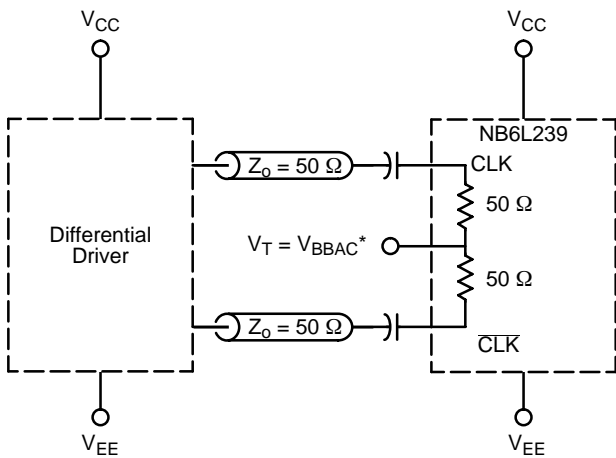


Figure 16. Capacitor-Coupled Differential Interface (V_T Connected to V_{BBAC})

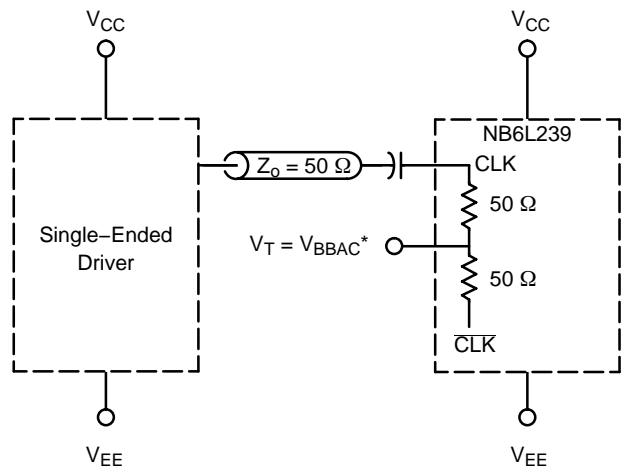


Figure 17. Capacitor-Coupled Single-Ended Interface (V_T Connected to V_{BBAC})

* V_{BBAC} bypassed to ground with a 0.01 μ F capacitor.

NB6L239

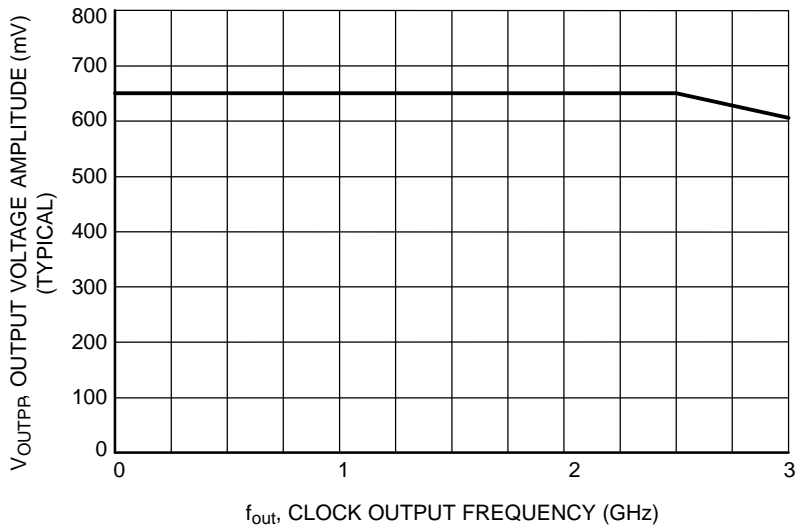


Figure 18. Output Voltage Amplitude (V_{OUTPP}) versus Clock Output Frequency at Ambient Temperature (Typical) ($f_{out\ QA/QB} = f_{in} \div n$; $f_{in} \leq 3.0$ GHz).

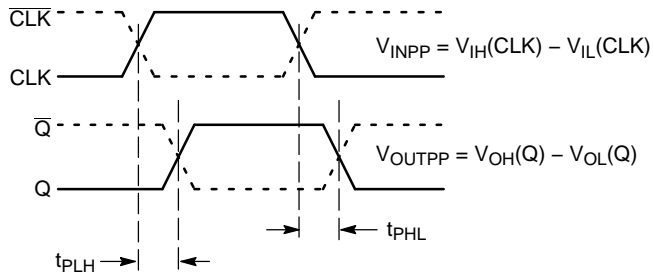


Figure 19. AC Reference Measurement

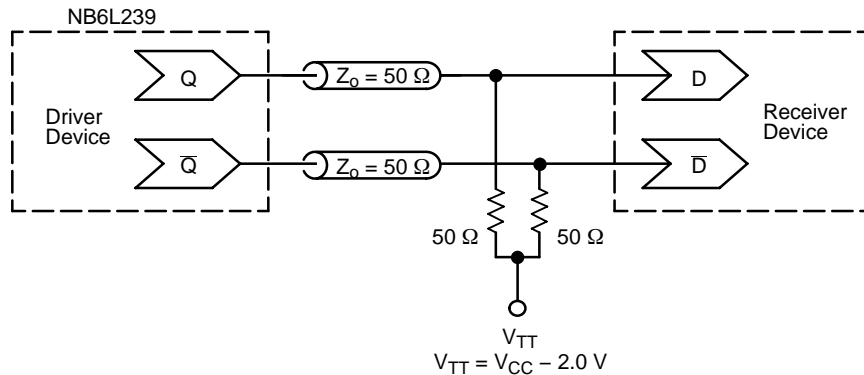


Figure 20. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

NB6L239

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------------------|--------------------|
| NB6L239MN | QFN-16, 3 x 3 mm | 123 Units / Rail |
| NB6L239MNG | QFN-16, 3 x 3 mm (Pb-Free) | 123 Units / Rail |
| NB6L239MNR2 | QFN-16, 3 x 3 mm | 3000 / Tape & Reel |
| NB6L239MNR2G | QFN-16, 3 x 3 mm (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

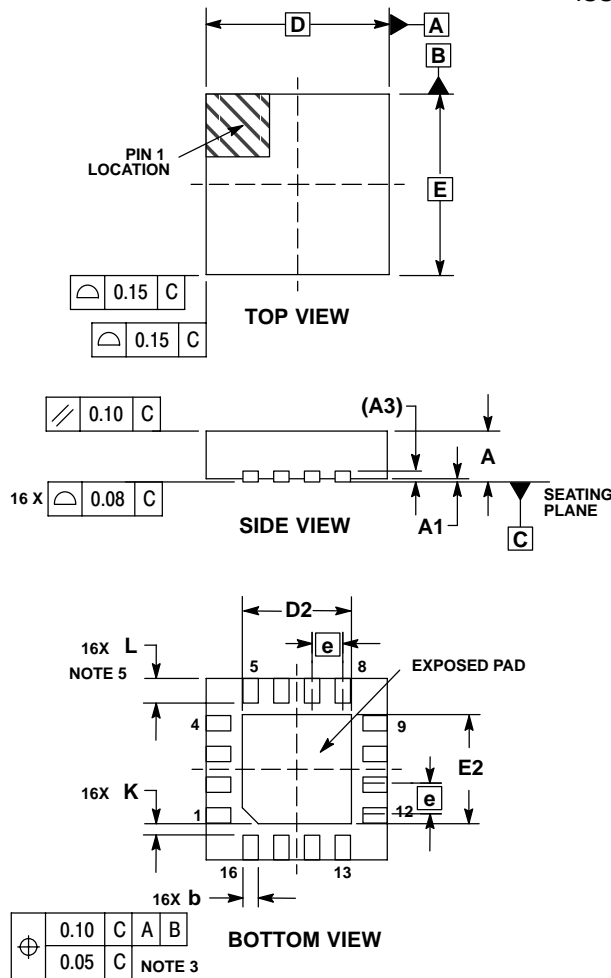
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

NB6L239

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G-01
ISSUE C

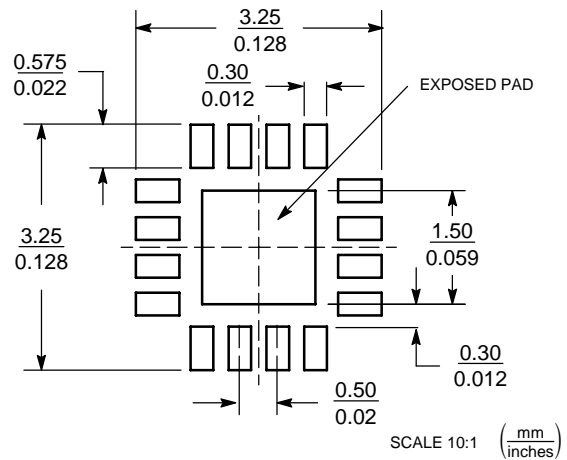


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.65 | 1.85 |
| E | 3.00 BSC | |
| E2 | 1.65 | 1.85 |
| e | 0.50 BSC | |
| K | 0.18 TYP | |
| L | 0.30 | 0.50 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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