VN2210

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-drain Diode
- High Input Impedance and High Gain

Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memory, Displays, Bipolar Transistors, etc.)

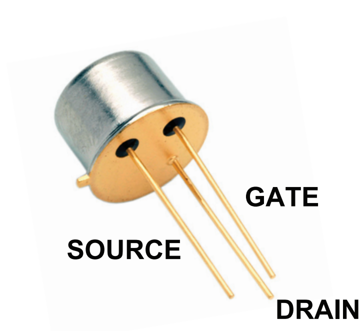
General Description

VN2210 is an Enhancement-mode (normally-off) transistor that utilizes a vertical Double-diffused Metal-Oxide Semiconductor (DMOS) structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors as well as the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

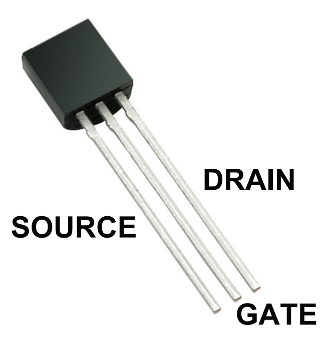
Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Types

TO-39



TO-92



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Drain-to-source Voltage .... BV_{DSS}
Drain-to-gate Voltage .... BV_{DGS}
Gate-to-source Voltage .... ±20V
Operating and Storage Temperatures .... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
DC PARAMETERS (Note 1 unless otherwise specified)						
Drain-to-source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 10 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2.4	V	$V_{GS} = V_{DS}$, I_D = 10 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	–4.3	–5.5	mV/°C	$V_{GS} = V_{DS}$, I_D = 10 mA (**Note 2**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	50	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	10	mA	V_{DS} = 0.8 maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 2**)
ON-State Drain Current	$I_{D(ON)}$	3	4.5	—	A	V_{GS} = 5V, V_{DS} = 25V
		8	17	—		V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-source ON-State Resistance	$R_{DS(ON)}$	—	0.4	0.5	Ω	V_{GS} = 5V, I_D = 1A
		—	0.27	0.35		V_{GS} = 10V, I_D = 4A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	0.85	1.2	%/°C	V_{GS} = 10V, I_D = 4A (**Note 2**)
AC PARAMETERS (Note 2)						
Forward Transconductance	G_{FS}	1200	—	—	mmho	V_{DS} = 25V, I_D = 2A
Input Capacitance	C_{ISS}	—	300	500	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	125	200		
Reverse Transfer Capacitance	C_{RSS}	—	50	65		
Turn-on Time	$t_{d(ON)}$	—	10	15	ns	V_{DD} = 25V, I_D = 2A, R_{GEN} = 10Ω
Rise Time	t_r	—	10	15		
Turn-off Time	$t_{d(OFF)}$	—	50	65		
Fall Time	t_f	—	30	50		
DIODE PARAMETERS						
Diode Forward Voltage Drop	V_{SD}	—	1	1.6	V	V_{GS} = 0V, I_{SD} = 4A (**Note 1**)
Reverse Recovery Time	t_{rr}	—	500	—	ns	V_{GS} = 0V, I_{SD} = 1A (**Note 2**)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25°C$.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TEMPERATURE RANGES						
Operating Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCES						
TO-39	θ_{JA}	—	N/A	—	—	
TO-92	θ_{JA}	—	132	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (A)	I_D (Pulsed) (A)	Power Dissipation at $T_C = 25°C$ (W)	I_{DR} (Note 1) (A)	I_{DRM} (A)
TO-39	1.7	10	0.36	1.7	10
TO-92	1.2	8	0.74	1.2	8

Note 1: I_D (continuous) is limited by maximum T_j.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

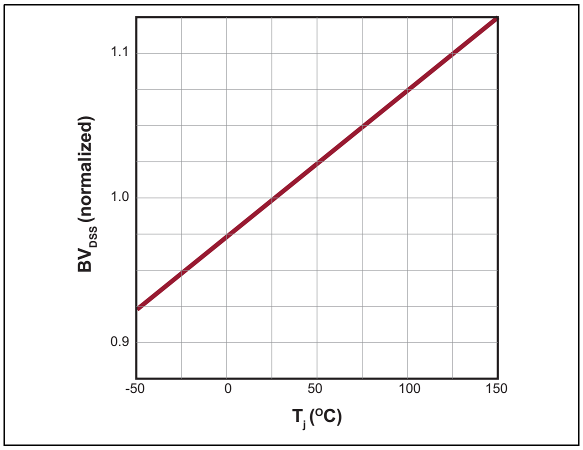


FIGURE 2-1: *BV_{DSS} Variation with Temperature.*

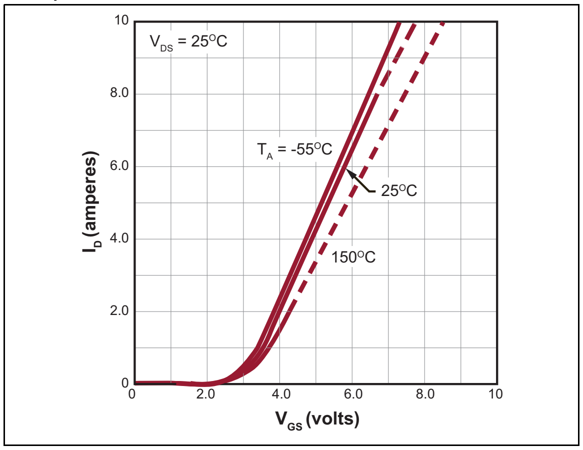


FIGURE 2-2: *Transfer Characteristics.*

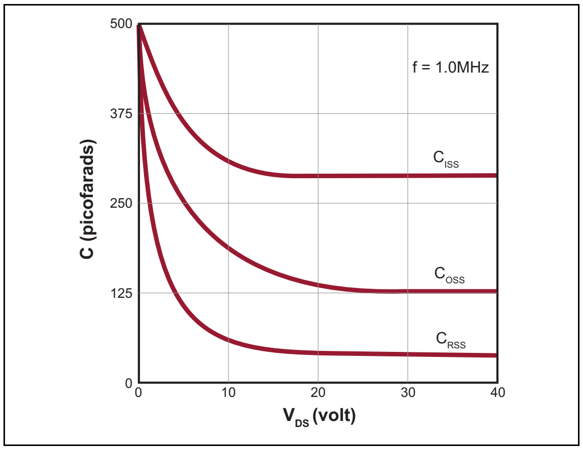


FIGURE 2-3: *Capacitance vs. Drain-to-source Voltage.*

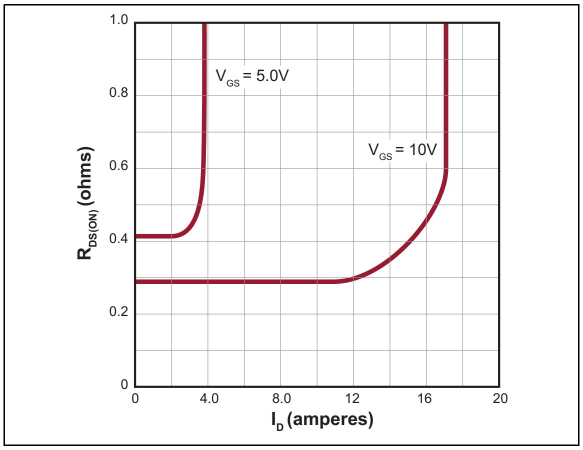


FIGURE 2-4: *On-resistance vs. Drain Current.*

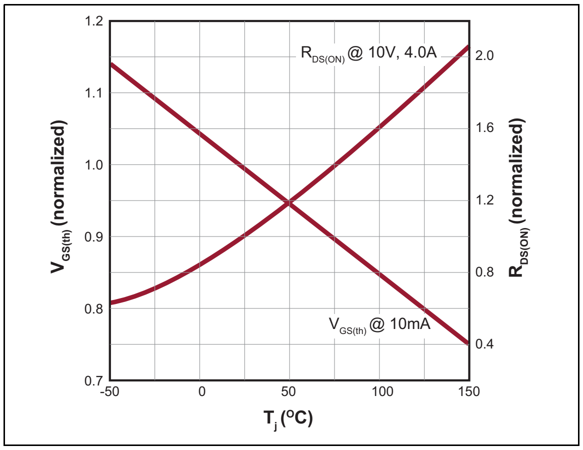


FIGURE 2-5: *V_{GS} and RV_{DS} Variation with Temperature.*

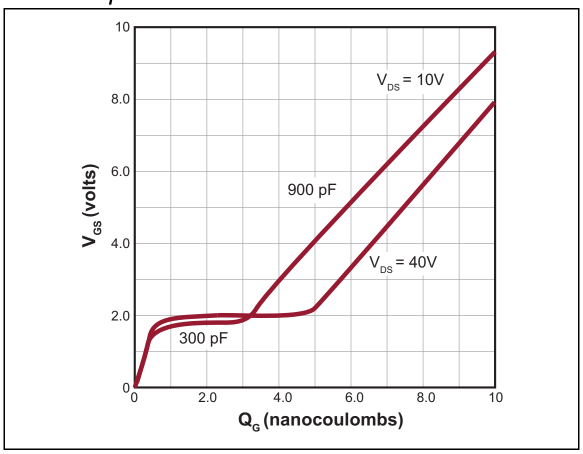


FIGURE 2-6: *Gate Drive Dynamic Characteristics.*

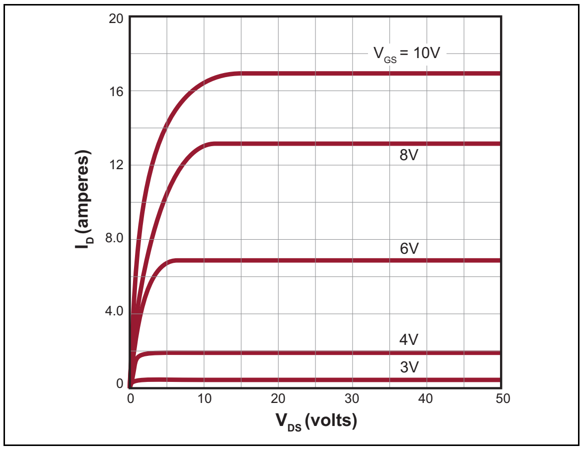


FIGURE 2-7: *Output Characteristics.*

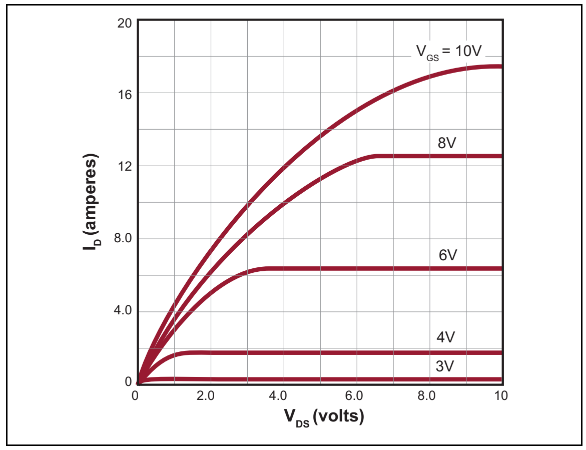


FIGURE 2-10: *Saturation Characteristics.*

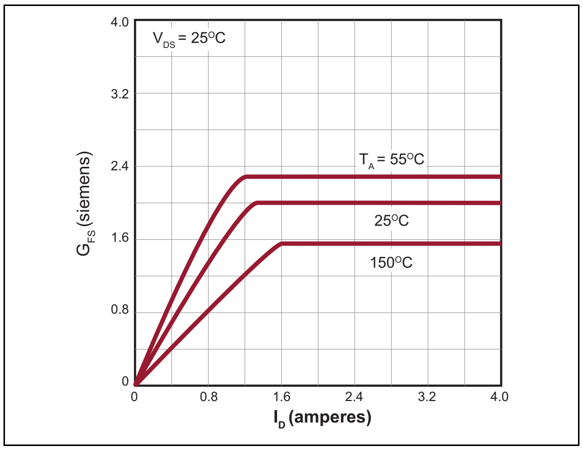


FIGURE 2-8: *Transconductance vs. Drain Current.*

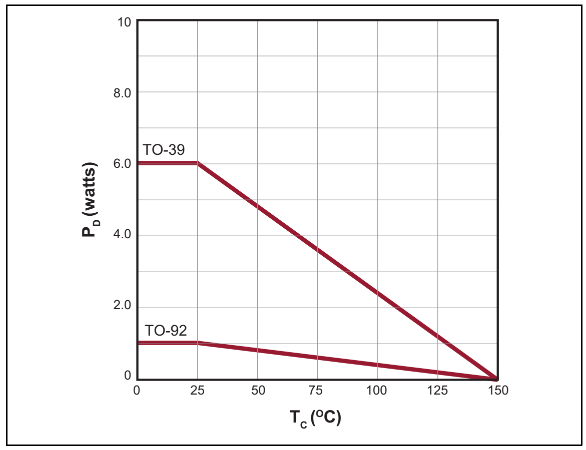


FIGURE 2-11: *Power Dissipation vs. Case Temperature.*

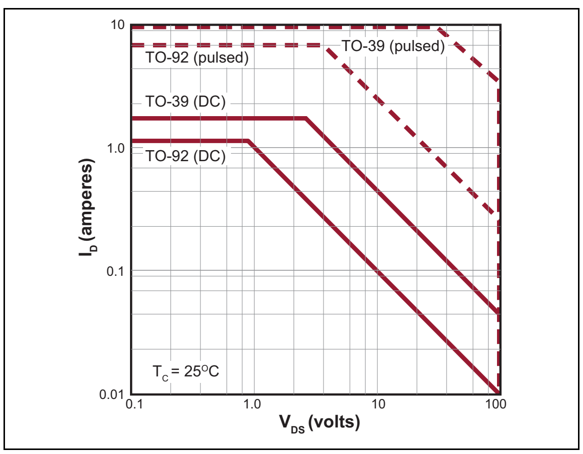


FIGURE 2-9: *Maximum Rated Safe Operating Area.*

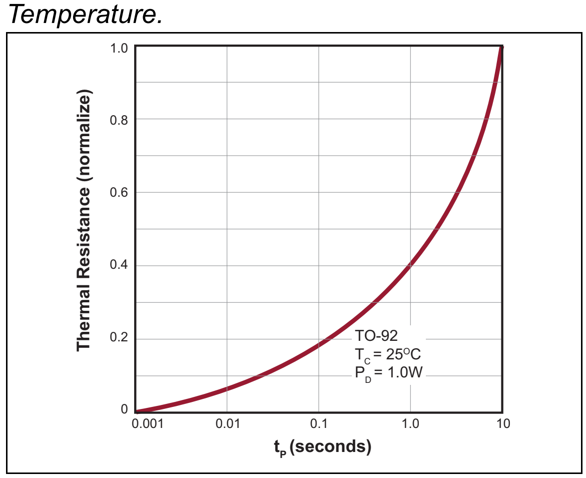


FIGURE 2-12: *Thermal Response Characteristics.*

3.0 PIN DESCRIPTION

Table 3-1 shows the description of pins in TO-39 and TO-92.

TABLE 3-1: TO-39/TO-92 PIN FUNCTION TABLE

Pin Number	TO-39	TO-92	Description
1	Source	Source	Source
2	Gate	Gate	Gate
3	Drain	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VN2210.

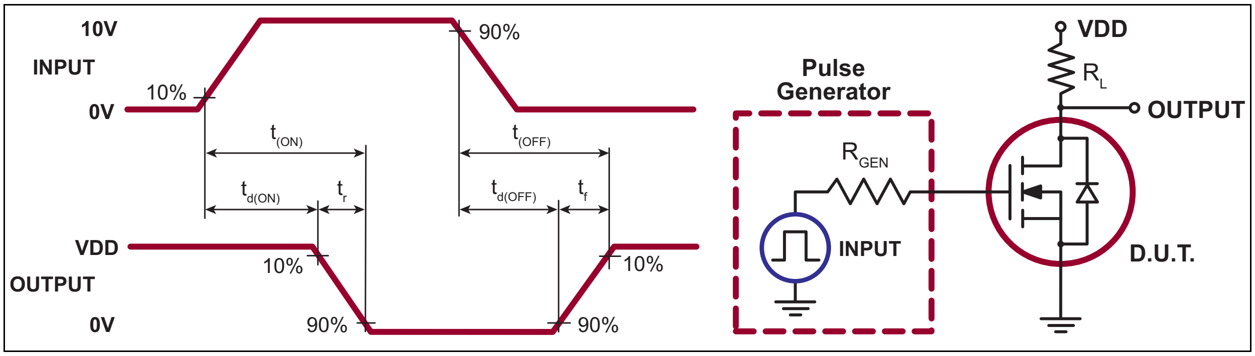


FIGURE 4-1: Switching Waveforms and Test Circuit.

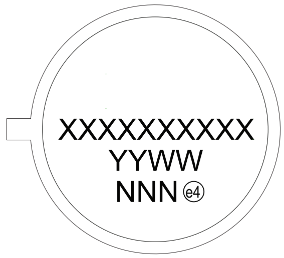
PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(th)}$ (Maximum) (V)
100	0.35	2.4

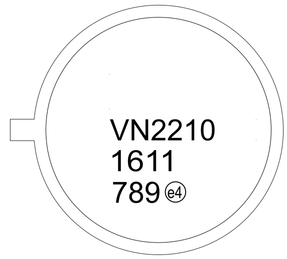
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

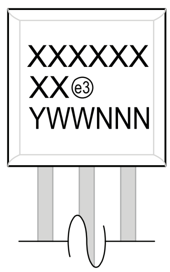
3-Lead TO-39



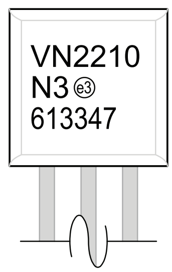
Example



3-lead TO-92



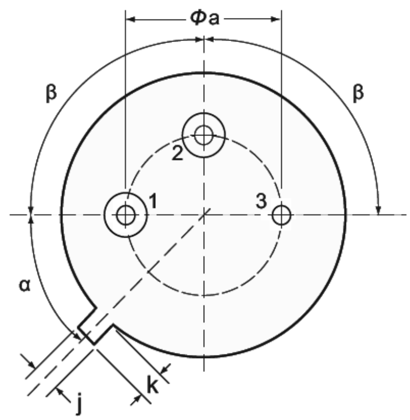
Example



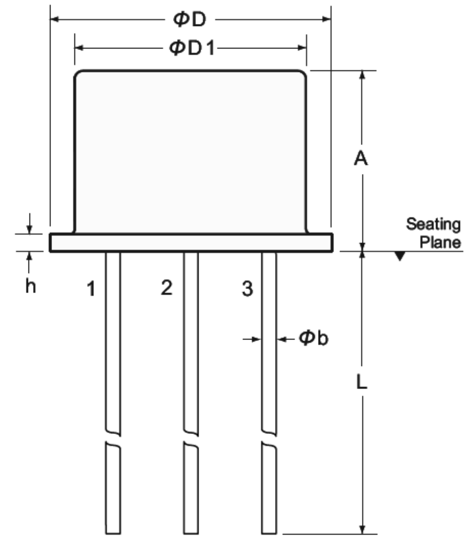
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	e4	Pre-plated

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-39 Package Outline (N2)



Bottom View



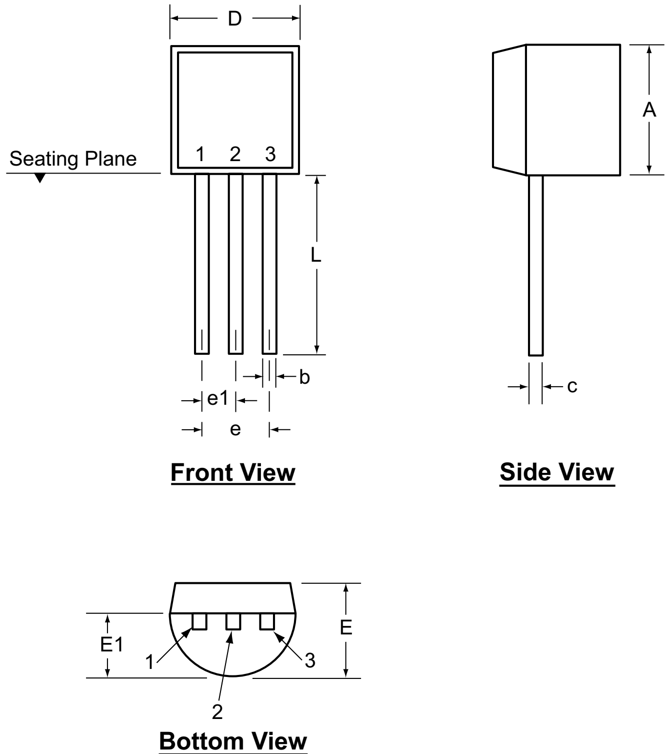
Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		α	β	A	Φa	Φb	ΦD	ΦD1	h	j	k	L
Dimension (inches)	MIN	45° NOM	90° NOM	.240	.190	.016	.350	.315	.009	.028	.029	.500
	NOM			-	-	-	-	-	-	-	-	-
	MAX			.260	.210	.021	.370	.335	.125	.034	.040	.560*

JEDEC Registration TO-39.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (June 2016)

- Converted Supertex Doc# DSFP-VN2210 to Microchip DS20005559A.
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	VN2210	=	N-Channel Enhancement-Mode Vertical DMOS FET
Packages:	N2	=	3-lead TO-39
	N3	=	3-lead TO-92
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	500/Bag for N2 Package
			1000/Bag for N3 Package

Note: VN2210N2 does not include a “-G” designator. However, the package is an RoHS-compliant product.

Examples:

a) VN2210N2: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-39 Package, 500/Bag

b) VN2210N3-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92 Package, 1000/Bag

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