ISL6740A

Flexible Double-Ended Voltage-Mode PWM Controller with Voltage Feed Forward

FN9195
Rev 3.00
February 9, 2012

The ISL6740A is an enhanced ISL6740 PWM controller featuring built-in voltage feed forward functionality. It is pin and feature compatible with the ISL6740 double-ended pulse width modulating (PWM) voltage-mode controller, allowing easy drop-in replacement on existing designs.

Voltage feed forward compensates for input voltage variation without intervention of the feedback control loop. It is particularly useful in unregulated bus converters and DC transformers where wide input voltage variation would otherwise result in large output voltage swings.

In addition to voltage feed forward compensation, the ISL6740A features an extremely flexible oscillator that allows precise control of frequency, duty cycle, and deadtime. Deadtimes of under 40ns are easily achievable.

This advanced BiCMOS design features low operating current, adjustable switching frequency up to 1MHz, adjustable soft-start, internal and external over-temperature protection, fault annunciation, and a bidirectional SYNC signal that allows the oscillator to be locked to paralleled units or to an external clock for noise sensitive applications.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6740AIVZA	6740 AIVZ	-40 to +105	16 Ld TSSOP	M16.173

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6740A. For more information on MSL please see techbrief TB363.

Features

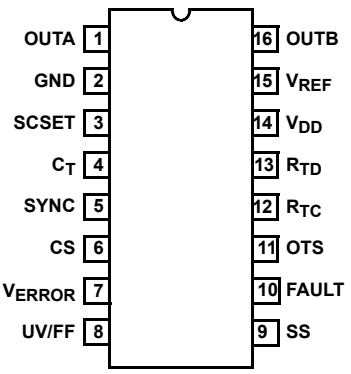
- Input Voltage Feed Forward Compensation
- Precision Duty Cycle and Deadtime Control
- Adjustable Delayed Overcurrent Shutdown and Re-Start
- Adjustable Short Circuit Shutdown and Re-Start
- Adjustable Oscillator Frequency Up to 2MHz
- Bidirectional Synchronization
- Adjustable Input Undervoltage Lockout/Inhibit
- Tight Tolerance Voltage Reference Over Line, Load, and Temperature
- Adjustable Soft-Start
- Fault Signal
- 95µA Startup Current
- Internal Over-Temperature Protection
- System Over-Temperature Protection Using a Thermistor or Sensor
- Pb-free and ELV, WEEE, RoHS Compliant

Applications

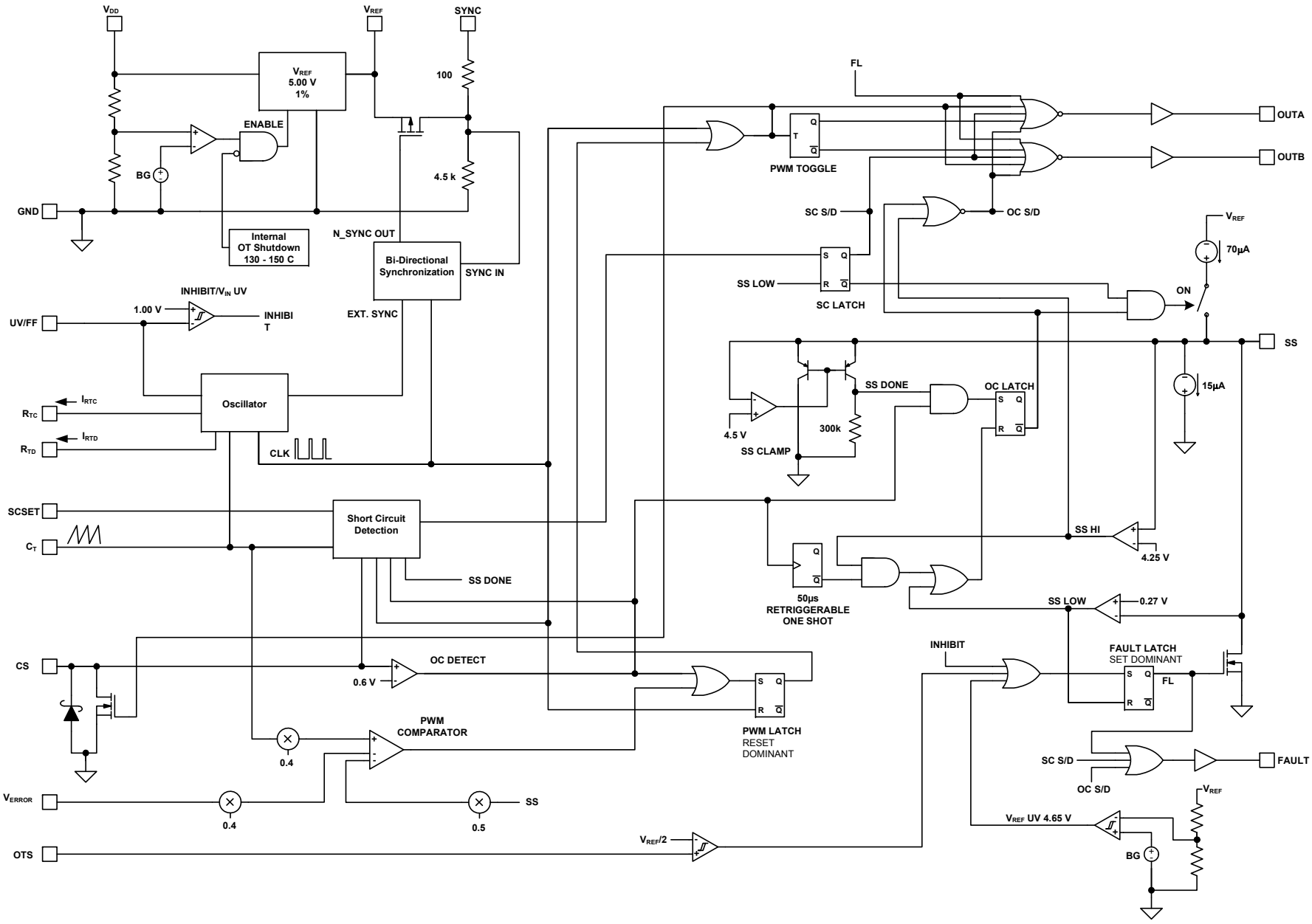
- Telecom and Datacom Power
- Wireless Base Station Power
- File Server Power
- Industrial Power Systems
- DC Transformers and Bus Converters

Pin Configuration

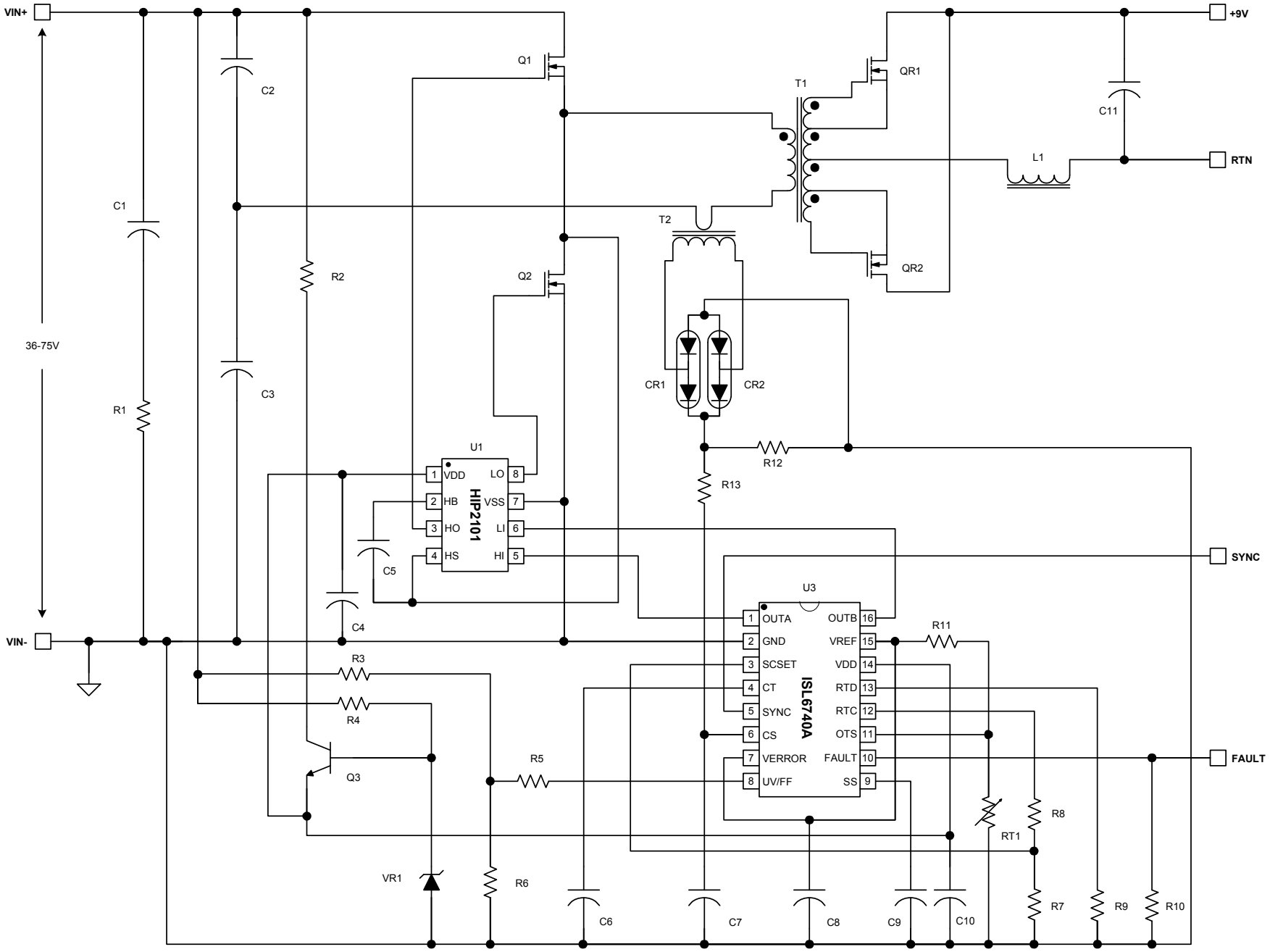
ISL6740A
(16 LD TSSOP)
TOP VIEW



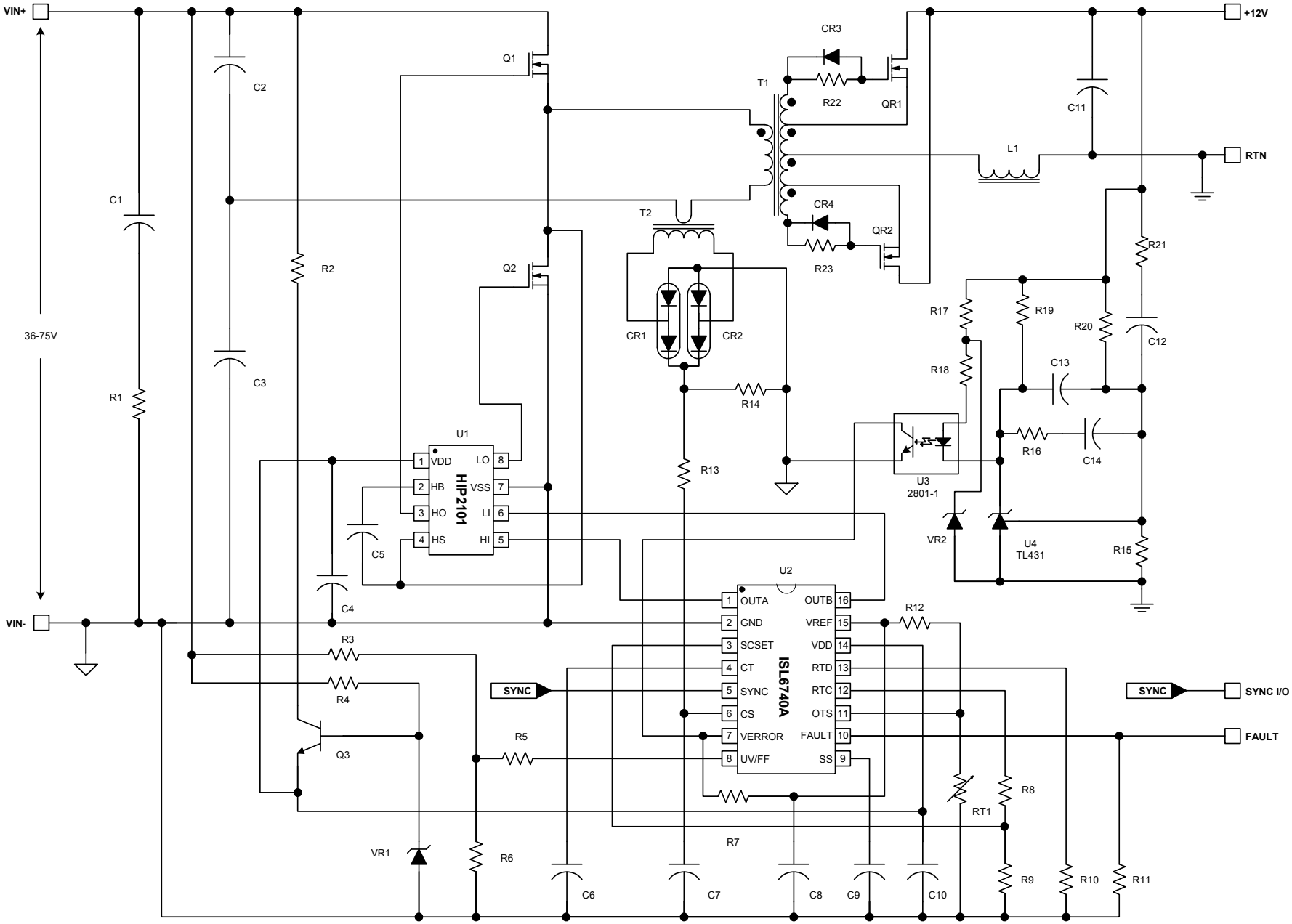
Functional Block Diagram



Typical Application - 48V Input Bus Converter, 9V @ 10A Output



Typical Application - 36 to 75 V Input, Regulated 12V @ 8A Output



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUTA, OUTB, Signal Pins . . . . . GND - 0.3V to V_{REF}
VREF . . . . . .GND - 0.3V to 6.0V
Peak GATE Current 0.5A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) 1500V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) 1000V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TSSOP (Notes 4, 5)	98	30

Maximum Junction Temperature . . . . . .-55°C to 150°C
Maximum Storage Temperature Range . . . . . .-65°C to 150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
ISL6740AIVx . . . . . .-40°C to 105°C
Supply Voltage Range (Typical) . . . . . 9VDC - 16 VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and Typical Application Schematics on page 3 and page 4. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40°C to 105°C, Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY VOLTAGE					
Start-Up Current, I_{DD}	V_{DD} < START Threshold	-	95	**140**	µA
Operating Current, I_{DD}	R_{LOAD}, $C_{OUTA,B}$ = 0	-	5.0	**8.0**	mA
	$C_{OUTA,B}$ = 1nF	-	7.0	**12.0**	mA
UVLO START Threshold		**6.50**	7.25	**8.00**	V
UVLO STOP Threshold		**6.00**	6.75	**7.50**	V
Hysteresis		**0.35**	0.50	**0.75**	V
REFERENCE VOLTAGE					
Overall Accuracy	I_{VREF} = 0, -20mA	**4.900**	5.000	**5.050**	V
Long Term Stability	T_A = 125°C, 1000 hours	-	3	-	mV
Fault Voltage		**4.10**	4.55	**4.75**	V
VREF Good Voltage		**4.25**	4.75	**V_{REF} -0.05**	V
Hysteresis		**75**	165	**250**	mV
Operational Current (Source)		**-20**	-	**-**	mA
Operational Current (Sink)		**5**	-	**-**	mA
Current Limit		**-25**	-	**-100**	mA
CURRENT SENSE					
Current Limit Threshold	V_{ERROR} = V_{REF}	**0.55**	0.6	**0.65**	V
CS to OUT Delay		-	35	**50**	ns
CS Sink Current		-	10	-	mA
Input Bias Current		**-1.00**	-	**1.00**	µA
SCSET Input Impedance		**1**	-	-	MΩ

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and Typical Application Schematics on page 3 and page 4. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40°C to 105°C, Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SC Setpoint Accuracy		-	10	-	%
PULSE WIDTH MODULATOR					
V_{ERROR} Input Impedance		**400**	-	-	kΩ
Minimum Duty Cycle	V_{ERROR} < C_T Valley Voltage	-	-	0	%
Maximum Duty Cycle	V_{ERROR} > 4.75V, $V_{UV/FF}$ = 2.5V (Note 9) R_{TD} = 5.11kΩ, R_{TC} = 25.5kΩ, C_T = 220pF	-	83	-	%
		-	99	-	%
V_{ERROR} to PWM Comparator Input Gain		-	0.4	-	V/V
C_T to PWM Comparator Input Gain		-	0.4	-	V/V
SS to PWM Comparator Input Gain		-	0.5	-	V/V
OSCILLATOR					
Frequency Accuracy	T_A = +25°C (Note 10)	333	351	369	kHz
Frequency Variation with V_{DD}	T_A = +105°C, $\|(F_{20V} - F_{9V})/F_{9V}\|$, UV/FF = 2.00V	-	0.1	0.4	%
	T_A = +25°C, $\|(F_{20V} - F_{9V})/F_{9V}\|$, UV/FF = 2.00V	-	0.1	0.3	
	T_A = -40°C, $\|(F_{20V} - F_{9V})/F_{9V}\|$, UV/FF = 2.00V	-	0.2	0.7	
Frequency Variation with $V_{UV/FF}$	T_A = +25°C, $\|(F_{4.25V} - F_{2.00V})/F_{2.00V}\|$				%
	V_{DD} = 9V	-	1.2	**3**	%
	V_{DD} = 20V	-	1.2	**3**	%
Temperature Stability	$V_{UV/FF}$ = 2.0V, V_{DD} = 9V	-	0.5	**1.5**	%
Charge Current Gain		**1.88**	2.0	**2.12**	µA/µA
Discharge Current Gain		**45**	55	**65**	µA/µA
C_T Valley Voltage	Static operation	**0.75**	0.80	**0.85**	V
C_T Peak Voltage	Static operation				
	$V_{UV/FF}$ = 2.00V	**2.30**	2.40	**2.50**	V
	$V_{UV/FF}$ = 4.25V	**4.10**	4.20	**4.30**	V
R_{TD}, R_{TC} Voltage	R_{LOAD} = 0Ω				
	$V_{UV/FF}$ = 2.00V	-	1.60	-	V
	$V_{UV/FF}$ = 4.25V	-	3.40	-	V
SYNCHRONIZATION					
Input High Threshold (VIH), Minimum		**4.0**	-	-	V
Input Low Threshold (VIL), Maximum		-	-	**0.8**	V
Input Impedance		-	4.5	-	kΩ
Input Frequency Range		**Free Running**	-	**1.67 x Free Running**	Hz
Input Pulse Width		**100**	-	-	ns
High Level Output Voltage (VOH)	I_{LOAD} = -1mA	-	4.5	-	V
Low Level Output Voltage (VOL)	I_{LOAD} = 10µA	-	-	**100**	mV
SYNC Output Current	VOH > 2.0V	**-10**	-	-	mA
SYNC Output Pulse Duration (Minimum)		**250**	-	**532**	ns
SYNC Advance	SYNC rising edge to GATE falling edge, $C_{OUTA/B}$ = C_{SYNC} = 100pF	-	5	-	ns

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 2 and Typical Application Schematics on page 3 and page 4. 9V < V_{DD} < 20 V, R_{TD} = 51.1kΩ, R_{TC} = 10kΩ, C_T = 470pF, T_A = -40°C to 105°C, Typical values are at T_A = 25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SOFT-START					
Charging Current	SS = 2V	**-45**	-55	**-75**	µA
SS Clamp Voltage		**4.35**	4.5	**4.65**	V
Sustained Overcurrent Threshold Voltage	Charged Threshold minus:	**0.20**	0.25	**0.30**	V
Overcurrent/Short Circuit Discharge Current	SS = 2V	**13**	18	**23**	µA
Fault SS Discharge Current	SS = 2V	-	10.0	-	mA
Reset Threshold Voltage		**0.25**	0.27	**0.33**	V
FAULT					
Fault High Level Output Voltage (VOH)	I_{LOAD} = -10mA	**2.85**	3.5	-	V
Fault Low Level Output Voltage (VOL)	I_{LOAD} = 10mA	-	0.4	**0.9**	V
Fault Rise Time	C_{LOAD} = 100pF	-	15	-	ns
Fault Fall Time	C_{LOAD} = 100pF	-	15	-	ns
OUTPUT					
High Level Output Voltage (VOH)	V_{REF} - OUTA or OUTB, I_{OUT} = -50mA, 1µS duration, C_{VREF} = 1.0µF	-	0.5	**1.0**	V
Low Level Output Voltage (VOL)	OUTA or OUTB - GND, I_{OUT} = 50mA, 1µs duration, C_{VREF} = 1.0µF	-	0.5	**1.0**	V
Rise Time	C_{GATE} = 1nF, V_{DD} = 15V	-	50	**100**	ns
Fall Time	C_{GATE} = 1nF, V_{DD} = 15V	-	40	**80**	ns
THERMAL PROTECTION					
Thermal Shutdown		135	145	155	°C
Thermal Shutdown Clear		120	130	140	°C
Hysteresis, Internal Protection		-	15	-	°C
OTS					
Threshold		**2.375**	2.50	**2.625**	V
Hysteresis, Switched Current Amplitude		**18**	25	**30**	µA
UV/FF Undervoltage Inhibit/Feed Forward					
Input Voltage Low/Inhibit Threshold		**0.97**	1.00	**1.03**	V
Hysteresis, Switched Current Amplitude		**7**	10	**15**	µA
Input High Clamp Voltage		**4.8**	-	-	V
Input Impedance		**1**	-	-	MΩ
FF Gain	V_{RTD}/V_{FF}, V_{RTC}/V_{FF}	**0.78**	0.8	**0.82**	V/V
Maximum Control Voltage		**4.20**	-	**V_{REF}**	V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. SYNC pulse width is the greater of this value or the C_T discharge time.
9. This is the maximum duty cycle achievable using the specified values of R_{TC}, R_{TD}, and C_T. Larger or smaller maximum duty cycles may be obtained using other values for these components. See Equations 2-4.
10. The oscillator frequency is affected by the tolerance of the timing components used. In particular, parasitic capacitance at the CT pin introduced by layout, leads, and probes, etc. will lower the frequency.

Typical Performance Curves

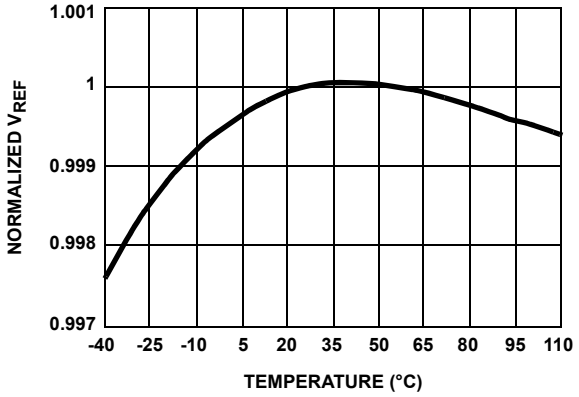


FIGURE 1. REFERENCE VOLTAGE vs TEMPERATURE

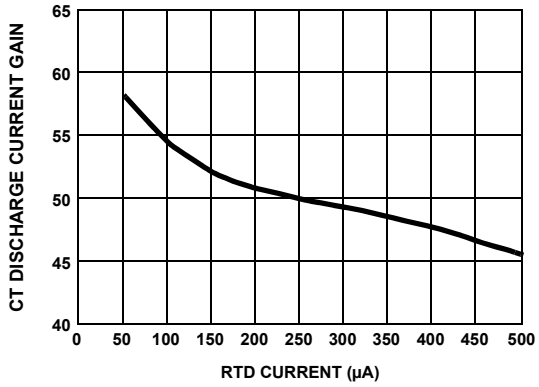


FIGURE 2. OSCILLATOR CT DISCHARGE CURRENT GAIN

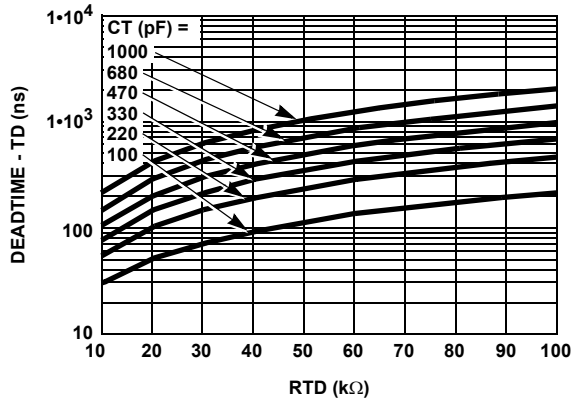


FIGURE 3. DEADTIME (DT) vs CAPACITANCE

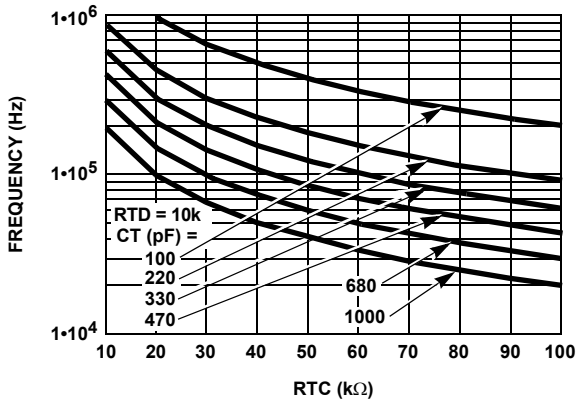


FIGURE 4. CAPACITANCE vs FREQUENCY

Pin Descriptions

V_{DD} - V_{DD} is the power connection for the IC. To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

The total supply current, I_{DD}, will be dependent on the load applied to outputs OUTA and OUTB. Total I_{DD} current is the sum of the quiescent current and the average output current. Knowing the operating frequency, Fsw, and the output loading capacitance charge, Q, per output, the average output current can be calculated from:

$$I_{OUT} = 2 \bullet Q \bullet F_{SW} \quad A \qquad \text{(EQ. 1)}$$

SYNC - A bidirectional synchronization signal used to coordinate the switching frequency of multiple units. Synchronization may be achieved by connecting the SYNC signal of each unit together or by using an external master clock signal. The oscillator timing capacitor, C_T, is always required regardless of the synchronization method used. The paralleled unit with the highest oscillator frequency assumes control. Self-synchronization is not recommended for oscillator frequencies above 900kHz. For higher switching frequencies, an external clock with a pulse width less than one-half of the oscillator period must be used.

R_{TC} - This is the oscillator timing capacitor charge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the charge current. The charge current is nominally twice this current. The PWM maximum ON time is determined by the timing capacitor charge duration. The voltage appearing on this pin is nominally 80% of the voltage applied to the UV/FF pin.

R_{TD} - This is the oscillator timing capacitor discharge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the discharge current. The discharge current is nominally 50x this current. The PWM deadtime is determined by the timing capacitor discharge duration. The voltage appearing on this pin is nominally 80% of the voltage applied to the UV/FF pin.

C_T - The oscillator timing capacitor is connected between this pin and GND.

V_{ERROR} - The inverting input of the PWM comparator. The error voltage is applied to this pin to control the duty cycle. Increasing the signal level increases the duty cycle. The node may be driven with an external error amplifier or opto-coupler.

The ISL6740A features a built-in soft-start capability. Soft-start is implemented as a clamp on the error voltage input.

OTS - The non-inverting input to the over temperature shutdown comparator. The signal input at this pin is compared to an internal threshold of $V_{REF}/2$. If the voltage at this pin exceeds the threshold, the Fault signal is asserted and the outputs are disabled until the condition clears. There is a nominal 25µA switched current source used for hysteresis. The amount of hysteresis is adjustable by varying the source impedance of the signal into this pin.

OTS may be used to monitor parameters other than temperature, such as voltage. Any signal for which a high out-of-bounds monitor is desired may utilize the OTS comparator.

FAULT - The Fault signal is asserted high whenever the outputs, OUTA and OUTB, are disabled. This occurs during an over temperature fault, an input UV fault, a V_{REF} UV fault, or during an overcurrent or short circuit shutdown fault. Fault can be used to disable synchronous rectifiers whenever the outputs are disabled.

Fault is a three-state output and is high impedance during the soft-start cycle. Adding a pull-up resistor to VREF or a pull-down resistor to ground determines the state of Fault during soft-start. This feature allows the designer to use the Fault signal to enable or disable output synchronous rectifiers during soft-start.

UV/FF - Undervoltage monitor and voltage feed forward input pin. A resistor divider between the input source voltage and GND sets the undervoltage lock-out threshold and provides voltage sensing for the feed forward compensation circuit.

The signal is compared to an internal 1.00V reference to detect an undervoltage or inhibit condition. For voltages in excess of the UV threshold, the signal provides voltage information to the voltage feed forward function.

CS - This is the input to the current sense comparator. The overcurrent comparator threshold is set at 0.600V nominal.

The CS pin is shorted to GND at the termination of each output pulse. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. This delay may allow an overlap such that the CS signal may be discharged while the current signal is still active. If the current sense source is low impedance it will cause increased power dissipation.

Exceeding the overcurrent threshold will start a delayed shutdown sequence. Once an overcurrent condition is detected, the soft-start charge current source is disabled. The soft-start capacitor begins discharging through a 25µA current source, and if it discharges to less than 4.25V (Sustained Overcurrent Threshold), a shutdown condition occurs and the OUTA and OUTB outputs are forced low. When the soft-start voltage reaches 0.27V (Reset Threshold) a soft-start cycle begins.

An overcurrent condition must be absent for 50µs before the delayed shutdown control resets. If the overcurrent condition ceases, and an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs. The SS charging current is re-enabled and the soft-start voltage is allowed to recover.

GND - Reference and power ground for all functions on this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.

OUTA and OUTB - Alternate half cycle output stages. Each output is capable of 0.5A peak currents for driving logic level power MOSFETs or MOSFET drivers. Each output provides very low impedance to overshoot and undershoot.

VREF - The 5.00V reference voltage output. +1/-2% tolerance over line, load and operating temperature. Bypass to GND with a 0.047µF to 2.2µF ceramic capacitor. Capacitors outside of this range may cause oscillation.

SS - Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor determines the rate of increase of the duty cycle during start up, controls the overcurrent shutdown delay, and the overcurrent and short circuit hiccup restart period.

SCSET - Sets the duty cycle threshold that corresponds to a short circuit condition. A resistive divider between R_{TC} and GND, V_{REF} to GND, R_{TD} and GND, or a voltage between 0 and 2V may be used to adjust the SCSET threshold. If using a resistor divider from either RTC or RTD, the impedance to GND affects the oscillator timing and should be considered when determining the oscillator timing components. Connecting SCSET to GND disables short circuit shutdown and hiccup.

Functional Description

Features

The ISL6740A PWM is an excellent choice for low cost feed forward voltage mode bridge topologies for applications requiring accurate duty cycle and deadtime control. With its many protection and control features, a highly flexible design with minimal external components is possible. Among its many features are voltage feed forward compensation, adjustable soft-start, overcurrent protection, thermal protection, bidirectional synchronization, fault indication, and adjustable frequency.

Oscillator

The ISL6740A has an oscillator with a programmable frequency range to 2MHz, and can be programmed with two resistors and a capacitor. The use of three timing elements, R_{TC}, R_{TD}, and C_T allows great flexibility and precision when setting the oscillator frequency.

The switching period is the sum of the timing capacitor charge and discharge durations. The charge duration is determined by

R_{TC} and C_T. The discharge duration is determined by R_{TD} and C_T.

$$t_C \approx 0.5 \bullet R_{TC} \bullet C_T \quad S \qquad \text{(EQ. 2)}$$

$$t_D \approx 0.02 \bullet R_{TD} \bullet C_T \quad S \qquad \text{(EQ. 3)}$$

$$t_{SW} = t_C + t_D = \frac{1}{F_{SW}} \quad S \qquad \text{(EQ. 4)}$$

where t_C and t_D are the charge and discharge times, respectively, t_{SW} is the oscillator free running period, and f is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay ads directly to the switching duration, but also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be increased error due to the input impedance at the C_T pin.

The maximum duty cycle, D, and percent deadtime, DT, can be calculated from:

$$D = \frac{t_C}{t_{SW}} \qquad \text{(EQ. 5)}$$

$$DT = 1 - D \qquad \text{(EQ. 6)}$$

Figures 3 and 4 graphically portray the deadtime and oscillator frequency as function of the timing components.

Implementing Synchronization

The oscillator can be synchronized to an external clock applied to the SYNC pin or by connecting the SYNC pins of multiple ICs together. If an external master clock signal is used, the free running frequency of the oscillator should be ~10% slower than the desired synchronous frequency. The external master clock signal should have a pulse width greater than 20ns. The SYNC circuitry will not respond to an external signal during the first 60% of the oscillator switching cycle. Self-synchronization is not recommended for oscillator frequencies above 900kHz. For higher switching frequencies, an external clock with a pulse width less than one-half of the oscillator period must be used.

The SYNC input is edge triggered and its duration does not affect oscillator operation. However, the deadtime is affected by the SYNC frequency. A higher frequency signal applied to the SYNC input will shorten the deadtime. The shortened deadtime is the result of the timing capacitor charge cycle being prematurely terminated by the external SYNC pulse. Consequently, the timing capacitor is not fully charged when the discharge cycle begins. This effect is only a concern when an external master clock is used, or if units with different operating frequencies are paralleled.

Soft-Start Operation

Soft-start is controlled using an external capacitor in conjunction with an internal current source. Soft-start reduces stresses and surge currents during start up.

Upon start up, the soft-start circuitry clamps the error voltage input (V_{ERROR} pin) indirectly to a value equal to the soft-start voltage. The soft-start clamp does not actually clamp the error voltage input as is done in many implementations. Rather the PWM comparator has two inverting inputs such that the lower voltage is in control.

The output pulse width increases as the soft-start capacitor voltage increases. This has the effect of increasing the duty cycle from zero to the regulation pulse width during the soft-start period. When the soft-start voltage exceeds the error voltage at the PWM comparator inputs, soft-start is completed. Soft-start occurs during start-up, after recovery from a Fault condition or overcurrent/short circuit shutdown. The soft-start voltage is clamped to 4.5V.

The Fault signal output is high impedance during the soft-start cycle unless an active fault (see “Fault Conditions” on page 13) is present. A pull-up resistor to VREF or a pull-down resistor to ground should be added to achieve the desired state of Fault during soft-start.

Gate Drive

The outputs are capable of sourcing and sinking 0.5A peak current, but are primarily intended to be used in conjunction with a MOSFET driver due to the 5V drive level. To limit the peak current through the IC, an external resistor may be placed between the totem-pole output of the IC (OUTA or OUTB pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank formed by the parasitic inductances in the traces of the board and the device’s input capacitance.

Undervoltage Monitor, Inhibit, and Feed-Forward

The UV/FF input is used for input source undervoltage lockout and inhibit functions as well as sensing the input voltage for feed forward compensation.

If the node voltage falls below 1.00V, a UV shutdown fault occurs. This may be caused by low source voltage or by intentional grounding of the pin to disable the outputs. There is a nominal 10µA switched current source used to create hysteresis. The current source is active only during a UV/Inhibit fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis is a function of the external resistor divider impedance. If the resistor divider impedance results in too little hysteresis, a series resistor between the UV pin and the divider may be used to increase the hysteresis. A soft-start cycle begins when the UV/Inhibit fault clears.

The voltage hysteresis created by the switched current source and the external impedance is generally small due to the large resistor divider ratio required to scale the input voltage down to the UV threshold level. A small capacitor placed between the UV input and ground may be required to filter noise out.

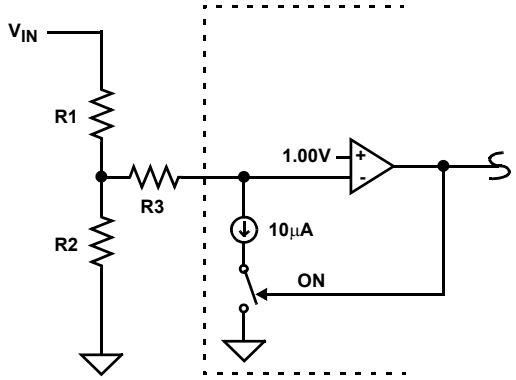


FIGURE 5. UV HYSTERESIS

As V_{IN} decreases to a UV condition, the threshold level is:

$$V_{IN(DOWN)} = \frac{R1 + R2}{R2} \quad V \qquad \text{(EQ. 7)}$$

The hysteresis voltage, ΔV, is:

$$\Delta V = 10^{-5} \bullet \left\langle R1 + R3 \bullet \left(\frac{R1 + R2}{R2}\right)\right\rangle \quad V \qquad \text{(EQ. 8)}$$

Setting R3 equal to zero results in the minimum hysteresis, and yields:

$$\Delta V = 10^{-5} \bullet R1 \quad V \qquad \text{(EQ. 9)}$$

As V_{IN} increases from a UV condition, the threshold level is:

$$V_{IN(UP)} = V_{IN(DOWN)} + \Delta V \quad V \qquad \text{(EQ. 10)}$$

Output voltage variation caused by changes in the supply voltage may be virtually removed through a technique known as feed forward compensation. Using feed forward, the duty cycle is directly modulated based on changes in the input voltage only. No closed loop feedback system is required. The feed forward circuit uses the voltage applied to the UV/FF pin to modulate the oscillator ramp amplitude with minimal effect on the switching frequency and deadtime of the oscillator. The voltage feed forward operates over a 3:1 input voltage range.

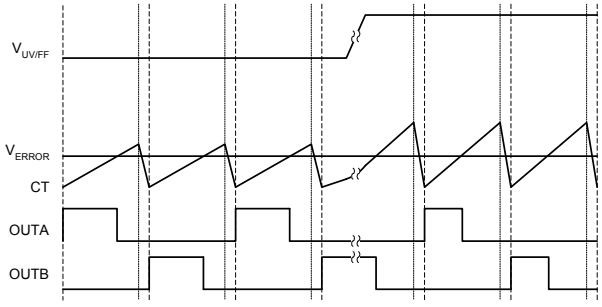


FIGURE 6. FEED FORWARD BEHAVIOR

The voltage applied to the UV/FF pin is multiplied by 0.8 and output on the R_{TC} and R_{TD} pins. This voltage is also summed with the C_T valley threshold voltage (0.8 V) to create the C_T peak threshold voltage. As the voltage applied to UV/FF varies, the CT peak voltage and the CT charge and discharge currents vary, all in direct proportion to each other. The result is an amplitude modulated sawtooth waveform on C_T that is frequency invariant.

The voltage amplitude of C_T ranges from 1.6V to 4.2V as the voltage on UV increases. The UV threshold defines the minimum amplitude of C_T and corresponds to maximum duty cycle operation.

For unregulated bus converters and DC transformers, feed forward can compensate for input voltage variations without a closed loop feedback network. A resistive voltage divider from V_{REF} to V_{ERROR} sets the feed forward control voltage. For example, if the desired duty cycle at the minimum operating voltage is 90%, then:

$$V_{ERROR} = D_{max}(V_{UV/FF} \bullet 0.8) + 0.8 \quad V \qquad \text{(EQ. 11)}$$

$$= 0.9(1.0 \bullet 0.8) + 0.8 = 1.52 \quad V$$

Overcurrent Protection

There are two overcurrent protection mechanisms in the ISL6740A, one for light overcurrent and one for heavy over load. They are referred to, respectively, as overcurrent protection and short circuit protection.

OVERCURRENT OPERATION

Overcurrent delayed shutdown is enabled once the soft-start cycle is complete. If an overcurrent condition is detected, the soft-start charging current source is disabled and the soft-start capacitor is allowed to discharge through a 15µA source. At the same time a 50µs re-triggerable one-shot timer is activated. It remains active for 50µs after the overcurrent condition ceases. If the soft-start capacitor discharges by more then 0.25V to 4.25V, the output is disabled and the Fault signal asserted. This state continues until the soft-start voltage reaches 270mV, at which time a new soft-start cycle is initiated. If the overcurrent condition stops at least 50µs prior to the soft-start voltage decreasing to 4.25V, the soft-start charging currents revert to normal operation and the soft-start voltage is allowed to recover.

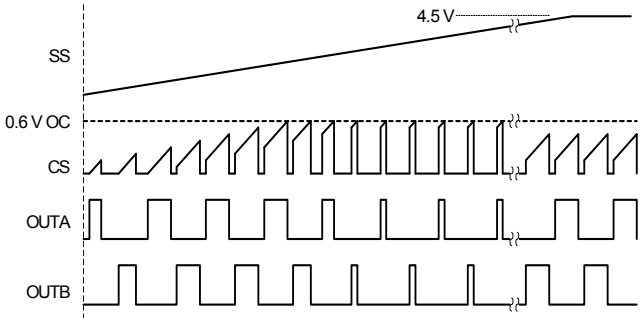


FIGURE 7. PULSE-BY-PULSE OC BEHAVIOR DURING SS

Figure 7 shows the overcurrent behavior during SS. Although an overcurrent condition exists, a shutdown is not allowed prior to completion of the SS cycle. Only peak current limit operates during the soft-start cycle. If the overcurrent condition were to continue beyond the soft-start cycle, a delayed overcurrent shutdown would occur as shown in Figure 8.

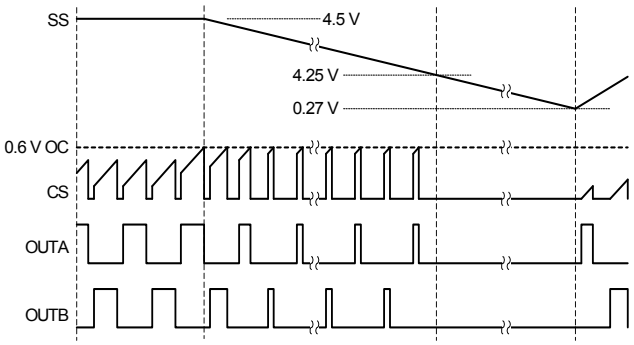


FIGURE 8. OC SHUTDOWN BEHAVIOR

Figure 8 portrays the typical delayed overcurrent shutdown behavior. Once SS has discharged to 4.25V, the outputs are disabled and remain that way until SS has discharged to 0.27V, and then a new SS cycle begins.

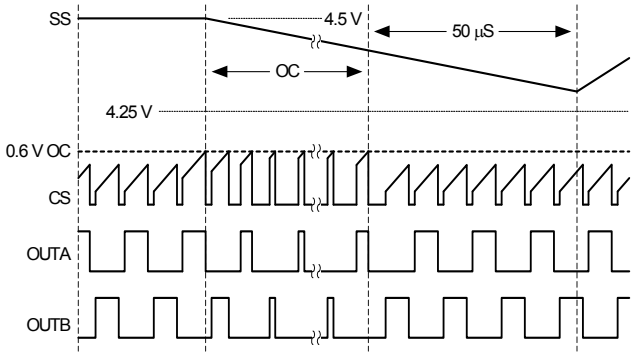


FIGURE 9. OC RECOVERY PRIOR TO SHUTDOWN

If the overcurrent condition is removed prior to a shutdown, a recovery can occur as indicated in Figure 9. When the load decreases below the overcurrent threshold and an additional 50µs elapses without the SS dropping below 4.25V, the overcurrent circuitry resets and the soft-start voltage recovers.

The duration of the OC shutdown period can be increased by adding a resistor between VREF and SS. The value of the resistor must be large enough so that the minimum specified SS discharge current is not exceeded. Using a 422kΩ resistor, for example, will result in a small current being injected into SS, effectively reducing the discharge current. This will nearly double the OFF time. The external pull-up resistor will also decrease the SS duration, so its effect should be considered when selecting the value of the SS capacitor.

Latching OC shutdown is also possible by using a lower valued resistor between VREF and SS. If the SS node is not allowed to discharge below the SS reset threshold, the IC will not recover from an overcurrent fault. The value of the resistor must be low enough so that the maximum specified discharge current is not sufficient to pull SS below 0.33V. A 200kΩ resistor, for example, prevents SS from discharging below ~0.4V. Again, the external pull-up resistor will decrease the SS duration, so its effect should be considered when selecting the value of the SS capacitor.

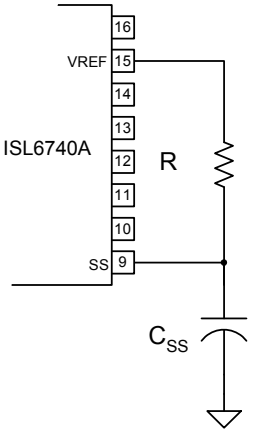


FIGURE 10. MODIFYING OC SHUTDOWN TIMING

Short Circuit Operation

If the output current increases beyond the overcurrent threshold, peak current limit will reduce the duty cycle. As the load current continues to increase, the duty cycle continues to decrease. A short circuit event is defined as the simultaneous occurrence of current limit and a reduced duty cycle.

The degree of reduced duty cycle that defines a short circuit condition is user adjustable using the SCSET input. A resistor divider between R_{TD}, R_{TC}, or V_{REF} and GND to RCSET sets a threshold that is compared to the voltage on the timing capacitor, C_T. The resistor divider voltage divided by 2 corresponds to the duty cycle below which a short circuit can exist.

$$D_{SC} = \frac{V_{SCSET}}{2} \cdot D_{max} \quad \text{(EQ. 12)}$$

where D_{SC} is the maximum short circuit duty cycle, V_{SCSET} is the voltage applied to SCSET, and D_{max} is the maximum duty cycle. If the timing capacitor voltage fails to exceed the threshold before an overcurrent pulse is detected, a short circuit condition exists. A shutdown will occur if 8 short circuit events occur within 32 oscillator cycles. Once shutdown occurs, SS will discharge through a 15µA current source. A new soft-start cycle will begin when SS reaches 0.27V.

Latching shutdown may be implemented in the same manner as described in the overcurrent section. Short circuit shutdown is enabled once the soft-start cycle is complete. Connecting SCSET to GND inhibits short circuit shutdown.

If either R_{TC} ar R_{TD} are used as the voltage source for the divider, the effect of the SCSET divider must be included in the timing calculations since the current sourced from R_{TC} and R_{TD} determine the charge and discharge currents for the timing capacitor. Typically the resistor between either R_{TC} or R_{TD} and GND is formed by two series resistors with the center node connected to SCSET.

Alternatively, SCSET may be set using a voltage between 0V and 2V. This voltage divided by 2 determines the percentage of the maximum duty cycle that corresponds to a short circuit when current limit is active. For example, if the maximum duty cycle is 95% and 1V is applied to SCSET, then the short circuit duty cycle is 50% of 95% or 47.5%.

Fault Conditions

A fault condition occurs if any of the following conditions occur:

- V_{REF} falls below 4.65V
- UV falls below 1.00V
- the internal thermal protection triggers
- OTS faults

When any of the above faults are detected, OUTA and OUTB outputs are disabled, Fault is asserted, and the soft-start capacitor is quickly discharged. When the fault condition clears and the soft-start voltage is below the reset threshold, a soft-start cycle begins. Fault is high impedance during the soft-start cycle unless an active fault is present.

A shutdown resulting from an overcurrent or short circuit condition also causes assertion of Fault, but the soft-start capacitor is not quickly discharged. The initiation of a new soft-start cycle is delayed while the soft-start capacitor is discharged at a 15µA rate. This reduces the repetition rate of the hiccup behavior and keeps the average output current to a minimum.

Thermal Protection

Two methods of over temperature protection are provided. The first method is an on board temperature sensor that protects the device should the junction temperature exceed 145°C. There is approximately 15°C of hysteresis.

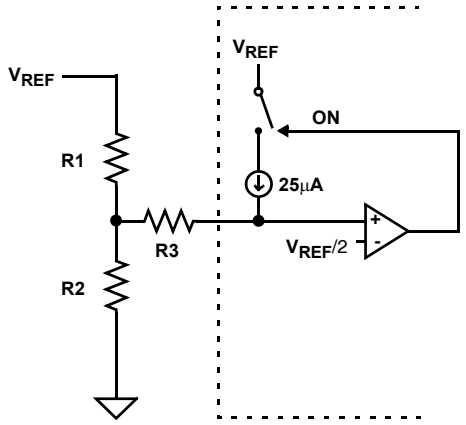


FIGURE 11. OTS HYSTERESIS

The second method uses an internal comparator with a 2.5V reference ($V_{REF}/2$). The non-inverting input to the comparator is accessible through the OTS pin. A thermistor or thermal sensor located at or near the area of interest may be connected to this input. There is a nominal 25µA switched current source used to create hysteresis. The current source is active only during an OT fault; otherwise, it is inactive and does not affect the node voltage. The magnitude of the hysteresis is a function of the external resistor divider impedance. Either a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) thermistor may be used. If a NTC thermistor is desired, position R1 may be substituted. If a PTC is desired, then position R2 may be substituted. The threshold with increasing temperature is set by making the fixed resistance equal in value to the thermistor resistance at the desired trip temperature.

$V_{TH}\uparrow$ = 2.5V and R1 = R2 (HOT)

To determine the value of the hysteresis resistor, R3, select the value of thermistor resistance that corresponds to the desired reset temperature.

$$R3 = \frac{10^5 \bullet (R1 - R2) - R1 \bullet R2}{R1 + R2} \quad \Omega \qquad \text{(EQ. 13)}$$

If the hysteresis resistor, R3, is not desired, the value of the thermistor resistance at the reset temperature can be determined from:

$$R1 = \frac{2.5 \bullet R2}{2.5 - 10^{-5} \bullet R2} \quad \Omega \quad (\text{NTC}) \qquad \text{(EQ. 14)}$$

$$R2 = \frac{2.5 \bullet R1}{2.5 + 10^{-5} \bullet R1} \quad \Omega \quad (\text{PTC}) \qquad \text{(EQ. 15)}$$

OTHER USES FOR OTS

The OTS comparator may also be used to monitor signals other than as suggested above. It may also be used to monitor any voltage signal for which an excess requires a response as described above. Input and output voltage monitoring are examples of this.

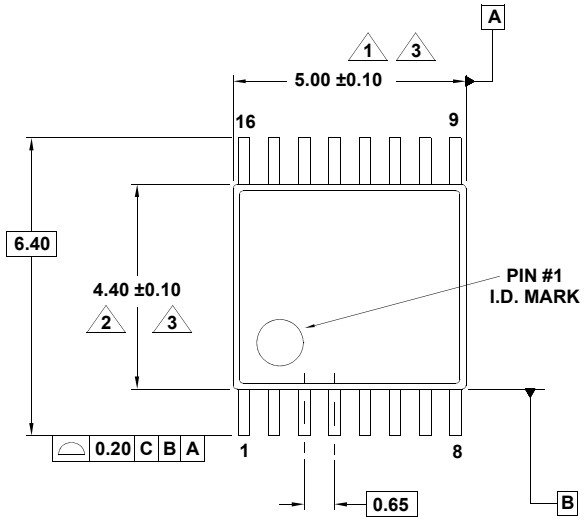
Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} and V_{REF} should be bypassed directly to GND with good high frequency capacitance.

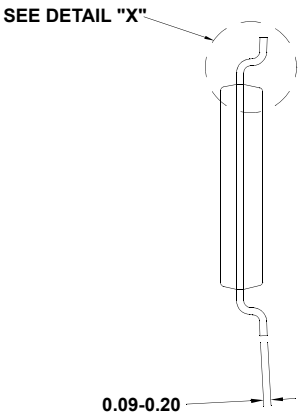
Package Outline Drawing

M16.173

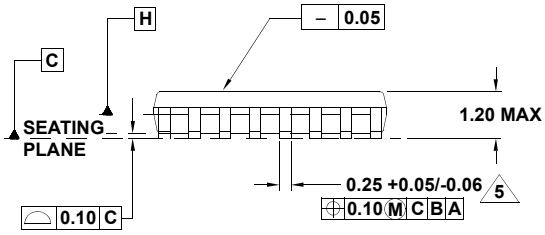
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



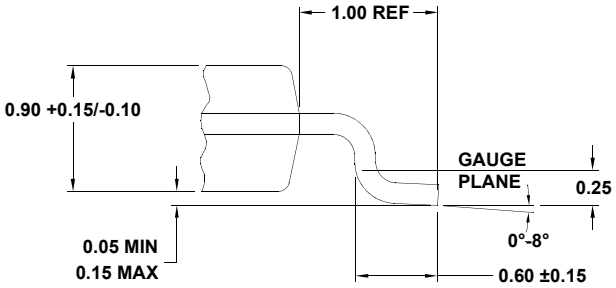
TOP VIEW



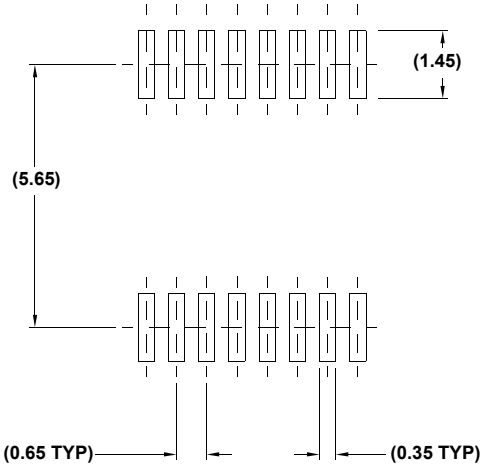
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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