



PL60208X

PCIe Octal, Ultra-Low Jitter, HCSL Frequency Synthesizer

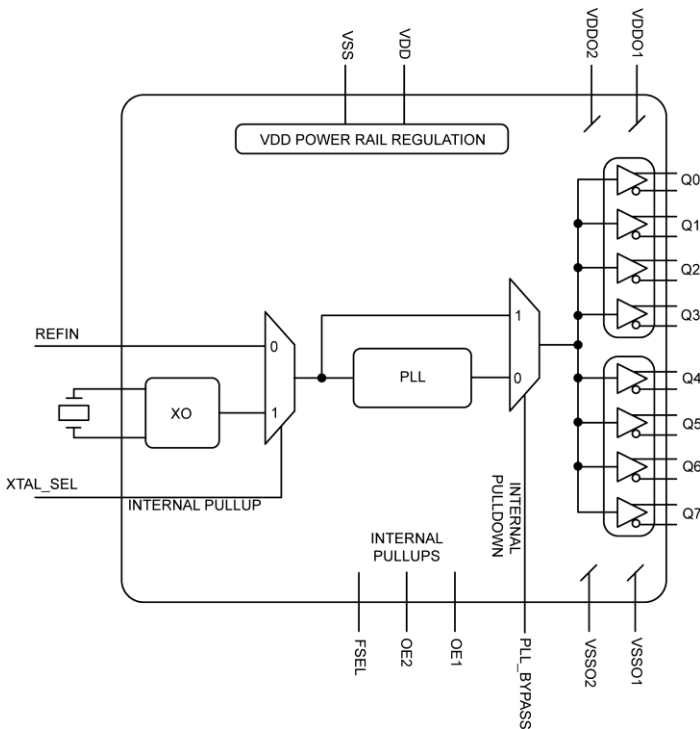
General Description

The PL602081 and PL602082 are members of the PCI Express family of devices from Micrel and provide an extremely low-noise timing solution for PCI Express clock signals. They are based upon a unique synthesizer architecture that provides very low phase noise.

The devices operate from a 3.3V or 2.5V power supply and synthesize eight HCSL output clocks. The PL602081 synthesizes 25MHz, 100MHz, or 200MHz and the PL602082 synthesizes 25MHz, 125MHz, or 250MHz. The PL60208x devices accept a 25MHz crystal or LVCMOS reference clock.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Generates eight HCSL clock outputs.
- PL602081 output frequencies: 25MHz, 100MHz, or 200MHz.
- PL602082 output frequencies: 25MHz, 125MHz, or 250MHz.
- 2.5V or 3.3V operating range.
- Typical phase jitter: 250fs for 12KHz to 20MHz.
- Compliant with PCI Express Gen1, Gen2, and Gen3.
- Industrial temperature range (-40°C to +85°C).
- RoHS and PFOS compliant.
- Available in 44-pin 7mm × 7mm QFN package.

Applications

- Servers
- Storage systems
- Switches and routers
- Gigabit Ethernet
- Set-top boxes/DVRs

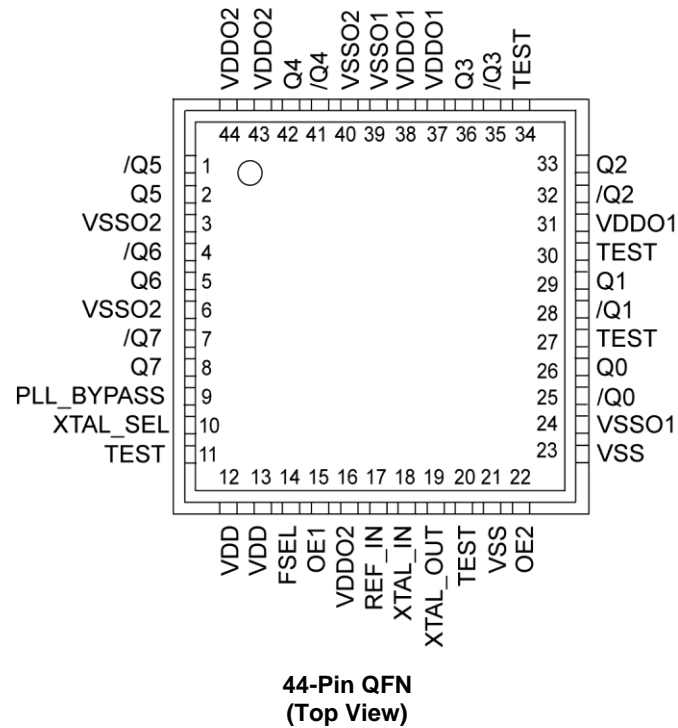
Ordering Information⁽¹⁾

| Part Number | Marking | Shipping | Junction Temperature Range | Package |
|----------------|-------------|---------------|----------------------------|------------|
| PL602081UMG | PL602081UMG | Tray | -40° to +85°C | 44-Pin QFN |
| PL602081UMG TR | PL602081UMG | Tape and Reel | -40° to +85°C | 44-Pin QFN |
| PL602082UMG | PL602082UMG | Tray | -40° to +85°C | 44-Pin QFN |
| PL602082UMG TR | PL602082UMG | Tape and Reel | -40° to +85°C | 44-Pin QFN |

Note:

1. Devices are RoHS and PFOS compliant.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Name |
|------------|----------------------|----------|-----------|--|
| 1, 2 | /Q5, Q5 | O, (DIF) | HCSL | Differential clock output. |
| 4, 5 | /Q6, Q6 | | | |
| 7, 8 | /Q7, Q7 | | | |
| 25, 26 | /Q0, Q0 | | | |
| 28, 29 | /Q1, Q1 | | | |
| 32, 33 | /Q2, Q2 | | | |
| 35, 36 | /Q3, Q3 | | | |
| 41, 42 | /Q4, Q4 | | | |
| 14 | FSEL | I, (SE) | LVC MOS | Frequency select, 1 = 100MHz, 0 = 200MHz, 45KΩ pull-up. |
| 12, 13 | VDD | PWR | | Power supply. |
| 31, 37, 38 | VDDO1 | PWR | | Power supply for outputs Q0 – Q3. |
| 16, 43, 44 | VDDO2 | PWR | | Power supply for outputs Q4 – Q7. |
| 21, 23 | VSS (exposed pad) | PWR | | Core power supply ground. The exposed pad must be connected to the VSS ground plane. |
| 24, 39 | VSSO1 | PWR | | Power supply ground for outputs Q0 – Q3. |
| 3, 6, 40 | VSSO2 | PWR | | Power supply ground for outputs Q4 – Q7. |

Pin Description (Continued)

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Name |
|-----------------------|------------|----------|--------------|--|
| 9 | PLL_BYPASS | I, (SE) | LVC MOS | PLL bypass, selects output source. 0 = normal PLL operation 1 = output from input reference clock or crystal 45K Ω pull down |
| 10 | XTAL_SEL | I, (SE) | LVC MOS | Selects PLL input reference source 0 = REF_IN, 1 = XTAL, 45K Ω pull-up |
| 11, 20, 27, 30, 34 | TEST | | | Factory test pins. Do not connect anything to these pins. |
| 17 | REF_IN | I, (SE) | LVC MOS | Reference clock input |
| 18 | XTAL_IN | I, (SE) | 10pF crystal | Crystal reference input, no load caps needed (see Figure 6) |
| 19 | XTAL_OUT | O, (SE) | 10pF crystal | Crystal reference output, no load caps needed (see Figure 6) |
| 15 | OE1 | I, (SE) | LVC MOS | Output enable, outputs Q0 – Q3 disable to tri-state, 0 = disabled, 1 = enabled, 45K Ω pull-up |
| 22 | OE2 | I, (SE) | LVC MOS | Output enable, outputs Q4 – Q7 disable to tri-state, 0 = disabled, 1 = enabled, 45K Ω pull-up |

Absolute Maximum Ratings⁽²⁾

| | |
|--|--------------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +4.6V |
| Input Voltage (V_{IN}) | -0.50V to V_{DD} +0.5V |
| Lead Temperature (soldering, 20s) | 260°C |
| Case Temperature | 115°C |
| Storage Temperature (T_S) | -65°C to +150°C |

Operating Ratings⁽³⁾

| | |
|--|--------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +2.375V to +3.465V |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Junction Thermal Resistance ⁽⁴⁾ | |
| QFN (θ_{JA}) Still-Air | 24°C/W |
| QFN (ψ_{JB}) Junction-to-Board | 8°C/W |

DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------------------|-----------------------------------|--|-------|------|-------|-------|
| V_{DD} , $V_{DDO1/2}$ | 2.5V operating range | | 2.375 | 2.5 | 2.625 | V |
| V_{DD} , $V_{DDO1/2}$ | 3.3V operating range | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Supply current $V_{DD} + V_{DDO}$ | Eight outputs enabled, 100MHz Outputs 50Ω to V_{SS} | | 217 | 270 | mA |
| | | Eight outputs enabled, 200MHz Outputs 50Ω to V_{SS} | | 229 | 285 | |
| | | Four outputs enabled, 100MHz Outputs 50Ω to V_{SS} , OE1 or OE2 = 0 | | 149 | 185 | |
| | | Four outputs enabled, 200MHz Outputs 50Ω to V_{SS} , OE1 or OE2 = 0 | | 158 | 197 | |

HCSL DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. $R_L = 50\Omega$ to V_{SS}

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------|------------------------|-----------|------|------|------|-------|
| V_{OH} | Output high voltage | | 660 | 700 | 850 | mV |
| V_{OL} | Output low voltage | | -150 | 0 | 27 | mV |
| V_{CROSS} | Crossing point voltage | | 250 | 350 | 550 | mV |

LVCMOS (PLL_BYPASS, XTAL_SEL, FSEL, OE1, OE2) DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|--------------------------------|------|------|----------------|---------|
| V_{IH} | Input high voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{iL} | Input low voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input high current | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{iL} | Input low current | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

REF_IN DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|---|------|------|----------------|---------|
| V_{IH} | Input high voltage | | 1.1 | | $V_{DD} + 0.3$ | V |
| V_{iL} | Input low voltage | | -0.3 | | 0.6 | V |
| I_{IN} | Input current | $XTAL_SEL = V_{iL}, V_{IN} = 0V$ to V_{DD} | -5 | | 5 | μA |
| | | $XTAL_SEL = V_{IH}, V_{IN} = V_{DD}$ | | 20 | | |

Crystal Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------------------|-----------|--------------------------------|------|------|----------|
| Mode of oscillation | 10pF load | Fundamental, parallel resonant | | | |
| Frequency | | | 25 | | MHz |
| Equivalent series resistance (ESR) | | | | 50 | Ω |
| Shunt capacitor, C0 | | | 2 | 5 | pF |
| Correlation drive level | | | 10 | 100 | μW |

AC Electrical Characteristics^(4, 6)

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. $R_L = 50\Omega$ to V_{SS}

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------------|---------------------------------|--|------|--|------|-------|
| T_R/T_F | HCSL output rise/fall time | 20% - 80% | 150 | 300 | 450 | ps |
| ODC | Output duty cycle | | 48 | 50 | 52 | % |
| T_{SKEW} | Output-to-output skew | Note 7 | | | 45 | ps |
| T_{LOCK} | PLL lock time | | | | 20 | ms |
| $T_{jit}(\emptyset)$ | RMS phase jitter ⁽⁸⁾ | 100MHz or 125MHz Integration range (12kHz – 20MHz) Integration range (10kHz – 1.5MHz) Integration range (1.5MHz – Nyquist) 200MHz or 250MHz Integration range (12kHz – 20MHz) Integration range (10kHz – 1.5MHz) Integration range (1.5MHz – Nyquist) | | 254 220 142 253 222 112 | | fs |

Notes:

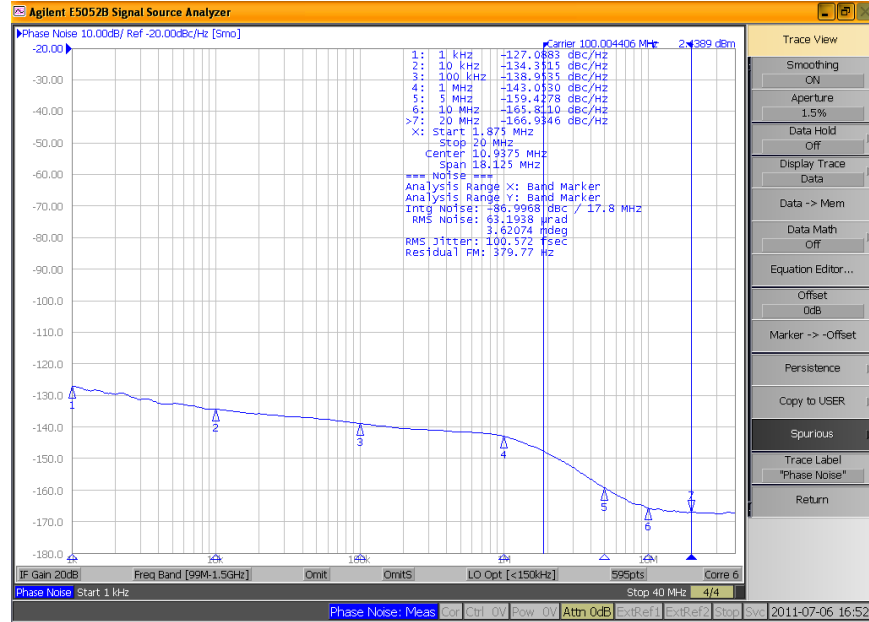
- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
- Specification for packaged product only
- All phase noise measurements were taken with an Agilent 5052B phase noise system.
- Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
- Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Truth Tables

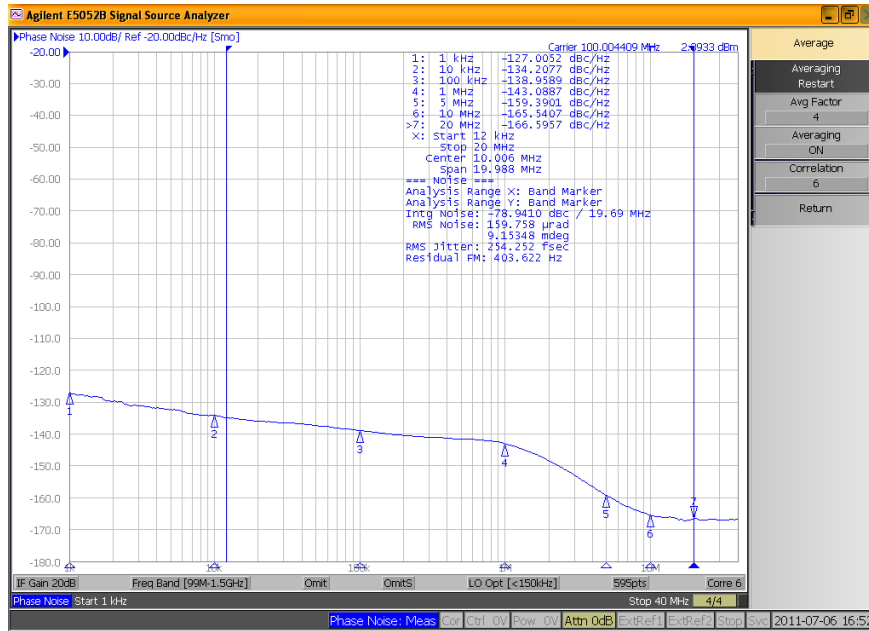
| PLL_BYPASS | XTAL_SEL | OE2 | OE1 | INPUT | OUTPUT |
|------------|----------|-----|-----|--------|-----------------|
| 0 | – | 1 | 1 | – | PLL |
| 1 | – | 1 | 1 | – | XTAL/REF_IN |
| – | 0 | 1 | 1 | REF_IN | – |
| – | 1 | 1 | 1 | XTAL | – |
| – | – | 0 | 1 | – | Q4-Q7 Tri-state |
| – | – | 1 | 0 | – | Q0-Q3 Tri-state |

| FSEL | PLL_BYPASS | Output Frequency (MHz) | |
|------|------------|------------------------|----------|
| | | PL602081 | PL602082 |
| 0 | 0 | 200 | 250 |
| 1 | 0 | 100 | 125 |
| X | 1 | 25 | 25 |

Phase Noise Plots

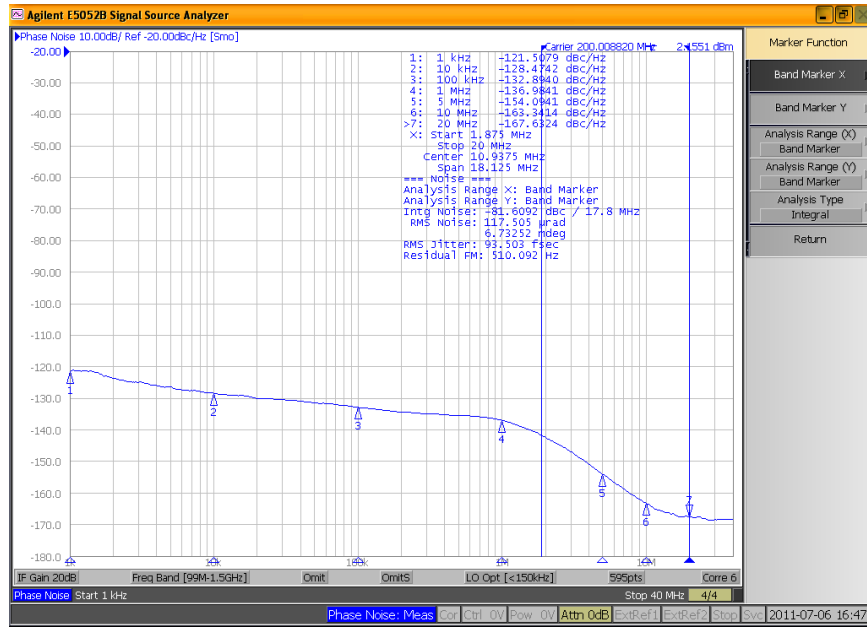


Phase Noise Plot: 100MHz, 1.875MHz – 20MHz 101fs

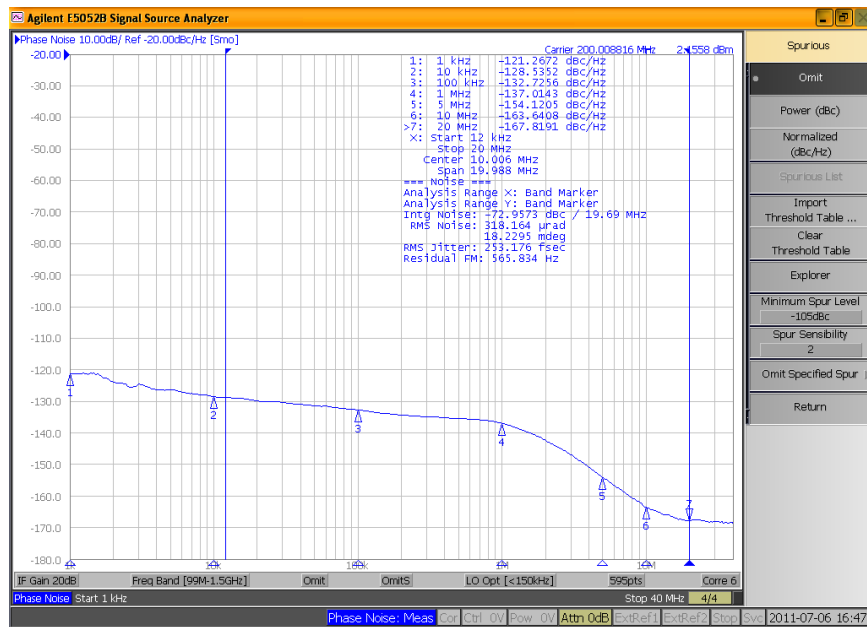


Phase Noise Plot: 100MHz, 12kHz – 20MHz 254fs

Phase Noise Plots (Continued)



Phase Noise Plot: 200MHz, 1.875MHz – 20MHz 94fs



Phase Noise Plot: 200MHz, 12kHz – 20MHz 253fs

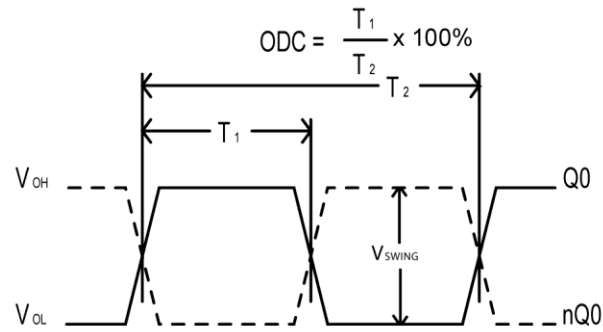


Figure 1. Duty Cycle Timing

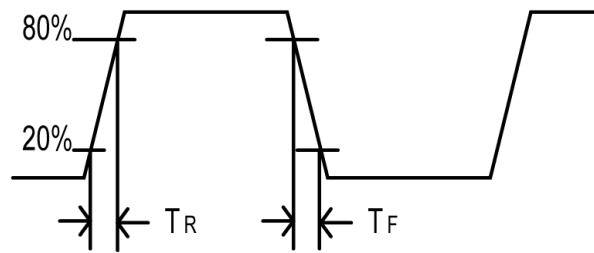


Figure 2. All Outputs Rise/Fall Time

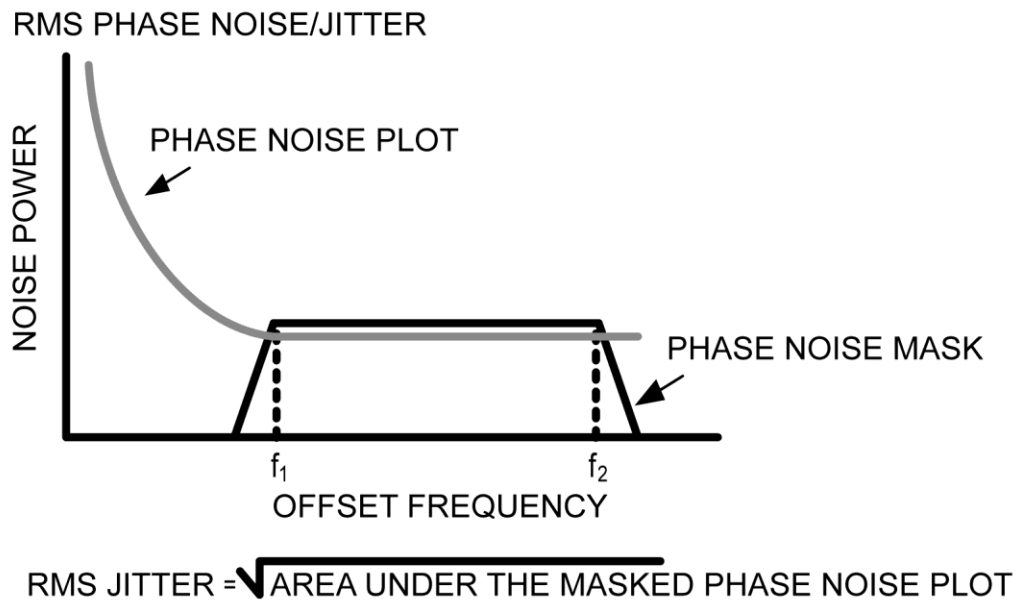


Figure 3. RMS Phase/Noise Jitter

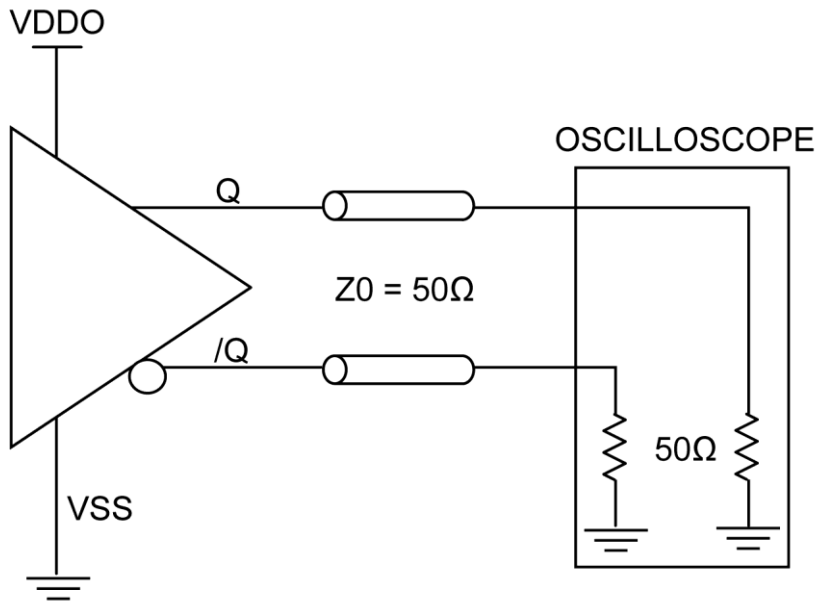


Figure 4. HCSL Output Load and Test Circuit

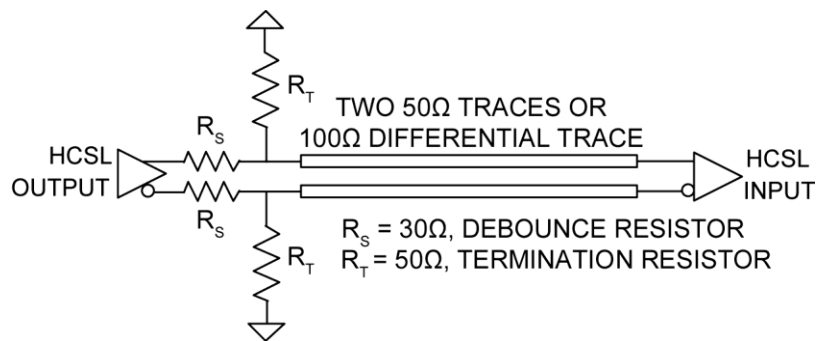


Figure 5. HCSL recommended application termination (source terminated)

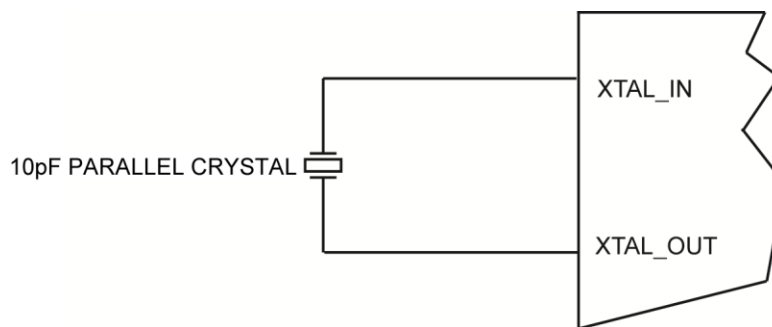


Figure 6. Crystal Input Interface

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the Selecting a Quartz crystal for the *Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's TCG applications group if you need assistance on selecting a suitable crystal for your application at: hbwhelp@micrel.com.

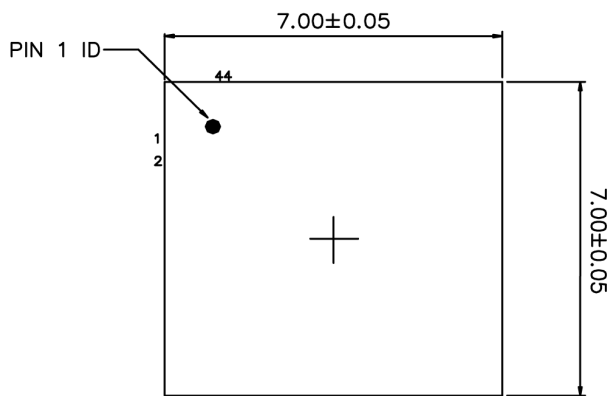
Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL60208X.

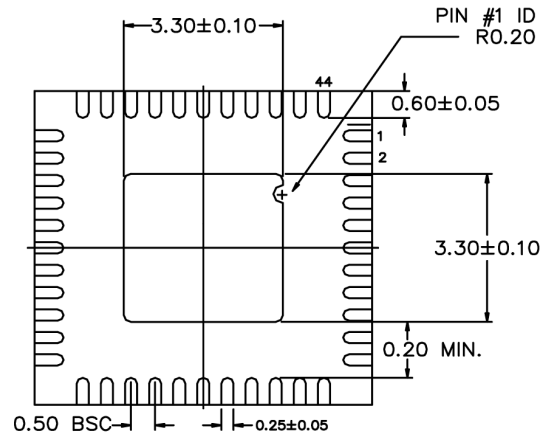
HCSL Outputs

HCSL outputs are to be terminated with 50Ω to VSS. For best performance load all outputs. If you want to AC-couple or change the termination, contact Micrel's application group at: hbwhelp@micrel.com.

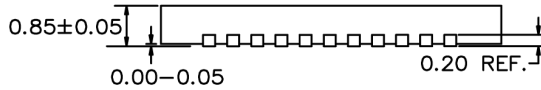
Package Information⁽⁹⁾



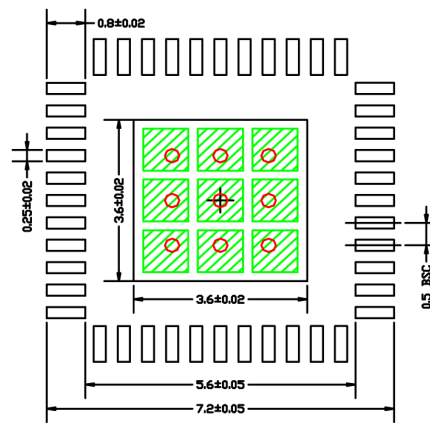
TOP VIEW
NOTE 1, 2, 3



BOTTOM VIEW
NOTE 1, 2, 3



SIDE VIEW
NOTE 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE 4, 5

NOTE:

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

44-Pin QFN

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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