Quasi-Resonant Control DC/DC converter and Power Factor Correction converter IC for AC/DC Converter

BM1051F

●General Description

BM1051F is compounded LSI of Power Factor Correction converter (PFC) for harmonic solution and DC/DC converter (DC/DC). Because DC/DC operates on Quasi-resonant method, DC/DC contributes to Low EMI.
BM1051F built in a HV starter circuit that tolerates 650V. Because of putting the current sense resistors externally both the PFC part and the DC/DC part, IC enables power supply design free.

In the PFC part, IC adopts peak current control operation. Suitable application is proposed by a various protection circuit, such as the multiplier with a revision circuit on the AC voltage falls, the load regulation revision circuit, and the maximum power feed-forward circuit, etc.

The Quasi-resonant system of a DC/DC part contributes to low EMI because PFC operates by soft switching.
A burst mode is built in, so the power is reduced at light load. Various protection functions, such as a soft start function, a burst function, an over-current limiting for every cycle, overvoltage protection, and over current protection, are built in. The pin for communicated control with a controller and the external stop pin are prepared; it proposes the system that can be adapted for various applications.

●Basic specifications

- Operating Power Supply Voltage Range:
  VCC：8.0 to 24.0V
- Operating Current:
  QR ON (PFC OFF)：1.20mA(pulse on)
  QR ON (PFC OFF)：1.00mA(pulse off)
  QR ON (PFC ON)：1.80mA(pulse on)
- Oscillation Frequency QR part :120kHz(FB=2.0V typ)
- Operating Temperature: -40℃ to +85℃

●Typical Application Circuit(s)

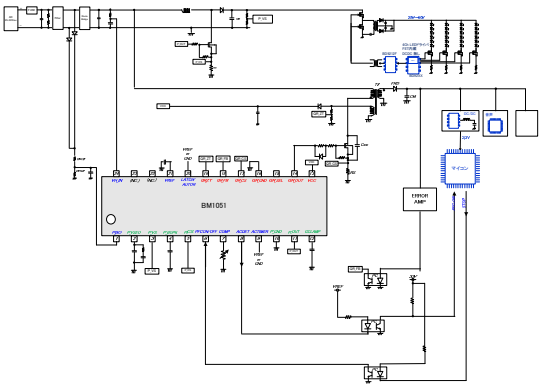


Figure 1. Application circuit

●Features

- Quasi-resonant circuit + PFC circuit
- Built-in HV Starter circuit
- Low consumption current (typ.10uA) when starter circuit is OFF.
- Quasi resonant circuit
  Max operating frequency(120kHz)
  Frequency reduction function
  Over-current limiting variable function
  Pulse-by-pulse over-current protection circuit
  Built-in Soft start
  Voltage protection function (brown out) during low input
  ZT pin Over Voltage Protection
  Output overload protection (auto recovery /latch switching enabled)
  250nsec Leading-Edge Blanking
- Power Factor Correction circuit
  Peak current control (65kHz)
  Per-cycle over current protection circuit
  Maximum power revision
  the multiplier with a revision circuit when the AC voltage falls
  the load change measure circuit
- Selectable protection method by LATCH/AUTOR terminal.
  LATCH/AUTOR=H : Latch
  LATCH/AUTOR=L : Auto recovery
- External stop function (COMP pin)
- AC input voltage stop detected function (ACDET)
- Built-in PFC stop terminal (PFCON/OFF)

●Package(s)

SOP24	15.0mm (Typ.)	× 5.40mm (Typ.)	× 1.80mm (TYP.)	pitch1.27mm (TYP.)

●Applications

TV, AC adapters, printers, LED lighting

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

●Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Rating	Unit	Conditions
Maximum applied voltage 1	V_{max1}	650	V	VH_IN
Maximum applied voltage 2	V_{max2}	30	V	VCC, QR_SEL
Maximum applied voltage 3	V_{max3}	5.5	V	P_BO, P_VSEO, P_VS, P_BOPK P_CS,PFCON/OFF,COMP, ACDET, ACTIMER,QR_CS, QR_ZT, QR_FB,LATCH/AUTOR, VREF
Maximum applied voltage 4	V_{max4}	15	V	GCLAMP, P_OUT, QR_OUT
output peak current 1	I_{OH}	-0.5	A	QR_OUT, P_OUT
output peak current 2	I_{OL}	1.0	A	QR_OUT, P_OUT
QR_ZT pin current 1	I_{SZT1}	-2.0	mA	
QR_ZT pin current 2	I_{SZT2}	3.0	mA	
Allowable dissipation	P_d	687.6 (Note1)	mW	
Operating temperature range	T_{opr}	-40 ～ +85	°C	
Maximum junction temperature	T_{jmax}	150	°C	
Storage temperature range	T_{str}	-55 ～ +150	°C	

(Note1) When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Reduce to 5.5 mW/°C when Ta = 25°C or above.

●Operating Conditions (Ta = 25℃)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	VCC	8.0～24.0	V	VCC
Power supply voltage range 2	VH_IN	80～600	V	VH_IN
Power supply voltage range 3	P_BO	0.0～1.8	V	P_BO

●**Electrical Characteristics (Unless otherwise noted, Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Circuit current]						
Circuit current (ON) 1	I_{ON1}	0.700	1.200	1.700	mA	VCC=12.0V (QR=ON, PFC=OFF) QR_FB=1.0V (during pulse operation)
Circuit current (ON) 2	I_{ON2}	0.700	1.000	1.300	mA	VCC=12.0V (QR =ON, PFC=OFF) QR_FB=VREF (during pulse operation when OFF)
Circuit current (ON) 3	I_{ON3}	0.800	1.800	2.800	mA	VCC=12.0V (QR =ON, PFC=ON) QR_FB=1.0V (during pulse operation)
[Start circuit Block]						
Start current 1	I_{START1}	0.100	0.500	1.000	mA	VCC= 0V
Start current 2	I_{START2}	1.000	3.000	5.000	mA	VCC=10V
OFF Current	I_{START3}	-	10	16	uA	Input current from VH_IN terminal after releasing UVLO
VH voltage switched start current	V_{SC}	0.400	0.800	1.400	V	
[VREF Block]						
VREF output voltage	V_{REF1}	3.500	4.000	4.500	V	
VREF output capacitor	C_{REF}	0.68	1.00	2.20	uF	
GCLAMP voltage 1	GCL1	11.0	12.5	14.0	V	VCC=15V
GCLAMP voltage 2	GCL2	11.0	12.5	14.0	V	VCC=22V
VREF UVLO 1	V_{RUVLO1}	77.5 (3.100V)	87.5 (3.500V)	97.5 (3.900V)	%	When VREF rise The ratio of VREF pin voltage.
VREF UVLO 2	V_{RUVLO2}	52.5 (2.100V)	62.5 (2.500V)	72.5 (2.900V)	%	When VREF drop The ratio of VREF pin voltage.
VREF UVLO hysteresis	V_{RUVLO3}	-	25 (1.000V)	-	%	$V_{RUVLO3}= V_{RUVLO1}- V_{RUVLO2}$
VCC UVLO voltage 1	V_{UVLO1}	12.50	13.50	14.50	V	VCC rise
VCC UVLO voltage 2	V_{UVLO2}	6.00	7.00	8.00	V	VCC drop
VCC UVLO hysteresis	V_{UVLO3}	-	6.50	-	V	$V_{UVLO3}= V_{UVLO1}- V_{UVLO2}$
VCC OVP voltage 1	V_{OVP1}	24.0	27.0	30.0	V	VCC rise
VCC OVP voltage 2	V_{OVP2}	20.0	23.0	26.0	V	VCC drop
VCC OVP hysteresis	V_{OVP3}	-	4.0	-	V	$V_{OVP3}= V_{OVP1} - V_{OVP2}$
Brown out detection voltage 1	V_{BO1}	0.350	0.400	0.450	V	P_BO rise
Brown out detection voltage 2	V_{BO2}	-	0.200	-	V	P_BO drop
Brown out hysteresis	V_{BO3}	-	0.200	-	V	$V_{BO3} = V_{BO1} - V_{BO2}$
Brown out detection delay time 1	T_{BO1}	21.8	32.0	42.2	ms	Times until ACDET logic change (ACTIMER=L)
Brown out detection delay time 2	T_{BO2}	87.0	128.0	169.0	ms	Times until ACDET logic change (ACTIMER=H)
Brown out detection delay time 3	T_{BO3}	170	250	330	ms	Times until PFC and QR stop

●**Electrical Characteristics (Unless otherwise noted ,Ta=25,VH_IN=320Vdc,VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[ACDET pin characteristics]						
ACDET pin ON resister	R_{ACDET}	50	100	200	Ω	
[ACTIMER pin characteristics]						
ACTIMER pin input L level	$V_{ACTIMEL}$	-	-	0.3	V	
ACTIMER pin input H level	$V_{ACTIMEH}$	1.2	-	-	V	
ACTIMER pin pull-down resistor	$R_{ACTIMEH}$	165	330	500	kΩ	
[PFCON/OFF pin characteristics]						
PFCON/OFF pin input L level	$V_{PON/OFFL}$	-	-	0.3	V	PFC = ON
PFCON/OFF pin input H level	$V_{PON/OFFH}$	1.2	-	-	V	PFC = OFF
PFCON/OFF pin pull-down resistor	$R_{PON/OFFH}$	50	100	150	kΩ	
PFCON/OFF pin timer time	$T_{PFCON/OFF}$	0.50	1.50	3.00	ms	
[LATCH/AUTOR pin characteristics]						
LATCH/AUTOR pin input L level	V_{MODEL}	-	-	0.3	V	
LATCH/AUTOR pin input H level	V_{MODEH}	1.2	-	-	V	
LATCH/AUTOR pin pull-down resistor	R_{MODEH}	50	100	150	kΩ	
[COMP pin characteristics]						
COMP pin detection voltage	V_{COMP}	0.370	0.500	0.630	V	
COMP pin pull-up resistor	R_{COMP}	19.4	25.9	32.3	kΩ	
External Thermistor resistor	R_T	3.32	3.70	4.08	kΩ	
Latch release voltage （VCC pin voltage）	$V_{LATCHOFF}$	-	V_{UVLO2} -0.5	-	V	
Latch mask time	T_{COMP}	70	150	240	us	

●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Quasi-resonant Control Block]						
[Quasi-resonant DC/DC converter Block (turn off)]						
QR_FB pin pull-up resistance	R_{FB}	15	20	25	kΩ	
CS over-current detect voltage 1A	V_{lim1A}	0.950	1.000	1.050	V	I_{zt}<1.0mA
CS over-current detect voltage 1B	V_{lim1B}	0.630	0.700	0.770	V	I_{zt}>1.0mA
CS over-current detect voltage 1C	V_{lim1C}	-	0.250	-	V	I_{zt}<1.0mA
CS over-current detect voltage 1D	V_{lim1D}	-	0.750	-	V	I_{zt}<1.0mA
CS over-current detect voltage 2A	V_{lim2A}	-	0.150	-	V	QR_FB=0.3V (I_{zt}<1.0mA)
CS switched ZT current	I_{ZT}	0.800	1.000	1.200	mA	
CS Leading Edge Blanking time	T_{LEB}	-	0.250	-	us	
Turn off time	T_{OFF}	-	0.250	-	us	*1
Minimum ON width	T_{min}	-	0.500	-	us	T_{LEB}＋T_{OFF}
[Quasi-resonant DC/DC converter Block (turn on)]						
Maximum operating frequency 1	F_{SW1}	106	120	134	KHz	QR_FB=2.00V
Maximum operating frequency 2	F_{SW2}	24	30	36	KHz	QR_FB=0.50V
Frequency reduction start FB voltage	V_{FBSW1}	1.15	1.250	1.350	V	
Frequency reduction end FB voltage	V_{FBSW2}	0.35	0.50	0.65	V	
Voltage gain	AV_{CS}	1.70	2.00	2.30	V/V	⊿V (QR_FB)/⊿V（QR_CS）
ZT comparator voltage 1	V_{ZT1}	60	100	140	mV	QR_ZT drop
ZT comparator voltage 2	V_{ZT2}	300	400	500	mV	QR_ZT rise
ZT trigger timeout period	T_{ZTOUT}	-	15	-	us	Count from final ZT trigger
[Quasi-resonant DC/DC converter protection functions]						
Soft start time1	T_{SS1}	0.60	1.00	1.40	ms	
Soft start time2	T_{SS2}	2.60	4.00	5.40	ms	
FB OLP Voltage 1a	V_{FOLP1A}	2.5	2.8	3.1	V	Operate QR_FB rise
FB OLP Voltage 1b	V_{FOLP1B}	-	2.6	-	V	Operate QR_FB drop
FB OLP Voltage 2a	V_{FOLP2A}	3.3	3.6	3.9	V	Switched latch / Auto recovery rise
FB OLP Voltage 2b	V_{FOLP2B}	-	3.4	-	V	Switched latch / Auto recovery drop
FB OLP mode switched external connected resistor	R_{FOLP2}	90	100	110	kΩ	QR_FB pin external resistance value (during latch mode)
FB OLP timer	T_{FOLP}	44	64	84	ms	
ZT OVP Voltage	V_{ZTL}	3.2	3.5	3.8	V	
[QR_OUT pin]						
QR_OUT pin PMOS ON resistor	R_{POUT}	5	15	30	Ω	
QR_OUT pin NMOS ON resistor	R_{NOUT}	2	5	10	Ω	
[QR_SEL pin]						
QR_SEL pin Ron	R_{MASK}	-	150	-	Ω	

*1 Pulse is applied to QR_CS pin
*2 Pulse is applied to QR_ZT pin

●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Power Factor Correction（PFC）controller block]						
[Power Factor Correction (PFC) Gm amplifier block]						
P_VS pin pull-up current	I_{P_VS}	-	0.50	-	uA	
Gm amplifier normal voltage	V_{VSAMP}	2.460	2.500	2.540	V	
Gm amplifier trans-conductance	V_{VSGM}	30.8	44.0	57.2	uS	
Maximum Gm amplifier source current	I_{VSAMP1}	15	25	35	uA	P_VS=1.0V
Maximum Gm amplifier sink current	I_{VSAMP2}	24	40	56	uA	P_VS=3.5V
[Power Factor Correction (PFC) input voltage monitor block]						
P_BO input voltage range	V_{P_BOIN}	0.000	-	1.800	V	
P_BO pin leak current	I_{BOLEAK}	-1.00	0.00	1.00	uA	
[Power Factor Correction (PFC) input voltage peak detect block]						
P_BOPK max charge current	$I_{BOPKCHG}$	36	72	144	uA	
P_BOPK max discharge current	$I_{BOPKDIS}$	0.1	0.2	0.4	uA	
[Power Factor Correction (PFC) multiplier block]						
Multiplier constant	K_{MULTI}	0.37	0.54	0.71		
P_VSEO stop voltage 1	V_{VSEO1}	181	226	271	mV	BOPK=0.56V
P_VSEO stop voltage 2	V_{VSEO2}	88	128	168	mV	BOPK=1.30V
[Power Factor Correction (PFC) Oscillation frequency block]						
PFC Oscillation frequency	F_{PSW1}	60	65	70	KHz	
Minimum Pulse width	T_{min}	-	500	-	ns	
Maximum DUTY	D_{max}	90.0	94.0	98.0	%	
[Power Factor Correction (PFC) Driver block]						
P_OUT pin PMOS ON resistor	RP_{POUT}	5	15	30	Ω	
P_OUT pin NMOS ON resistor	RP_{NOUT}	2	5	10	Ω	

●**Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)**

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Power Factor Correction (PFC) controller block]						
[Power Factor Correction (PFC) protection function block]						
Leading Edge Blanking time	T_{PLEB}	-	250	-	ns	
P_CS over current limit voltage 1	V_{PCS1}	0.93	1.16	1.40	V	P_BOPK=0.56V
P_CS over current limit voltage 2	V_{PCS2}	0.48	0.60	0.72	V	P_BOPK=1.30V
P_VS short protection voltage	V_{P_SHORT}	0.200 (-92%)	0.300 (-88%)	0.400 (-84%)	V	Figure of () is comparison with P_VS standard voltage 2.5V
QR power-limit P_VS voltage1	V_{PFCON}	1.800 (-28%)	2.000 (-20%)	2.200 (-12%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
QR power limit P_VS voltage2	V_{PFCOFF}	1.100 (-56%)	1.250 (-50%)	1.400 (-44%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS QR power limit hysteresis	V_{PFCHYS}	-	0.750 (30%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS gain rise voltage	V_{PGUP}	2.050 (-18%)	2. 250 (-10%)	2.450 (-2%)	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS gain fall voltage	V_{POVP1}	-	2.625 (+5%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS over voltage protection voltage	V_{POVP2}	-	2.725 (+9%)	-	V	Figure of () is the ratio of P_VS standard voltage 2.5V
P_VS over voltage protection timer	T_{POVP2}	16	32	48	ms	The time to detect P_VS over voltage protection

●**PIN Configure**

Table 1. I/O Pin Functions

NO	PIN	I/O	Function	ESD protection system	
				VCC	GND
1	P_BO	I	Input AC Voltage monitor pin	○	○
2	P_VSEO	I/O	PFC gm amplifier output pin	○	○
3	P_VS	I	PFC Output voltage monitor pin	○	○
4	P_BOPK	O	Connected capacitor to the pin	○	○
5	P_CS	I	PFC Coil current monitor pin	○	○
6	PFCON/OFF	I	PFC ON/OFF control input pin	○	○
7	COMP	I	External latch stop pin	○	○
8	ACDET	O	Input AC voltage state communication pin	○	○
9	ACTIMER	I	Brown out detection time setting input pin	○	○
10	GND	I/O	GND	○	-
11	P_OUT	O	PFC Output drive pin	○	○
12	GCLAMP	I/O	Gate H level clamp pin	○	○
13	VCC	I/O	Power supply pin	-	○
14	QR_OUT	O	Quasi-resonant Output drive pin	○	○
15	QR_SEL	O	Quasi-resonant Mask pin	-	○
16	GND	I/O	GND	○	-
17	QR_CS	I	Quasi-resonant Over current detected pin	○	○
18	QR_FB	I	Quasi-resonant Feedback detected pin	○	○
19	QR_ZT	I	Quasi-resonant Zero cross detected pin	-	○
20	LATCH/AUTOR	I	Protection mode switched input pin	○	○
21	VREF	O	Internal power supply pin	○	○
22	-	-	-	-	-
23	-	-	-	-	-
24	VH_IN	I	AC Input voltage applied pin	-	○

●I/O Equivalent Circuit Diagram

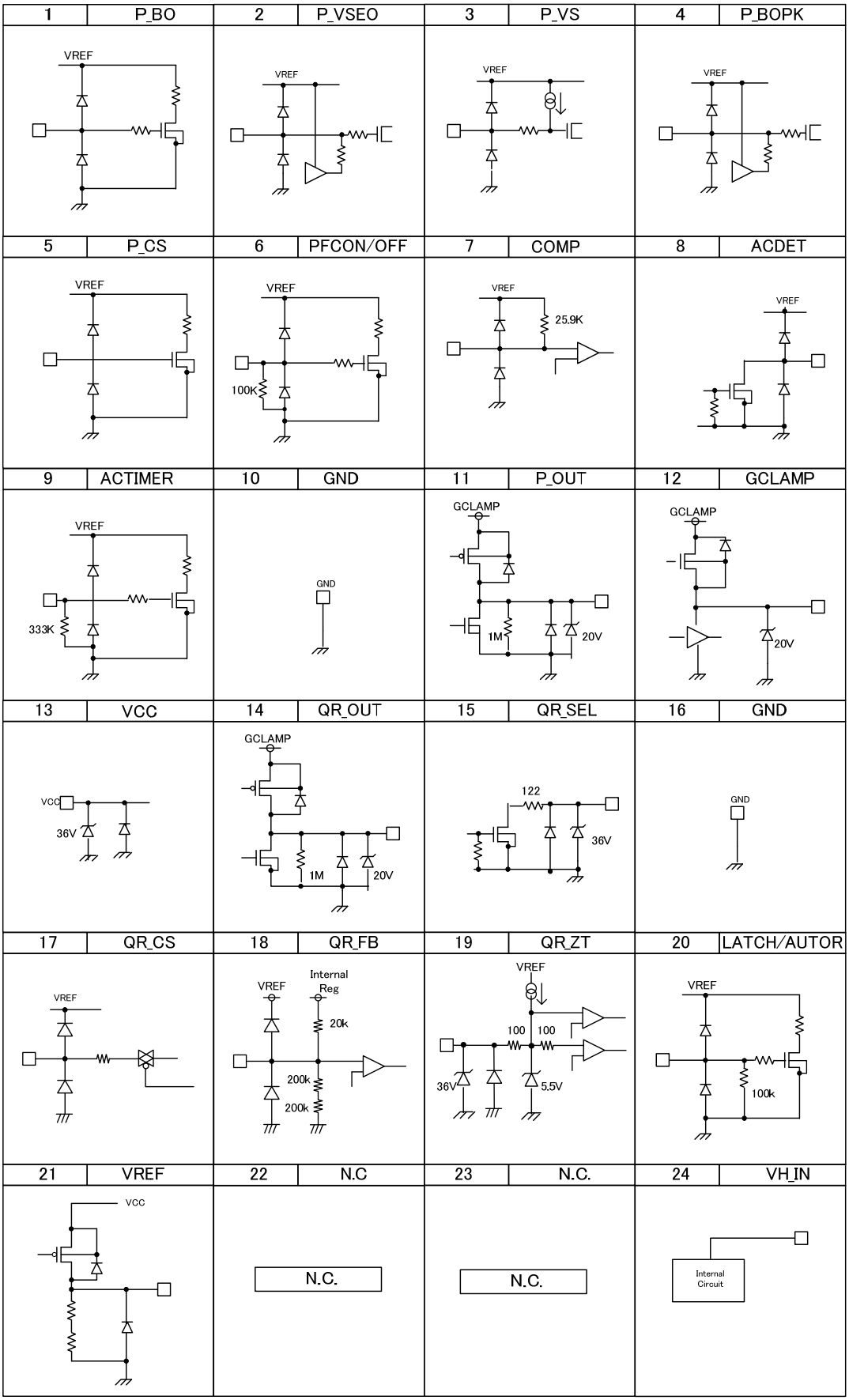


Figure 2. I/O Equivalent Circuit Diagram

●Block Diagram

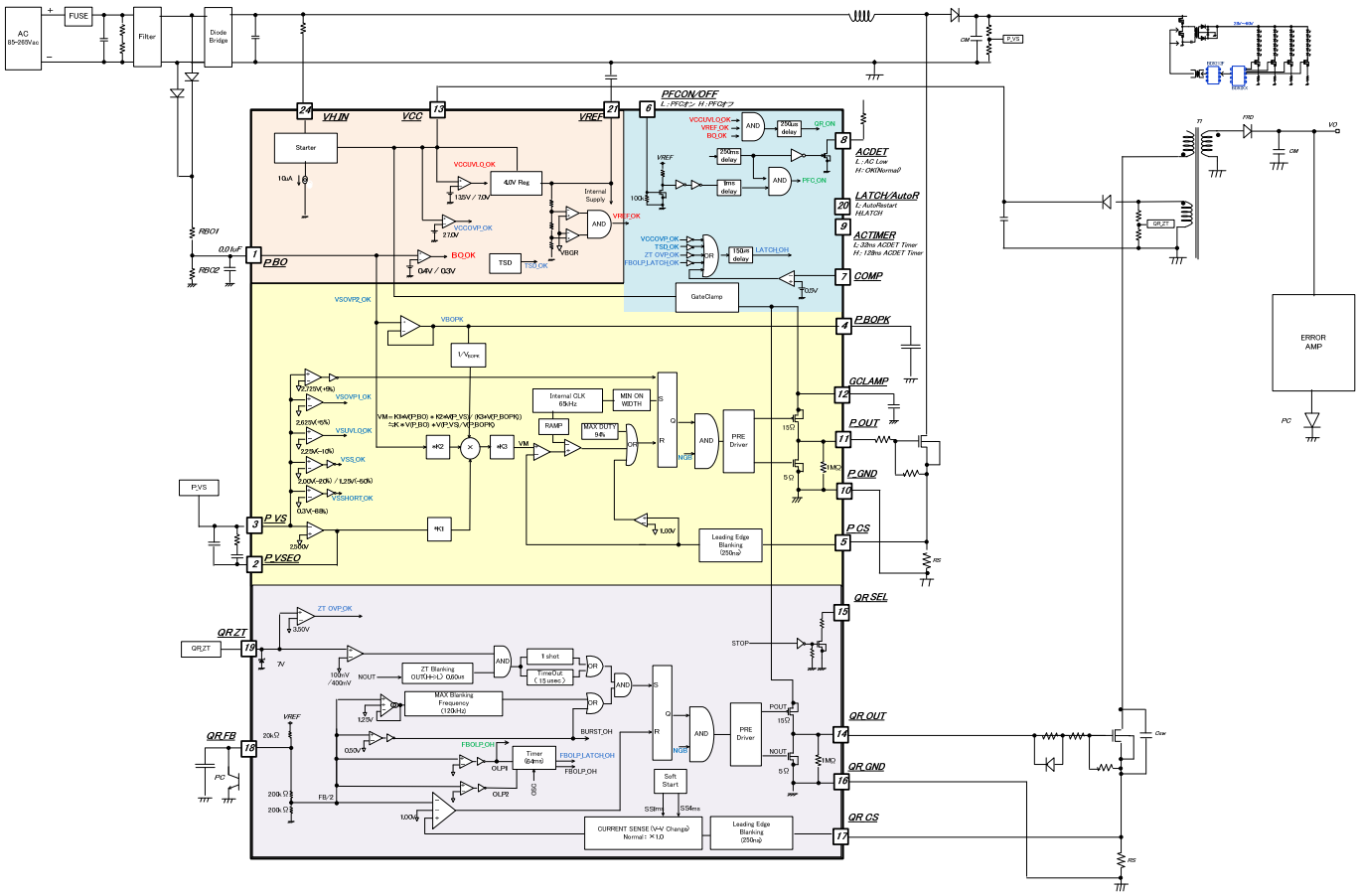


Figure 3. Block Diagram

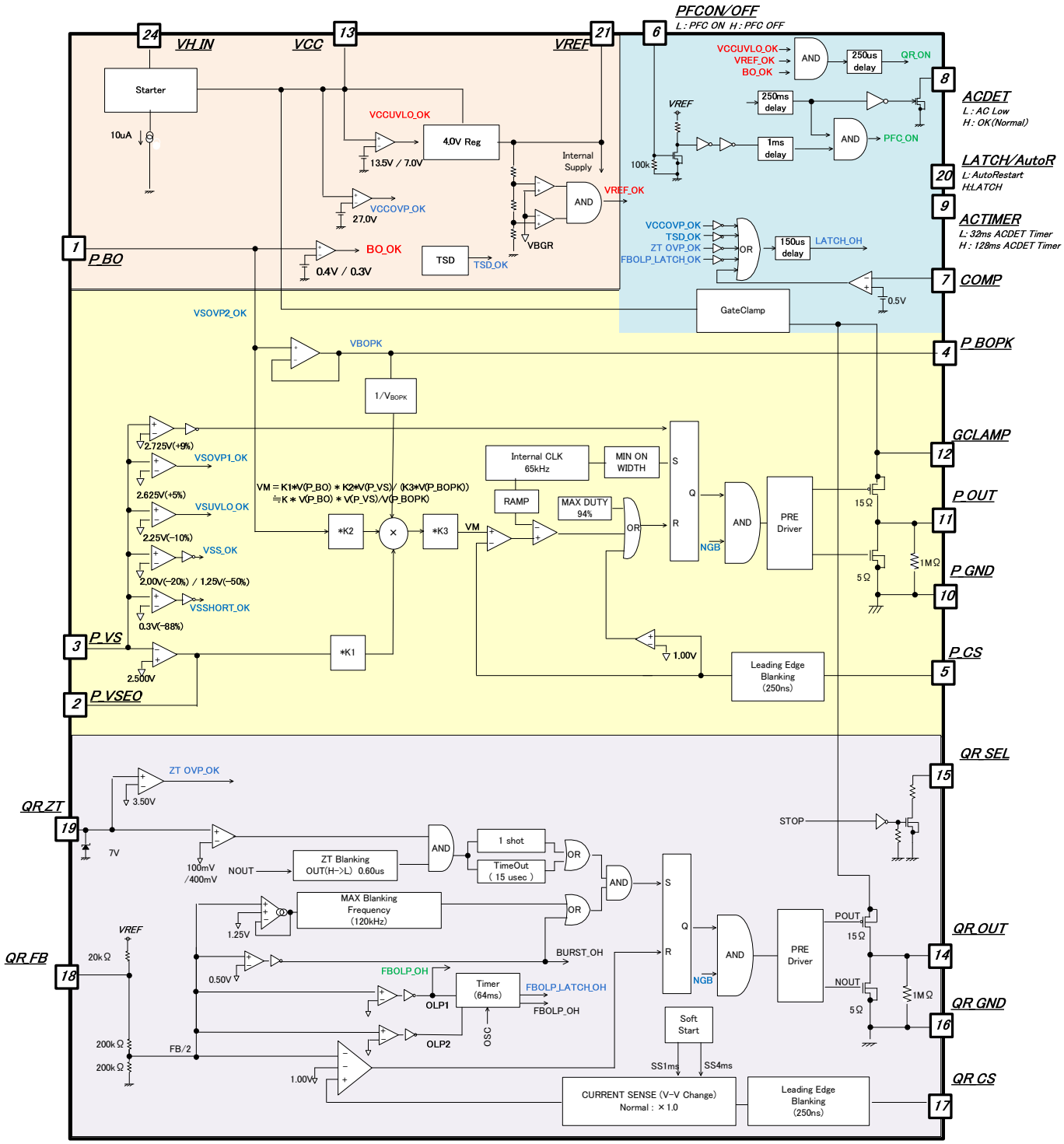


Figure 3-2. Block Diagram

●Explanation of each block

(1) Starter block (24pin)

BM1051F built in the starter circuit that withstands 650V. For that, application used the IC is enabled faster start time and low standby power. After start-up, consumption power is idling current I_{START3} (typ=10uA) only.
Reference of start-up time is shown in Figure 4.
It can start-up less than 0.1sec when C_{VCC}=10uF.

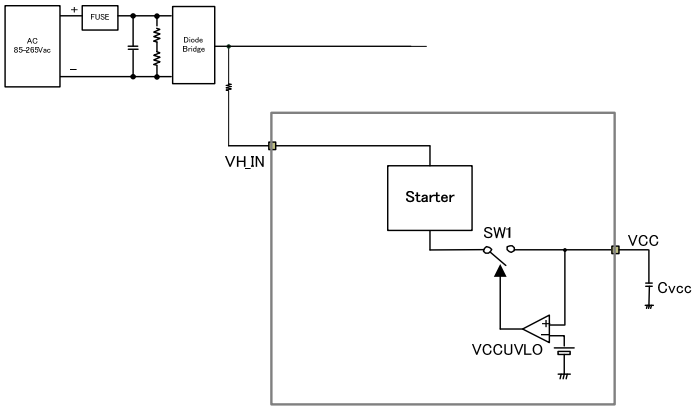


Figure 4. Start Circuit Block Diagram

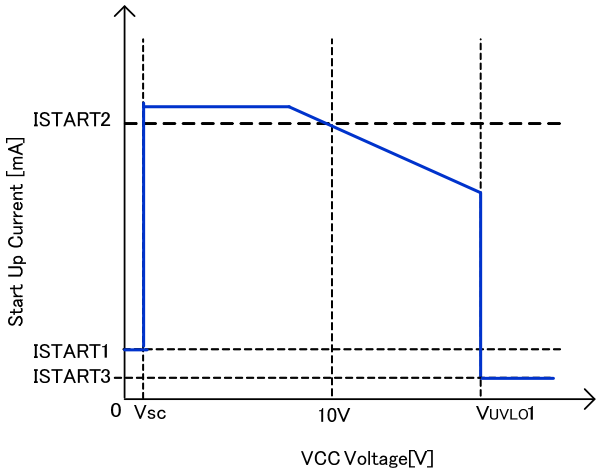


Figure 5. Start-up current vs VCC voltage

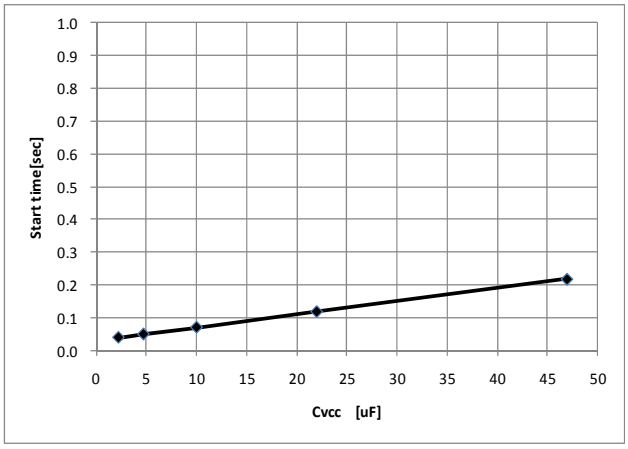


Figure 6. Start time vs C_{VCC} (Reference values)

*Start current flows from VH_IN pin to VCC pin.

ex) When V_{ac}=100V; consumption power of start-up circuit only.
PVH＝100V*√2*10uA=1.41mW

ex) When V_{ac}=240V; consumption power of start-up circuit only.
PVH＝240V*√2*10uA=3.38mW

(2) Start sequence

The start sequence of IC operates DC/DC part, next PFC part (See the figure 7).

A : Input voltage VH is applied.

B : Charge current flows from VH_IN pin to the VCC pin capacitor. Then VCC pin voltage rises.

C : Monitor the AC voltage by P_BO pin. And confirm normal state by releasing brown out.

D :When V_{UVLO1} (typ=13.5V) < VCC pin, release the inside UVLO and ON the inside regulator VREF.

E : When V_{RUVLO1} (typ=87.5%) < VREF pin, release the inside VREFUVLO.

F : If the 'E' state continues constant period, DC/DC part starts because it recognizes normal state.
When the switching starts, VOUT voltage rises.
When the DC/DC start-up, please set external parts to be regulated output voltage within the T_{FOLP} period (64ms .typ).

[QR start-up operation]

G: This IC adjusts over current limiter of DC/DC by operation of soft start 1 against over voltage and current rising.
That term continues T_{ss1} (typ=1ms).

H: This IC adjusts over current limiter of DC/DC by operation of soft start 2 against over voltage and current rising.
Soft start 2 operation continues power limiter operation until P_VS pin voltage > V_{PFCON} (2.00V typ) and T_{SS2} (typ=4ms) .
This IC operates the state that maximum power of QR is 50% at this state.

I: If secondary voltage is setting value, QR_FB pin voltage is constant value corresponded load by current from photo coupler.
At normal state, QR_FB voltage is QR_FB<$V_{FBOLP1B}$ (2.60V typ).

[PFC start up operation]

J: At the point in I time, This IC recognizes that the part of DC/DC operation is normal, Part of PFC starts operation.

K: If P_VS pin voltage is upper V_{P_SHORT} (typ = 0.3V), this IC judges short detection normal.

L: P_VSEO voltage rises from 0V to prevent from over rising voltage and current at PFC part.
At this time P_OUT pin DUTY increase from 0% with P_VSEO voltage increasing.

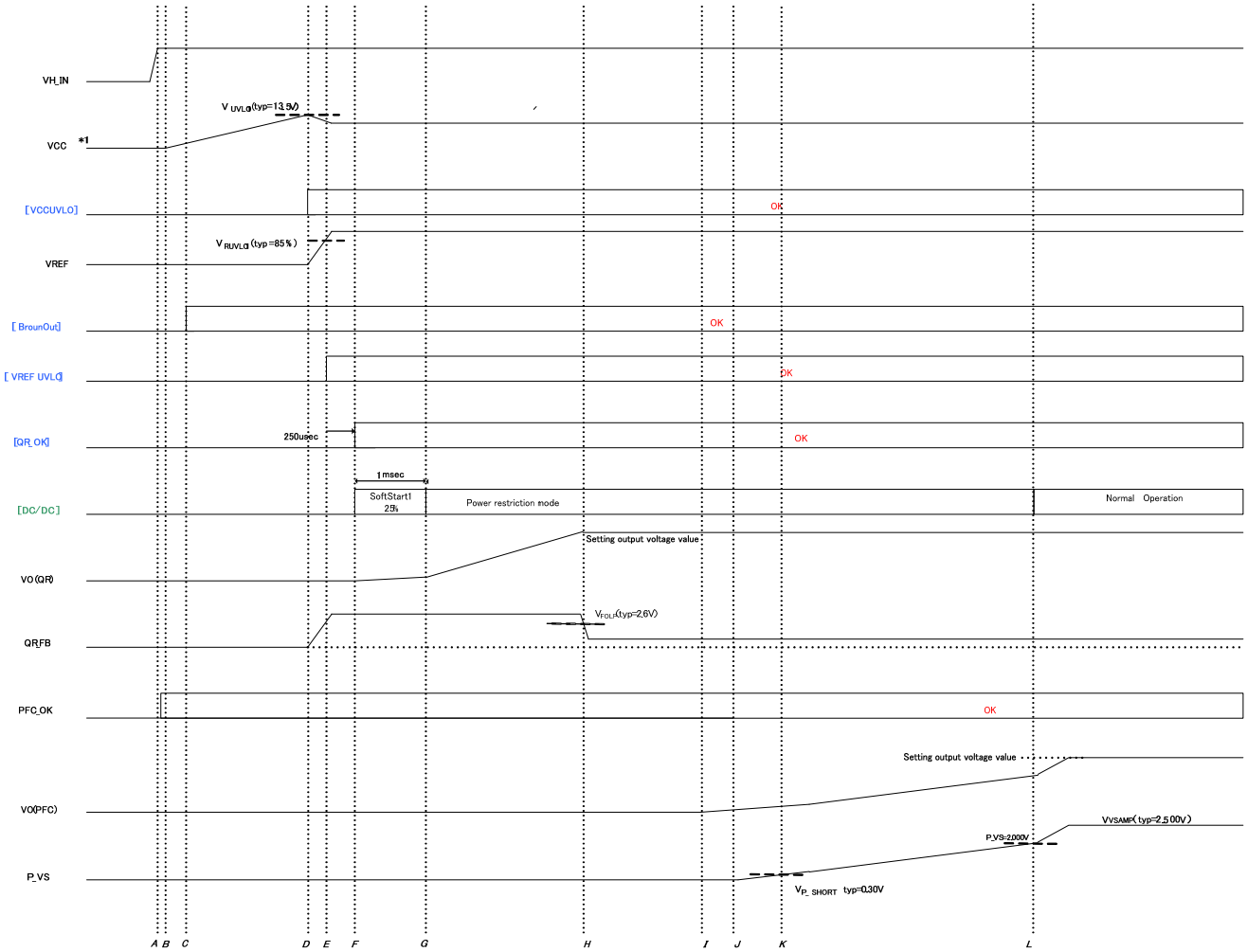


Figure 7. Start sequences Timing chart

About figure7, condition is PFCON/OFF=L.
Start up operation is shown at figure8, 9 by the state shift figure.
Figure 8 is LATCH/AUTOR=L (auto return operation), and figure 9 is LATCH/AUTOR=H (LATCH operation)

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

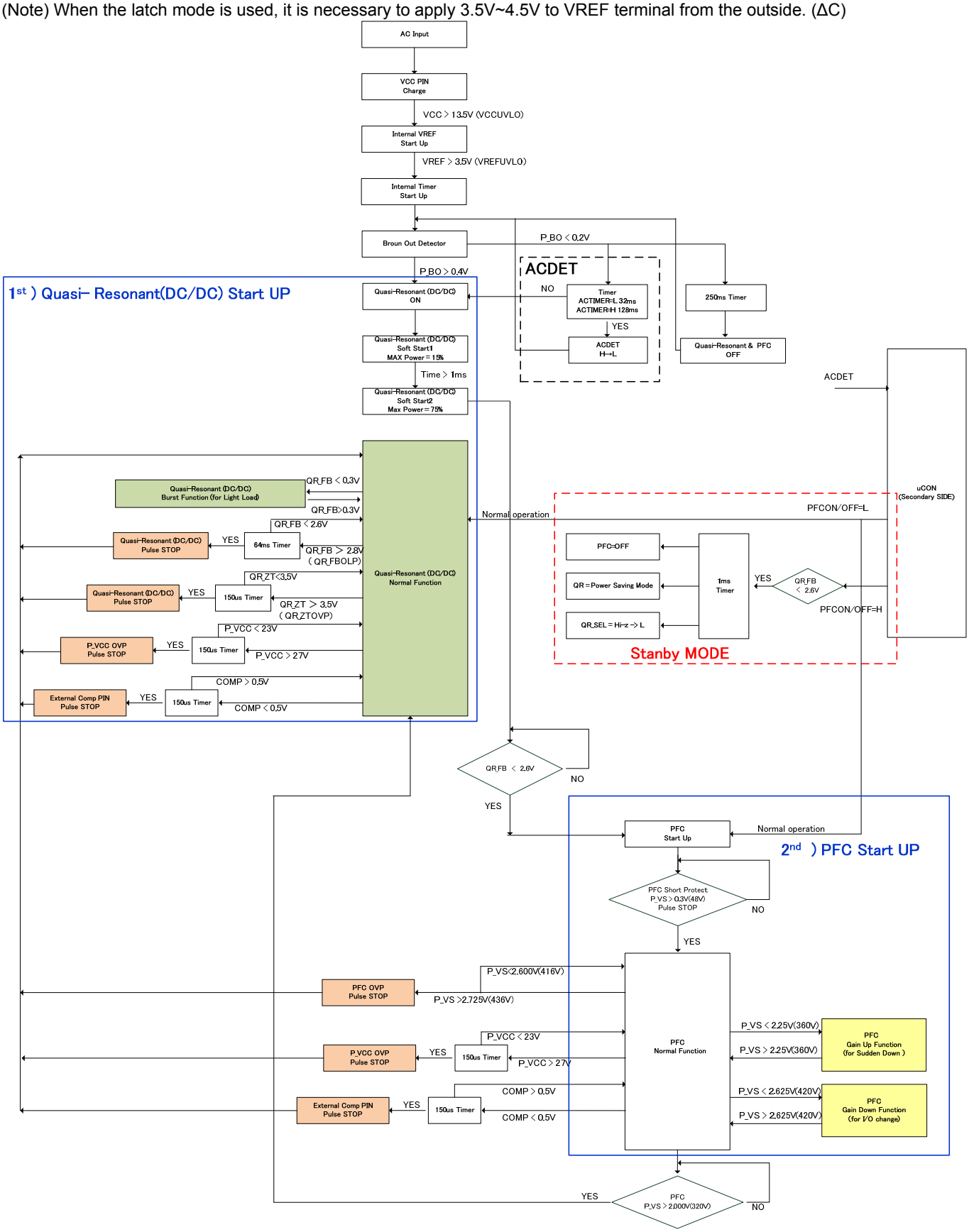


Figure 8. Diagram of state machine (LATCH/AUTOR=L)

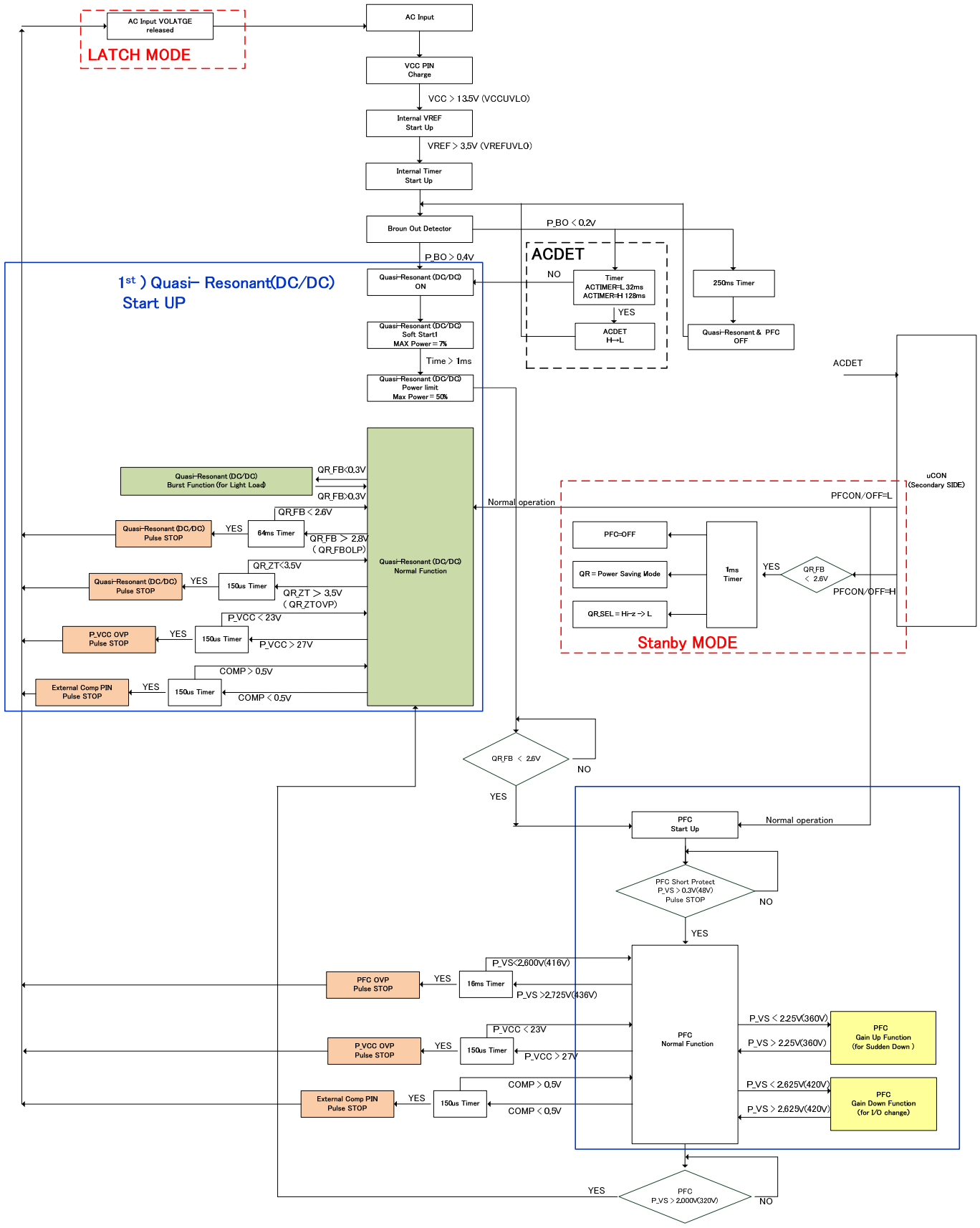


Figure 9. Diagram of state machine (LATCH/AUTOR=H)

(3) VCC protection function and VREF pin function

(3-1) VCC pin protection function(13pin)

BM1051F built in VCC low voltage protection function of VCCUVLO (Under Voltage Lock Out) and over voltage protection function of VCC OVP (Over Voltage Protection).

This function monitors VCC pin and prevent VCC pin from destroying switching MOSFET at abnormal voltage.

VCCUVLO is auto recovery comparator that has voltage hysteresis. VCCOVP operates as latch mode comparator in the LATCH/AUTOR=H and as auto return comparator in the LATCH/AUTOR=L.

VCC<$V_{LATCHOFF}$ (typ = V_{uvlo1} - 0.5) is condition of latch release (reset) after detection of latch operation by VCCOVP.

Refer to the operation figure10.

VCCOVP built in mask time T_{COMP} (typ=150us), in case of continuing VCCOVP 150us, operates over voltage detection.

By this function, this IC masks pin generated surge etc.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

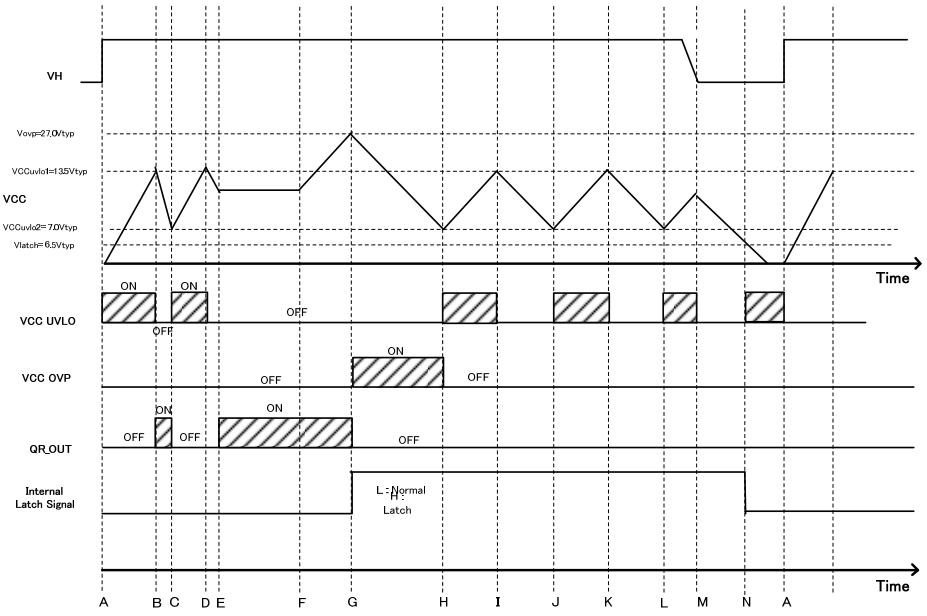


Figure10. VCC UVLO / OVP (LATCH/AUTOR=H at Latch stop)

A:VH input, VCC voltage rise

B:VCC>V_{uvlo1},DC/DC operation start

C:VCC<V_{uvlo2},DC/DC operation stop

D:VCC>V_{uvlo1},DC/DC operation start

E:VCC voltage decreases until starting DC/DC switching

F:VCC rise

F:When VCC>Vovp1,DC/DC operation is stopped. Switching is stopped by internal latch signal.

G:Then DC/DC operation is stopped, power supply is lost from auxiliary, VCC voltage downs.

H:VCC<Vuvlo2, VCC voltage rises for dropping IC's consumption current.

I:VCC>Vuvlo1, this IC dose not operate DC/DC for latch operation. VCC voltage drops because of dropping of IC's consumption current.

J:same of H

K:same of I

L:same of J

M:VH is open(the state is outlet out).VCC drops.

N:VCC <V_{COMP}, latch releases.

(3-2) VREF pin function(21pin)

VREF pin is internal regulator output pin.
The use of VREF pin is IC's internal supply and connection of LATCH/AUTOR pin changing.
This pin needs an external capacitance, please use the capacitance following table.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

Table 2. VREF pin output capacitor capacitance

Parameter	Symbol	Specification			Unit	Conditions
		Minimum	Standard	Maximum		
VREF Output Capacitor	C_{REF}	0.68	1.00	2.20	uF	

(3-3) VREF pin protection function(21pin)

VREF pin built in low voltage protection function VREF UVLO (Under Voltage Protection).
This IC prevents from error operating at the time, VREF starts up and VREF is low, by this function.

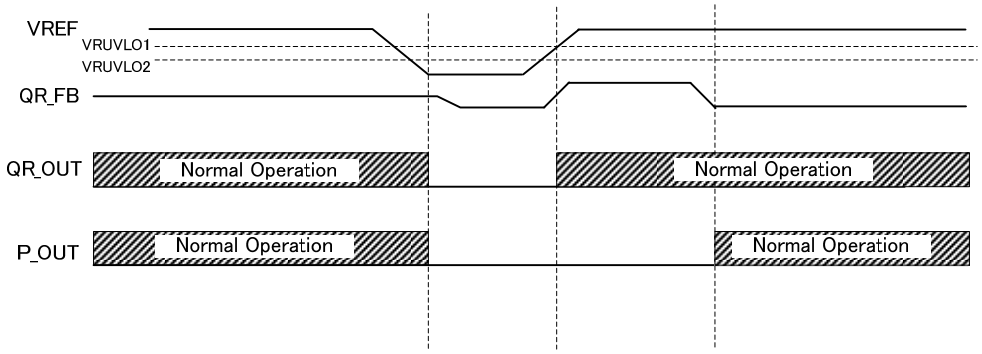


Figure11. VREF UVLO Function

(3-4) Blown out function(1 pin)

BM1051F built in blown out function. This function is that this IC stops DCDC operating at the time when input AC voltage is low. Show the example figure12. This IC divides input voltage by the resistance, and input P_BO pin.

This IC detects from circuit normal state, and starts DC/DC operation the time when P_BO pin exceeds V_{bo1}(0.4V typ).

ACDET=L after T_{BO1}(typ.32ms) or T_{bo2}(typ.128ms) from P_BO pin drops from V_{BO2}(0.2V typ).

Moreover, if T_{BO3} (typ.250ms) passes from P_BO<V_{BO2}, DC/DC part and PFC part is stopped.

About every resistance of fugure12, because P_BO pin is used PFC operation, please set R_{bo1}=4Mohm,R_{bo2}=16kohm for operating the range of P_BO pin voltage 0~1.8V. In this case, by the following formula, P_BO=0V~0.56V at the case AC100V, P_BO=0V~1.237V at the case AC220V.

$$P\_BO = (\sqrt{2} \times V_{AC} \quad V_{F1}) \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}$$

Then

$$\sqrt{2} \times V_{AC} >> V_{F1}$$

$$P\_BO = \sqrt{2} \times V_{AC} \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}$$

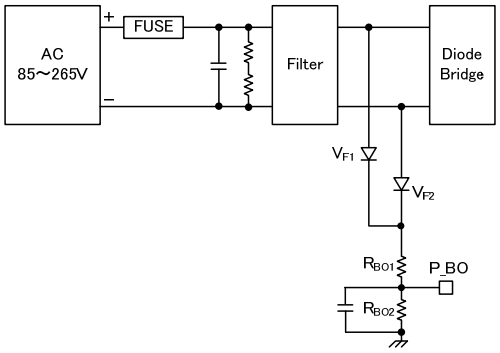


Figure12. Block Diagram of Blown out Function

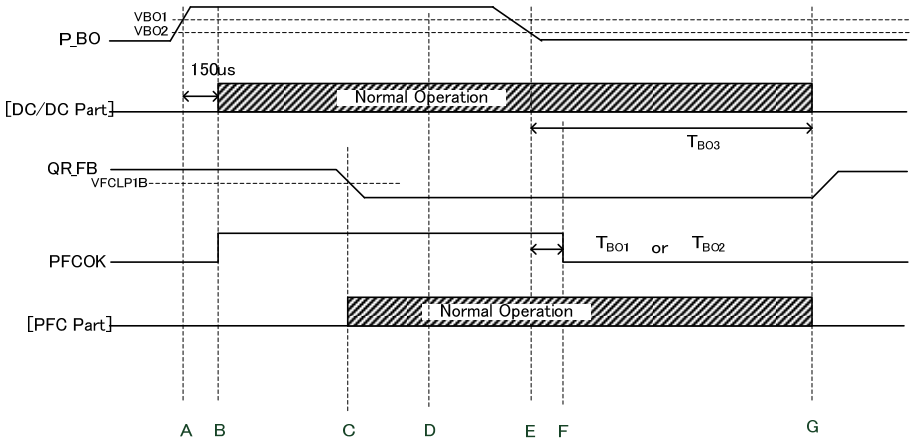


Figure13. Detection Way of Blown out Function

A : P_BO > V_{BO1}(typ.0.4V) 、ACDET=L->H

B: After 150us from A DC/DC part starts up.

C:QR_FB<V_{FCLP1B}(typ.2.6V). PFC part starts up.

D: If PFC output is larger than constant voltage, ACTIMER=L->H.

E: P_BO<V_{BO2}(typ.0.2V) Timer start operation by detection blown out protection.

F:After T_{BO1}(typ.32ms) or T_{BO2}(typ.128ms) from E, ACDET=H->L. It is possible to set T_{BO1} and T_{BO2} at ACTIMER pin

G:After T_{BO2}(typ.250ms) from E, DC/DC part and PFC part are OFF

(4)Controller part

(4-1)ACDET pin (8pin)

ACDET pin is NMOS open drain output. It monitors AC voltage, and is used for controlling secondary micon.
Show the using example figure14, 15. Please set VIN is H voltage of micon.

ACDET=L ： Abnormal state（P_BO < 0.2V）

ACDET=H ： Normal state

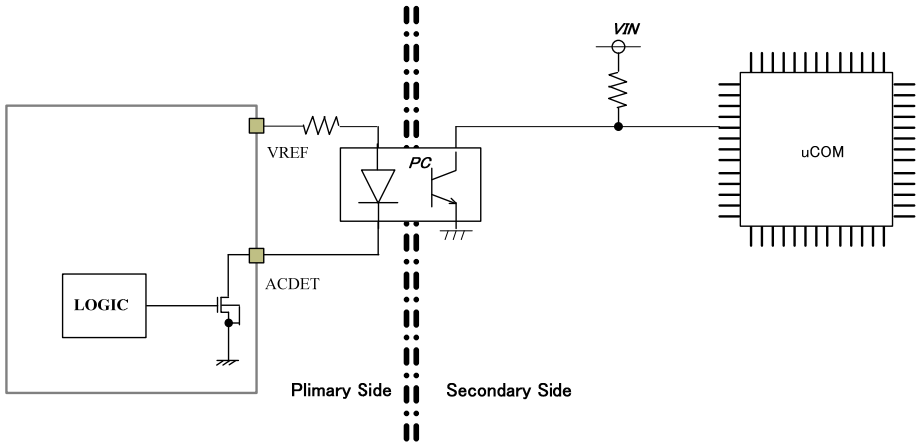


Figure14. Using Example of ACDET Pin

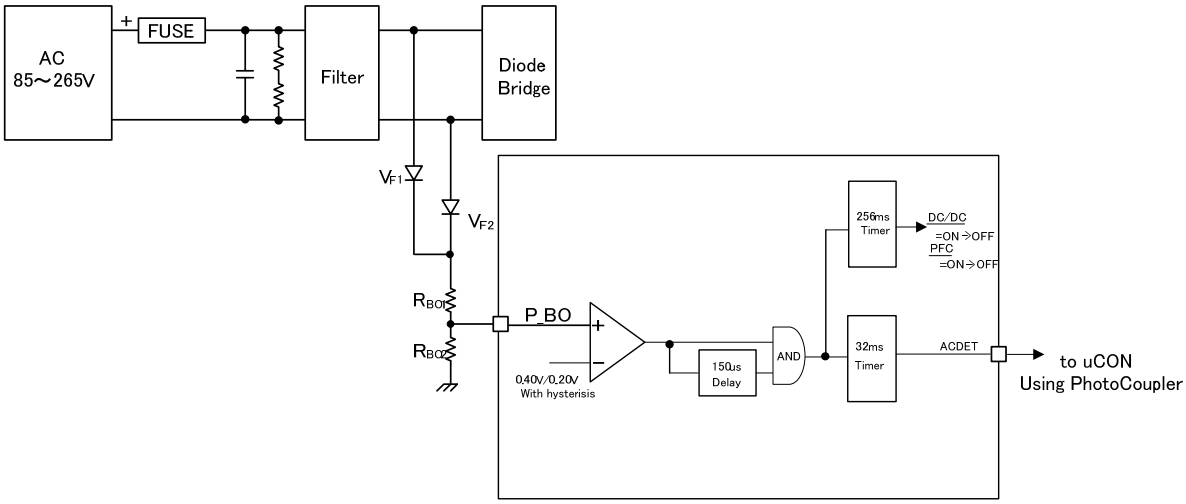


Figure15. Explanation of ACDET Pin

Next, show an easy sequence.

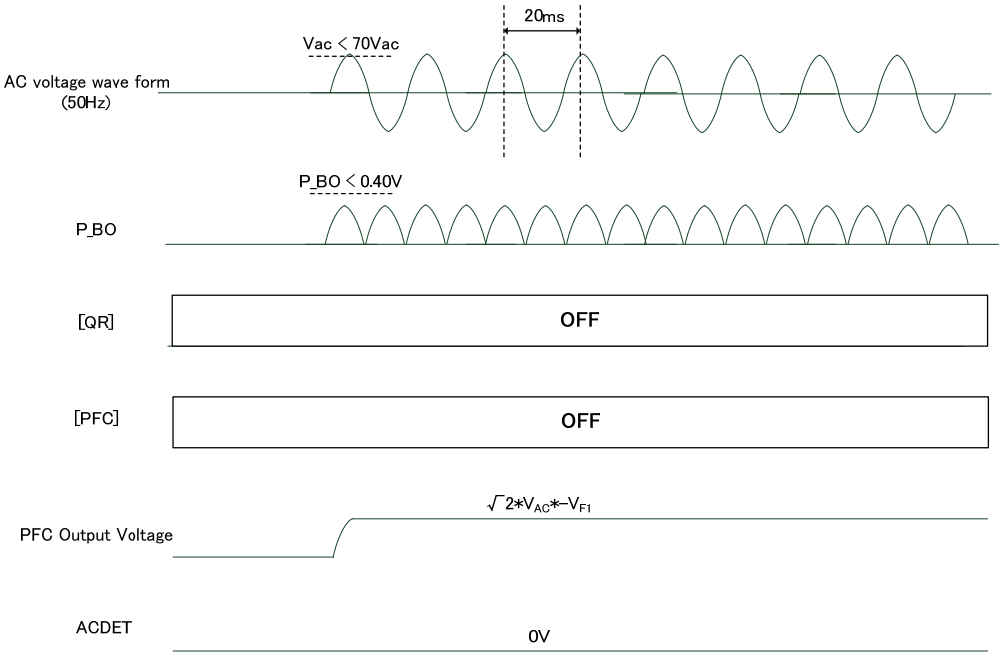


Figure16. At applied AC Input Voltage（P_BO voltage<0.4V）

Because P_BO < 0.4V, DC/DC part is OFF.
VCC voltage>13.5V

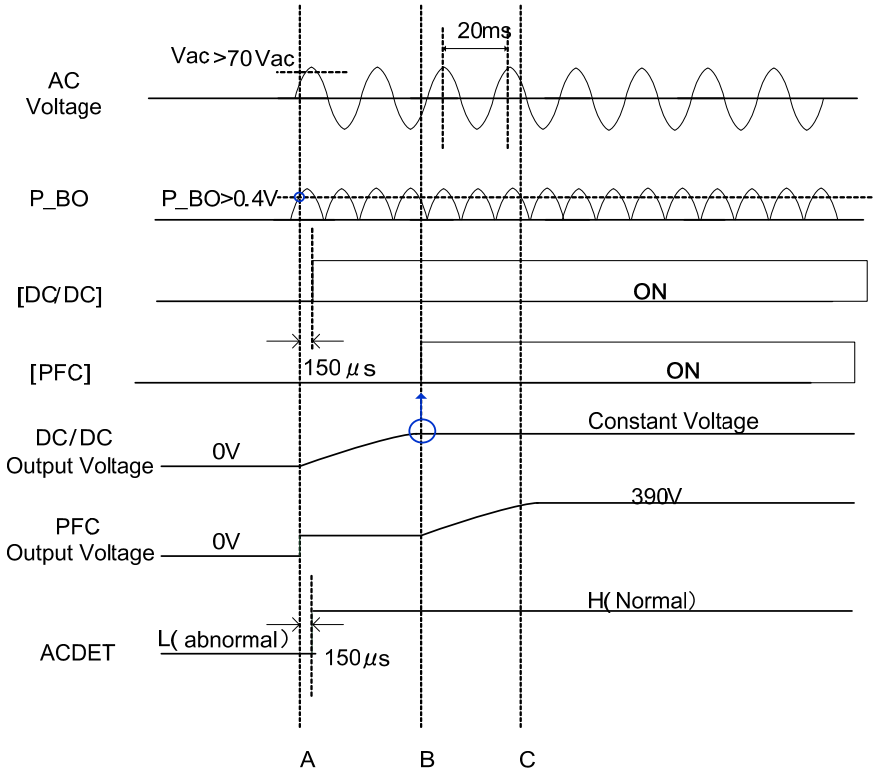


Figure17. At applied AC Input Voltage（P_BO voltage >0.4V）

A：Detect P_BO＞0.4V, Quasi resonance starts operation After 150μs
B：PFC start up
C：PFC output stabilized
*About PFC operation, by the micon, is able to be controlled using PFCON/OFF pin.

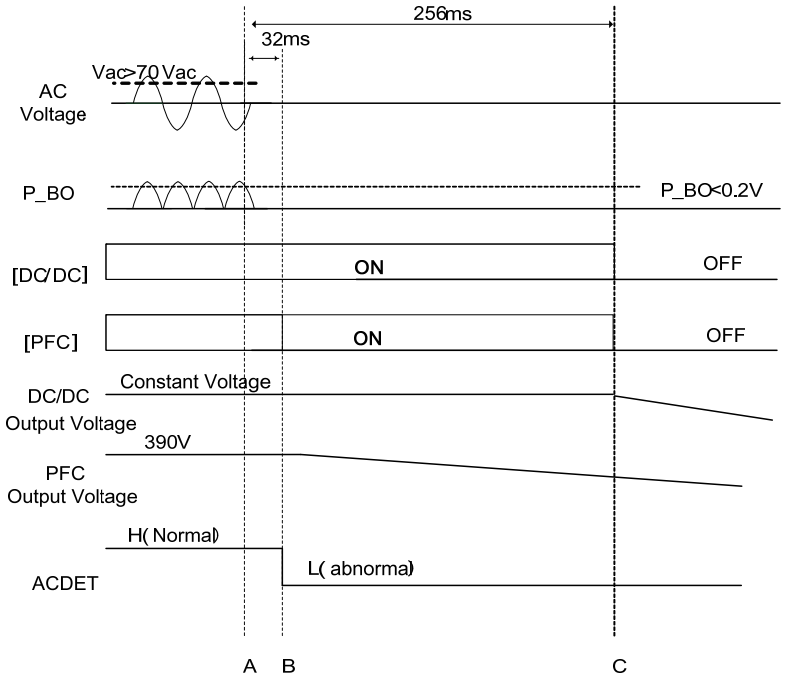


Figure18. At AC Power Supply OFF

A：Detect P_BO＜0.2V, internal ACDET timer operates. At this time, output of PWC downs.
B：After 32ms（ACTIMER=L）from the point A, ACDET pin voltage is H->L, send to the μ-controller abnormal signals.
C：After 250ms from the point of A,PFC and Quasi Resonant are stopped

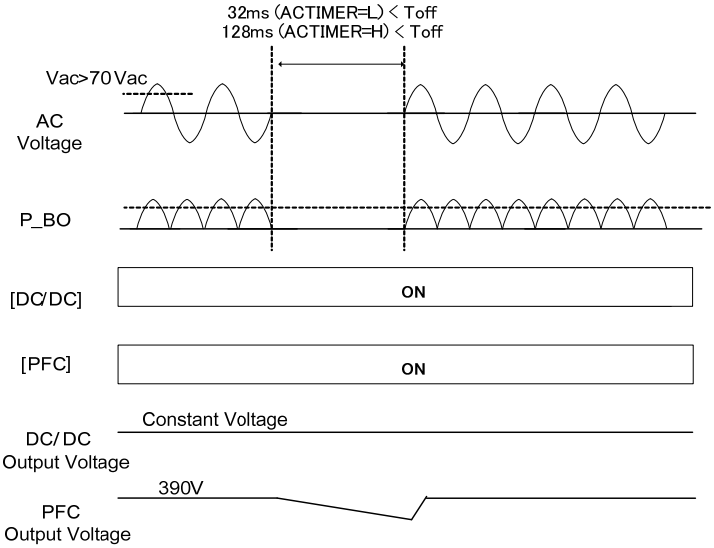


Figure19. At AC Power Supply the case of operation moment stop

The case of AC voltage is OFF suddenly, constant area is masked.
The time of constant area of masking is depends on ACTIMER pin.
The case of ACTIMER pin=L, Mask time=32ms、 the case of ACTIMER pin=H, mask time=128ms.
The moment of AC voltage momentary power interruption, because PFC output voltage is down by corresponding to load, please watch out.

(4-3) PFCON/OFF pin

PFCON/OFF pin is NMOS gate input pin. Refer to following the functions.

An internal timer is integrated for noise protection on PFCON/OFF pin.

After $T_{PFCON/OFF}$(typ.1ms) from PFCON/OFF H→L, PFCON/OFF L operation starts. At PFCON/OFF L→H, internal timer is not integrated.

function1）PFC circuit operation is OFF control.

In order to reduce standby power, IC controls PFC part operation at PFCON/OFF pin.

function2）QR_SEL pin is Hi-z→L

Refer to example of using at figure 20.

PFCON/OFF=L ： DC/DC part＝ON、 PFC part＝ON、QR_SEL＝Hi-Z

PFCON/OFF=H ： DC/DC part＝ON、 PFC part＝OFF、QR_SEL=L

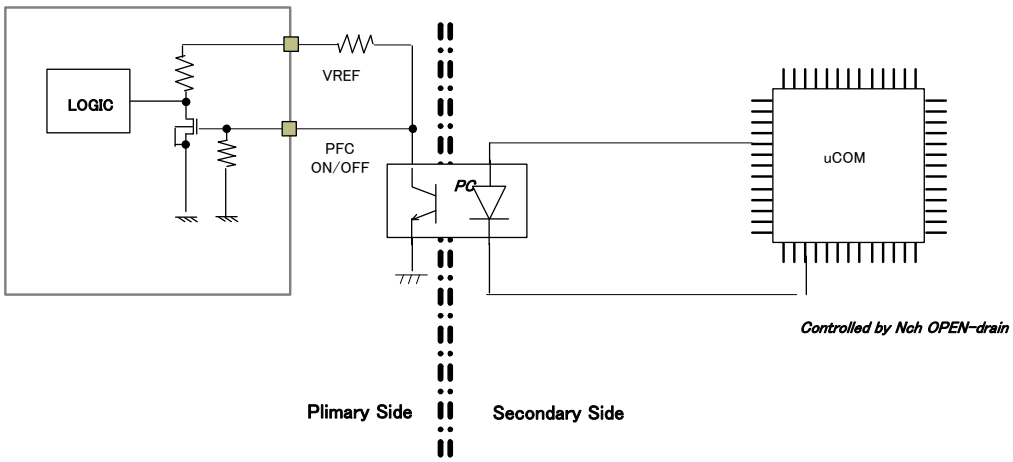


Figure20. Using example of PFCON/OFF pin

(4-4) LATCH/AUTOR pin

LATCH/AUTOR pin is NMOS gate input pin. Refer to example of using at figure21.
Operation setting of protection function is shown at table3.

LATCH/AUTOR=L : Auto recovery
LATCH/AUTOR=H : Latch

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

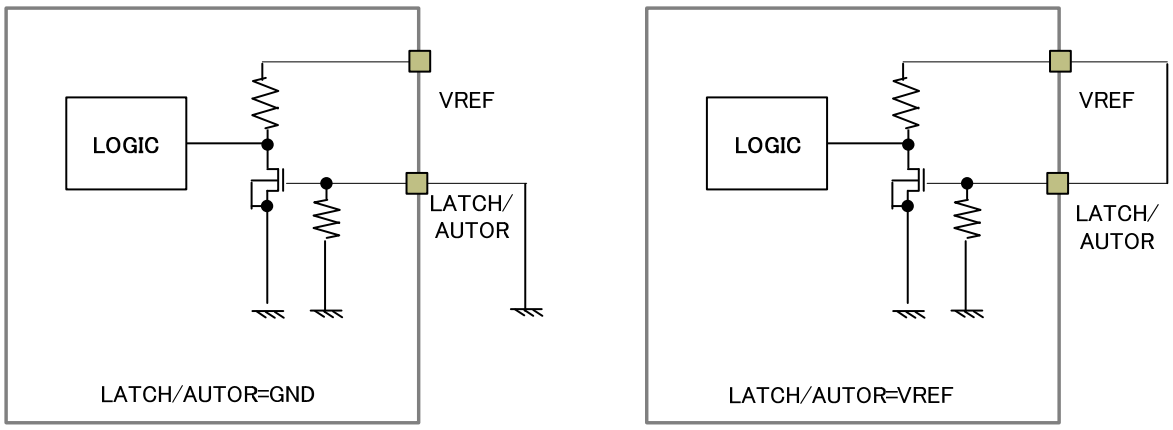


Figure21. Using example of LATCH/AUTOR pin

ITEM	Contents	LATCH/AUTOR=GND				LATCH/AUTOR			
		detection method	operation at detection	release mothod	operaetion at detection	detection method	operation at detection	release mothod	operaetion at detection
VREFUVLO	VREF PIN Low voltage protection function	VREF<2.5V (VREF falling)	PFC part, DC/DC part operation stops	VREF>3.5V (VREFrising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
VCCUVLO	VCC PIN Low voltage protection function	VCC<7.0V (VCC falling)	PFC part, DC/DC part operation stops	VCC>13.5V (VCC rising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
VCCOVP	VCC PIN Over voltage protection function	VCC>27V state continues between 150us(VCC rising)	PFC part, DC/DC part operation stops	VCC<23.0V (VCCfalling)	PFC partDC/DC part enable to operate	VCC>27V (VCC rising)	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	PFC part, DC/DCpart enable to operate
blown out	Input AC voltage Low voltage protection function	P_BO＜0.2V state continues between 250ms	PFC part, DC/DC part operation stops	P_BO>0.4V (P_BOrising)	PFC partDC/DC part enable to operate	same as LATCH/AUTOR=GND			
QR_FB_OLP1	QR_FB pin Over current protection function	QR_FB>2.8V state continues between 250ms(QR_FB	DC/DC part operation stops	QR_FB<2.6V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_FB_OLP2	QR_FB pin Over current protection function	QR_FB>3.6V (QR_FB rising)	DC/DC part operation stops	QR_FB<3.4V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_ZT OVP	QR_ZT pin Over voltage protection function	QR_ZT>3.5V state continues between 150us(QR_ZT	DC/DC part operation stops	QR_ZT<3.5V (QR_ZT falling)	normal operation	QR_ZT>3.5V state continues between 150us(QR_ZT	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	normal operation
P_VS short protection	P_VS pin Short protection function	P_VS<0.30V (P_VS falling)	PFC part operation stops	P_VS>0.30V (P_VS rising)	normal operation	same as LATCH/AUTOR=GND			
P_VS GAIN increasing	P_VS pin Low voltage gain increasing function	P_VS<2.25V (P_VS falling)	GM AMP GAIN increasing	P_VS>2.25V (P_VS rising)	normal operation	same as LATCH/AUTOR=GND			
P_VS OVP1	P_VS pin Over voltage protection function1	P_VS>2.625V (P_VS rising)	GM AMP GAIN falling	P_VS<2.625V (P_VS falling)	normal operation	same as LATCH/AUTOR=GND			
P_VS OVP2	P_VS pin Over voltage protection function2	P_VS>2.725V (P_VS rising)	PFC part stops	P_VS<2.600V (P_VS falling)	normal operation	P_VS>2.725V (P_VS rising)	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC下降時)	normal operation
COMP function	COMP pin Protection function	COMP<0.5V state continues between 150us(COMP	PFC part, DC/DC part operation stops	COMP>0.50V (COMP rising)	normal operation	COMP<0.5V state continues between 150us(COMP	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	normal operation

Table 3. List of Protection Function Operation Setting by LATCH/AUTOR pin

*Comparator level of protection function is shown by TYP value.

(4-5) ACTIMER pin

ACTIMER pin is NMOS gate input pin. Show example of using figure 22, 23
Set the detect timer of AC voltage drop.（please refer to ACDET pin page）

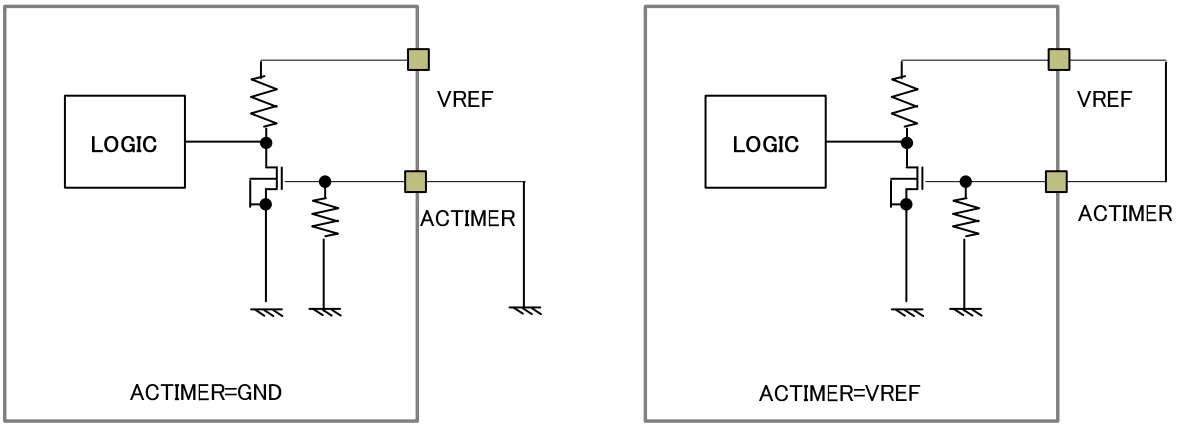


Figure22. Using example of ACTIMER pin

ACTIMER=GND : 32ms Timer
ACTIMER=VREF :128ms Timer

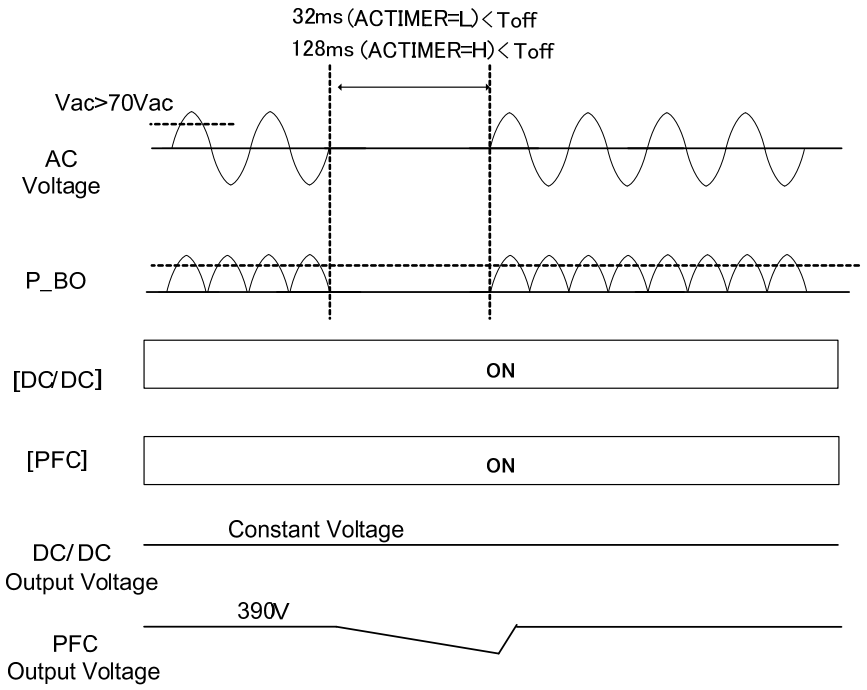


Figure23. AC power at the case momentary power interruption OFF

(4-6) COMP pin（external stop control function）

COMP pin is stop control pin. When COMP pin voltage drops from V_{COMP} (0.5V. typ), COMP pin stops PFC and DC/DC part operation.
This IC built in T_{COMP} (150us .typ) until stopping switching, prevent from stopping by noise.
COMP pin is in pull-up resistor R_{COMP} (25.9kΩ. typ), When COMP pin is the state of pull-down with lower resistance than R_T(3.70kΩ.typ), COMP pin detects abnormal. Show application examples at the figure24, 25, and 26.

Temperature protection by NTC thermister

By putting a thermister at the COMP pin, it is possible to stop latch on temperature rising.
The case of this application, please design thermister resister is R_T(3.70kΩ.typ) on temperature detection.
（Figure24 and 25 is application circuit that latch on Ta=110℃）
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

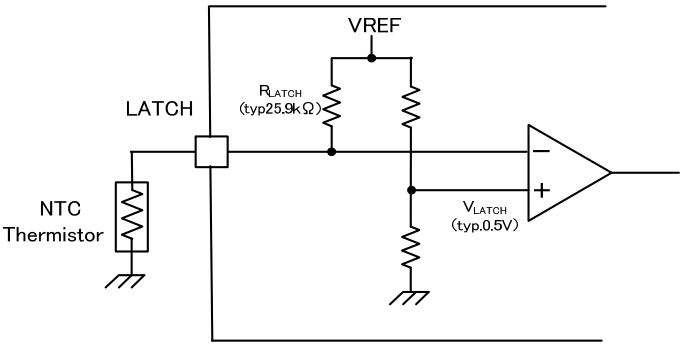


Figure 24. Temperature Protection Application

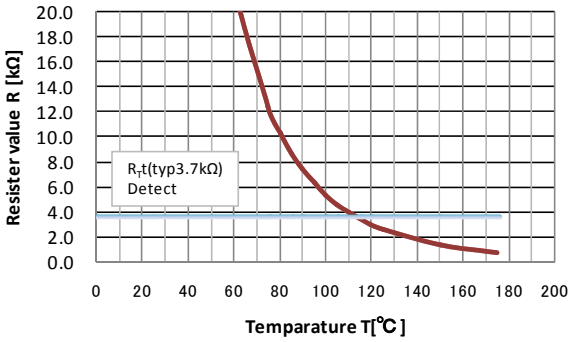


Figure 25. Temperature–Thermistor Resistor characteristic

Secondary over- voltage protection

This IC can detect secondary over-voltage by putting photo coupler to COMP pin.

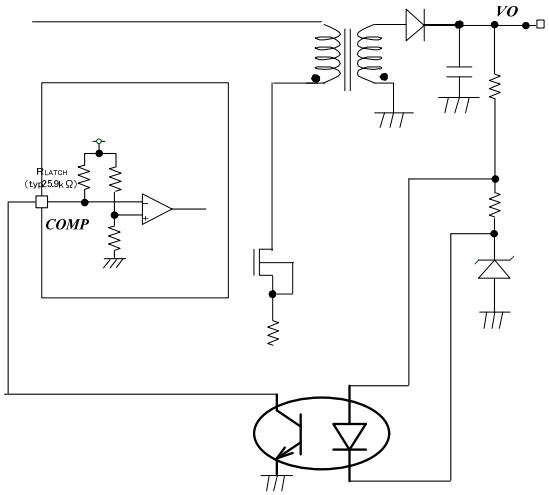


Figure26.Output Over Voltage Protection Application

Table 4. Changes of COMP function Operation by LATCH/AUTOR pin

ITEM	contents	LATCH/AUTOR=GND				LATCH/AUTOR=VREF			
		detection method	operation at detection	release mothod	operaetion at detection	detection method	operation at detection	release mothod	operaetion at detection
COMP function	COMP pin protection function	COMP<0.5V state continues between 150us(COMP falling)	PFC part, DC/DC part operation stops	COMP>0.50V (COMP rising)	normal operation	COMP<0.5V state continues between 150us(COMP falling)	PFC part, DC/DC part latch operation stops	P_VCC<6.5V (P_VCC falling)	normal operation

(5)Quasi-Resonant DC/DC converter function

Part of quasi-resonant DC/DC uses PFM(Pulse Frequency Modulation)mode control.
The QR_FB pin, QR_ZT pin and QR_CS pin are monitored to provide a system optimized for DC/DC."
The switching MOSFET ON width (turn OFF) is controlled via the QR_FB pin and QR_CS pin, and the OFF width(turn ON).
Show following detail explanation. (refer to figure27).

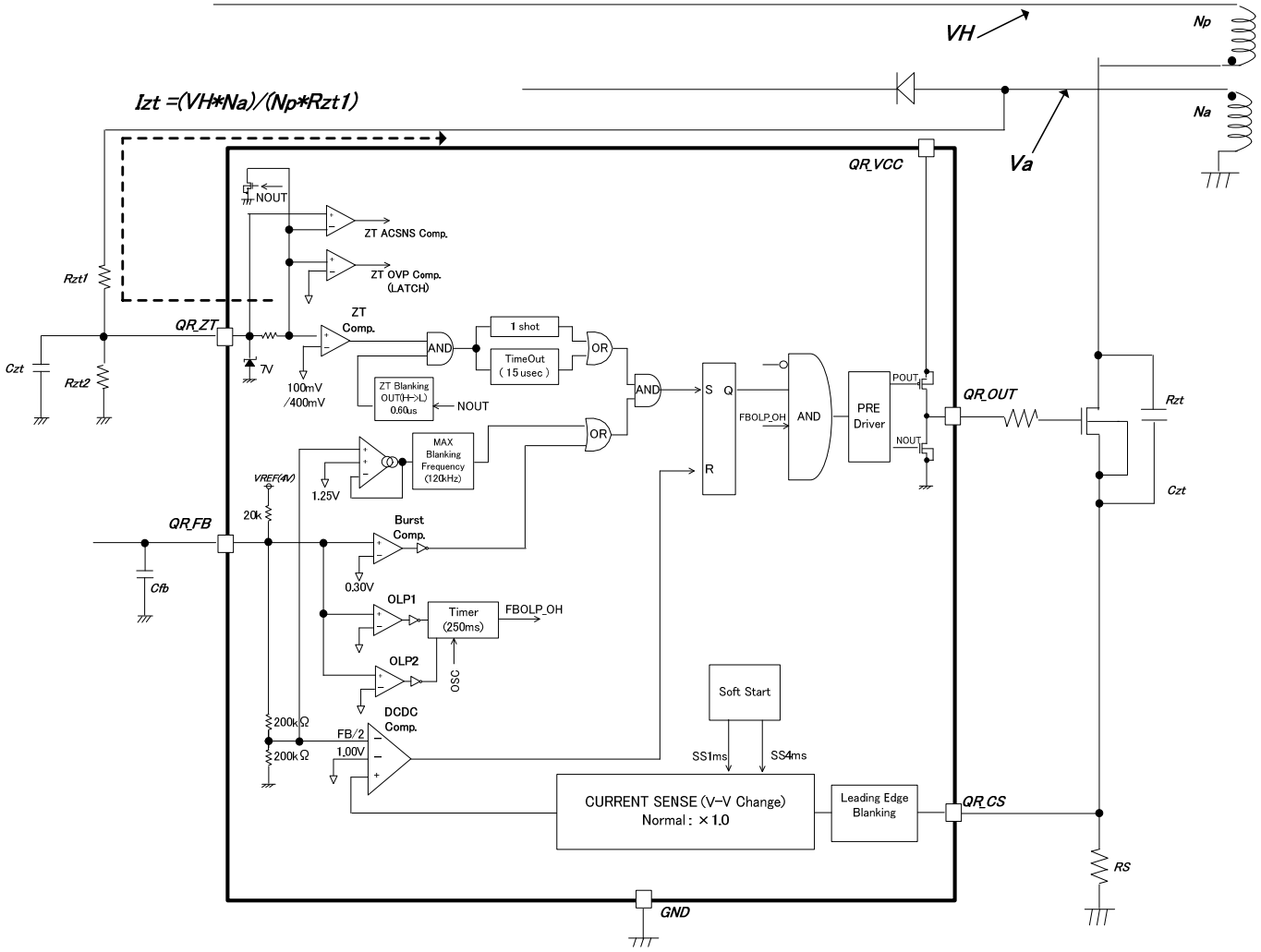


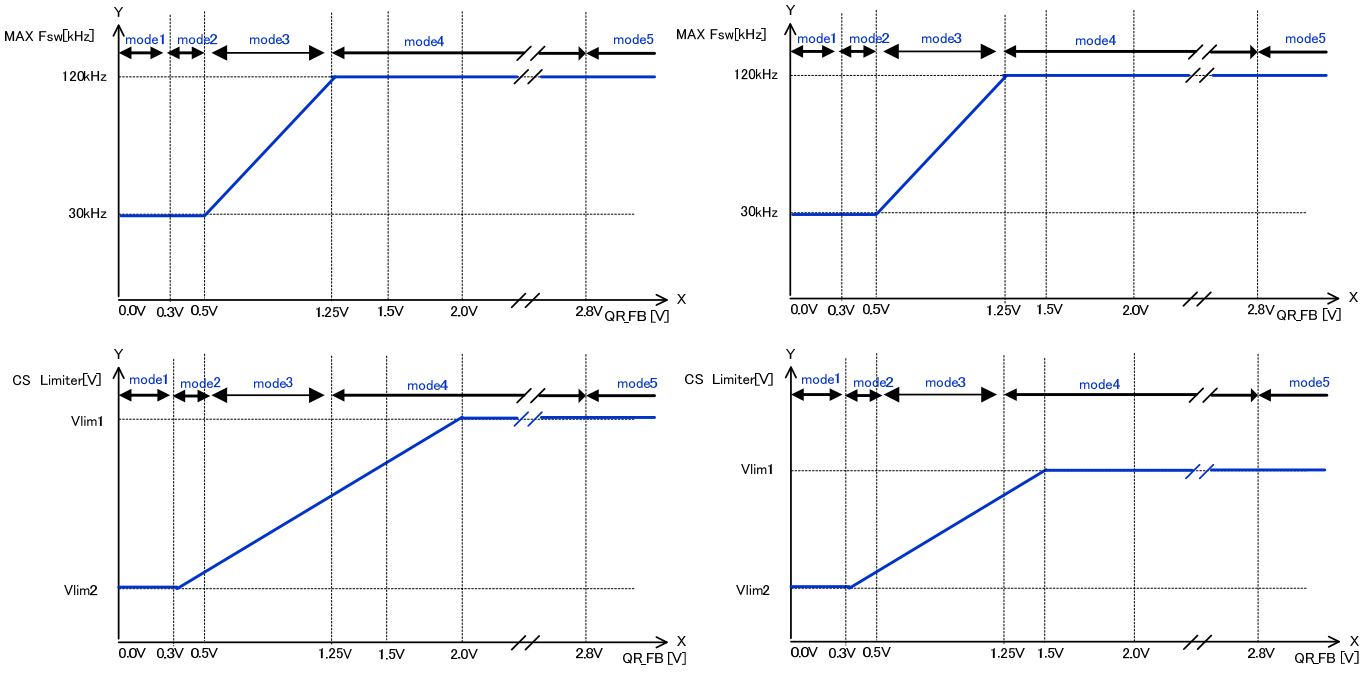
Figure27. Diagram of Quasi-resonant DC/DC Operation

(5-1) Determination of ON width (turn OFF)

ON width is controlled via the QR_FB pin and QR_CS pin.
The QR_FB pin voltage is compared with the IC internal voltage V_{lim1} (1.0V typ) and, as is shown in Figure28.
And the comparator level changes linearly.

The QR_CS pin is also used for the pulse-by-pulse over current limiter circuit.
By changing voltage at the QR_FB pin, DC/DC results in changes of the maximum blanking frequency and over-current limiter level.

・mode1: Burst operation
・mode2: Frequency reduction operation(reduces maximum frequency)
・mode3: Maximum frequency operation(operates at maximum frequency)
・mode4: Overload operation(pulse operation is stopped when overload is detected)



(a) I_{zt}<1.0mA (b) I_{zt}>1.0mA

Figure 28. Relation of QR_FB pin, over current limiter and maximum frequency

The over current limiter level is adjusted, when the input voltage is changed, operate the soft start function.
In this case, the Vlim1 and Vlim2 values are as listed below."

Table 5. current protection voltage of Quasi-resonant DC/DC

Soft start	AC=100V		AC=230V	
	Vlim1	Vlim2	Vlim1	Vlim2
Start～1ms	0.250V (25.0%)	0.039V (3.9%)	0.176V (17.6%)	0.026V (2.6%)
1ms～PFC Start &4ms	0.750V (75.0%)	0.113V (11.3%)	0.525V (52.5%)	0.079V (7.9%)
PFC Start & 4ms～	1.000V (100.0%)	0.150V (15.0%)	0.700V (70.0%)	0.105V (10.5%)

*( ) is AC=100V, these show relative value of compare with V_{lim1}（1.0Vtyp） of normal operation.

This table is separated AC100V and AC230V for the function of QR_CS current changing function that is shown（4-3）.

(5-2)LEB(Leading Edge Blanking)function

When the switching MOSFET is turned ON, surge current occurs at each capacitor charge /discharge or drive current.
For that, QR_CS voltage rise temporarily, over current limiter may be detected errors.
To prevent detection errors blanking time is built in to mask T_{LEB} (typ=250ns).
This blanking function enables a reduction of CS pin filtering.

(5-3) CS over current protection function

When the AC input voltage (VHIN) is high, the ON time is reduced and the operating frequency increases. As a result, the maximum rated power is increased for a constant over current limiter level. As a countermeasure, DC/DC is switched over current detected level.

AC input voltage detection method is that monitoring QR_ZT current.
When MOSFET is turn ON, the auxiliary voltage (V_a) is the minus voltage that depends on input voltage（VH）.
QR_ZT pin is clamped about 0V internal IC.
Following is the formula for that case.
Refer to the block figure29. See the graph figure30 and 31.

$Izt = (Va - Vzt)/Rzt1 \fallingdotseq Va/Rzt1 = VH * Na/Np /Rzt1$

$Rzt1 = Va/Izt$

For that, VH voltage is set by the resistance value of R_{zt1}. Then, QR_ZT bottom detection voltage is decided, Please set timing by C_{zt}.

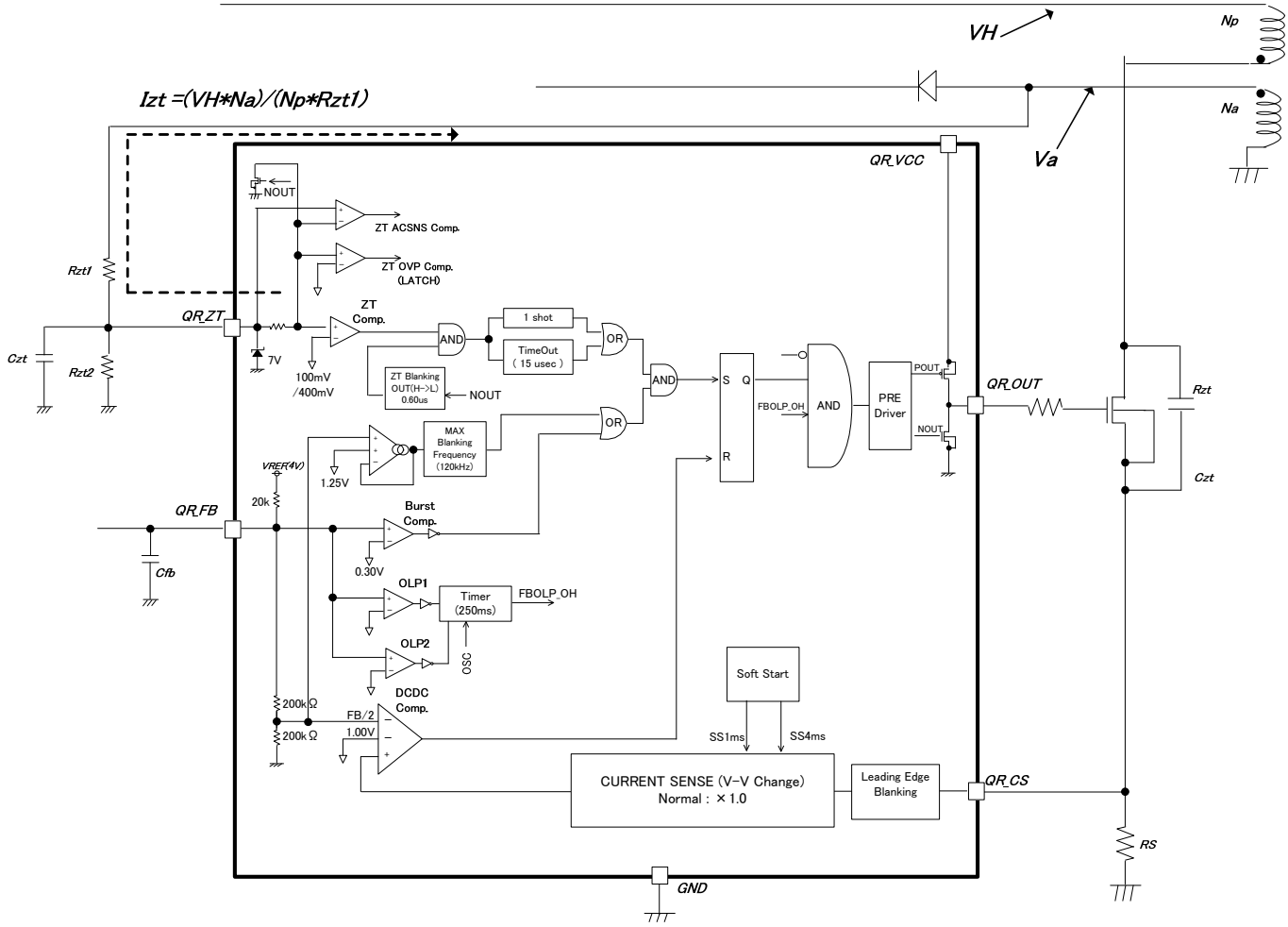


Figure 29. Diagram of CS switching current

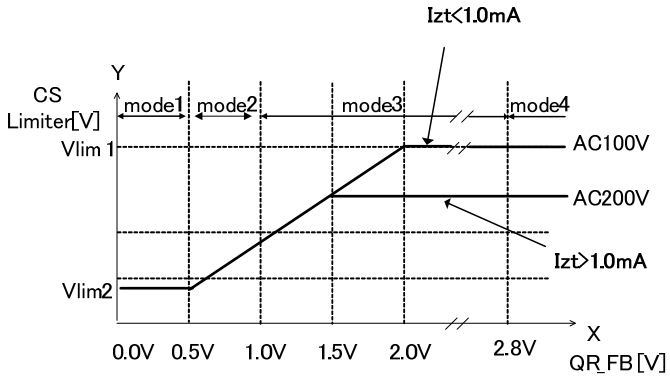


Figure 30. QR_CS Switching QR_FB Voltage VS QR_CS Voltage

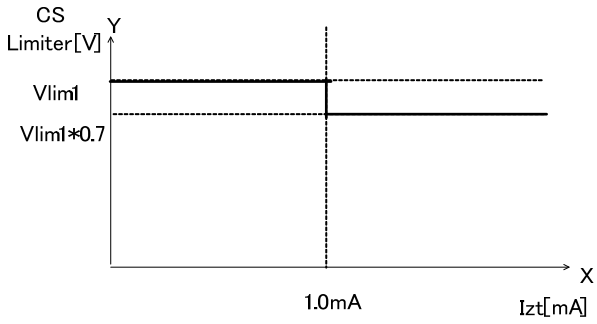


Figure 31. QR_CS Switching I_{zt} Current VS QR_CS Voltage

ex) setting method（operate changing AC100V and AC220V）
AC100V 141V±42V（±30% margin）
AC220V 308V±62V（±20% margin）
The case of above, Between 182V～246V, operates changing of CS current => Operate VH＝214VH
N_p=100, N_a=15

$V_a=V_{in}*N_a/N_p$ = 214V*15/100 *(-1) = -32.1V
$R_{zc} = V_a/ I_{ZT}$ = -32.1V/-1mA = 32.1kΩ

By the above explanation, R_{zt}=32KΩ

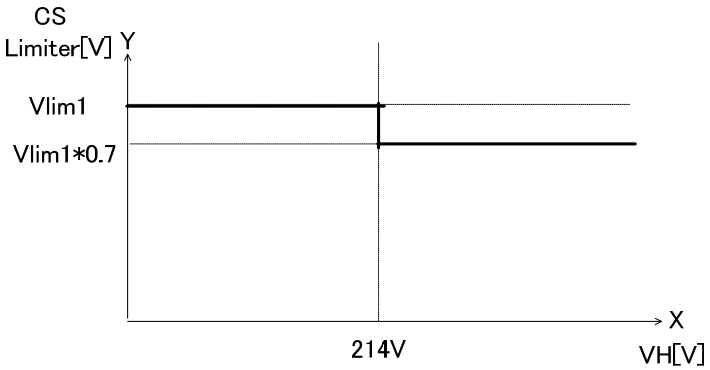


Figure 32. Example of Over current limiter of CS switching

(5-4) Determination of OFF width(turn ON)

OFF width is controlled at the QR_ZT pin.
When switching is OFF, the power stored in the coil is supplied to the secondary-side output capacitor.
When this power supply ends there is no more current flowing to secondary side, so the switching MOS drain pin voltage drops.
Consequently, the voltage on the auxiliary coil side also drops.
A voltage that was resistance-divided from the QR_ZT pin by R_{zt1} and R_{at2} is applied. When this voltage level drops to Vzt1(100mV typ) or below, switching is turned ON the QR_ZT comparator. Since bottom status is detected at the QR_ZT pin, time constants are generated using C_{zt}, R_{zt1}, and R_{zt2}.
Additionally, a QR_ZT trigger mask function (described in section 5-5) and a QR_ZT time out function
(described in section 5-6) are built in.

(5-5)QR_ZT trigger mask function

The QR_ZT trigger mask function is shown below figure33.
When switching is set ON -> OFF, super position of noise may occur at the QR_ZT pin.
At such times, the QR_ZT comparator is masked for the T_{ztmask} time to prevent QR_ZT comparator operation errors.

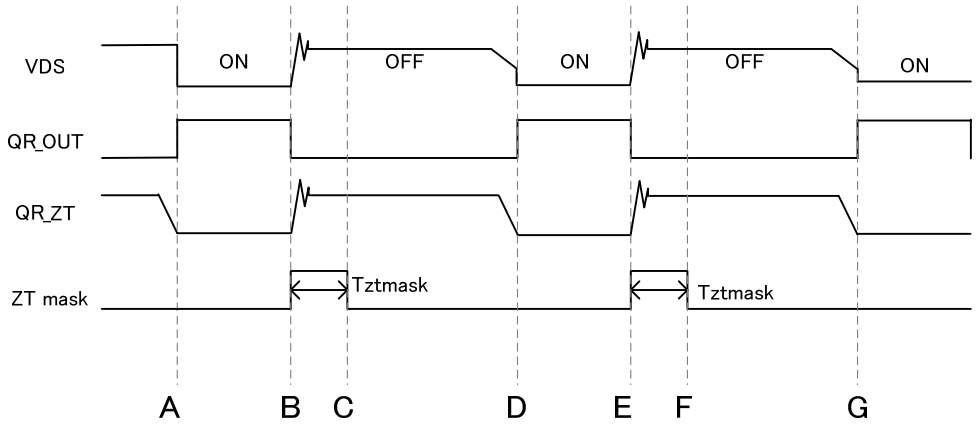


Figure 33. ZT trigger mask Function

A: QR_OUT OFF=>ON
B: QR_OUT ON=>OFF
C: Because of generation of QR_ZT pin noise, T_{ZTMASK} doesn't operate the QR_ZT comparator.
D: Same as A
E: Same as B
F: Same as C
G: Same as A

(5-6)ZT time out function(Figeure34)

After the ZT comparator is detected, this function forcibly turns switching ON if the following is not detected, even when T_{ztout} (15us typ) has elapsed.

If, the secondary output voltage is low, the auxiliary coil voltage VA is reduced, and the QR_ZT pin voltage drops below V_{zt1} (100mVtyp).

In such cases, this function turns switching ON forcibly.

As for T_{ztout}, since 15 us (typ) = 66.7kHz, when the maximum frequency is in frequency reduction mode, the QR_ZT timeout time depends on the frequency reduction mode

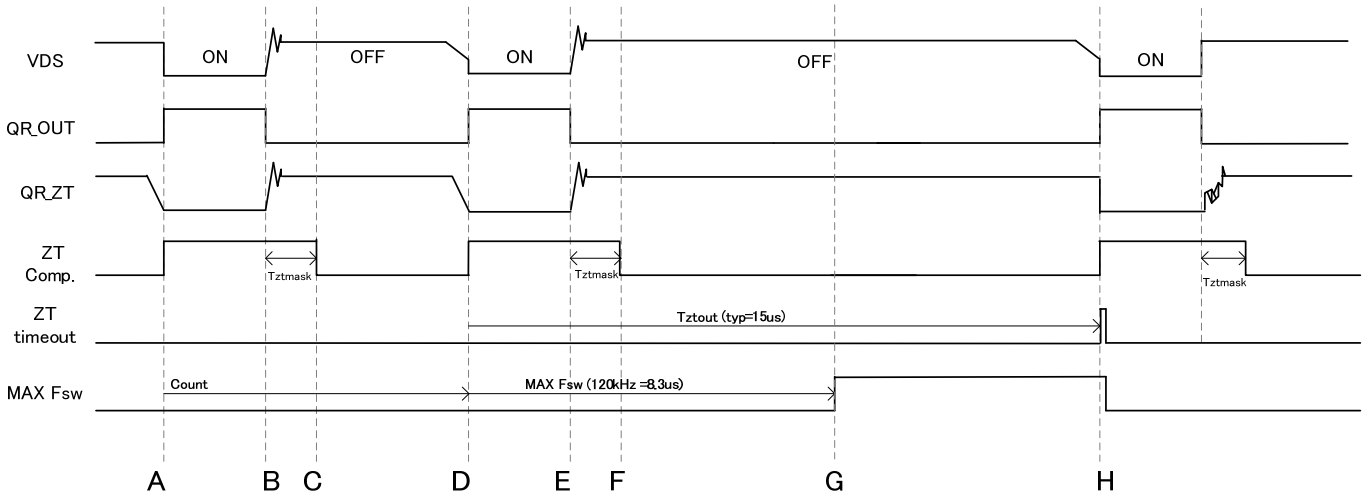


Figure 34. ZT Time out Function

A: QR_ZT＜V_{ZT1} 、DC/DC is ON. Count maximum frequency at this point.
B: DC/DC ON=>OFF
C: Because noise is generated at QR_ZT pin, T_{ZTMASK} doesn't operate QR_ZT comparator.
D: DC/DC OFF=>ON
E: Same as B
F: Same as C
G: Count maximum frequency
H: Because 1cycle>T_{ZTOUT}, forcibly be DC/DC OFF=>ON

(5-7)Soft start operations

Normally, when the power supply is turned ON, a large current flows to the AC/DC power supply. The BM1051F builds-in a soft start function to prevent large changes in the output voltage and output current during startup.

this function is reset when the VCC pin voltage is at V_{UVLO2}(7.0V typ) or below, soft start is performed again at the next AC power-on.

During a soft start, the following post-startup operations are performed. (See turn OFF described in section 5-1)

Start to 1ms -> Set to 25% when CS limiter value is normal

1ms PFC normal status -> Set to 75% when CS limiter value is normal

(5-8)Overload protection function/Overload protection mode switching

The overload protection function monitors the overload status of the secondary output current at the FB pin, and fixes the OUT pin at low level when overload status is detected.
During overload status, current no longer flows to the photocoupler, so the QR_FB pin voltage rises.
When this status continues for the T_{FOLP} time (64ms typ), it is considered an over load, and the OUT pin is fixed at low level.
Once the QR_FB pin voltage exceeds V_{FOLP1a} (2.8V typ), if it drops to lower than V_{FOLP1b} (2.6V typ) during the T_{FOLP} time (64ms typ), the overload protection timer is reset. At startup, the QR_FB voltage is pulled up to the internal voltage by pull-up resistor, and operation starts once the voltage reaches V_{FOLP1a} (2.8V typ) or above. Therefore, the design must set the QR_EB voltage at or below the V_{FOLP1b} (2.6V typ) voltage within the T_{FOLP} (64ms typ) time. In other words, the secondary output voltage start time must be set to within T_{FOLP} (64ms typ) after IC startup.

When an overload is detected, either auto recovery mode or latch mode can be selected for the BM1051F.When pull-down resistance R_{FOLP} (100kΩ typ)is attached to QR_FB pin, latch mode is set. Do not attach any R_{FOLP} value other than 100kΩtyp, since that would prevent latching due to the IC7s internal resistance ratio.

To release latching after selecting latch mode, first unplug the power supply, and then set VCC<V_{LATCH} (typ=6.5V) to release latching.
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

(5-9)QR_ZT pin OVP(Over Voltage Protection)

An OVP（Over Voltage Protection) function is built in for the QR_ZT pin.
When the QR_ZT pin voltage reaches V_{ZLT} (TYP=3.5V),over voltage status is detected. QR_ZT pin OVP protection performed latch mode.
A mask time defined as T_{LATCH} (TYP=150us) is built in for the QR_ZT pin OVP function. When QR_ZT OVP status continues for 150us, overvoltage is detected. This function masks any surges (etc.) that occur at the pin. See the illustration in Figure 35.
(Like VCC OVP, T_{LATCH} (TYP=150us) is built in)

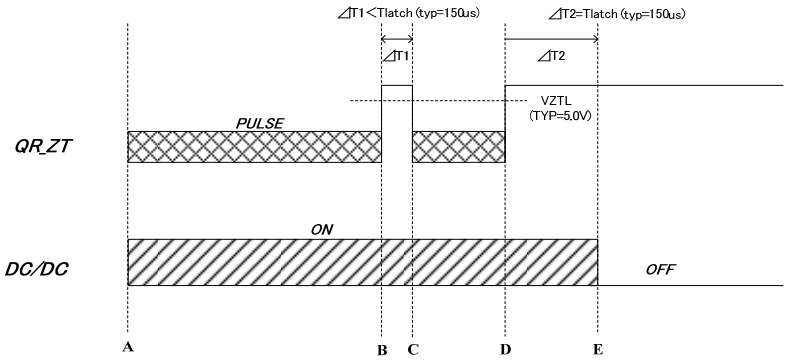


Figure 35. ZTOVP and Latch mask Function

A: DC/DC pulse operates. QR_ZT pin operates too.
B: QR_ZT pin voltage＞V_{ZTL} (TYP=3.5V)
C: QR_ZT pin voltage＞V_{ZTL} (TYP=3.5V) state within T_{COMP}（typ=150us）, returns to normal DC/DC operation.
D: QR_ZT pin voltage＞V_{ZTL} (TYP=3.5V)
E: QR_ZT pin voltage＞V_{ZTL} (TYP=3.5V) state continues T_{COMP}（typ=150us）, operates latch and DC/DC OFF.
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

(5-10) Quasi-resonant DC/DC block protection operation mode

Show every protection function operation mode table 6.
FB pin over load protection function is able to change AUTR/LATCH by FB pin pull down resistance.
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

Table 6. Protection Circuit Operation Mode of Quasi-resonant DC/DC

ITEM	contents	LATCH/AUTOR=GND				LATCH/AUTOR=VREF			
		detection method	operation at detection	release mothod	operation at detection	detection method	operation at detection	release mothod	operation at detection
QR_FB_OLP1	QR_FB pin over current protection function	QR_FB>2.8V state continues 250ms (QR_FB rising)	DC/DC part operation stop	QR_FB<2.6V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_FB_OLP2	QR_FB pin over current protection function	QR_FB>3.6V (QR_FB rising)	DC/DC part operation stop	QR_FB<3.4V (QR_FB falling)	normal operation	same as LATCH/AUTOR=GND			
QR_ZT OVP	QR_ZT ipn over voltage protection function	QR_ZT>3.5V state continue 150us (QR_QR_ZTrising)	DC/DC part operation stop	QR_ZT<3.5V (QR_ZT falling)	normal operation	QR_ZT>3.5V state continues 150us (QR_ZT rising)	DC/DC part LATCH operation stop	VCC<6.5V (VCC falling)	normal operation

(6)Power Factor Correction Circuit (PFC: Power Factor Correction)Part

Power Factor Correction Circuit is peak current control method of fixed frequency.

It is possible to supply proper system as PFC by monitoring P_VS pin, P_CS pin, and P_BO.

It is possible to control the MOSFET ON width by monitoring output voltage at P_VS pin, AC input voltage at P_BO pin, and MOSFET current at P_CS pin.

The switching frequency is F_{PSW1}(typ=65kH). Following is detail explanation of PFC (reference figure36).

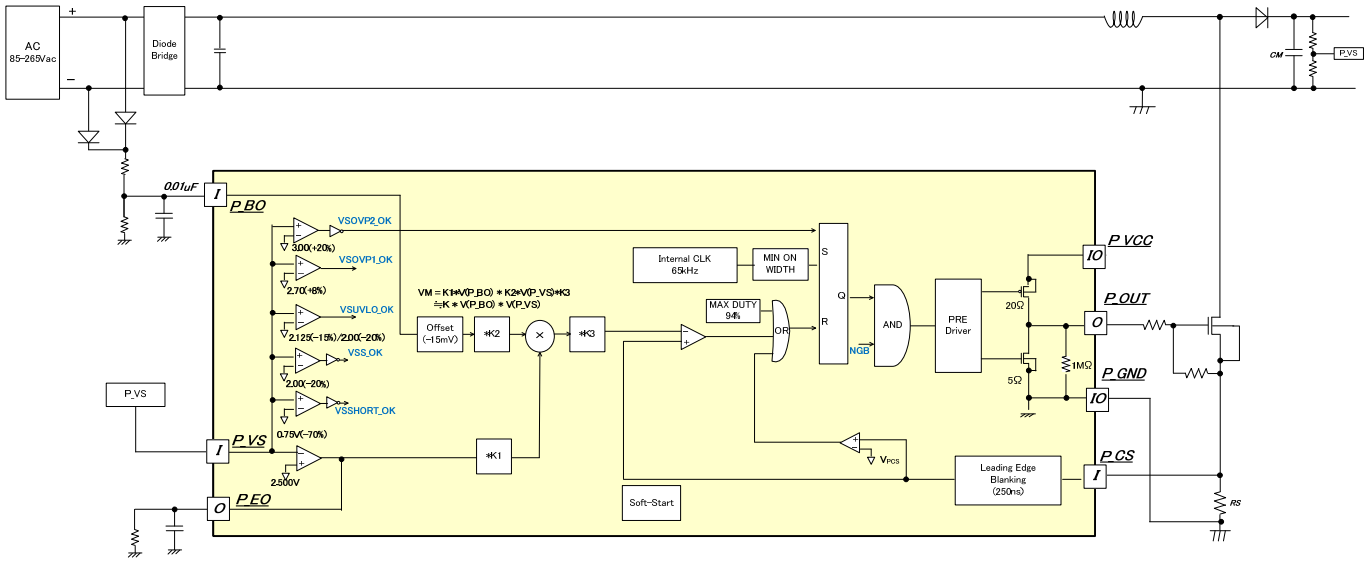


Figure 36. Diagram of PFC block

(6-1) gm AMP

P_VS pin monitors a divide voltage between resistors of PFC output voltage. P_VS pin is piled up ripple voltage of AC frequency (50kHz/60kHz).

The gmAMP filters this ripple voltage and controls the voltage level of P_VSEO, by responding to error of P_VS pin voltage P_VS pin voltage and internal reference voltage V_{VSAMP} (typ 2.5V).

Please set cut-off frequency of filter at P_VSEO pin showed in figure 37, to about 5~10Hz.

Gm constant is designed 44[uA/V].

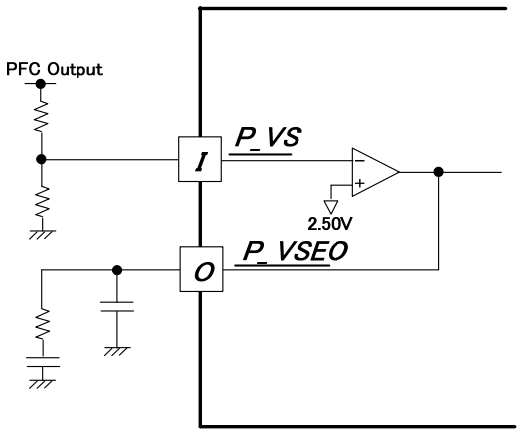


Figure 37. Diagram of gmAMP

(6-2)Monitor of input voltage

PFC is monitored AC input voltage at the P_BO pin.

Because the range of input voltage at P_BO pin is 0~1.8V, please select R_{bo1} and R_{bo2} to set P_BO voltage in the range.

Refer to block figure at figure38.

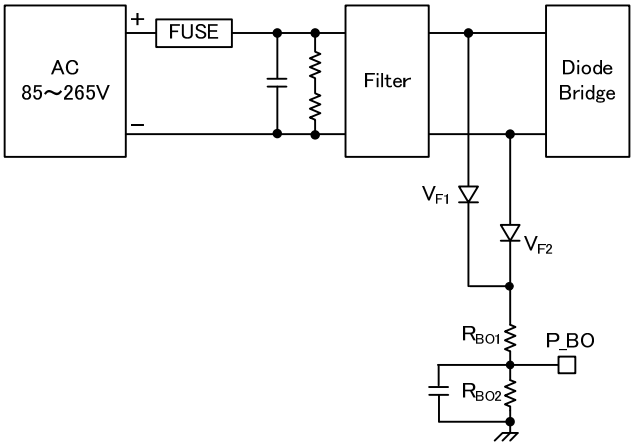


Figure 38. Diagram of Input Voltage Monitor

(6-3)Maximum power limiting function

PFC maximum power is also larger as input voltage is larger.
To compensate this maximum power, PFC built-in Maximum power limiting.
Maximum power is in proportion to the square of output of multiplier V_MULT, so it is possible to correct that maximum power depends on input voltage by dividing P_BO voltage by P_BOPK voltage which is peak voltage of P_BO pin.

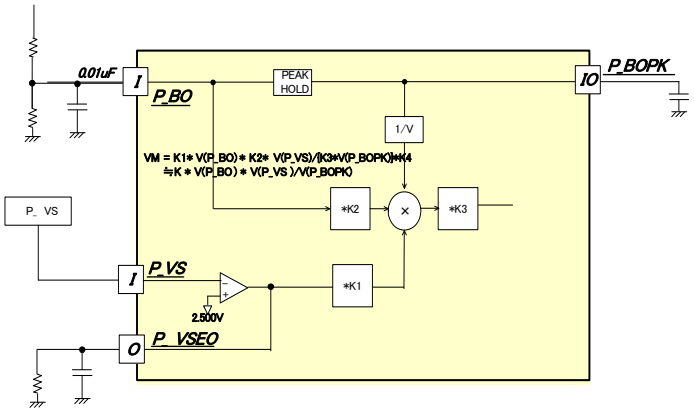


Figure 39. Diagram of Maximum Power Restriction Function

(6-4)Multiplier

A multiplier is calculated gmAMP output voltage and P_BO pin voltage, and P_BOPK pin voltage.
Following is formula of Multiplier output.

$$V_{MULT} = \frac{K1 \times \{V(P\_BO) \times K_2 \times V(P\_VSEO)\}}{K_3 \times \{V(P\_BOPK)\}}$$
$$= K \times V(P\_BO) \times V(P\_VSEO) / (V(P\_BOPK))$$

V_{MULT}: Multiplier output voltage K: Multiplier constant

(6-5) Switching frequency

Switching frequency is averaged typ.65kHz. MAX DUTY is D_{MAX} (typ 94%), always the period has OFF width.

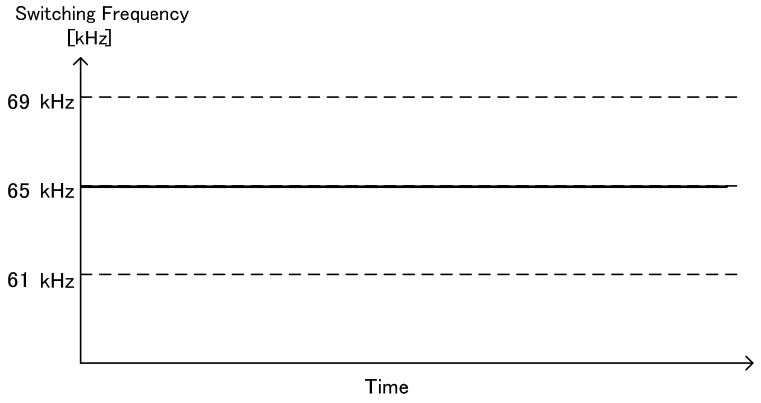


Figure 40. Frequency Function

(6-6)LEB(Leading Edge Blanking) function

When the switching MOSFET is turned ON, surge current occurs at each capacitor charge /discharge or drive current.
For that, P_CS voltage rise temporarily, over current limiter may be detected errors.
To prevent detection errors blanking time is built in during T_{PLEB} (typ=250ns) from P_OUT pin changing L →H..
This blanking function enables a reduction of P_CS pin noise filter.

(6-7) Over current protection function

P_CS pin built in over current protection function for MOSFET. This function operates in pulse by pulse, and detects over current. Over current detection voltage is changed by P_BOPK pin voltage. Over current detection voltage is V_{PCS1} (typ = 1.16V) at P_BOPK voltage =0.56V, V_{PCS2} (typ = 0.60V) at P_BOPK voltage = 1.30V.
Show figure41 changing of over current detection voltage by P_BOPK pin voltage.
Over-current detection value I_{PCS} is decided $I_{PCS}=V_{PCS}/R_S$ by external resistance R_S at figure42.

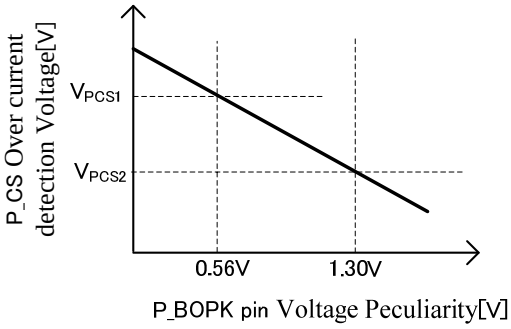


Figure 41. Over-current detection Voltage - P_BOPK Voltage Peculiarity

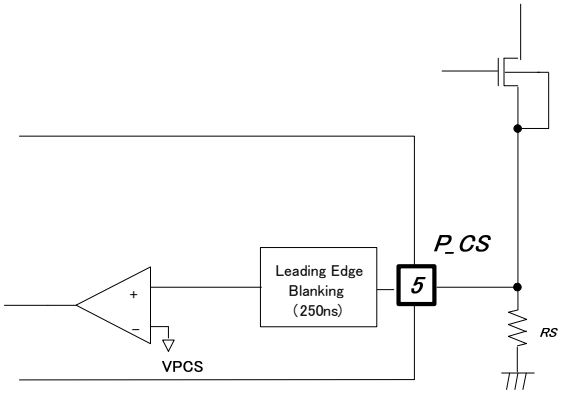


Figure 42. Diagram of Over current Protection

(6-8)P_VS short protection function

PFC built in short protection function at P_VS. Switching is stopped at P_VS voltage<V_{P_SHORT} (0.30Vtyp).

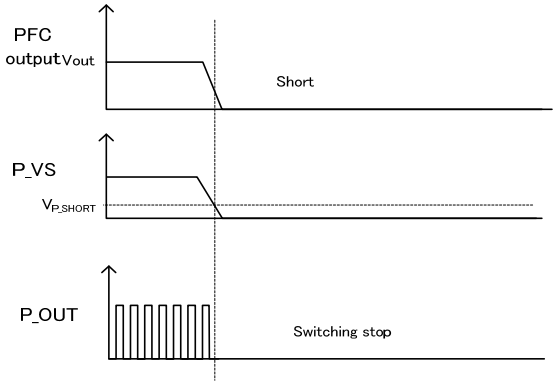


Figure 43. P_VS Short Protection Operation

(6-9) Gain increase function in P_VS low voltage

Dropping output voltage by suddenly load change, because PFC voltage response is slow, output voltage is low for a long time. Therefore, PFC is speed up voltage control loop gain when P_VS pin voltage is low up to V_{PGUP}(typ = 2.25V)(Output voltage -10%). In the operation, ON-duty at P_OUT pin increases, PFC prevents from output voltage dropping for a long time.
This operation is stopped when P_VS pin voltage is upper than V_{GUP} (typ=2.25V).

(6-10)P_VS first over voltage protection function

In case of output voltage is rise by starting up or output load suddenly change, because PFC voltage response is slow, output voltage is high for a long time. Therefore, PFC is speed up voltage control loop gain when P_VS pin voltage is rise V_{P_OVP1} (typ=2.625). In this operation, ON-duty at P_OUT pin decrease, PFC prevents from output voltage rising for a long time.
This operation is stopped when P_VS pin voltage is lower than V_{p_ovp1}(typ=2.625V).

(6-11)P_VS second over voltage protection function

PFC built in second over voltage protection, for the case that P_VS voltage exceeds over first over voltage protection voltage V_{P_OVP1}. It is possible to switch Latch protection (LATCH/AUTOR=H) or auto recovery (LATCH/AUTOR=L) by LATCH/AUTOR pin. In case of latch operation, P_VS pin voltage exceeds V_{P_OVP2} (typ=2.725V)(output voltage pulse9%) during T_{P_OVP2a} (Typ=32ms), PFC switching is stopped.

In case of auto recovery, P_VS pin voltage is exceeded V_{P_OVP2} (typ=2.725V), switching is stopped instantly. When P_VS pin voltage decrease lower than V_{P_OVP2} (typ=2.725V), switching operation is re-start. Refer to figure44.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

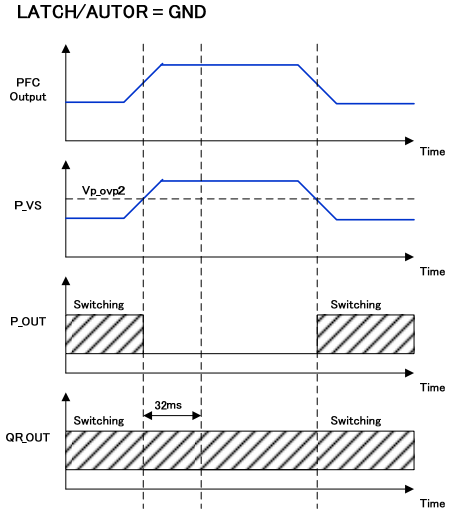


Figure 44. VS Second Over Voltage Protection (at auto recovery mode)

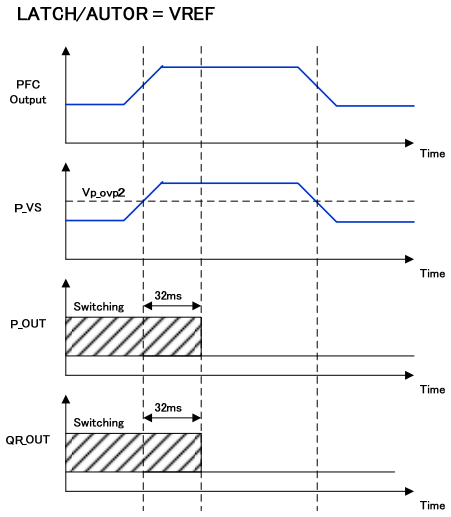


Figure 45. Operation of P_VS Second Over Voltage Protection (at latch mode)

Switching is stopped by second over voltage protection in the case that the P_VS pin loop of output voltage is open loop.

(6-12)PFC burst operation

PFC built-in burst operation for preventing PFC output voltage from rising at light load.
This function is that PFC monitors P_VSEO pin at light load, switched burst operation or not.
Burst operation voltage depends on P_BOPK voltage.
In case of P_BOPK voltage = 0.56V, burst function operates when P_VSEO voltage is lower than VSEO=V_{P_BURST} (0.266V typ). In case of P_BOPK voltage = 1.30V, burst function operates when P_VSEO voltage is lower than VSEO=V_{P_BURST1} (0.128V typ)
Refer to the change of burst voltage for P_BOPK voltage figure46.

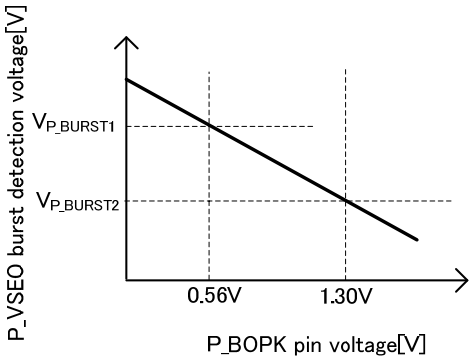


Figure 46. Diagram of P_VSEO burst voltage by P_BOPK voltage

(6-13) Operation mode of PFC block protection

Show operation mode every protection function at Table7.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside. (ΔC)

Table 7. Protection Circuit Operation mode of PFC

ITEM	contents	LATCH/AUTOR=GND				LATCH/AUTOR=VREF			
		detection method	operation at detection	release mothod	operaetion at detection	detection method	operation at detection	release mothod	operaetion at detection
P_VS SHORT PROTECTION	P_VS PIN short protection function	P_VS<0.30V (P_VS falling)	PFCpart operation stop	P_VS>0.30V (P_VS rising)	normal operation	Same as LATCH/AUTOR=GND			
P_VS GAIN INCREASING	P_VS PIN low voltage gain increasing function	P_VS<2.25V (P_VS falling)	GMAMP GAIN INCREASE	P_VS>2.25V (P_VSrising)	normal operation	Same as LATCH/AUTOR=GND			
P_VS OVP1	P_VS PIN over voltage protection function1	P_VS>2.625V (P_VS rising)	GM AMPGAIN DECREASE	P_VS<2.625V (P_VS falling)	normal operation	Same as LATCH/AUTOR=GND			
P_VS OVP2	P_VS PIN over voltage protection function2	P_VS>2.725V (P_VS rising)	PFC part operation stop	P_VS<2.725V (P_VS falling)	normal operation	P_VS>2.725V (P_VS rising)	PFC part, DC/DC part latch operation stops	VCC<6.5V (VCC falling)	normal operation

● **Basic Characteristics (This data is for reference only and is not guaranteed.)**

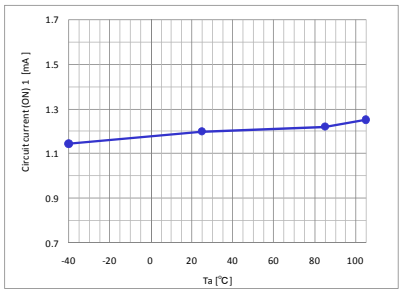


Fig-47-1 Circuit current (ON) 1

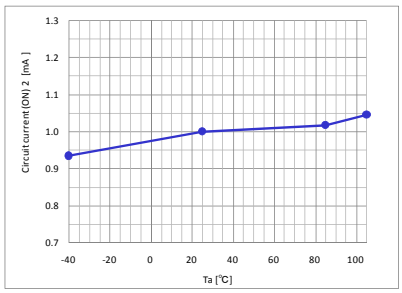


Fig-47-2 Circuit current (ON) 2

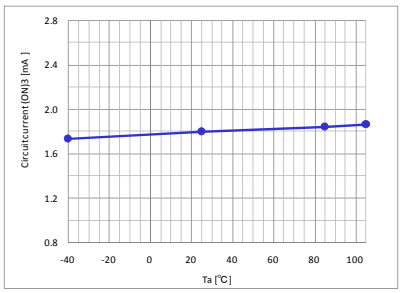


Fig-47-3 Circuit current (ON) 3

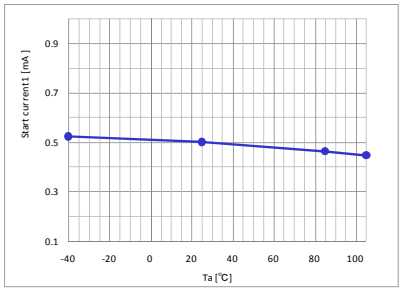


Fig-47-4 Start current 1

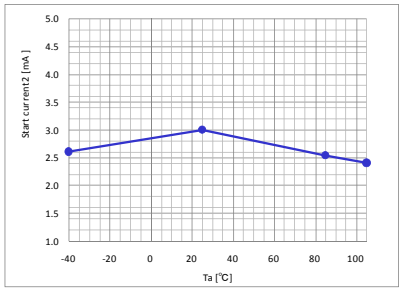


Fig-47-5 Start current 2

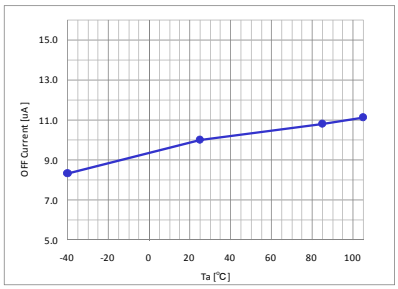


Fig-47-6 OFF Current

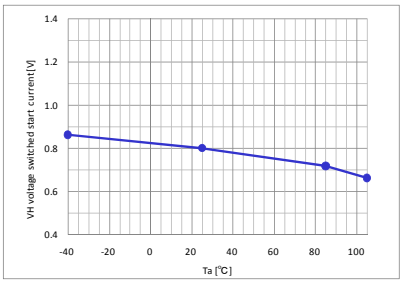


Fig-47-7 VH voltage switched start current

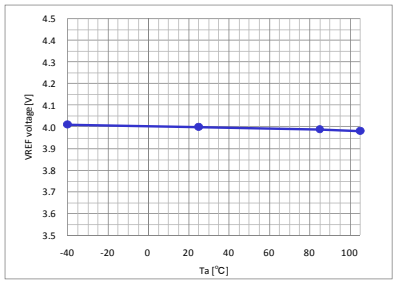


Fig-47-8 VREF output voltage

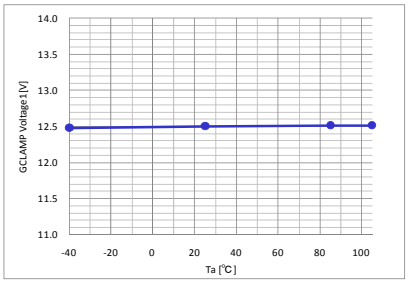


Fig-47-9 GCLAMP voltage 1

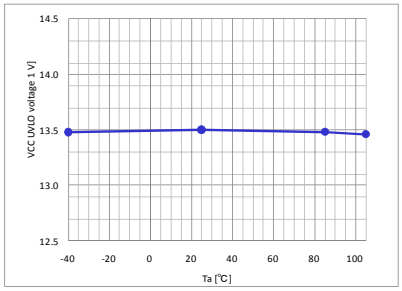


Fig-47-10 VCC UVLO voltage 1

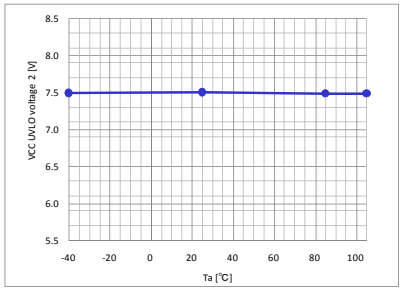


Fig-47-11 VCC UVLO voltage 2

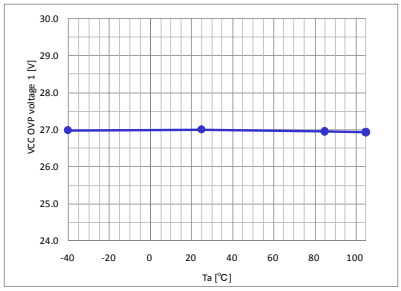


Fig-47-12 VCC OVP voltage 1

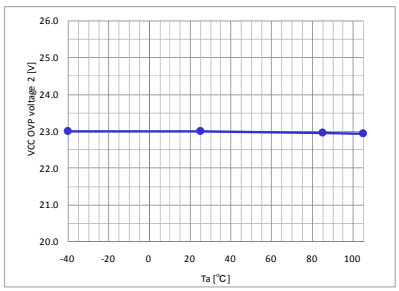


Fig-47-13 VCC OVP voltage 2

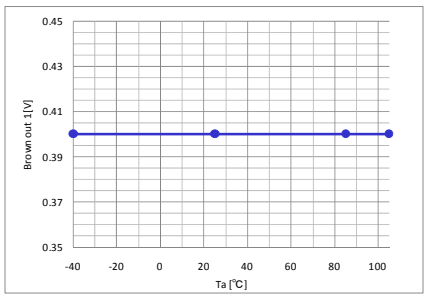


Fig-47-14 Brown out detection voltage 1

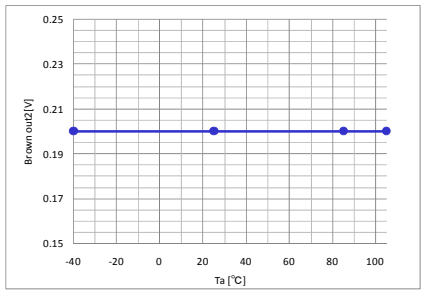


Fig-47-15 Brown out detection voltage 2

● **Basic Characteristics (This data is for reference only and is not guaranteed.)**

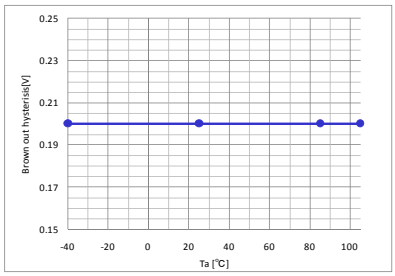


Fig-47-16 Brown out hysteresis

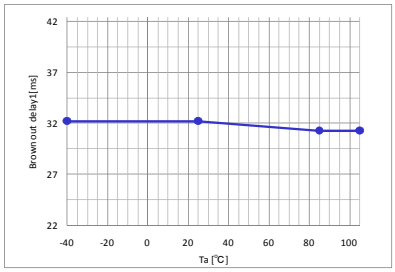


Fig-47-17 Brown out detection delay time 1

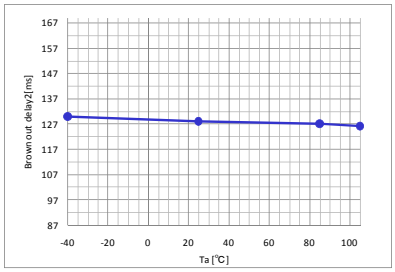


Fig-47-18 Brown out detection delay time 2

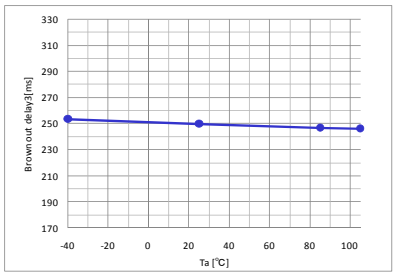


Fig-47-19 Brown out detection delay time 3

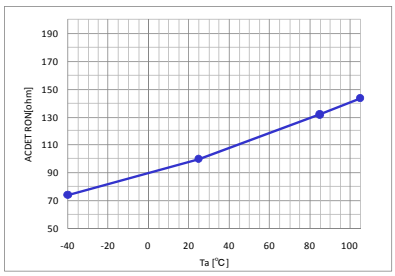


Fig-47-20 ACDET pin ON resister

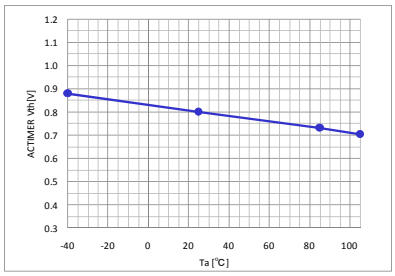


Fig-47-21 ACTIMER pin input level

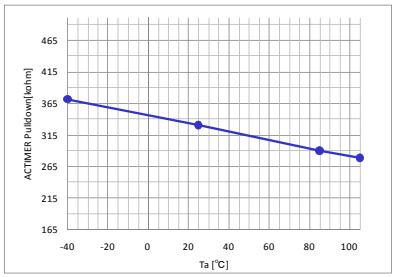


Fig-47-22 ACTIMER pin pull-down res.

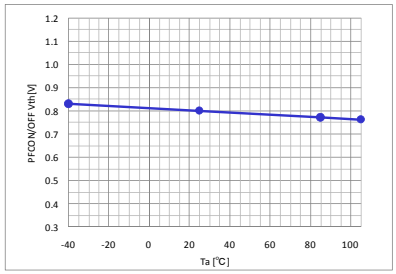


Fig-47-23 PFCON/OFF pin input level

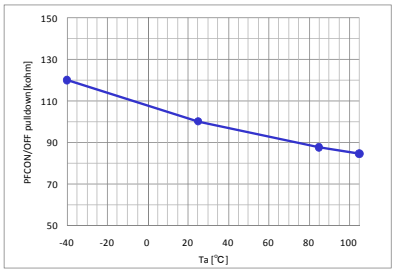


Fig-47-24 PFCON/OFF pin pull-down res.

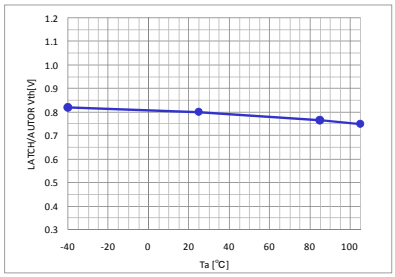


Fig-47-25 LATCH/AUTOR pin input level

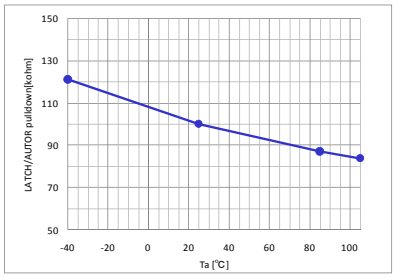


Fig-47-26 LATCH/AUTOR pin pull-down res.

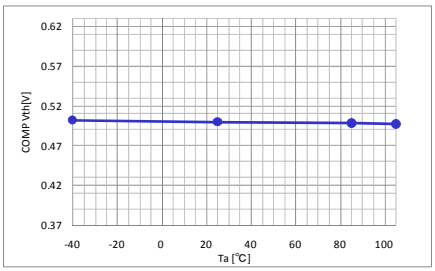


Fig-47-27 COMP pin detection voltage

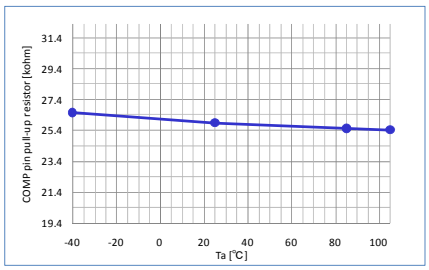


Fig-47-28 COMP pin pull-up resistor

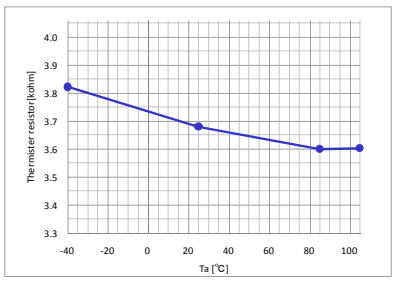


Fig-47-29 External Thermistor resistor

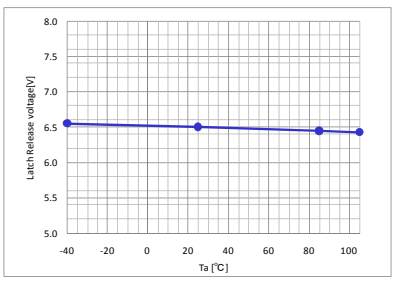


Fig-47-30 Latch release voltage2

● **Basic Characteristics (This data is for reference only and is not guaranteed.)**

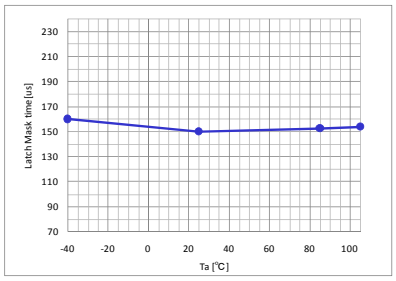


Fig-47-31 Latch mask time

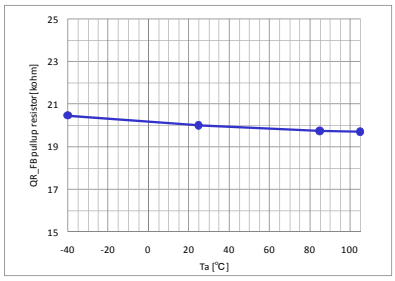


Fig-47-32 QR_FB pin pull-up resistance

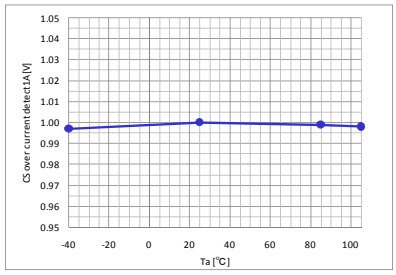


Fig-47-33 CS over-current detect voltage 1A

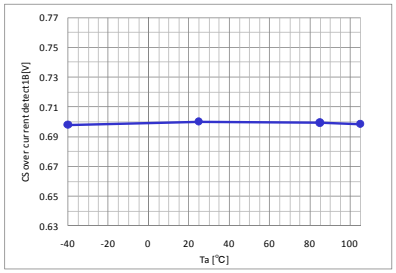


Fig-47-34 CS over-current detect vol.1B

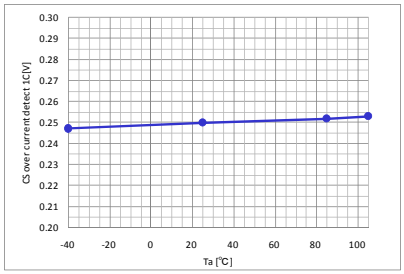


Fig-47-35 CS over-current detect vol.1C

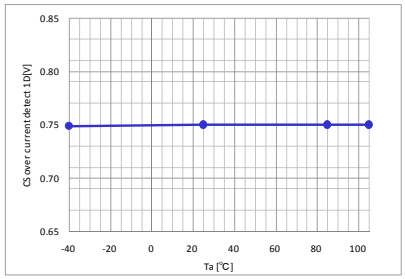


Fig-47-36 CS over-current detect vol.1D

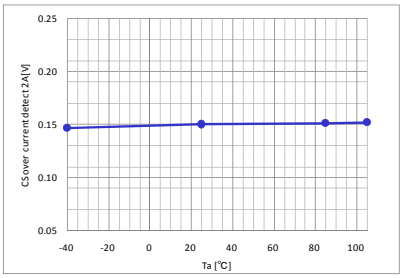


Fig-47-37 CS over-current detect vol. 2A

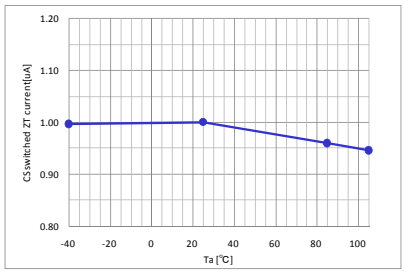


Fig-47-38 CS switched ZT current

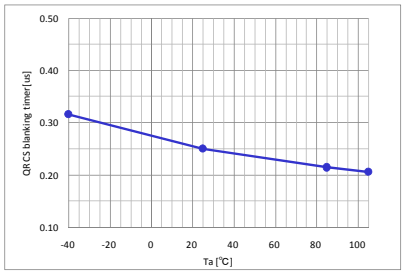


Fig-47-39 CS Leading Edge Blanking time

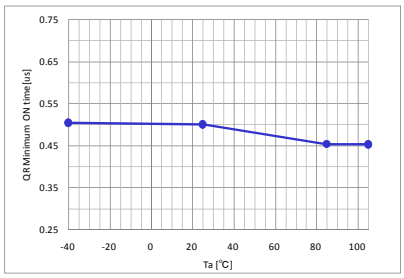


Fig-47-40 Minimum ON width

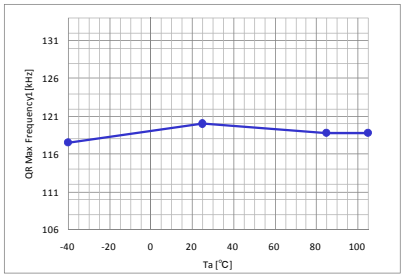


Fig-47-41 Maximum operating frequency 1

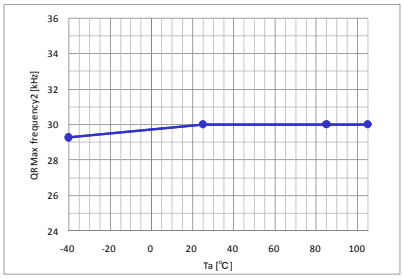


Fig-47-42 Maximum operating frequency 2

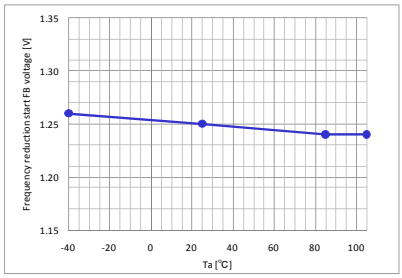


Fig-47-43 Freq. reduction start FB voltage

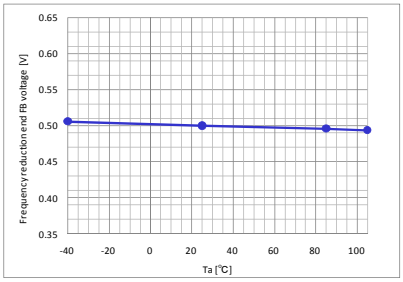


Fig-47-44 Freq. reduction end FB voltage

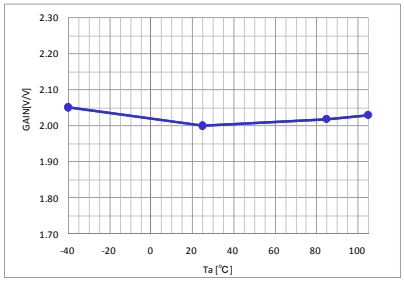


Fig-47-45 Voltage gain

● **Basic Characteristics (This data is for reference only and is not guaranteed.)**

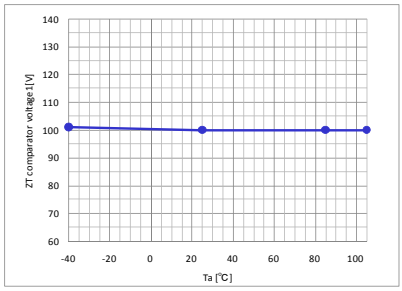


Fig-47-46 ZT comparator voltage 1

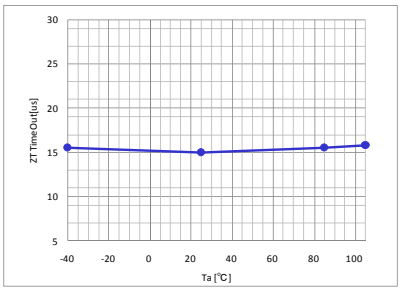


Fig-47-47 ZT trigger timeout period

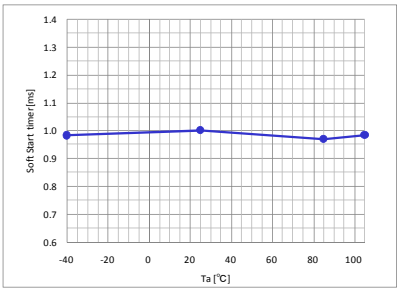


Fig-47-48 Soft start time

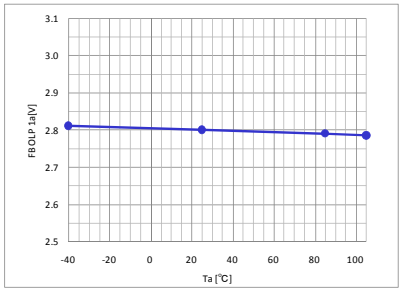


Fig-47-49 FB OLP Voltage 1a

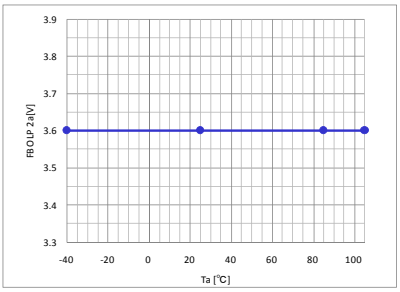


Fig-47-50 FB OLP Voltage 2a

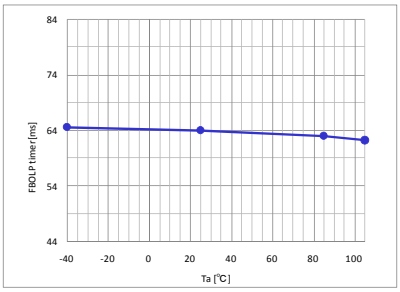


Fig-47-51 FB OLP timer

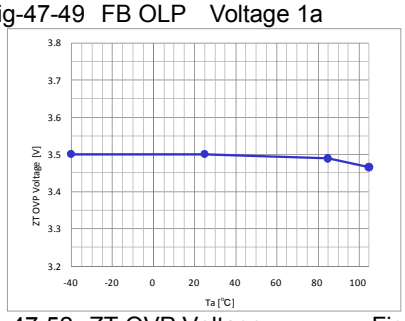


Fig-47-52 ZT OVP Voltage

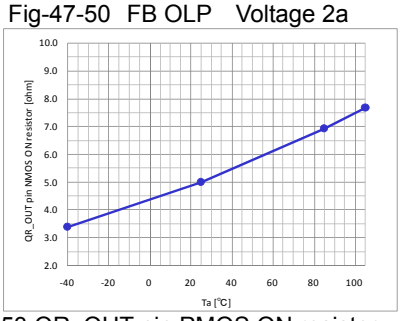


Fig-47-53 QR_OUT pin PMOS ON resistor

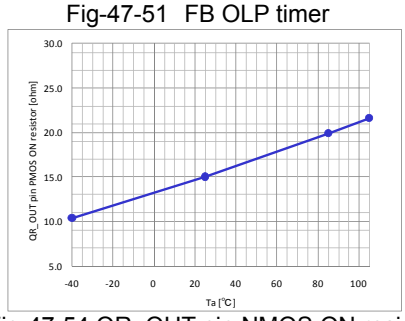


Fig-47-54 QR_OUT pin NMOS ON resistor

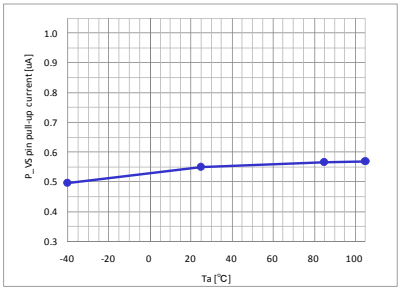


Fig-47-55 P_VS pin pull-up current

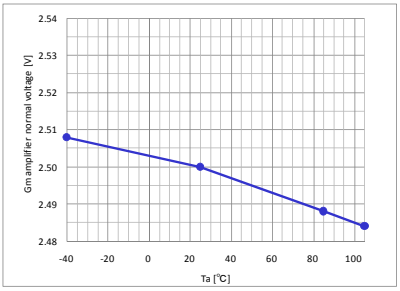


Fig-47-56 Gm amplifier normal voltage

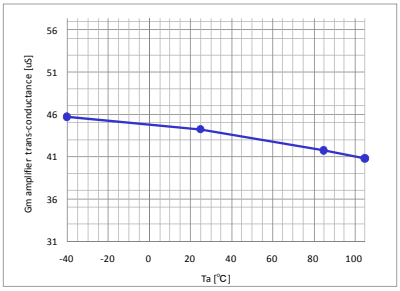


Fig-47-57 Gm amplifier trans-conductance

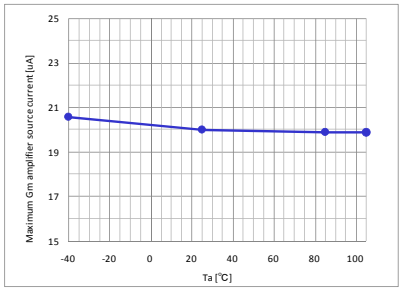


Fig-47-58 Max. Gm amplifier source current

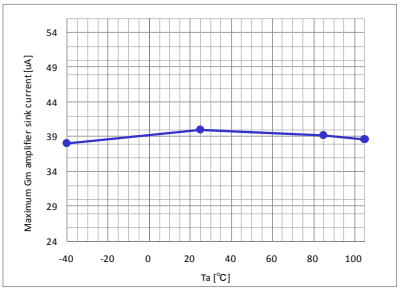


Fig-47-59 Max. Gm amplifier sink current

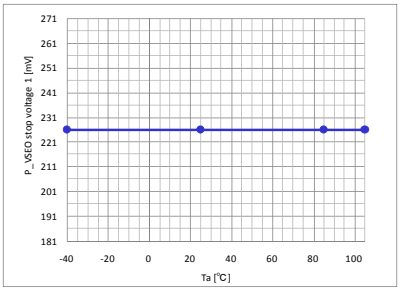


Fig-47-60 P_VSEO stop voltage1

● **Basic Characteristics (This data is for reference only and is not guaranteed.)**

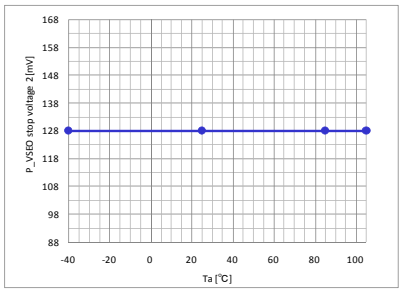


Fig-47-61 P_VSEO stop voltage 2

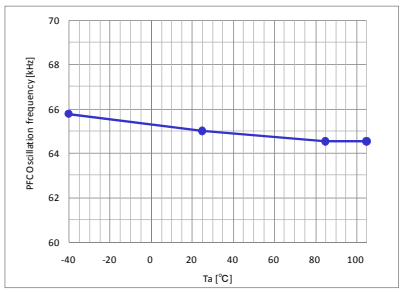


Fig-47-62 PFC Oscillation frequency

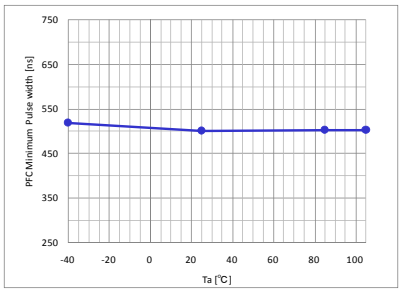


Fig-47-63 PFC Min. Pulse width

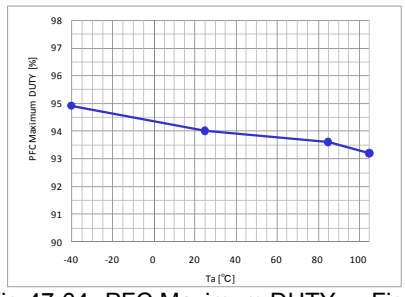


Fig-47-64 PFC Maximum DUTY

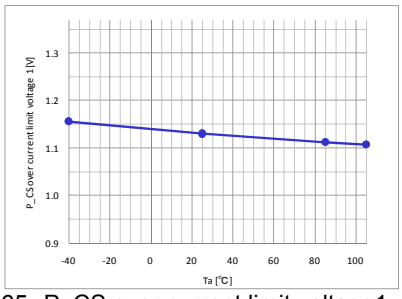


Fig-47-65 P_CS over current limit voltage1

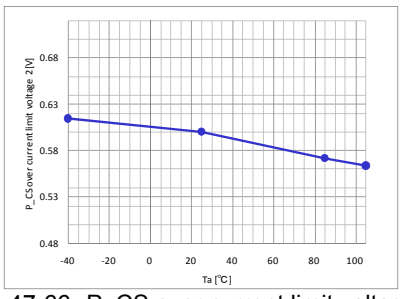


Fig-47-66 P_CS over current limit voltage 2

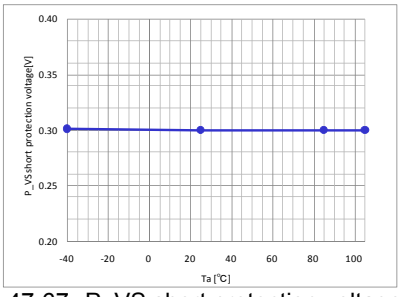


Fig-47-67 P_VS short protection voltage

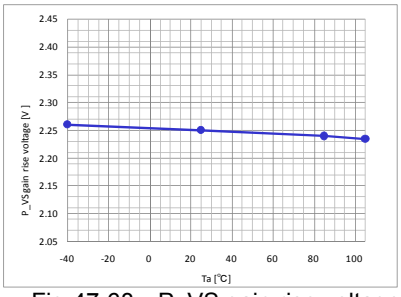


Fig-47-68 P_VS gain rise voltage

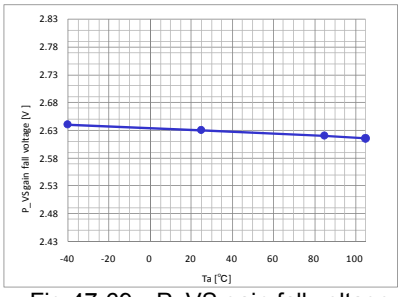


Fig-47-69 P_VS gain fall voltage

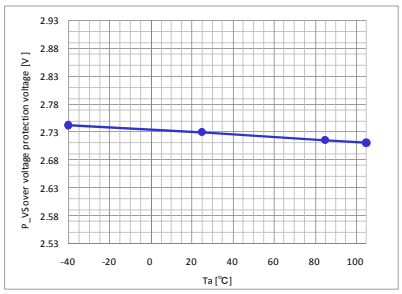


Fig-47-70 P_VS over voltage protection voltage

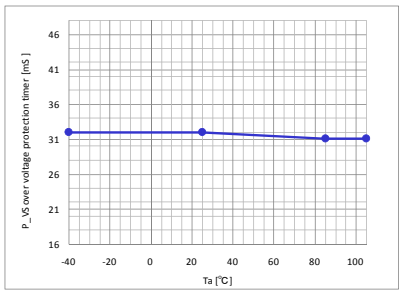


Fig-47-71 P_VS over voltage protection timer

● **Thermal loss**

The thermal design should set operation for the following conditions.
(Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature Ta must be 85℃ or less.
2. The IC's loss must be within the allowable dissipation P_d.

The thermal abatement characteristics are as follows. (Figure 47)

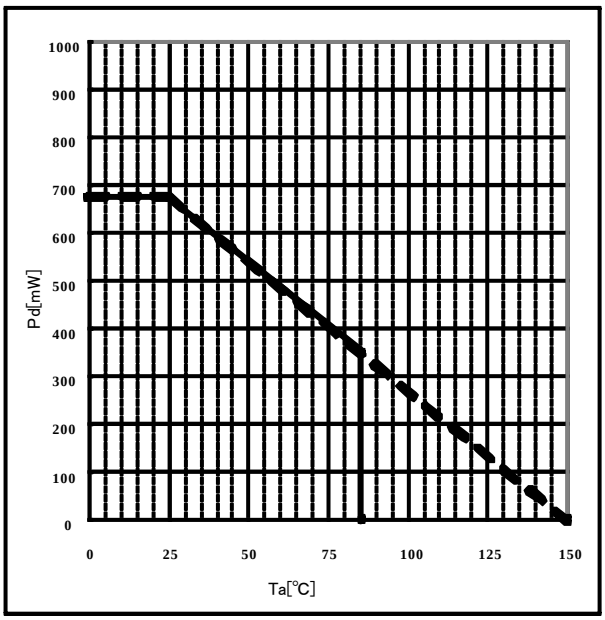


Figure 48. SOP24 Temperature reduction peculiarity

● Use-related cautions

(1) Absolute maximum ratings

Damage may occur if the absolute maximum ratings such as for applied voltage or operating temperature range are exceeded, and since the type of damage (short, open circuit, etc.) cannot be determined, in cases where a particular mode that may exceed the absolute maximum ratings is considered, use of a physical safety measure such as a fuse should be investigated.

(2) Power supply and ground lines

In the board pattern design, power supply and ground lines should be routed so as to achieve low impedance. If there are multiple power supply and ground lines, be careful with regard to interference caused by common impedance in the routing pattern. With regard to ground lines in particular, be careful regarding the separation of large current routes and small signal routes, including the external circuits. Also, with regard to all of the LSI's power supply pins, in addition to inserting capacitors between the power supply and ground pins, when using capacitors there can be problems such as capacitance losses at low temperature, so check thoroughly as to whether there are any problems with the characteristics of the capacitor to be used before determining constants.

(3) Ground potential

The ground pin's potential should be set to the minimum potential in relation to the operation mode.

(4) Pin shorting and attachment errors

When attaching ICs to the set board, be careful to avoid errors in the IC's orientation or position. If such attachment errors occur, the IC may become damaged. Also, damage may occur if foreign matter gets between pins, between a pin and a power supply line, or between ground lines.

(5) Operation in strong magnetic fields

Note with caution that these products may become damaged when used in a strong magnetic field.

(6) Input pins

In IC structures, parasitic elements are inevitably formed according to the relation to potential. When parasitic elements are active, they can interfere with circuit operations, can cause operation faults, and can even result in damage. Accordingly, be careful to avoid use methods that enable parasitic elements to become active, such as when a voltage that is lower than the ground voltage is applied to an input pin. Also, do not apply voltage to an input pin when there is no power supply voltage being applied to the IC. In fact, even if a power supply voltage is being applied, the voltage applied to each input pin should be either below the power supply voltage or within the guaranteed values in the electrical characteristics.

(7) External capacitors

When a ceramic capacitor is used as an external capacitor, consider possible reduction to below the nominal capacitance due to current bias and capacitance fluctuation due to temperature and the like before determining constants.

(8) Thermal design

The thermal design should fully consider allowable dissipation (Pd) under actual use conditions.

Also, use these products within ranges that do not put output Tr beyond the rated voltage and ASO.

(9) Rush current

In a CMOS IC, momentary rush current may flow if the internal logic is undefined when the power supply is turned ON, so caution is needed with regard to the power supply coupling capacitance, the width of power supply and GND pattern wires, and how they are laid out.

(10) Handling of test pins and unused pins

Test pins and unused pins should be handled so as not to cause problems in actual use conditions, according to the descriptions in the function manual, application notes, etc. Contact us regarding pins that are not described.

(11) Document contents

Documents such as application notes are design documents used when designing applications, and as such their contents are not guaranteed. Before finalizing an application, perform a thorough study and evaluation, including for external parts.

●**Ordering Information**

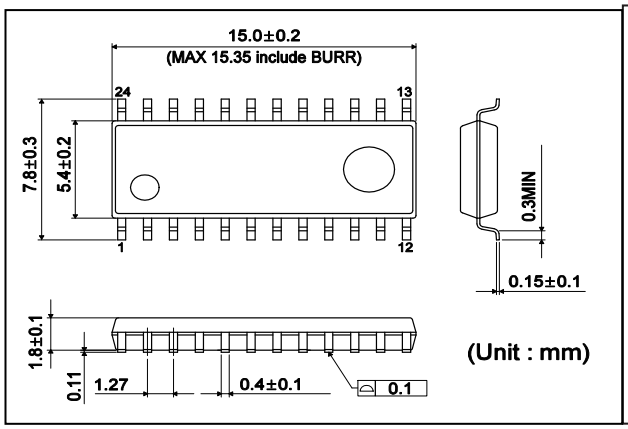
B M 1 0 5 1 F	-	G E 2

Product name

Package
F : SOP24

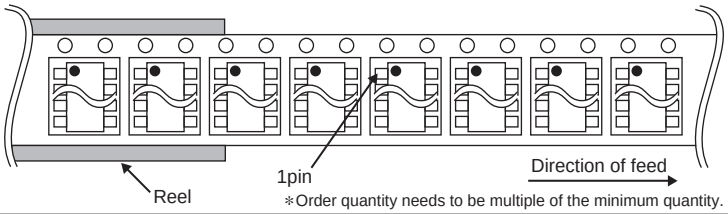
Packaging and
forming specification
E2: Embossed tape and reel

●**Physical Dimension Tape and Reel Information**



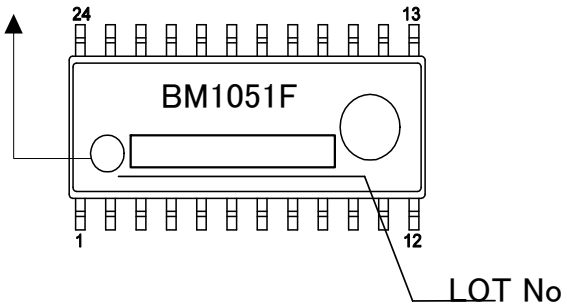
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Marking Diagram**



Revision History

Date	Revision	Changes
4.Jun.2014	001	New Release
11.Apr.2015	002	P13, P16, P17, P23, P25, P31, P32, P37, P38 The note external application of VREF when the latch mode is used.
11.Apr.2015	002	P12 Figure4->Figure6 (Reference of start-up time)
11.Apr.2015	002	P25 Figure25->Figure24
11.Apr.2015	002	P25 Figure26->Figure25
30.Apr.2015	003	P13, P16, P17, P23, P25, P31, P32, P37, P38 ΔC is mentioned in the note of VREF external application.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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