

# NX3DV42

## Dual high-speed USB 2.0 double-pole double-throw analog switch

Rev. 3.1 — 20 October 2016

Product data sheet

### 1. General description

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The NX3DV42 is a double-pole double-throw analog switch suitable for use as an analog or digital multiplexer/demultiplexer. Its wide bandwidth and low bit-to-bit skew allows the NX3DV42 to pass high-speed differential signals with good signal integrity. Its high channel to channel crosstalk rejection results in minimal noise interference. The bandwidth is wide enough to pass high-speed USB 2.0 differential signals (480 Mb/s). It consist of two switches, each with two independent input/outputs (HSDn+ and HSDn-) and a common input/output (D+ or D-). One digital input (S) is used to select the switch position. When pin OE is HIGH, the switches are turned off. Schmitt trigger action at the select input (S) and output enable input (OE) makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 3.0 V to 4.3 V.

### 2. Features and benefits

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- Supply voltage range from 3.0 V to 4.3 V
- 4  $\Omega$  typical ON resistance
- 7.3 pF typical ON capacitance
- 950 MHz typical bandwidth or data frequency
- Low crosstalk of -30 dB at 240 MHz
- Break-before-make switching
- ESD protection:
  - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
  - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
  - ◆ HBM exceeds 12000 V for power to GND protection
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from -40 °C to +125 °C

### 3. Applications

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- Cell phone, PDA, digital camera and notebook
- LCD monitor, TV and set-top box



## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NX3DV42GU	-40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1
NX3DV42GU10	-40 °C to +125 °C	XQFN10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm	SOT1337-1
NX3DV42GU33	-40 °C to +125 °C	X2QFN10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.33 mm	SOT1430-1

## 5. Marking

Table 2. Marking

Type number	Marking code
NX3DV42GU	x4
NX3DV42GU10	x4
NX3DV42GU33	x4

## 6. Functional diagram

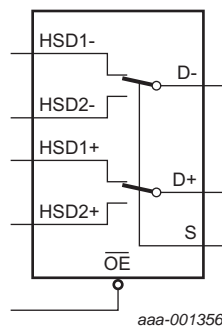
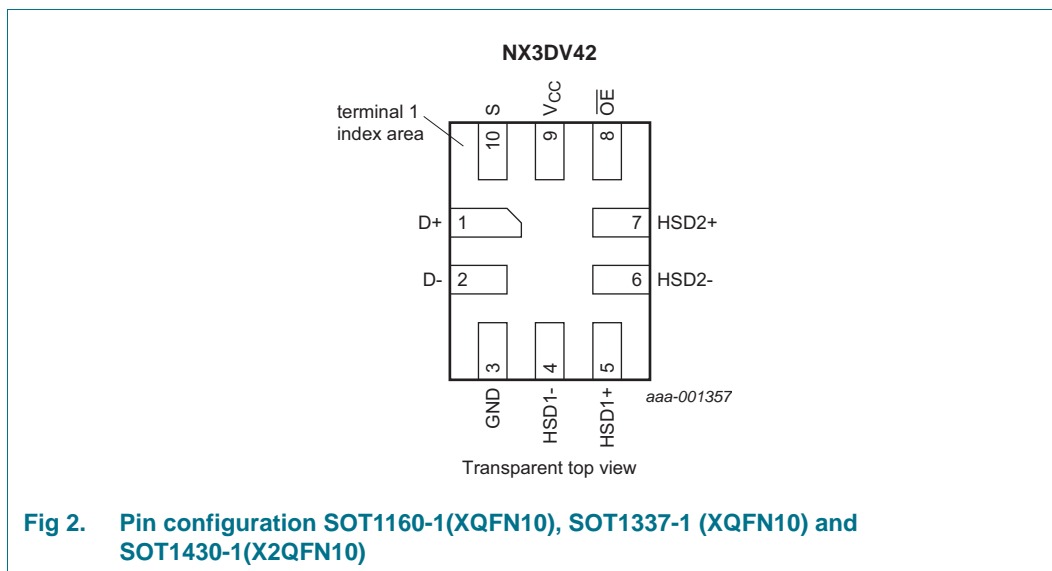


Fig 1. Logic symbol

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

**Table 3. Pin description**

Symbol	SOT1160-1, SOT1337-1, SOT1430-1	Description
HSD1-, HSD2-	4, 6	independent input or output
HSD1+, HSD2+	5, 7	independent input or output
D+, D-	1, 2	common output or input
GND	3	ground (0 V)
$\overline{\text{OE}}$	8	output enable input (active LOW)
S	10	select input
V <sub>CC</sub>	9	supply voltage

## 8. Functional description

**Table 4. Function table<sup>[1]</sup>**

Input		Channel on
S	$\overline{\text{OE}}$	
L	L	HSD1+ and HSD1-
H	L	HSD2+ and HSD2-
X	H	switch off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+5.5	V
$V_I$	input voltage	pins S and $\overline{OE}$ [1]	-0.5	+5.5	V
$V_{SW}$	switch voltage		-0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{SK}$	switch clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{SW}$	switch current		-	$\pm 100$	mA
$I_{CC}$	supply current		-	+50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For XQFN10 package: above 100 °C derate linearly with 4 mW/K.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		3.0	4.3	V
$V_I$	input voltage	pins S and $\overline{OE}$	0	4.5	V
$V_{SW}$	switch voltage	[1]	0	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+125	°C

[1] To avoid sinking GND current from terminals D+ and D- when switch current flows in terminals HSDn+ and HSDn-, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals D+ and D-, no GND current will flow from terminals HSDn+ and HSDn-. In this case, there is no limit for the voltage drop across the switch.

## 11. Static characteristics

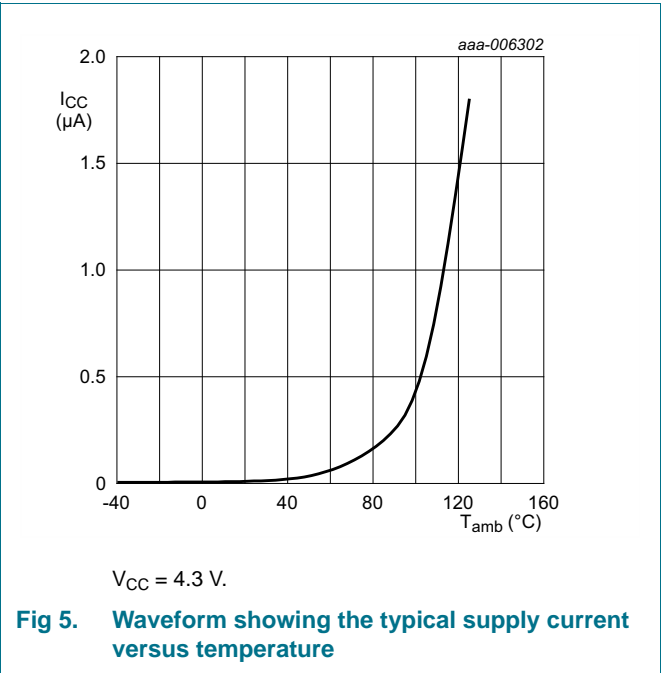
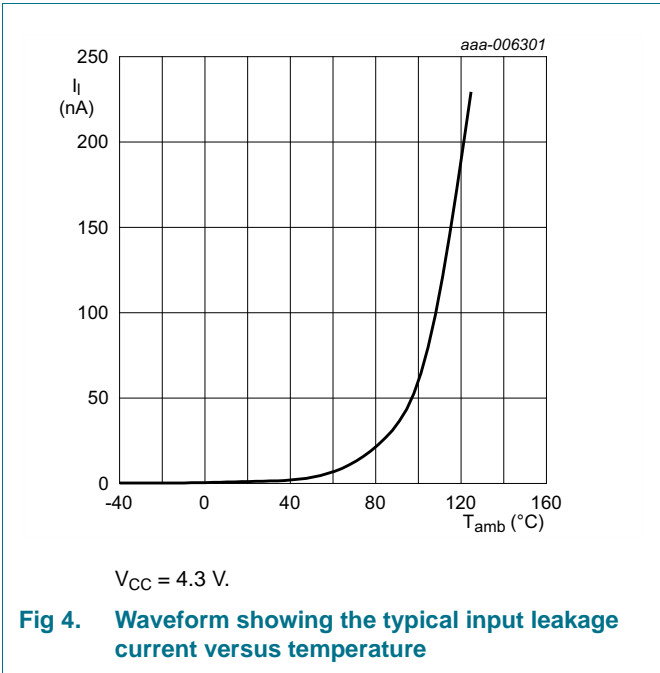
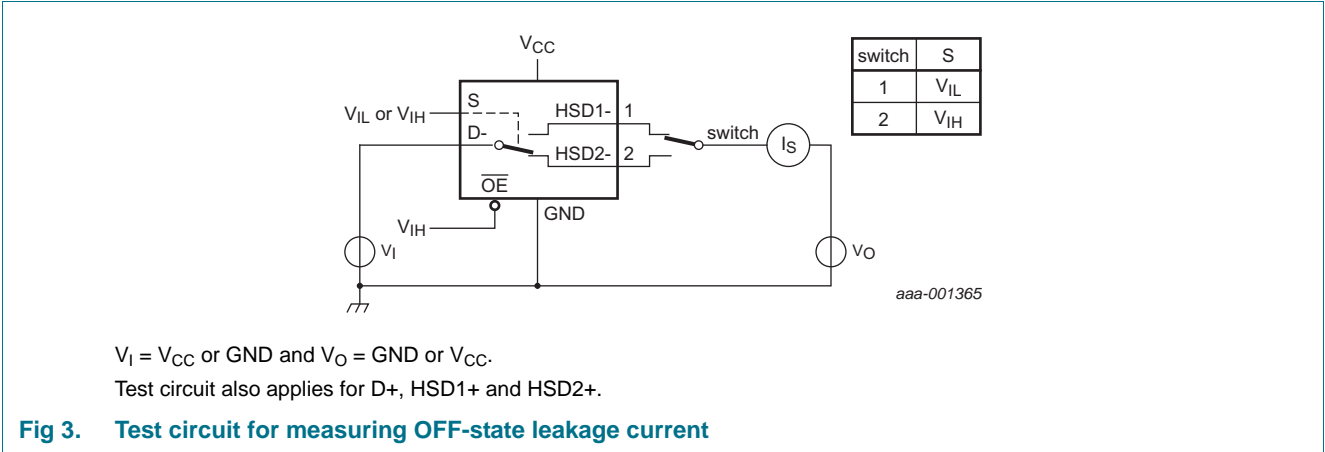
**Table 7. Static characteristics**

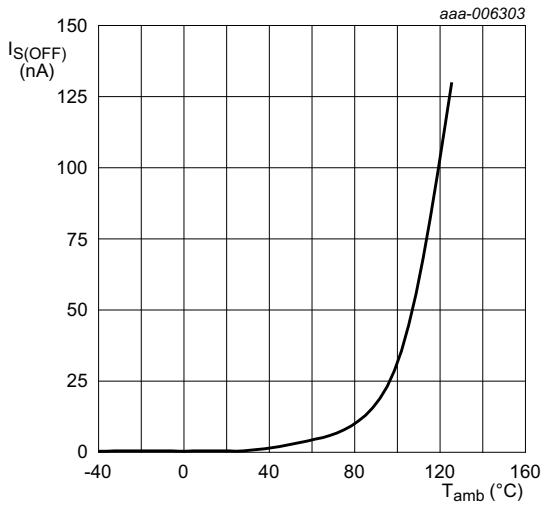
At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	-	-	1.3	-	V
		V <sub>CC</sub> = 4.3 V	1.7	-	-	1.7	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.3 V	-	-	0.7	-	0.7	V
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 3.0 V; I <sub>I</sub> = -18 mA	-	-	-1.2	-	-1.2	V
I <sub>I</sub>	input leakage current	pins S and $\overline{OE}$ ; V <sub>I</sub> = GND to 4.3 V; V <sub>CC</sub> = 4.3 V; see <a href="#">Figure 4</a>	-	-	±1	-	±10	μA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>CC</sub> = 4.3 V; see <a href="#">Figure 3</a> and <a href="#">Figure 6</a>	-	-	±1	-	±2	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.3 V; V <sub>CC</sub> = 0 V; see <a href="#">Figure 7</a>	-	-	±1	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.3 V; V <sub>SW</sub> = GND or V <sub>CC</sub> ; see <a href="#">Figure 5</a>	-	-	1	-	10	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = 2.6 V; V <sub>CC</sub> = 4.3 V; V <sub>SW</sub> = GND or V <sub>CC</sub>	-	-	10	-	10	μA
		V <sub>I</sub> = 1.8 V; V <sub>CC</sub> = 4.3 V; V <sub>SW</sub> = GND or V <sub>CC</sub>	-	-	15	-	15	μA
C <sub>I</sub>	input capacitance	pins S and OE	-	1.0	-	-	-	pF
C <sub>S(OFF)</sub>	OFF-state capacitance	pins HSDn+ and HSDn-; V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to 3.3 V	-	2.8	-	-	-	pF
C <sub>S(ON)</sub>	ON-state capacitance	pins D+ and D-; V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to 3.3 V	-	7.3	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

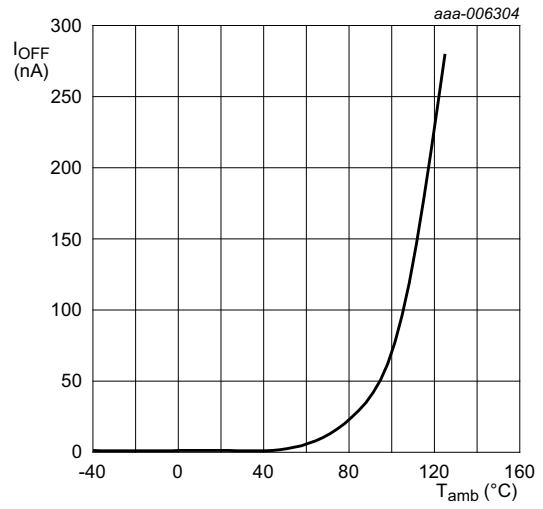
11.1 Test circuit and graphs





V<sub>CC</sub> = 4.3 V.

**Fig 6. Waveform showing the typical OFF-state leakage current versus temperature**



V<sub>CC</sub> = 4.3 V.

**Fig 7. Waveform showing the typical power-off leakage current versus temperature**

### 11.2 ON resistance

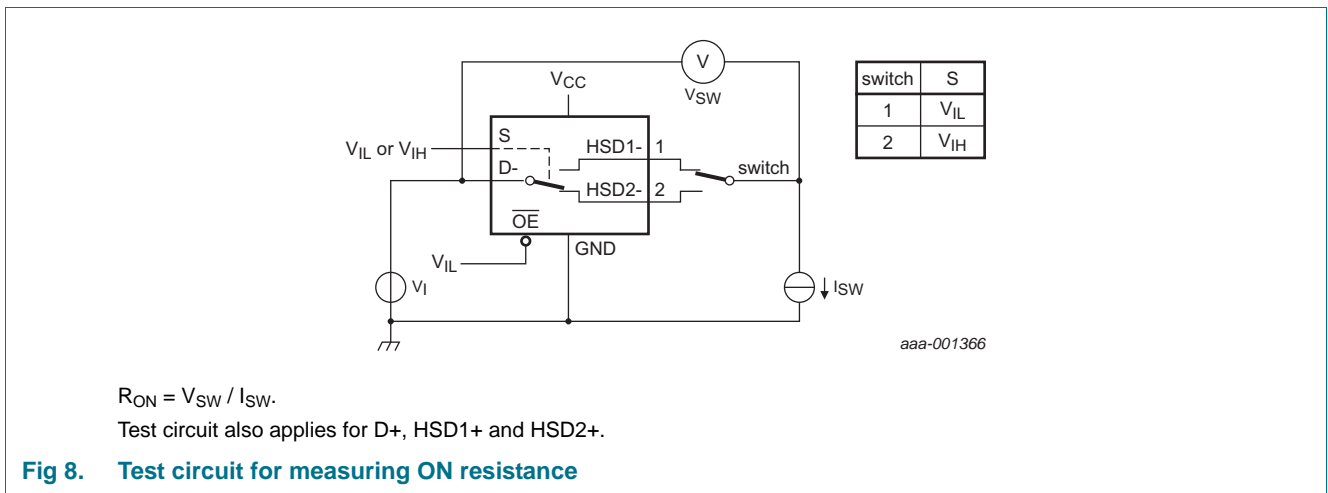
**Table 8. ON resistance**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON</sub>	ON resistance	V <sub>I</sub> = 0.4 V; I <sub>SW</sub> = 8 mA; see <a href="#">Figure 8</a> V <sub>CC</sub> = 3.0 V	-	3.9	6.5	-	10	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0.4 V; I <sub>SW</sub> = 8 mA <sup>[2]</sup> V <sub>CC</sub> = 3.0 V	-	0.65	-	-	-	Ω

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] Measured at identical V<sub>CC</sub>, temperature and input voltage.

### 11.3 ON resistance test circuit





## 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	HSDn+ to D+ or HSDn- to D- or D+ to HSDn+ or D- to HSDn-; see <a href="#">Figure 9</a> <a href="#">[2][3]</a>						
		V <sub>CC</sub> = 3.3 V	-	0.25	-	-	-	ns
t <sub>en</sub>	enable time	S or $\overline{OE}$ to D+ or D-; see <a href="#">Figure 10</a> <a href="#">[4]</a>						
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	11.2	30	-	40	ns
t <sub>dis</sub>	disable time	S or $\overline{OE}$ to D+ or D-; see <a href="#">Figure 10</a> <a href="#">[5]</a>						
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	3.9	25	-	30	ns
t <sub>b-m</sub>	break-before-make time	see <a href="#">Figure 11</a> <a href="#">[3]</a>						
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	5.9	-	2.0	-	ns
t <sub>sk(p)</sub>	pulse skew time	see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 3.0 V to 3.6 V <a href="#">[3]</a>	-	20	-	-	-	ps
t <sub>jit</sub>	jitter time	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 5 pF; t <sub>r</sub> , t <sub>f</sub> = 500 ps (10 % to 90 %) at 480 Mbs (PRBS = 2 <sup>15</sup> - 1) <a href="#">[3]</a>	-	200	-	-	-	ps

[1] Typical values are measured at T<sub>amb</sub> = 25 °C, C<sub>L</sub> = 5 pF and V<sub>CC</sub> = 3.3 V.

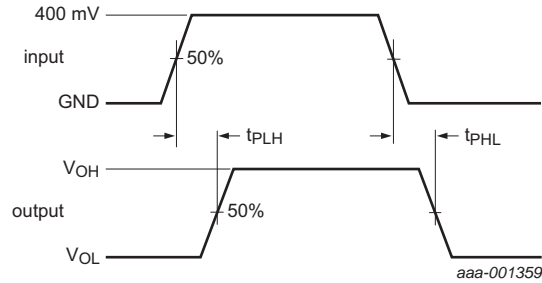
[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Guaranteed by design.

[4] t<sub>en</sub> is the same as t<sub>PZH</sub>.

[5] t<sub>dis</sub> is the same as t<sub>PHZ</sub>.

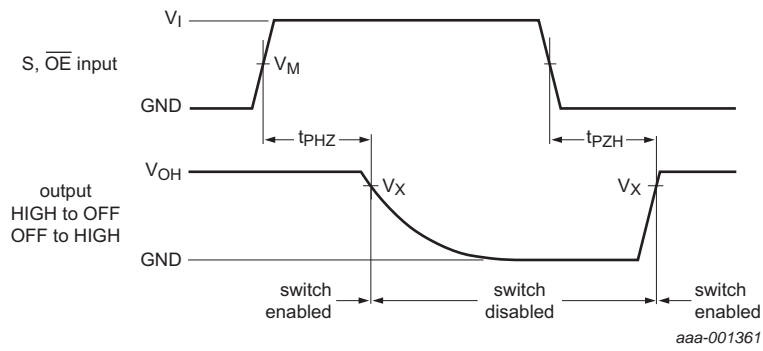
12.1 Waveforms and test circuits



Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

$$t_{sk(p)} = |t_{PHL} - t_{PLH}|$$

Fig 9. The data input to output propagation delay times and pulse skew time



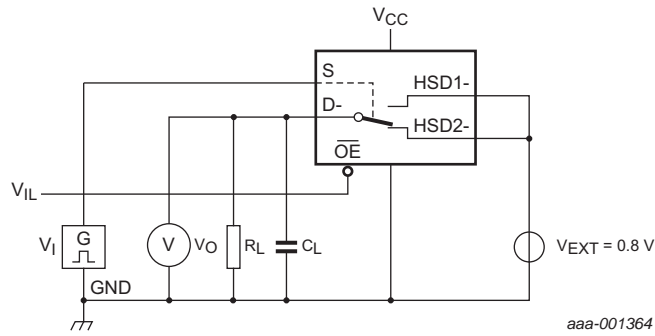
Measurement points are given in [Table 10](#).

Logic level:  $V_{OH}$  is the typical output voltage level that occurs with the output load.

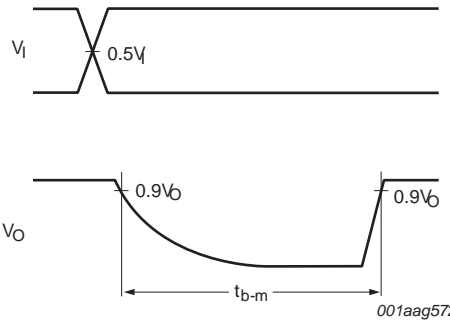
Fig 10. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output
$V_{CC}$	$V_M$	$V_I$	$V_X$
3.0 V to 3.6 V	$0.5V_{CC}$	$V_{CC}$	$0.9V_{OH}$



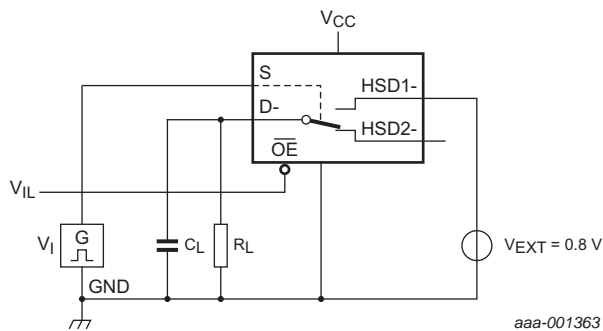
a. Test circuit.



b. Input and output measurement points.

Test circuit also applies for D+, HSD1+ and HSD2+.

**Fig 11. Test circuit for measuring break-before-make timing**



Test circuit also applies for D+, HSD1+ and HSD2+.

Test data is given in [Table 11](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$V_{EXT}$  = External voltage for measuring switching times.

$V_I$  may be connected to S or  $\overline{OE}$ .

**Fig 12. Test circuit for measuring switching times**

Table 11. Test data

Supply voltage	Input		Load	
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>
3.0 V to 3.6 V	V <sub>CC</sub>	≤ 2.5 ns	5 pF	50 Ω

### 12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V<sub>I</sub> = GND or V<sub>CC</sub> (unless otherwise specified); t<sub>r</sub> = t<sub>f</sub> < 2.5 ns.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			Unit
			Min	Typ <sup>[2]</sup>	Max	
f <sub>(-3dB)</sub>	-3 dB frequency response	R <sub>L</sub> = 50 Ω; see <a href="#">Figure 13</a> <sup>[1]</sup>				
		C <sub>L</sub> = 0 pF; V <sub>CC</sub> = 3.0 V to 3.6 V	-	950	-	MHz
		C <sub>L</sub> = 5 pF; V <sub>CC</sub> = 3.0 V to 3.6 V	-	450	-	MHz
α <sub>iso</sub>	isolation (OFF-state)	f <sub>i</sub> = 240 MHz; R <sub>L</sub> = 50 Ω; see <a href="#">Figure 14</a> <sup>[1]</sup>				
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-30	-	dB
Xtalk	crosstalk	between switches; f <sub>i</sub> = 240 MHz; R <sub>L</sub> = 50 Ω; see <a href="#">Figure 15</a> <sup>[1]</sup>				
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-30	-	dB

[1] f<sub>i</sub> is biased at 0.5V<sub>CC</sub>.

[2] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

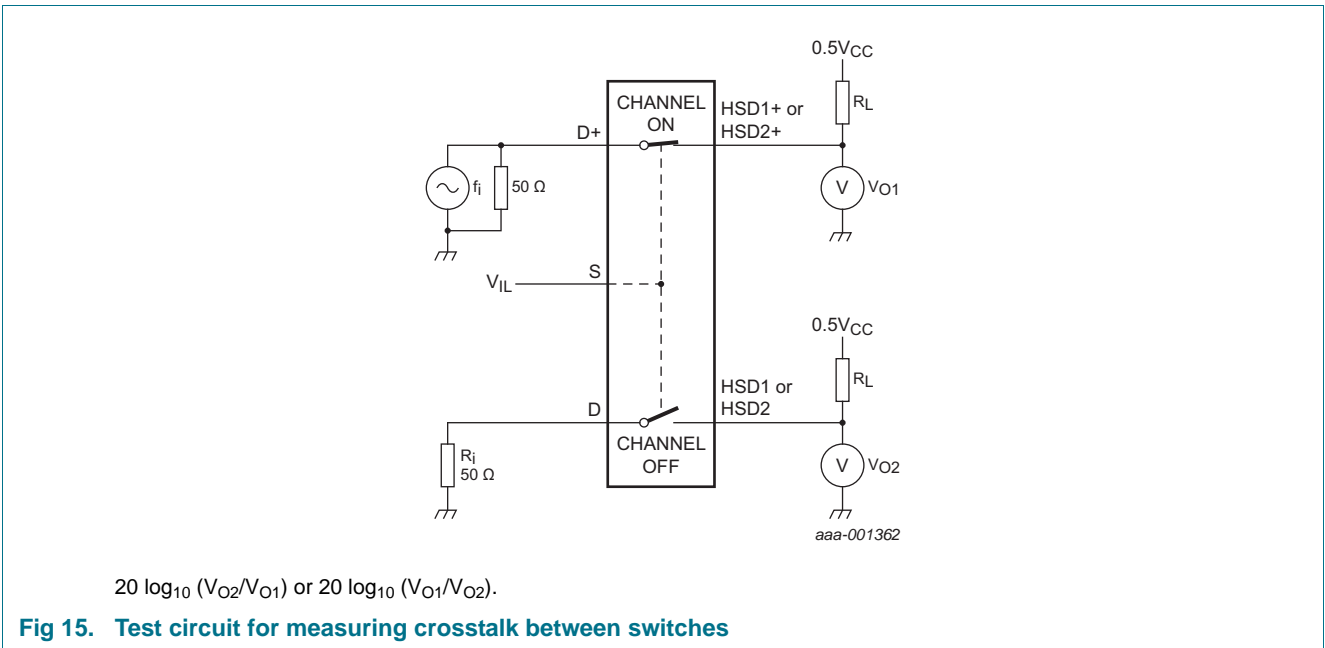
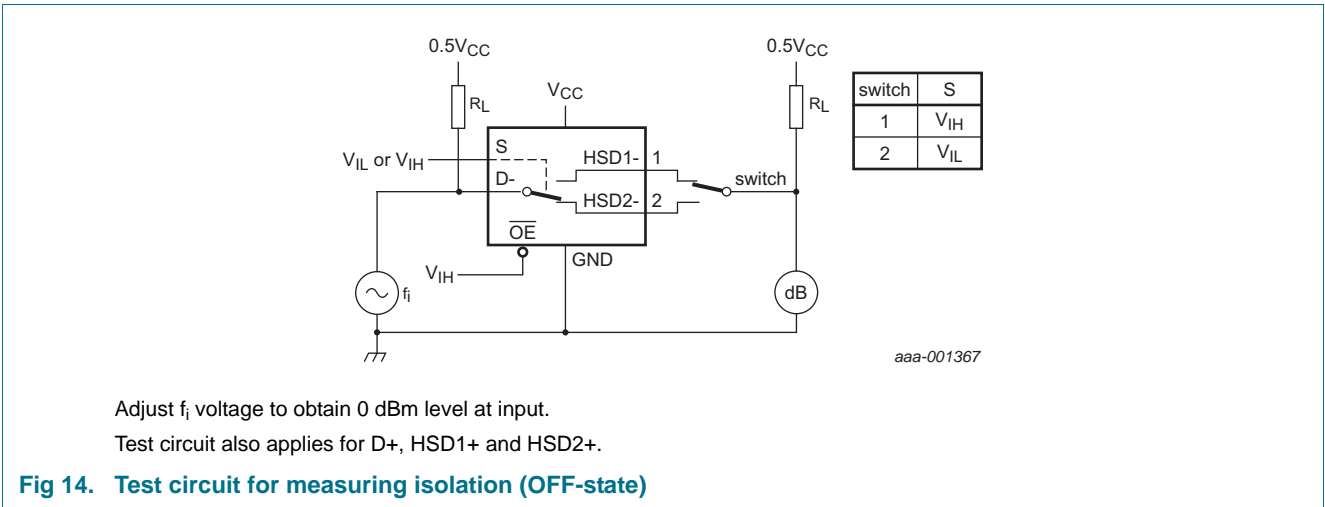
### 12.3 Test circuits

switch	S
1	V <sub>IL</sub>
2	V <sub>IH</sub>

aaa-001360

Adjust f<sub>i</sub> voltage to obtain 0 dBm level at output. Increase f<sub>i</sub> frequency until dB meter reads -3 dB.  
 Test circuit also applies for D+, HSD1+ and HSD2+.

**Fig 13. Test circuit for measuring the frequency response when channel is in ON-state**



### 13. Package outline

**XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm**

SOT1160-1

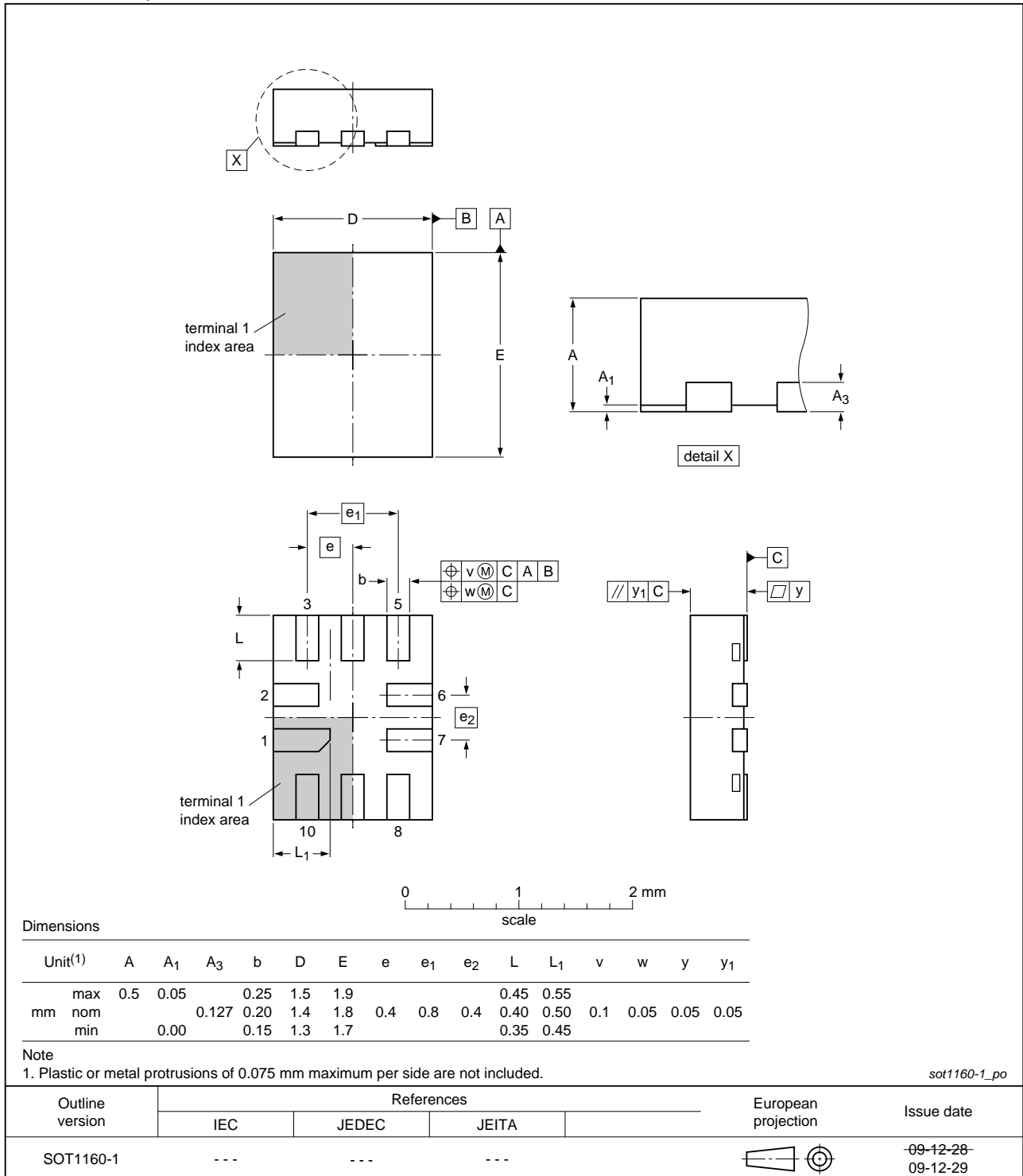


Fig 16. Package outline SOT1160-1 (XQFN10)

XQFN10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm

SOT1337-1

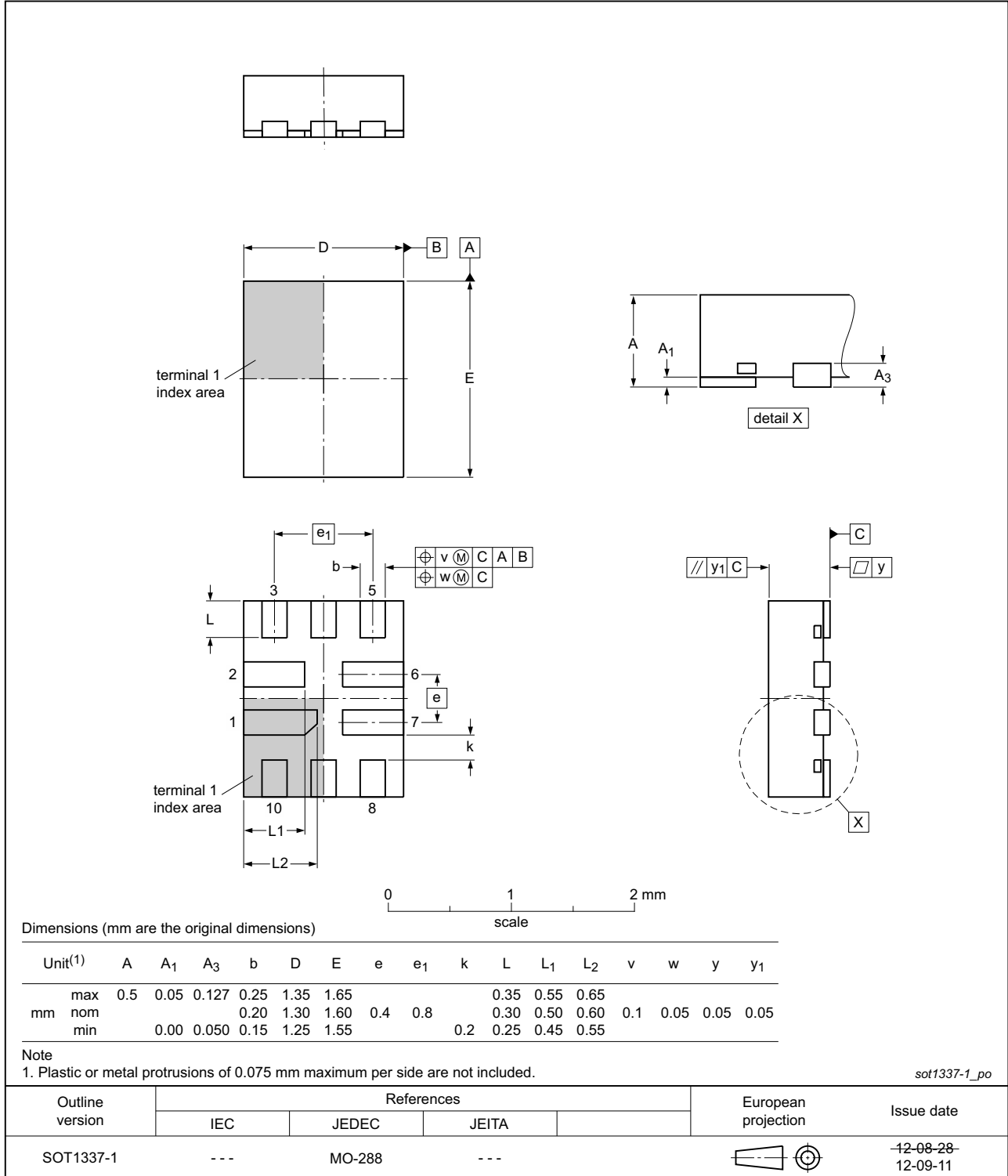


Fig 17. Package outline SOT1337-1 (XQFN10)

X2QFN10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.6 x 1.3 x 0.33 mm

SOT1430-1

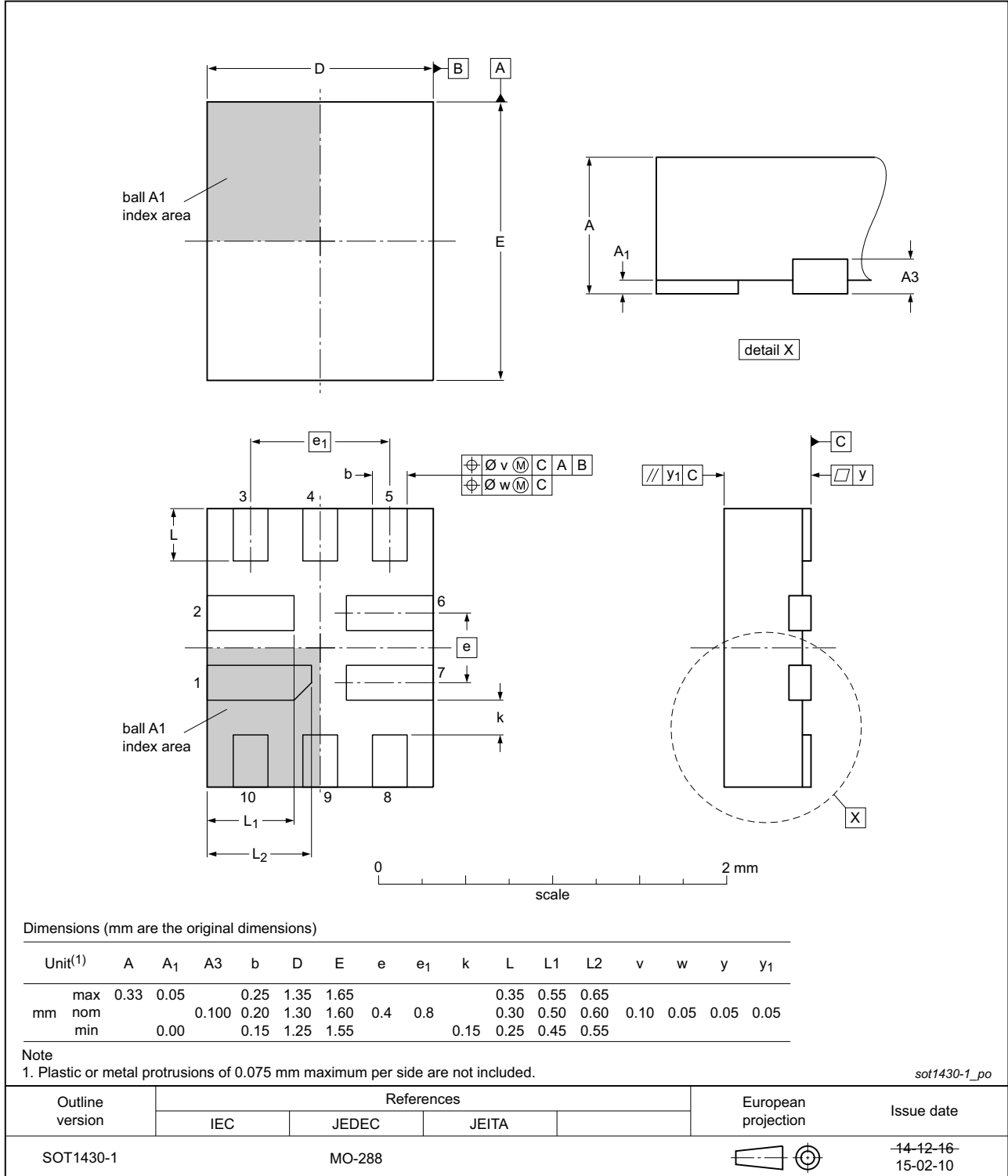


Fig 18. Package outline X2QFN10



## 14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LCD	Liquid Crystal Display
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3DV42 v.3.1	20161020	Product data sheet	-	NX3DV42 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Added NX3DV42GU33</li> <li>• Removed NX3DV42GM</li> </ul>			
NX3DV42 v.3	20130213	Product data sheet	-	NX3DV42 v.2
Modifications:	<ul style="list-style-type: none"> <li>• Values added for <math>T_{amb} = +125\text{ °C}</math> throughout the data sheet.</li> <li>• Type number NX3DV42GU10 added (<a href="#">Table 1</a>).</li> <li>• Marking code for type number NX3DV42GU10 added (<a href="#">Table 2</a>).</li> <li>• Package outline drawing SOT1337-1 added (<a href="#">Figure 17</a>).</li> </ul>			
NX3DV42 v.2	20120618	Product data sheet	-	NX3DV42 v.1
Modifications:	<ul style="list-style-type: none"> <li>• Package outline drawing SOT1049-2 changed to SOT1049-3 (<a href="#">Figure 17</a>).</li> </ul>			
NX3DV42 v.1	20120103	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А