High Performance Regulators for PCs

Nch FET Ultra LDO Controllers for PC Chipsets

BD3504FVM,BD3500FVM,BD3501FVM,BD3502FVM

No.10030EAT29

●Description

The BD3500/01/02/04FVM is an ultra-low dropout linear regulator controller for chipset that can achieve ultra-low voltage input to ultra-low voltage output. By using N-MOSFET for external power transistor, the controller can be used at ultra-low I/O voltage difference up to voltage difference generated by ON resistance. In addition, because best suited power transistor can be chosen in accord with the output current, downsizing and cost reduction of the set can be achieved. Because by reducing the I/O voltage difference, large current output is achieved and conversion loss can be reduced, switching power supply can be replaced. BD3500/01/02/04FVM does not need any choke coil, diode for rectification and power transistor which are required for switching power supply, total cost of the set can be reduced and compact size can be achieved for the set. Using external resistors, optional output from 0.65V to 2.5V can be set. In addition, since voltage output start-up time can be adjusted by using the NRCS terminal, it is possible to flexibly meet the power supply sequence of the set.

●Features

1) Reduced rush current by NRCS
2) Built-in driver for external Nch h transistor
3) Adoption of MSOP8 package: 2.9 x 4.0 x 0.9 (mm)
4) Built-in timer latch short protection circuit
5) Built-in low input maloperation prevention circuit
6) Output voltage variable type
7) Built-in overheat protection circuit

●Applications

Mobile PC, desktop PC, digital home appliances

●Line up matrix

Parameter	BD3500FVM	BD3501FVM	BD3502FVM	BD3504FVM
Output Voltage	1.8V (Fix)	1.5V (Fix)	1.2V (Fix)	Variable(0.65～2.5V)
NRCS (Soft start)	○ (Independent Setting)	○ (Independent Setting)	○ (Independent Setting)	○ (Same Timer Latch)
Timer latch short protection circuit	○ (Independent Setting)	○ (Independent Setting)	○ (Independent Setting)	○ (Same NRCS)
VIN UVLO	Hysterisis	Hysterisis	Hysterisis	Detected at start-up only (set by external resistor)
External FET GATE Drive Current	+1/-3mA	+1/-3mA	+1/-3mA	+3/-3mA

●Absolute maximum ratings (Ta=25℃)

◎BD3500/01/02FVM

Parameter	Symbol	Ratings	Unit
Input Voltage	VCC	7 *1	V
Drain Voltage (VIN)	VIN	7	V
Enable Input Voltage	Ven	7	V
Power Dissipation	Pd	437.5 *2	mW
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 However, not exceeding Pd.
*2 Pd derating at 3.5mW/℃ for temperature above Ta=25℃

◎BD3504FVM

Parameter	Symbol	Ratings	Unit
Supply Voltage	VCC	7 *3	V
Drain Voltage	VD	7	V
Enable Input Voltage	Ven	7	V
Power dissipation	Pd	437.5 *4	mW
Operating temperature range	Topr	-10～+100	℃
Storage temperature range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*3 However, not exceeding Pd.
*4 Pd derating at 3.5mW/℃ for temperature above Ta=25℃

●Recommended operating conditions

◎BD3500/01/02FVM

Parameter	Symbol	Ratings		Unit
		MIN	MAX	
Supply Voltage	VCC	4.5	5.5	V
Drain Voltage(VIN)	VIN	Vo×1.15	5.5	V
Enable Input Voltage	Ven	-0.3	5.5	V
Capacitor on NRCS Terminal	CNRCS	0.001	1	μF
Capacitor on SCP Terminal	CSCP	0.001	1	μF

★ No radiation-resistant design is adopted for the present product.

◎BD3504FVM

Parameter	Symbol	Ratings		Unit
		MIN	MAX	
Supply Voltage	VCC	4.5	5.5	V
Drain Voltage	VD	0.65	5.5	V
Enable Input Voltage	Ven	-0.3	5.5	V
Capacitor in NRCS pin	CNRCS	0.001	1	μF
Output Voltage	VOUT	0.65	2.5	V

★ No radiation-resistant design is adopted for the present product.

●Electrical characteristics (unless otherwise noted, Ta=25℃ VCC=5V Vin=3.3V Ven=3V)

◎BD3500FVM/BD3501FVM/BD3502FVM

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Bias Current	ICC	-	0.8	1.6	mA	
Shut Down Mode Current	IST	-	0	10	μA	Ven=0V
Output Voltage 1 (BD3500FVM)	Vo1	1.782	1.800	1.818	V	Io=50mA
Output Voltage 1 (BD3501FVM)	Vo1	1.485	1.500	1.515	V	Io=50mA
Output Voltage 1 (BD3502FVM)	Vo1	1.188	1.200	1.212	V	Io=50mA
Output Voltage 2 (BD3500FVM)	Vo2	1.746	1.800	1.854	V	Vcc=4.5V to 5.5V ,Io=0 to 3A Ta=-10℃ to 100℃(※)
Output Voltage 2 (BD3501FVM)	Vo2	1.455	1.500	1.545	V	Vcc=4.5V to 5.5V ,Io=0 to 3A Ta=-10℃ to 100℃(※)
Output Voltage 2 (BD3502FVM)	Vo2	1.164	1.200	1.236	V	Vcc=4.5V to 5.5V ,Io=0 to 3A Ta=-10℃ to 100℃(※)
Line Regulation	Reg.l	-	0.1	0.5	%/V	VCC=4.5V to 5.5V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 3A
[Enable]						
High Level Enable Input Voltage	Enhi	2	-	Vcc	V	
Low Level Enable Input Voltage	Enlow	-0.3	-	0.8	V	
Enable Pin Input Current	Ien	-	7	10	μA	Ven=3V
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	μA	Vnrcs=0.5V,VCC=4.5V to 5.5V Ta=-10℃ to 100℃ (※)
NRCS Standby Voltage	Vnrcs	-	0	50	mV	Ven=0V
[Voltage Feed Back]						
VFB Input Bias Current	IFB	-	0.7	1.2	mA	Ven=3V
VFB Standby Current	FBSTB	150	-	-	mA	Ven=0V,VFB=1V
[Output MOSFET Driver]						
MOSFET Driver Source Current	IGSO	0.5	1	1.5	mA	VFB=Vo-0.1V,G=Vo+1V
MOSFET Driver Sink Current	IGSI	2	3	4	mA	VFB=Vo+0.1V,G=Vo+1V
[UVLO]						
VCC UVLO	VccUVLO	4.2	4.35	4.5	V	Vcc:Sweep up
VCC UVLO Hysteresis	Vcchys	100	160	220	mV	Vcc:Sweep down
VIN UVLO	VINUVLO	Vo×1.05	Vo×1.1	Vo×1.15	V	VIN:Sweep up
VIN UVLO Hysteresis	VINhys	100	160	220	mV	VIN:Sweep down
[SCP]						
SCP Charge Current	Iscpch	14	20	26	μA	VSCP=0.5V,VCC=4.5V to 5.5V Ta=-10℃ to 100℃ (※)
SCP Discharge Current	IscpDi	0.5	-	-	mA	VSCP=0.5V
SCP Threshold Voltage	Vscpth	1.2	1.3	1.4	V	
Short Detect Voltage	Vscp	Vo×0.6	Vo×0.7	Vo×0.8	V	
SCP Stand-by Voltage	VSTB	-	0	50	mV	

(※) Design Guarantee

●Electrical characteristics (unless otherwise noted, Ta=25℃ VCC=5V VIN=3.3V Ven=3V. R1=R1'=∞Ω, R2=R2'=0Ω)

◎BD3504FVM

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Bias Current	ICC	-	0.85	1.7	mA	
Shut Down Mode Current	IST	-	0	10	μA	Ven=0V
Feed Back Voltage 1	VFB1	0.643	0.650	0.657	V	Io=50mA
Feed Back Voltage 2	VFB2	0.630	0.650	0.670	V	Vcc=4.5V to 5.5V , Ta=-10℃ to 100℃(※)
Output Voltage	Vo	-	1.20	-	V	R1=R1'=3.9kΩ, R2=R2'=3.3KΩ
Line Regulation	Reg.l	-	0.1	0.5	%/V	VCC=4.5V to 5.5V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 3A
[Enable]						
High Level Enable Input Voltage	Enhi	2	-	Vcc	V	
Low Level Enable Input Voltage	Enlow	-0.3	-	0.8	V	
Enable pin Input Current	Ien	-	7	10	μA	Ven=3V
[Voltage Feed Back]						
VFB Input Bias Current	IFB	-	80	-	nA	
[Source Voltage]						
VS Input Bias Current	ISBIAS	-	1.2	2.4	mA	
VS Standby Current	ISSTB	150	-	-	mA	VS=1V Ven=0V
[Output MOSFET Driver]						
MOSFET Driver Source Current	IGSO	2	3	4	mA	VFB=0.6V,VGATE=2.5V
MOSFET Driver Sink Current	IGSI	2	3	4	mA	VFB=0.7V,VGATE=2.5V
[UVLO]						
VCC UVLO	VccUVLO	4.20	4.35	4.50	V	Vcc:Sweep up
VCC UVLO Hysterisis	Vcchys	100	160	220	mV	Vcc:Sweep down
VD UVLO	VDUVLO	Vo×0.6	Vo×0.7	Vo×0.8	V	VD:Sweep up
[Drain Voltage Sensing]						
VD Input bias Current	Ivd	-	0	-	nA	
[NRCS/SCP]						
NRCS Charge Current	Inrcs	14	20	26	μA	VNRCS=0.5V
SCP Charge Current	Iscpch	14	20	26	μA	VNRCS=0.5V
SCP Discharge Current	IscpDi	0.3	-	-	mA	VNRCS=0.5V
SCP Threshold Voltage	Vscp	1.2	1.3	1.4	V	
Short Detect Voltage	Voscp	Vo×0.3	Vo×0.35	Vo×0.4	V	
NRCS Stand-by Voltage	VSTB	-	-	50	mV	

(※) Design Guarantee

●Reference Data

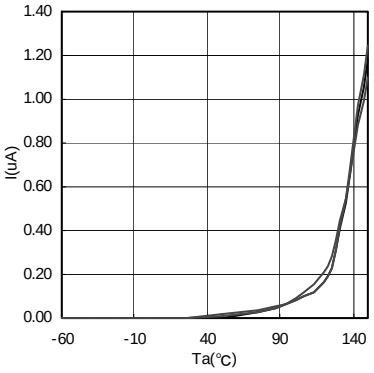


Fig.1 Ta-ISTB

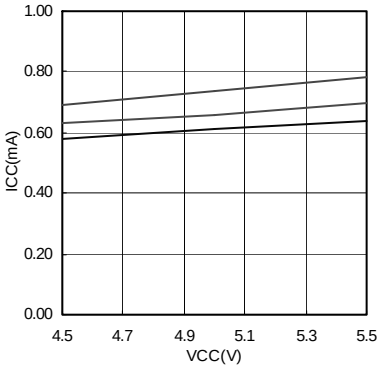


Fig.2 ICC-VCC

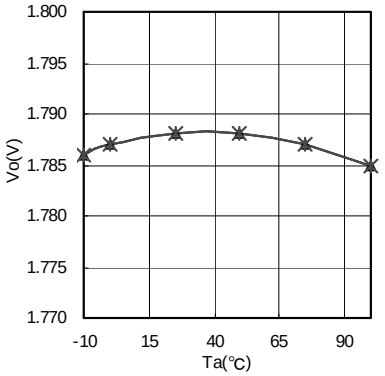


Fig.3 Ta-Vo

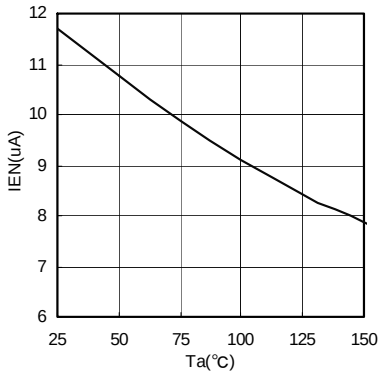


Fig.4 Ta-IEN

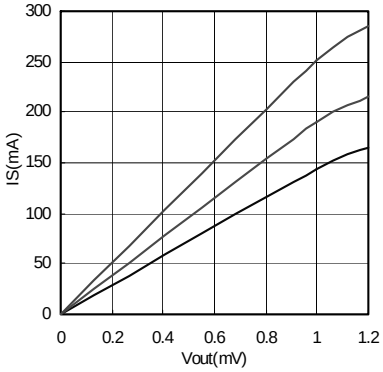


Fig.5 VS Discharge Current

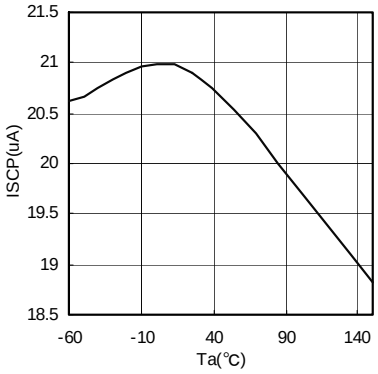


Fig.6 Ta-ISCP

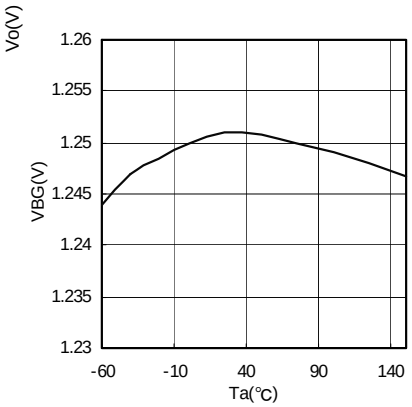


Fig.7 Ta-Vo

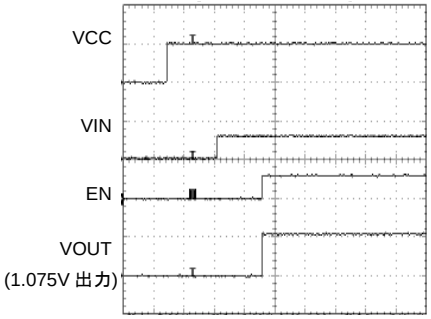


Fig.8 Input Sequence 1
EN

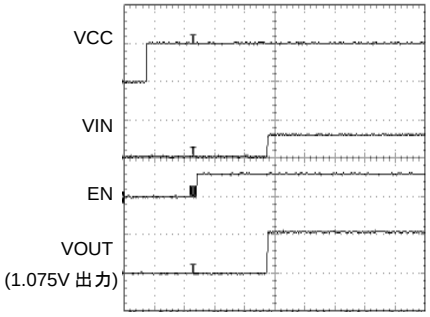


Fig 9. Input Sequence 2
VIN

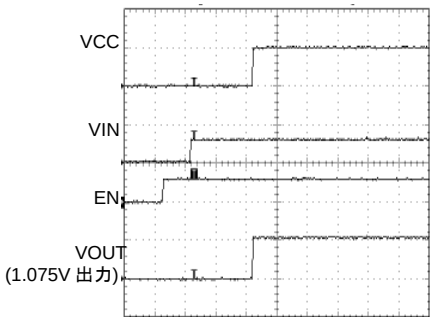


Fig.10 Input Sequence 3
Vcc

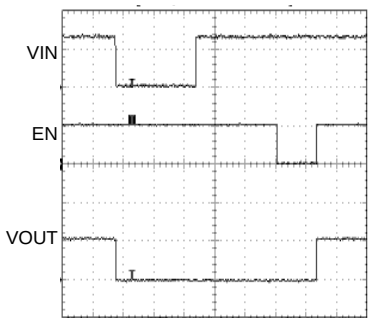


Fig.11 Input Sequence 4
(Only BD3504FVM)

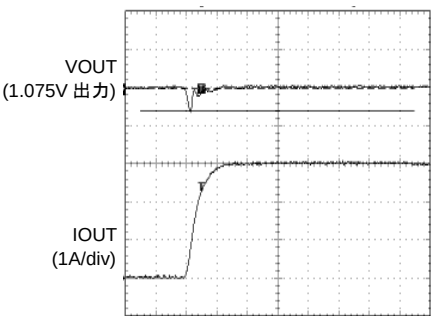


Fig.12 Transient Response
0→3A(0.6A/μs) ΔV=30mV

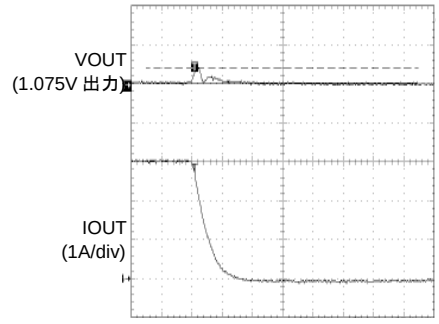


Fig.13 Transient Response
3→0A(0.6A/μs) ΔV=20mV

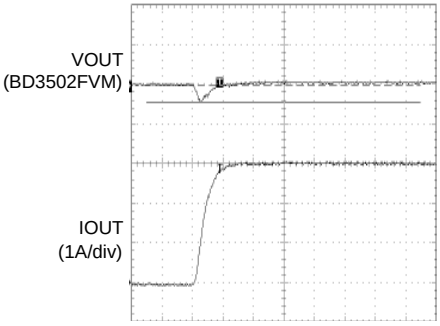


Fig.14 Transient Response
0→3A(0.6A/μs) ΔV=21mV

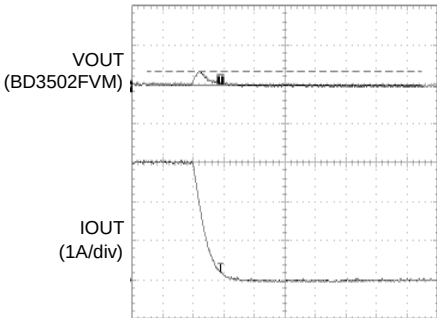


Fig.15 Transient Response
3→0A(0.6A/μs) ΔV=17mV

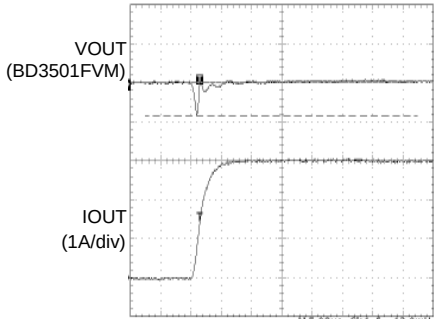


Fig.16 Transient Response
0→3A(0.6A/μs) ΔV=42mV

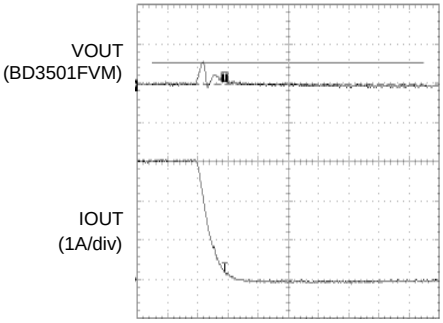


Fig.17 Transient Response
3→0A(0.6A/μs) ΔV=27mV

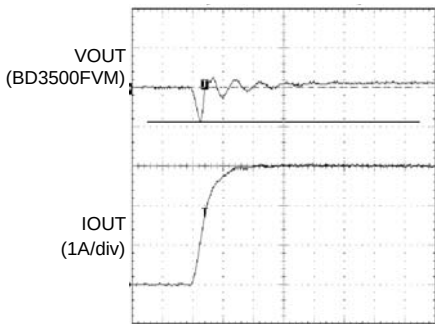


Fig.18 Transient Response
0→3A(0.6A/μs) ΔV=44mV

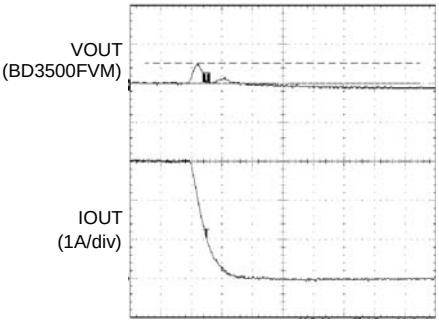


Fig.19 Transient Response
3→0A(0.6A/μs) ΔV=26mV

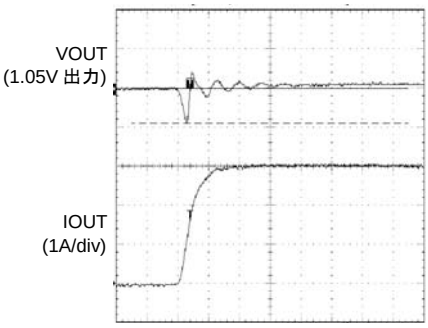


Fig.20 Transient Response
0→3A(0.6A/μs) ΔV=44mV

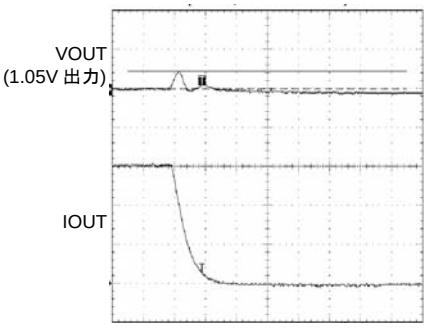
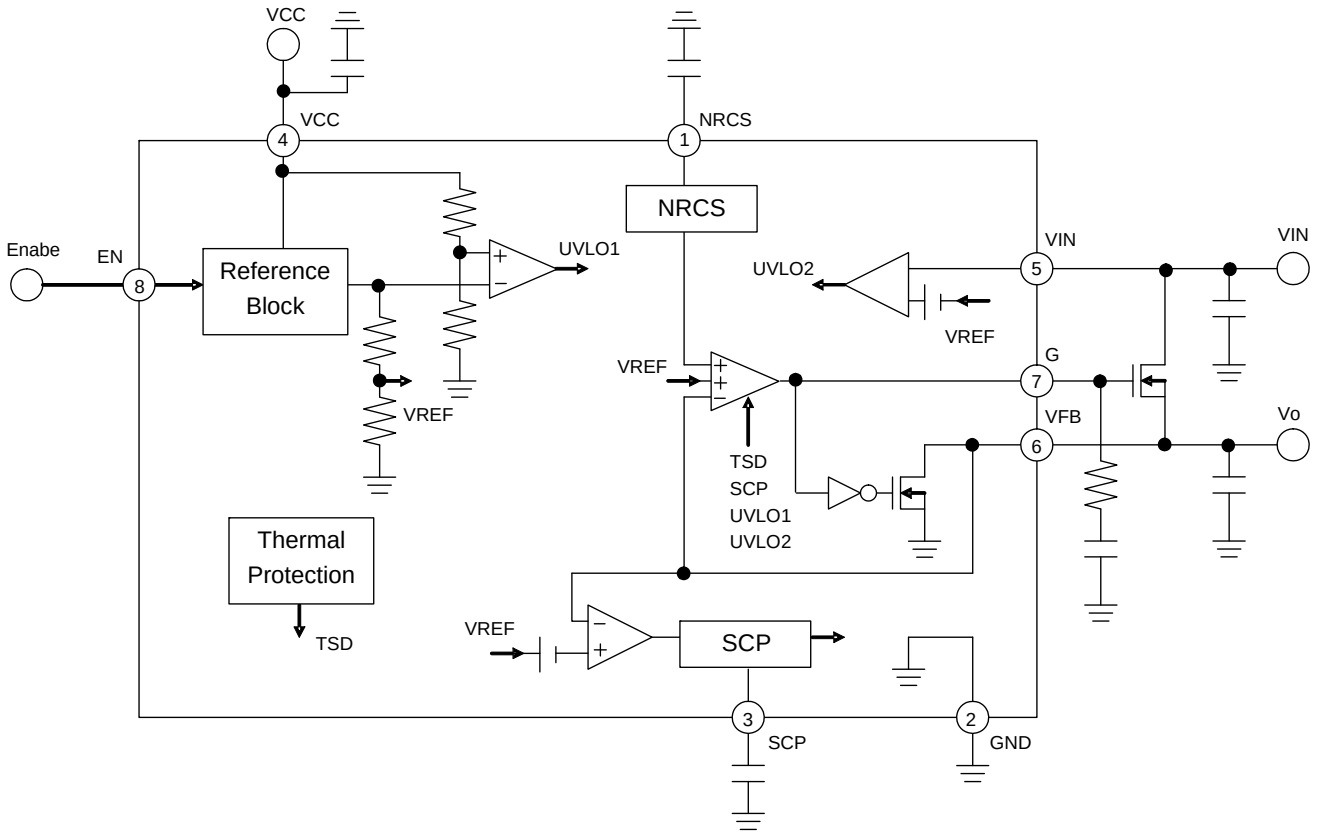


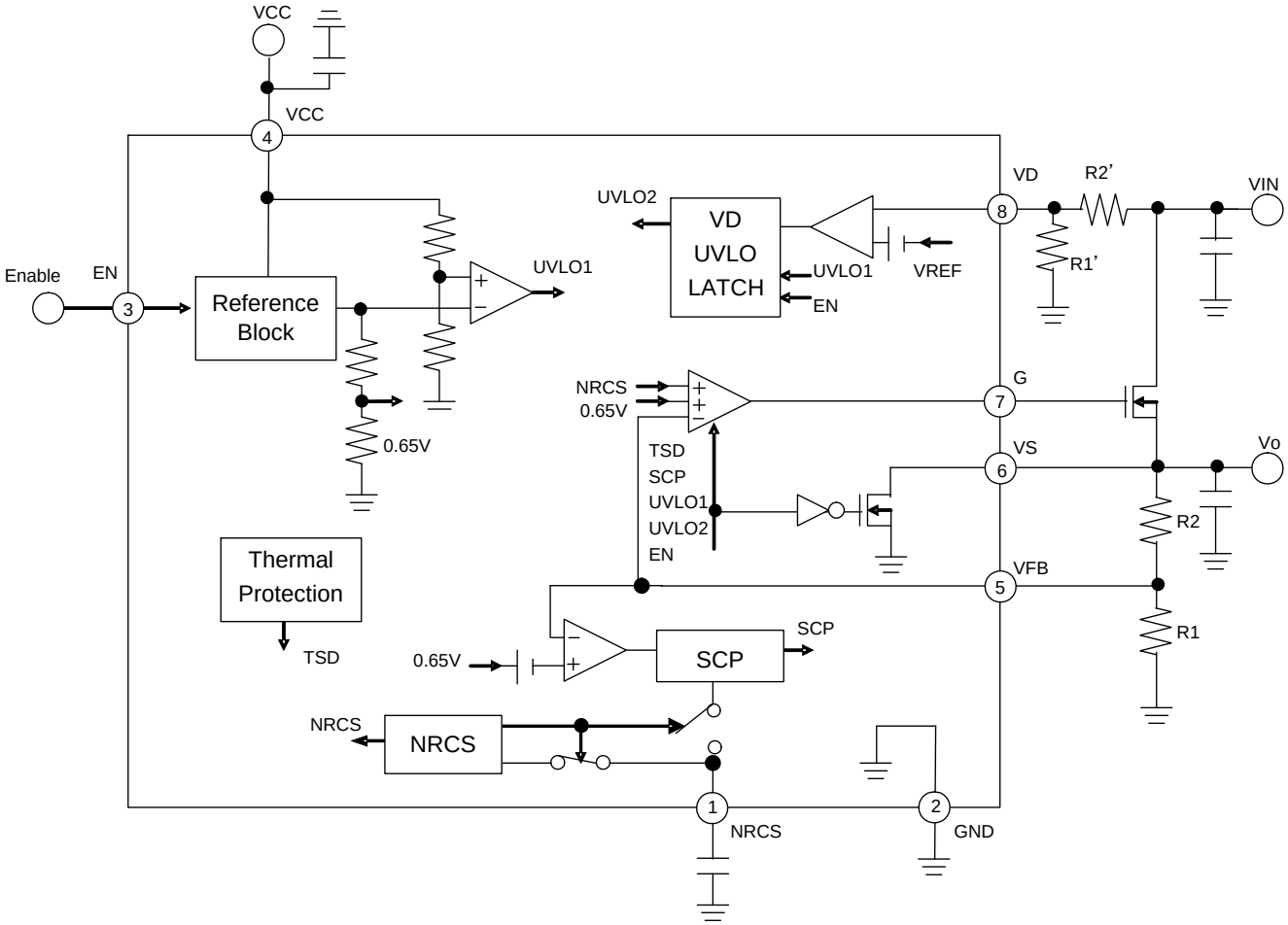
Fig.21 Transient Response
3→0A(0.6A/μs) ΔV=23mV

●Block Diagram

◎BD3500FVM/BD3501FVM/BD3502FVM



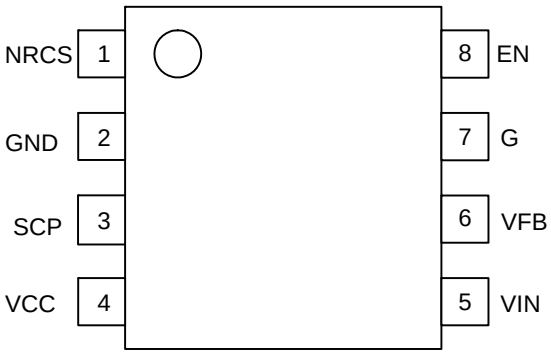
◎BD3504FVM



●Pin Configration and Pin Function

◎BD3500FVM/BD3501FVM/BD3502FVM

○Pin Configration

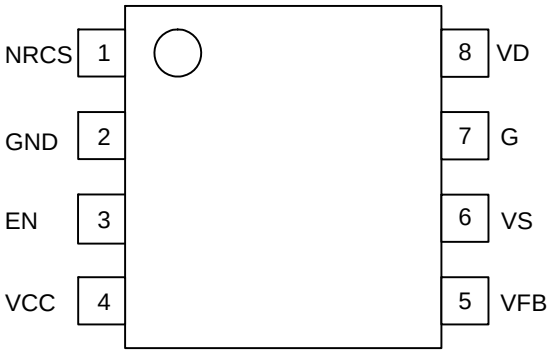


○Pin Function

Pin No.	Pin Name	PIN FUNCTION
1	NRCS	(Non Rush Current on Start up) time setup
2	GND	Ground pin
3	SCP	Timer latch setup for Short Circuit Protection
4	VCC	Power Source
5	VIN	Drain Voltage Sense
6	VFB	Output Voltage Feedback
7	G	MOSFET Driver Output
8	EN	Enable

◎BD3504FVM

○Pin Configration



○Pin Function

Pin No.	Pin Name	PIN FUNCTION
1	NRCS	NRCS (Non Rush Current on Start up) time setup. Timer latch setup for Short Circuit Protection operating time set up Pin.
2	GND	Ground Pin
3	EN	Enable Pin
4	VCC	Power Source
5	VFB	Output Voltage Feedback
6	VS	Source Voltage Pin
7	G	MOSFET Driver Output
8	VD	Drain Voltage Sense

●Pin Function Descriptions

・VCC

BD3500/01/02/04FVM has an independent power input pin for an internal circuit operation of IC. This is used for bias of IC internal circuit and external N-MOSFET. The voltage used of VCC terminal is 5.0V and maximum current is 1.7 mA. It is recommended to connect a bypass capacitor of 0.1 µF or so to VCC pin.

・EN

With an input of 2.0 volts or higher, the EN terminal turns to “High” level and VOUT is outputted. At 0.8V or lower, it detects “Low” level and VOUT is turned OFF and simultaneously, the discharge circuit inside the VS terminal is activated and lowers output voltage (150 mA (Min) when VFB//VS=1V and VEN=0V).

・VIN(BD3500/01/02FVM)

The VIN terminal is a drain voltage detection terminal of external N-MOSFET. In the event that the VIN terminal is lower than 1.1 times the output set voltage, output is turned OFF to prevent low-input maloperation.

・VD(BD3504FVM only)

The VD terminal is a drain voltage detection terminal of external N-MOSFET. In the event that drain voltage (VIN) is low, output voltage is turned OFF to prevent low-input maloperation. The reset voltage (VDUVLO) of drain voltage low-input maloperation prevention circuit is determined by the following equation:

$$VDUVLO=VFB\times 0.7\times\left(\frac{R1'+R2}{R1'}\right)$$

In the event that the maloperation prevention set resistance at the time of low-input drain voltage is set to a resistance value same as output voltage set resistor (R1 = R1', R2 = R2'), low-input maloperation prevention (UVLO) is reset when drain voltage (VIN) reaches 70% of the output voltage. UVLO detects only at the startup of the EN terminal.

・VFB(BD3504FVM only)

The VFB terminal is a terminal to decide output voltage and is determined by the following equation:

$$VOUT=VFB\times\left(\frac{R1'+R2}{R1'}\right)$$

VFB is controlled to achieve 0.65 V (typ.).

・NRCS terminal

he NRCS terminal is a constant current output terminal, and operates as

- Soft-Start ... during start-up
- SCP-Delay ... after start-up (BD3504FVM only).

How to set Soft-Start of NRCS terminal

The output voltage startup time (TNRCS) is determined by the time when the NRCS terminal reaches VFB (0.65V). During start-up, the NRCS terminal serves as a constant current source (INRCS) of 20 µA (Typ.) output, and charges capacitor (CNRCS) externally connected. By changing over to internal reference voltage (0.65V) when the NRCS terminal reaches 0.65V, output voltage (VOUT) is fixed.

How to set NRCS terminal short protection Delay (BD3504FVM only)

BD3504FVM has short protection (SCP) activated when output voltage becomes VOUT x 0.35 (typ.) or lower. The time when short protection is activated until latching takes place (TSCP) is determined by the following equation:

Tscp = CNRCS × Voscp ÷ Iscp

When short protection is activated, the NRCS terminal provides 20 µA (typ.) constant current output (Iscp), and charges the capacitor (CNRCS) externally connected. When the NRCS terminal reaches 1.3V (Voscp), latch operation is carried out and output voltage is turned OFF.

・SCP(BD3500/01/02FVM)

BD3500/01/02FVM has short protection (SCP) activated when output becomes 70% or lower than the set voltage. The time when short protection is activated until latching takes place (T_{SCP}) is determined by the following equation:

Tscp = CNRCS × Voscp ÷ Iscp

When short protection is activated, the NRCS terminal provides 20 µA (typ.) constant current output (Iscp), and charges the capacitor (CNRCS) externally connected. When the NRCS terminal reaches 1.3V (Voscp), latch operation is carried out and output voltage is turned OFF.

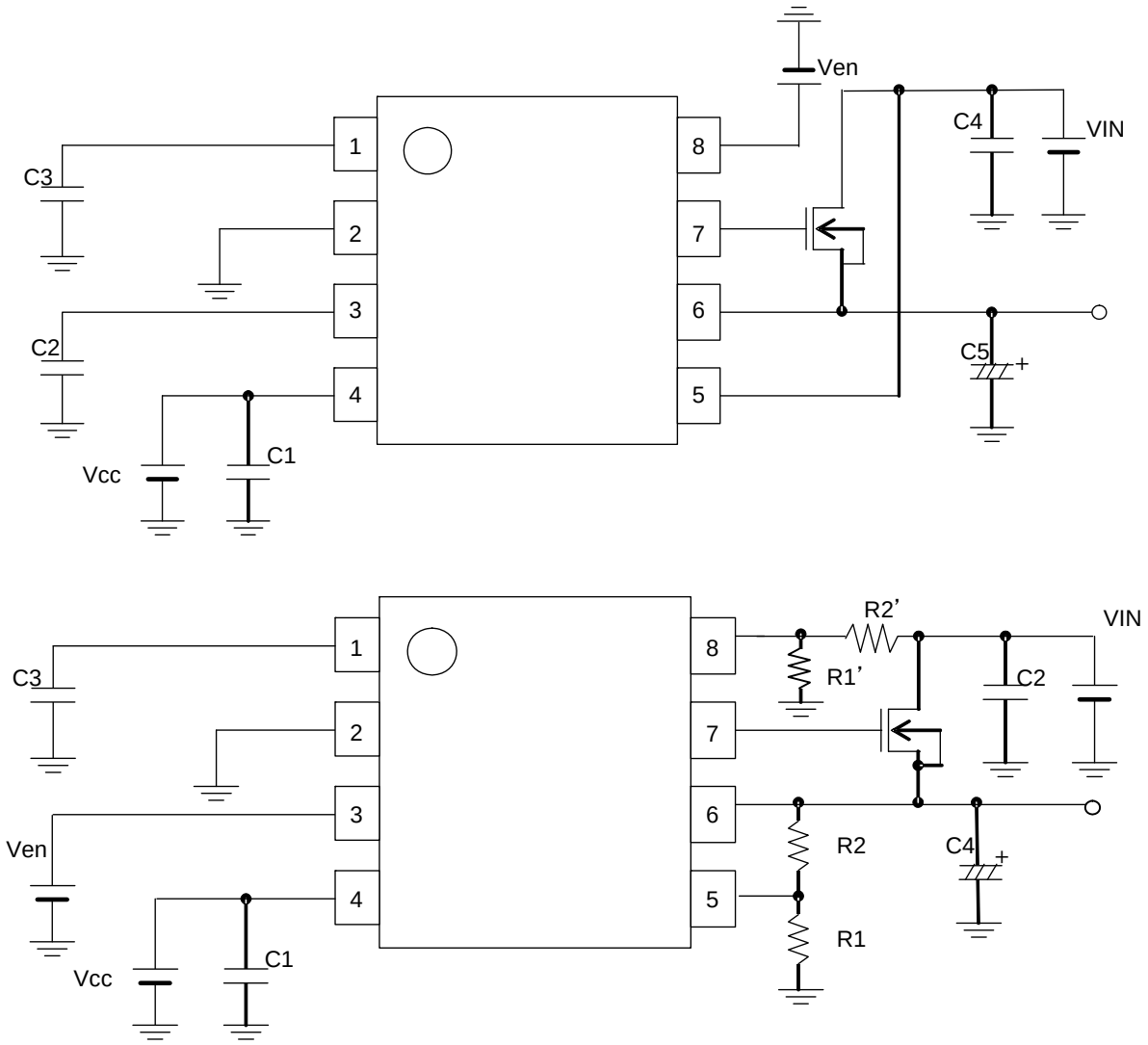
・VFB//VS (BD3500FVM/BD3501FVM/BD3502FVM//BD3504FVM)

VFB//VS terminal is a source voltage detection terminal of external N-MOSFET. VFB//VS terminal has the internal discharge circuit activated to lower output voltage when EN becomes a Low level or various protection circuits (TSD, SCP, UVLO) are activated.

・G

G terminal is a gate drive terminal of external N-MOSFET. Because the output voltage range of G terminal is up to 5V (VCC), it is necessary to use N-MOSFET whose threshold is lower than “5V-VOUT.” In addition, by incorporating a RC snubber circuit to the G terminal, phase allowance of loop gain can be increased and the terminal can accommodate ceramic capacitors.

●Application circuit



●Directions for pattern layout of PCB

- Because a VIN input capacitor causes impedance to drop, mount it as close to the VIN terminal as possible and use thick wiring patterns. In the event that it causes the wire to come in contact with the inner-layer ground plane, use a plurality of through holes.

- Because the NRCS terminal is analog I/O, take care to noise. In particular, high-frequency noise of GND may cause IC maloperation through capacitors. It is recommended to connect GND of NRCS capacitor to IC GND terminal at one point.

- The VFB terminal is an output voltage sense line. Effects of wiring impedance can be ignored by sensing the output voltage from the load side, but increased sense wiring causes VFB to be susceptible to noise, to which care must be taken.

- Because the GND terminal is GND to be used in analog circuit inside BD3501/02/04FVM, connect it at one point to inner-layer GND of substrate by as short pattern as possible. Arrange a bypass capacitor across VCC and GND as close as possible so that a loop can be minimized.

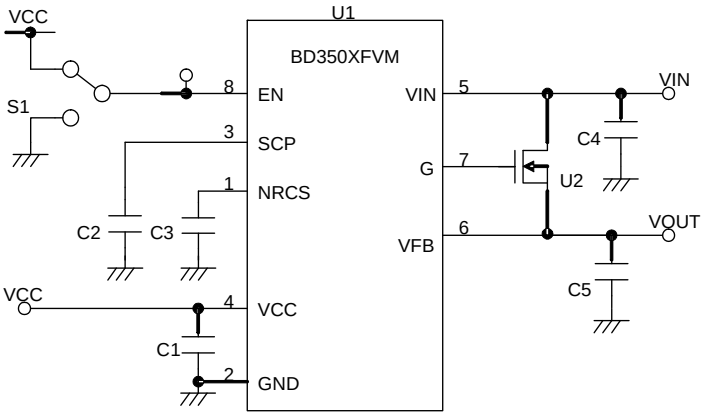
- The G terminal is a terminal for gate drive. If long wiring is inevitable, increase the pattern width and lower impedance.

- Heat generated in the output transistor can be calculated by:
  (VIN - VOUT) × Io(Max)
  Design heat generation not to exceed the guarantee temperature of transistor.

- Connect the output capacitor with thick short wiring so that the impedance is lowered. Connect capacitor GND to inner-layer GND plane by a plurality of through holes.

●Evaluation Board (BD3500/01/02FVM)

■BD350XFVM Evaluation Board Circuit



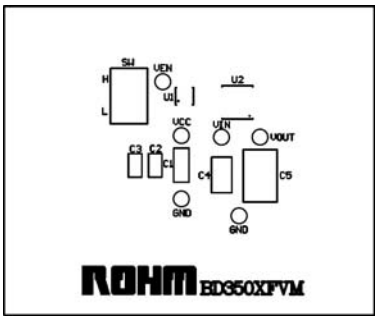
■BD350XFVM Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3500/01/02FVM
U2	NMOS	ROHM	RTW060N03
C1	1µF	MURATA	GRM18 series
C2	0.01µF	MURATA	GRM18 series

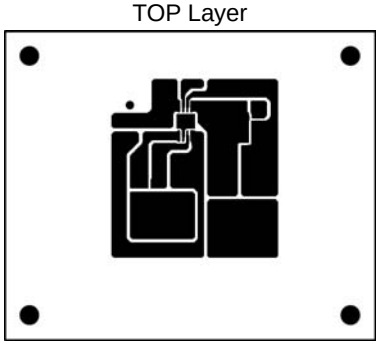
Part No	Value	Company	Parts Name
C3	0.01µF	MURATA	GRM18 series
C4	10µF	MURATA	GRM21 series
C5	220µF	SANYO,etc	2R5TPE220MF

■ BD350XFVM Evaluation Board Layout

Silk Screen



TOP Layer



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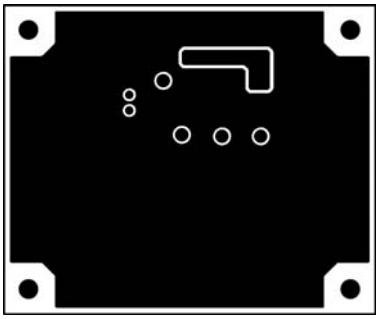
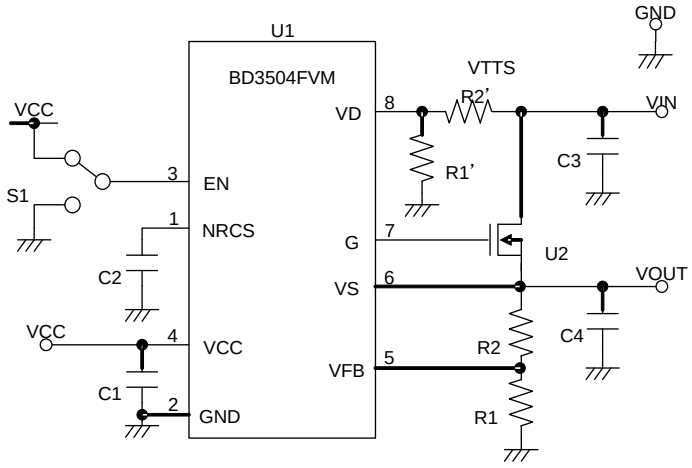


●Evaluation Board (BD3504FVM)

■BD3504FVM Evaluation Board Circuit



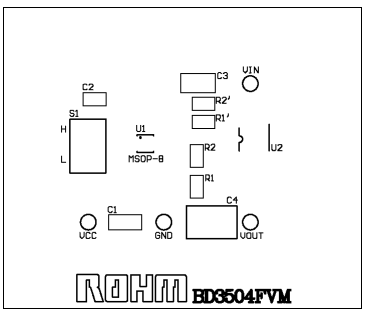
■BD3504FVM Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD35304FVM
U2	NMOS	ROHM	RTW060N03
R1	3.9K	ROHM	MCR03EZPF3901
R1'	3.3K	ROHM	MCR03EZPF3301
R2	3.9K	ROHM	MCR03EZPF3901

Part No	Value	Company	Parts Name
R2'	3.3K	ROHM	MCR03EZPF3301
C1	1µF	MURATA	GRM18 series
C2	0.01µF	MURATA	GRM18 series
C3	10µF	MURATA	GRM21 series
C4	220µF	SANYO,etc	2R5TPE220MF

■ BD3504FVM Evaluation Board Layout

Silk Screen



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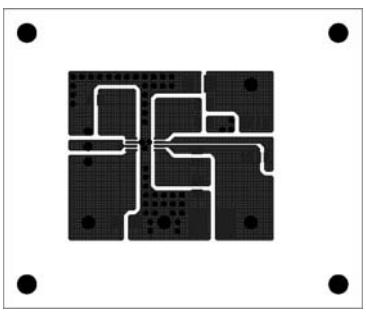
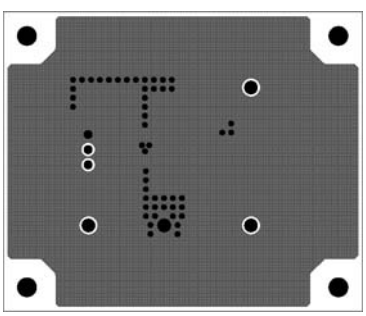
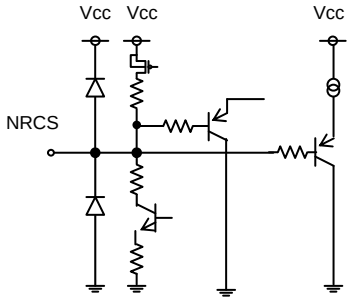


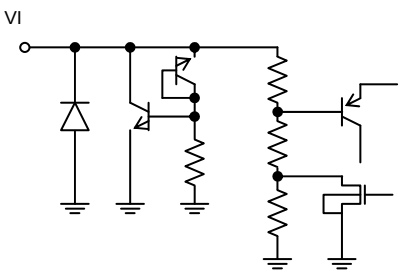
Bottom Layer

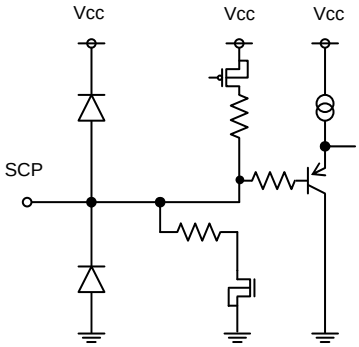


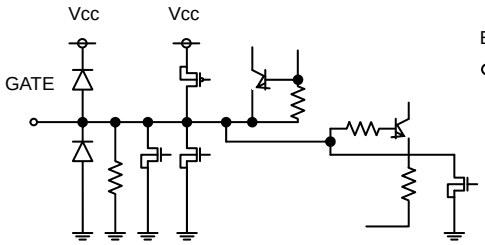
●I/O EQUIVALENCE CIRCUIT

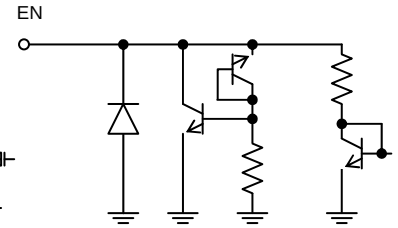
◎BD3500FVM/BD3501FVM/BD3502FVM

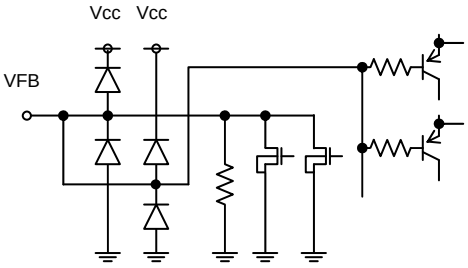




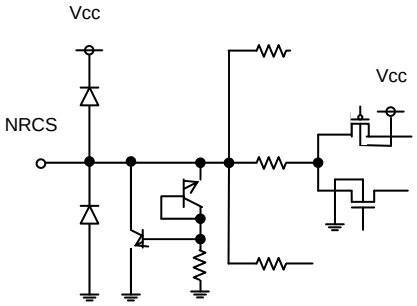


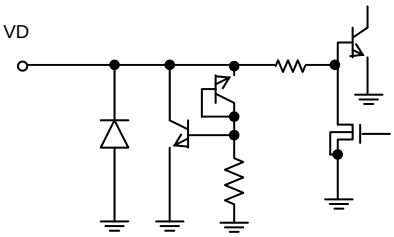


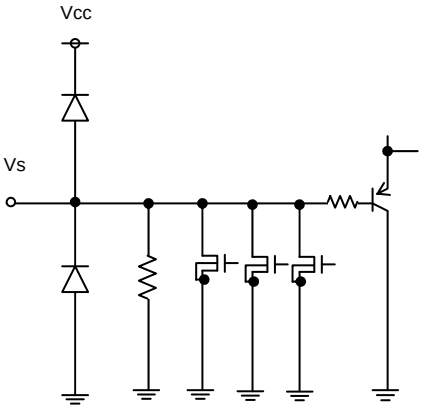


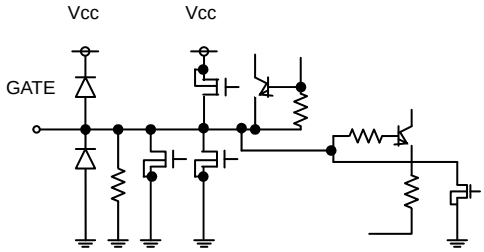


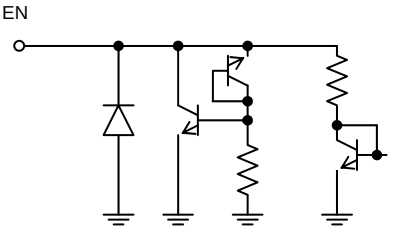
◎BD3504FVM

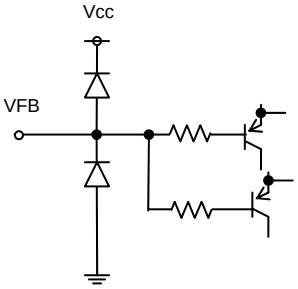








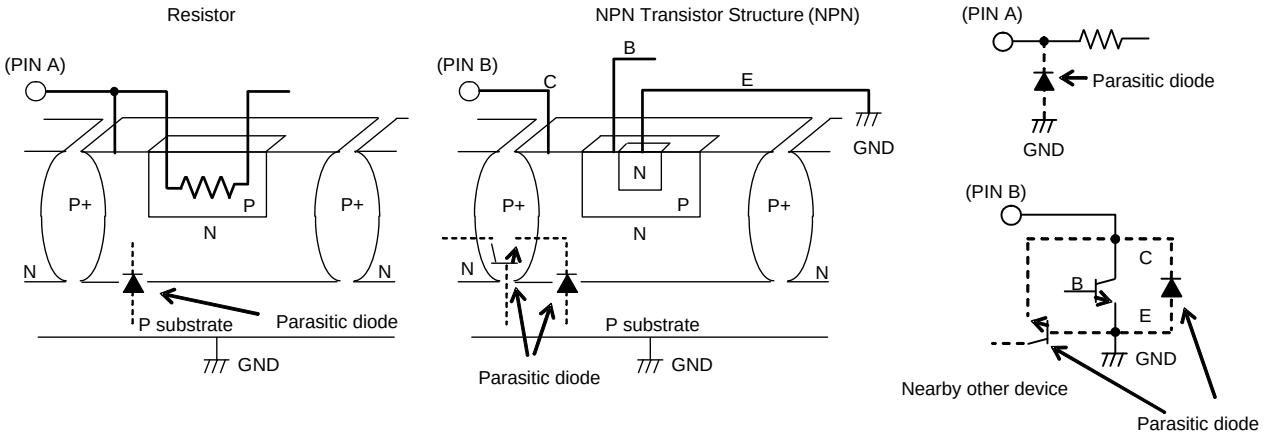




●Notes for use

1. Absolute maximum ratings
   For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.
2. GND potential
   Bring the GND terminal potential to the minimum potential in any operating condition.
3. Thermal design
   Consider allowable loss (Pd) under actual working condition and carry out thermal design with sufficient margin provided.
4. Terminal-to-terminal short-circuit and erroneous mounting
   When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.
5. Operation in strong electromagnetic field
   The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.
6. Built-in thermal shutdown protection circuit
   The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15℃ (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.
7. Capacitor across output and GND
   In the event a large capacitor is connected across output and GND, when Vcc and VIN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000 μF between output and GND.
8. Inspection by set substrate
   In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.
9. IC terminal input
   The present IC is a monolithic IC and has a P substrate and P+ isolation between elements.
   With this P layer and N layer of each element, PN junction is formed, and when the potential relation is
   - GND>terminal A>terminal B, PN junction works as a diode, and
   - terminal B>GND terminal A, PN junction operates as a parasitic transistor.

   The parasitic element is inevitably formed because of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC to operate the parasitic element such as applying voltage lower than GND (P substrate) to the input terminal.



10. Output capacitor (C5)
    Connect the output capacitor between Vo1, Vo2 terminals and GND terminal without fail in order to stabilize output voltage. The output capacitor has a role to compensate for the phase of loop gain and to reduce output voltage fluctuation when load is rapidly changed. When there is an insufficient capacity value, there is a possibility to cause oscillation, and when the equivalent serial resistance (ESR) of the capacitors is large, output voltage fluctuation is increased when load is rapidly changed. About 220 µF high-performance electrolytic capacitors are recommended, but this greatly depends on the gate capacity of external MOSFET and mutual conductance (gm), temperature and load conditions. In addition, when only ceramic capacitors with low ESR are used, or various capacitors are connected in series, the total phase allowance of loop gain becomes not sufficient, and oscillation may result. Thoroughgoing confirmation at application temperature and under load range conditions is requested.

11. Input capacitor setting method (C1, C4)
    The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (Vcc, VIN). When output impedance of this power supply increases, the input voltages (Vcc, VIN) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10 µF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, and MOSFET gate-drain capacity, thoroughgoing confirmation under the application temperature, load range, and M-MOSFET conditions is requested.

12. NRCS terminal capacitor setting method (C3)
    To the present IC, there mounted is a function (Non Rush Current on Start-up: NRCS) to prevent rush current from VIN to load and output capacitor via Vo at the output voltage start-up. When the EN terminal is reset from Hi or UVLO, constant current is allowed to flow from the NRCS terminal. By this current, voltage generated at the NRCS terminal becomes the reference voltage and output voltage is started. In order to stabilize the NRCS set time, it is recommended to use a capacitor (B special) with less capacity value change caused by temperature change.

13. SCP terminal capacitor setting method (C2)
    The present IC incorporates a timer-latch type short-circuit protection circuit in order to prevent MOSFET from being destroyed by abnormal current when output terminal is short-circuited (operates at the time of NRCS, too). When the output terminal voltage drops 30% from output setting voltage, IC judges that the output is short-circuited. In such event, constant current begins to flow. When the voltage generated in the SCP terminal reaches 1.3V (Typ) by this current, the gate terminal is brought to the Low level. In order to stabilize the SCP setting time, a capacitor (B special) with less capacity value change caused by temperature changes is recommended. When the SCP function is not used, short-circuit the SCP terminal to the GND terminal. In addition, when the output terminal is short-circuited, the MOSFET gate voltage reaches the Vcc voltage and the large current that meets MOSFET characteristics flows to the output while the timer latch type protection circuit operates. When the current capacity of VIN terminal power supply lacks, the Vin terminal voltage lowers and the UVLO circuit operates, and the latch operation may not be finished. In such event, connect a limiting resistor across drain terminal and VIN terminal of MOSFET.

14. Input terminals (VCC, VIN, EN)
    In the present IC, N terminal, VIN terminal, and VCC terminal have an independent construction. In addition, in order to prevent malfunction at the time of low input, the UVLO function is equipped with the VIN terminal and the VCC terminal. They begin to start output voltage when all the terminals reach threshold voltage without depending on the input order of input terminals.

15. Maximum output current (maximum load)
    The maximum output current capacity of the power supply which is composed by the use of the present IC depends on the external FET. Consequently, confirm the characteristics of the power required for the set to be used, choose the external FET.

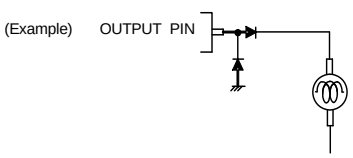
16. Operating ranges
    If it is within the operating ranges, certain circuit functions and operations are warranted in the working ambient temperature range. With respect to characteristic values, it is unable to warrant standard values of electric characteristics but there are no sudden variations in characteristic values within these ranges.

17. Allowable loss Pd
    With respect to the allowable loss, the thermal derating characteristics are shown in the Exhibit, which we hope would be used as a good-rule-of-thumb. Should the IC be used in such a manner to exceed the allowable loss, reduction of current capacity due to chip temperature rise, and other degraded properties inherent to the IC would result. You are strongly urged to use the IC within the allowable loss.

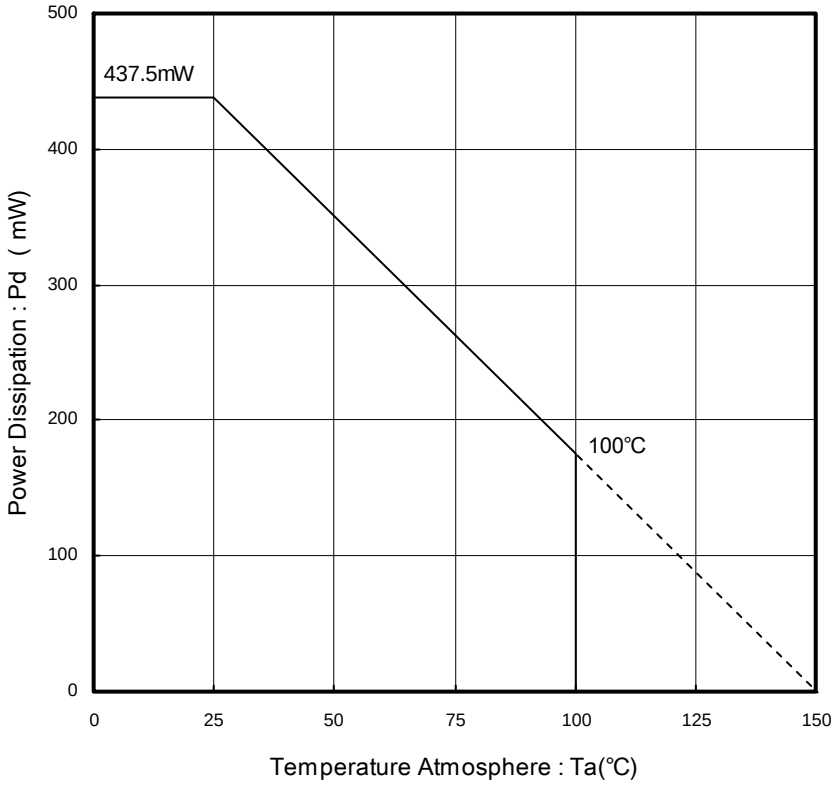
18. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.

19. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

20. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC. In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.



●**Power Dissipation**



Without heat sink.
θ j-a=286℃/W

●Ordering part number

B	D	3	5	0	4	F	V	M	-	T	R

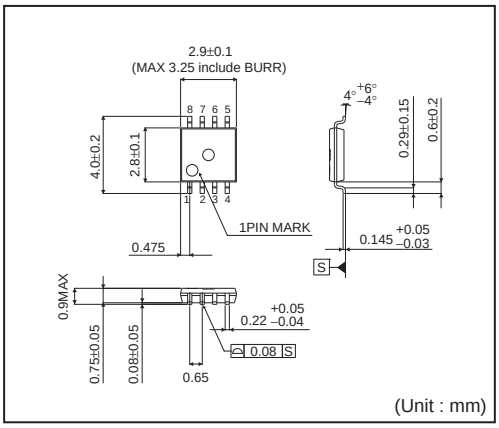
Part No.

Part No.
3504
3500
3501
3502

Package
FVM: MSOP8

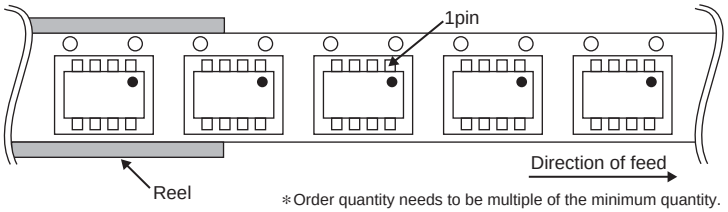
Packaging and forming specification
TR: Embossed tape and reel
(MSOP8)

MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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ROHM SEMICONDUCTOR

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OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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