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New 8FX 8-bit Microcontrollers

The MB95560H/570H/580H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

- F²MC-8FX CPU core
 - Instruction set optimized for controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operations
 - Bit test branch instructions
 - Bit manipulation instructions, etc.
- Clock (The main oscillation clock and the suboscillation clock are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)
 - Selectable main clock source
 - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
 - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
 - Main CR clock (4 MHz ± 2%)
 - The main CR clock frequency becomes 8 MHz when the PLL multiplication rate is 2.
 - The main CR clock frequency becomes 10 MHz when the PLL multiplication rate is 2.5.
 - The main CR clock frequency becomes 12 MHz when the PLL multiplication rate is 3.
 - The main CR clock frequency becomes 16 MHz when the PLL multiplication rate is 4.
 - Selectable subclock source
 - Suboscillation clock (32.768 kHz)
 - External clock (32.768 kHz)
 - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)
- Timer
 - 8/16-bit composite timer × 2 channels (only one channel on MB95F572H/F572K/F573H/F573K/F574H/F574K/F582H/F582K/F583H/F583K/F584H/F584K)
 - Time-base timer × 1 channel
 - Watch prescaler × 1 channel
- LIN-UART (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)
 - Full duplex double buffer
 - Capable of clock synchronous serial data transfer and clock asynchronous serial data transfer
- External interrupt
 - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
 - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
 - 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes
 - There are four standby modes as follows:
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
 - In standby mode, the device can be made to enter either normal standby mode or deep standby mode.
- I/O port
 - MB95F562H/F563H/F564H (maximum no. of I/O ports: 16)
 - General-purpose I/O ports (CMOS I/O): 15
 - General-purpose I/O ports (N-ch open drain): 1
 - MB95F562K/F563K/F564K (maximum no. of I/O ports: 17)
 - General-purpose I/O ports (CMOS I/O): 15
 - General-purpose I/O ports (N-ch open drain): 2
 - MB95F572H/F573H/F574H (maximum no. of I/O ports: 4)
 - General-purpose I/O ports (CMOS I/O): 3
 - General-purpose I/O ports (N-ch open drain): 1
 - MB95F572K/F573K/F574K (maximum no. of I/O ports: 5)
 - General-purpose I/O ports (CMOS I/O): 3
 - General-purpose I/O ports (N-ch open drain): 2
 - MB95F582H/F583H/F584H (maximum no. of I/O ports: 12)
 - General-purpose I/O ports (CMOS I/O): 11
 - General-purpose I/O ports (N-ch open drain): 1
 - MB95F582K/F583K/F584K (maximum no. of I/O ports: 13)
 - General-purpose I/O ports (CMOS I/O): 11
 - General-purpose I/O ports (N-ch open drain): 2
- On-chip debug
 - 1-wire serial control
 - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
 - Built-in hardware watchdog timer
 - Built-in software watchdog timer
- Power-on reset
 - A power-on reset is generated when the power is switched on.
- Low-voltage detection reset circuit (only available on MB95F562K/F563K/F564K/F572K/F573K/F574K/F582K/F583K/F584K)
 - Built-in low-voltage detector
- Clock supervisor counter
 - Built-in clock supervisor counter function
- Dual operation Flash memory
 - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
 - Protects the content of the Flash memory.

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1. Product Line-up

• MB95560H Series

| Part number | MB95F562H | MB95F563H | MB95F564H | MB95F562K | MB95F563K | MB95F564K |
|----------------------------------|---|-----------|-----------|---|-----------|-----------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max) : 16 • CMOS I/O : 15 • N-ch open drain: 1 | | | <ul style="list-style-type: none"> • I/O ports (Max) : 17 • CMOS I/O : 15 • N-ch open drain: 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | |
| LIN-UART | <ul style="list-style-type: none"> • A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave. | | | | | |
| 8/10-bit A/D converter | 6 channels 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 2 channels <ul style="list-style-type: none"> • The timer can be configured as an "8-bit timer \times 2 channels" or a "16-bit timer \times 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (7 types) and external clocks. • It can output square wave. | | | | | |
| External interrupt | 6 channels <ul style="list-style-type: none"> • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> • 1-wire serial control • It supports serial writing (asynchronous mode). | | | | | |

| Part number | MB95F562H | MB95F563H | MB95F564H | MB95F562K | MB95F563K | MB95F564K |
|-----------------|--|-----------|-----------|-----------|-----------|-----------|
| Parameter | | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | |
| Flash memory | <ul style="list-style-type: none"> It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Flash security feature for protecting the content of the Flash memory | | | | | |
| | Number of program/erase cycles | | 1000 | 10000 | 100000 | |
| | Data retention time | | 20 years | 10 years | 5 years | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | WNP032 SOJ020 STG020 | | | | | |

• MB95570H Series

| Part number | MB95F572H | MB95F573H | MB95F574H | MB95F572K | MB95F573K | MB95F574K |
|----------------------------------|---|-----------|-----------|---|-----------|-----------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | <ul style="list-style-type: none"> Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> I/O ports (Max) : 4 CMOS I/O : 3 N-ch open drain: 1 | | | <ul style="list-style-type: none"> I/O ports (Max) : 5 CMOS I/O : 3 N-ch open drain: 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | |
| LIN-UART | No LIN-UART | | | | | |
| 8/10-bit A/D converter | 2 channels 8-bit or 10-bit resolution can be selected. | | | | | |

| Part number | MB95F572H | MB95F573H | MB95F574H | MB95F572K | MB95F573K | MB95F574K | | | | | | | | |
|--------------------------------|--|-----------|-----------|-----------|-----------|-----------|--------------------------------|------|-------|--------|---------------------|----------|----------|---------|
| Parameter | | | | | | | | | | | | | | |
| 8/16-bit composite timer | 1 channel <ul style="list-style-type: none"> The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". It has the following functions: interval timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (7 types) and external clocks. It can output square wave. | | | | | | | | | | | | | |
| External interrupt | 2 channels <ul style="list-style-type: none"> Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from the standby mode. | | | | | | | | | | | | | |
| On-chip debug | <ul style="list-style-type: none"> 1-wire serial control It supports serial writing (asynchronous mode). | | | | | | | | | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | | | | | | | | | |
| Flash memory | <ul style="list-style-type: none"> It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Flash security feature for protecting the content of the Flash memory <table border="1" data-bbox="337 873 1239 961"> <tr> <td>Number of program/erase cycles</td> <td>1000</td> <td>10000</td> <td>100000</td> </tr> <tr> <td>Data retention time</td> <td>20 years</td> <td>10 years</td> <td>5 years</td> </tr> </table> | | | | | | Number of program/erase cycles | 1000 | 10000 | 100000 | Data retention time | 20 years | 10 years | 5 years |
| Number of program/erase cycles | 1000 | 10000 | 100000 | | | | | | | | | | | |
| Data retention time | 20 years | 10 years | 5 years | | | | | | | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | | | | | | | | | |
| Package | PDA008 SOD008 | | | | | | | | | | | | | |

• MB95580H Series

| Part number | MB95F582H | MB95F583H | MB95F584H | MB95F582K | MB95F583K | MB95F584K |
|-----------------------------|--|-----------|-----------|---|-----------|-----------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | <ul style="list-style-type: none"> Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> I/O ports (Max) : 12 CMOS I/O : 11 N-ch open drain: 1 | | | <ul style="list-style-type: none"> I/O ports (Max) : 13 CMOS I/O : 11 N-ch open drain: 2 | | |



| Part number | MB95F582H | MB95F583H | MB95F584H | MB95F582K | MB95F583K | MB95F584K | | | | | | | | |
|----------------------------------|--|-----------|-----------|-----------|-----------|-----------|--------------------------------|------|-------|--------|---------------------|----------|----------|---------|
| Parameter | | | | | | | | | | | | | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | | | | | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | | | | | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | | | | | | | | | |
| LIN-UART | <ul style="list-style-type: none"> A wide range of communication speed can be selected by a dedicated reload timer. It has a full duplex double buffer. Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. The LIN function can be used as a LIN master or a LIN slave. | | | | | | | | | | | | | |
| 8/10-bit A/D converter | 5 channels 8-bit or 10-bit resolution can be selected. | | | | | | | | | | | | | |
| 8/16-bit composite timer | 1 channel <ul style="list-style-type: none"> The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". It has the following functions: interval timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (7 types) and external clocks. It can output square wave. | | | | | | | | | | | | | |
| External interrupt | 6 channels <ul style="list-style-type: none"> Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from the standby mode. | | | | | | | | | | | | | |
| On-chip debug | <ul style="list-style-type: none"> 1-wire serial control It supports serial writing (asynchronous mode). | | | | | | | | | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | | | | | | | | | |
| Flash memory | <ul style="list-style-type: none"> It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Flash security feature for protecting the content of the Flash memory <table border="1" style="margin-left: 40px;"> <tr> <td>Number of program/erase cycles</td> <td>1000</td> <td>10000</td> <td>100000</td> </tr> <tr> <td>Data retention time</td> <td>20 years</td> <td>10 years</td> <td>5 years</td> </tr> </table> | | | | | | Number of program/erase cycles | 1000 | 10000 | 100000 | Data retention time | 20 years | 10 years | 5 years |
| Number of program/erase cycles | 1000 | 10000 | 100000 | | | | | | | | | | | |
| Data retention time | 20 years | 10 years | 5 years | | | | | | | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | | | | | | | | | |
| Package | WNP032 STB016 SO016 | | | | | | | | | | | | | |



2. Packages And Corresponding Products

• MB95560H Series

| Part number / Package | MB95F562H | MB95F562K | MB95F563H | MB95F563K | MB95F564H | MB95F564K |
|-----------------------|-----------|-----------|-----------|-----------|-----------|-----------|
| WNP032 | O | O | O | O | O | O |
| SOJ020 | O | O | O | O | O | O |
| STG020 | O | O | O | O | O | O |
| STB016 | X | X | X | X | X | X |
| SO016 | X | X | X | X | X | X |
| PDA008 | X | X | X | X | X | X |
| SOD008 | X | X | X | X | X | X |

• MB95570H Series

| Part number / Package | MB95F572H | MB95F572K | MB95F573H | MB95F573K | MB95F574H | MB95F574K |
|-----------------------|-----------|-----------|-----------|-----------|-----------|-----------|
| WNP032 | X | X | X | X | X | X |
| SOJ020 | X | X | X | X | X | X |
| STG020 | X | X | X | X | X | X |
| STB016 | X | X | X | X | X | X |
| SO016 | X | X | X | X | X | X |
| PDA008 | O | O | O | O | O | O |
| SOD008 | O | O | O | O | O | O |

• MB95580H Series

| Part number / Package | MB95F582H | MB95F582K | MB95F583H | MB95F583K | MB95F584H | MB95F584K |
|-----------------------|-----------|-----------|-----------|-----------|-----------|-----------|
| WNP032 | O | O | O | O | O | O |
| SOJ020 | X | X | X | X | X | X |
| STG020 | X | X | X | X | X | X |
| STB016 | O | O | O | O | O | O |
| SO016 | O | O | O | O | O | O |
| PDA008 | X | X | X | X | X | X |
| SOD008 | X | X | X | X | X | X |

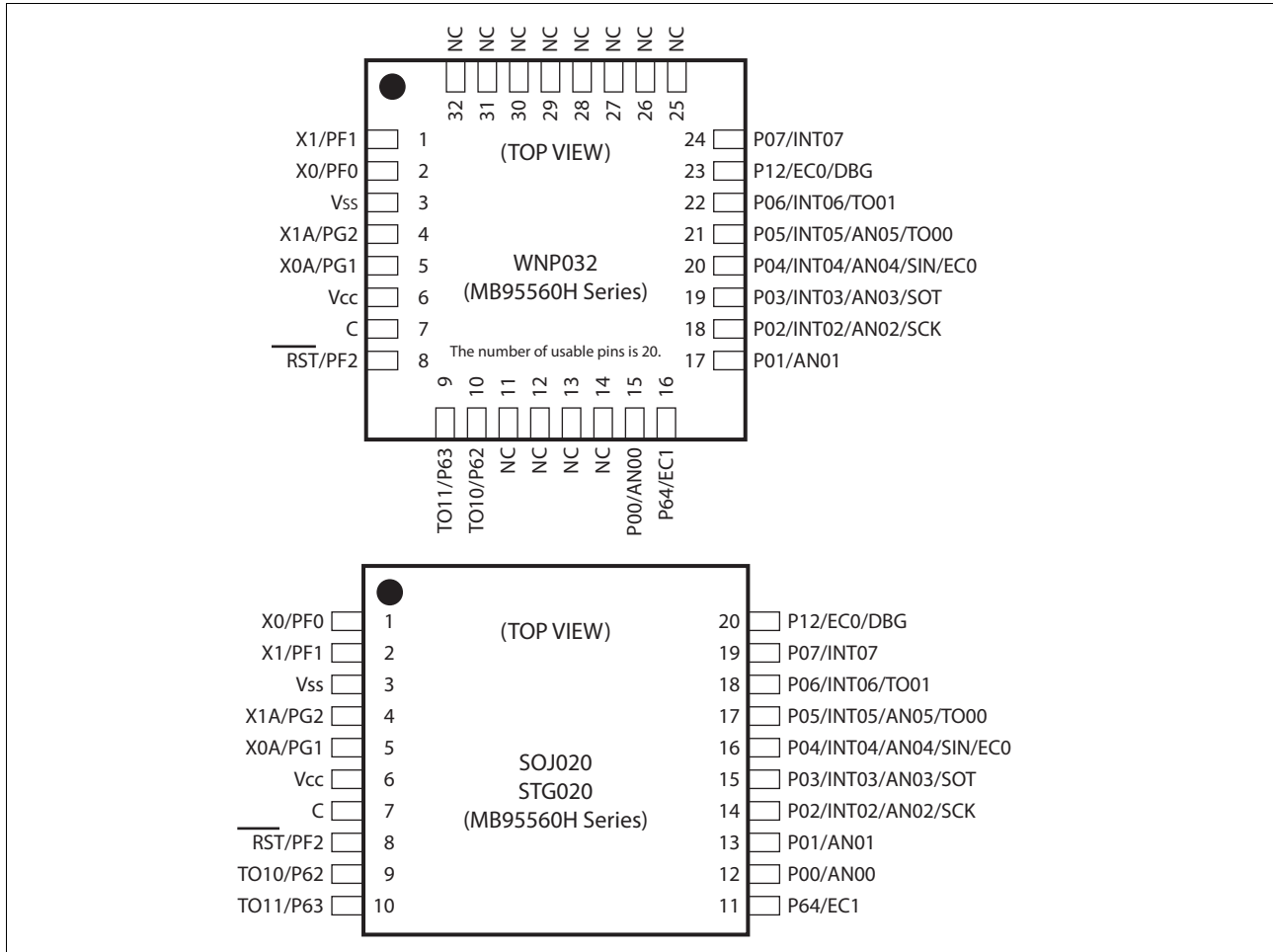
O: Available
X: Unavailable

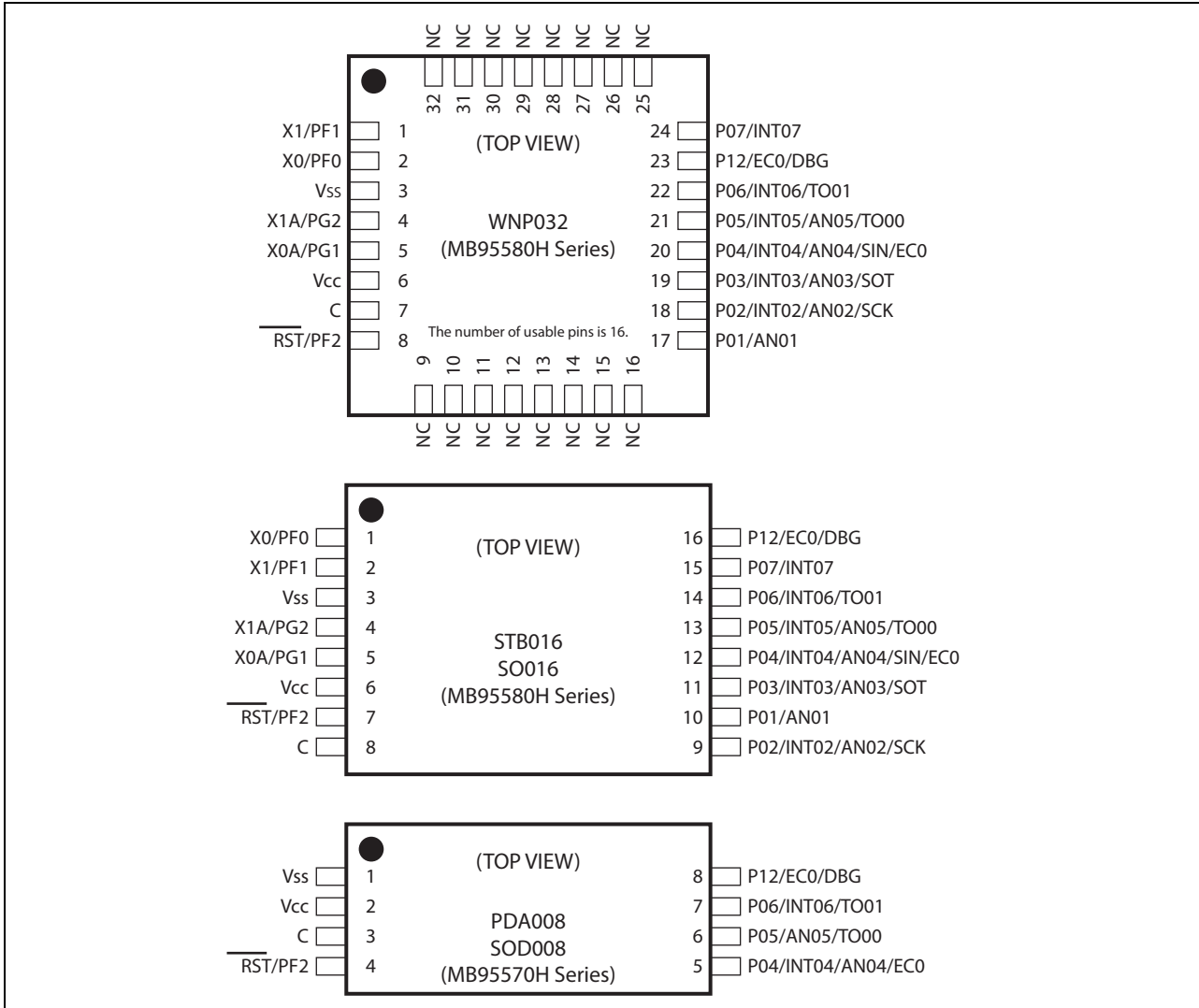


3. Differences Among Products And Notes On Product Selection

- **Current consumption**
When using the on-chip debug function, take account of the current consumption of Flash memory program/erase. For details of current consumption, see “Electrical Characteristics”.
- **Package**
For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.
- **Operating voltage**
The operating voltage varies, depending on whether the on-chip debug function is used or not. For details of the operating voltage, see “Electrical Characteristics”.
- **On-chip debug function**
The on-chip debug function requires that V_{CC} , V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95560H/570H/580H Hardware Manual”.

4. Pin Assignment







5. Pin Functions (MB95560H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | V _{ss} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{cc} | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin Dedicated reset pin on MB95F562H/F563H/F564H |
| 9 | P63 | E | General-purpose I/O port |
| | TO11 | | High-current pin 8/16-bit composite timer ch. 1 output pin |
| 10 | P62 | E | General-purpose I/O port |
| | TO10 | | High-current pin 8/16-bit composite timer ch. 1 output pin |
| 11 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | P00 | D | General-purpose I/O port |
| | AN00 | | High-current pin A/D converter analog input pin |
| 16 | P64 | E | General-purpose I/O port |
| | EC1 | | High-current pin 8/16-bit composite timer ch. 1 clock input pin |
| 17 | P01 | D | General-purpose I/O port |
| | AN01 | | High-current pin A/D converter analog input pin |
| 18 | P02 | D | General-purpose I/O port |
| | INT02 | | High-current pin External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |



| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|---|
| 19 | P03 | D | General-purpose I/O port High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 20 | P04 | D | General-purpose I/O port High-current pin |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 21 | P05 | D | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | E | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | E | General-purpose I/O port High-current pin |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | | | |
| 27 | | | |
| 28 | | | |
| 29 | | | |
| 30 | | | |
| 31 | | | |
| 32 | | | |

*: For the I/O circuit types, see "I/O Circuit Type".



6. Pin Functions (MB95560H Series, 20 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|---|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | V _{ss} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{cc} | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin Dedicated reset pin on MB95F562H/F563H/F564H |
| 9 | P62 | E | General-purpose I/O port High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 10 | P63 | E | General-purpose I/O port High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | P64 | E | General-purpose I/O port High-current pin |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 12 | P00 | D | General-purpose I/O port High-current pin |
| | AN00 | | A/D converter analog input pin |
| 13 | P01 | D | General-purpose I/O port High-current pin |
| | AN01 | | A/D converter analog input pin |
| 14 | P02 | D | General-purpose I/O port High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 15 | P03 | D | General-purpose I/O port High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |



| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--|
| 16 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 17 | P05 | D | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 18 | P06 | E | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 19 | P07 | E | General-purpose I/O port High-current pin |
| | INT07 | | External interrupt input pin |
| 20 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "I/O Circuit Type".



7. Pin Functions (MB95570H Series, 8 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|---|
| 1 | V _{ss} | — | Power supply pin (GND) |
| 2 | V _{cc} | — | Power supply pin |
| 3 | C | — | Decoupling capacitor connection pin |
| 4 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin Dedicated reset pin on MB95F572H/F573H/F574H |
| 5 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 6 | P05 | D | General-purpose I/O port High-current pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 7 | P06 | E | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 8 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "I/O Circuit Type".



8. Pin Functions (MB95580H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|---|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | V _{ss} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{cc} | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin Dedicated reset pin on MB95F582H/F583H/F584H |
| 9 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 10 | | | |
| 11 | | | |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | | | |
| 16 | | | |
| 17 | P01 | D | General-purpose I/O port High-current pin |
| | AN01 | | A/D converter analog input pin |
| 18 | P02 | D | General-purpose I/O port High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 19 | P03 | D | General-purpose I/O port High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |



| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|---|
| 20 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 21 | P05 | D | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | E | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | E | General-purpose I/O port High-current pin |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | | | |
| 27 | | | |
| 28 | | | |
| 29 | | | |
| 30 | | | |
| 31 | | | |
| 32 | | | |

*: For the I/O circuit types, see "I/O Circuit Type".



9. Pin Functions (MB95580H Series, 16 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|---|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | V _{ss} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{cc} | — | Power supply pin |
| 7 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin Dedicated reset pin on MB95F582H/F583H/F584H |
| 8 | C | — | Decoupling capacitor connection pin |
| 9 | P02 | D | General-purpose I/O port High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 10 | P01 | D | General-purpose I/O port High-current pin |
| | AN01 | | A/D converter analog input pin |
| 11 | P03 | D | General-purpose I/O port High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 12 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |



| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--|
| 13 | P05 | D | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 14 | P06 | E | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 15 | P07 | E | General-purpose I/O port High-current pin |
| | INT07 | | External interrupt input pin |
| 16 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "I/O Circuit Type".



10. I/O Circuit Type

| Type | Circuit | Remarks |
|------|---------|---|
| A | | <ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input • Reset output |
| B | | <ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input |
| C | | <ul style="list-style-type: none"> • Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available |

| Type | Circuit | Remarks |
|------|---------|--|
| D | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available • Analog input |
| E | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available |
| F | | <ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input |

11. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

11.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.



- **Processing and Protection of Pins**

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

- (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.



11.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

• Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

• Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

• Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

• Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

• Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

• Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:



- (1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 M Ω).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

11.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

12. Notes On Device Handling

- Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "24.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage



Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

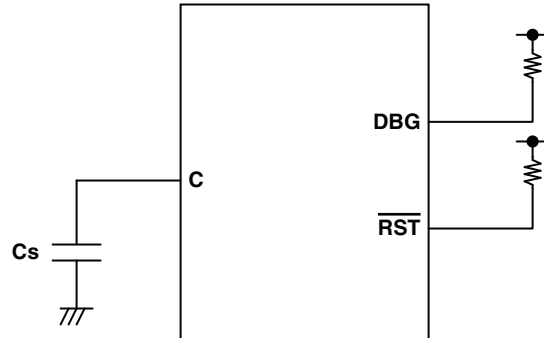
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

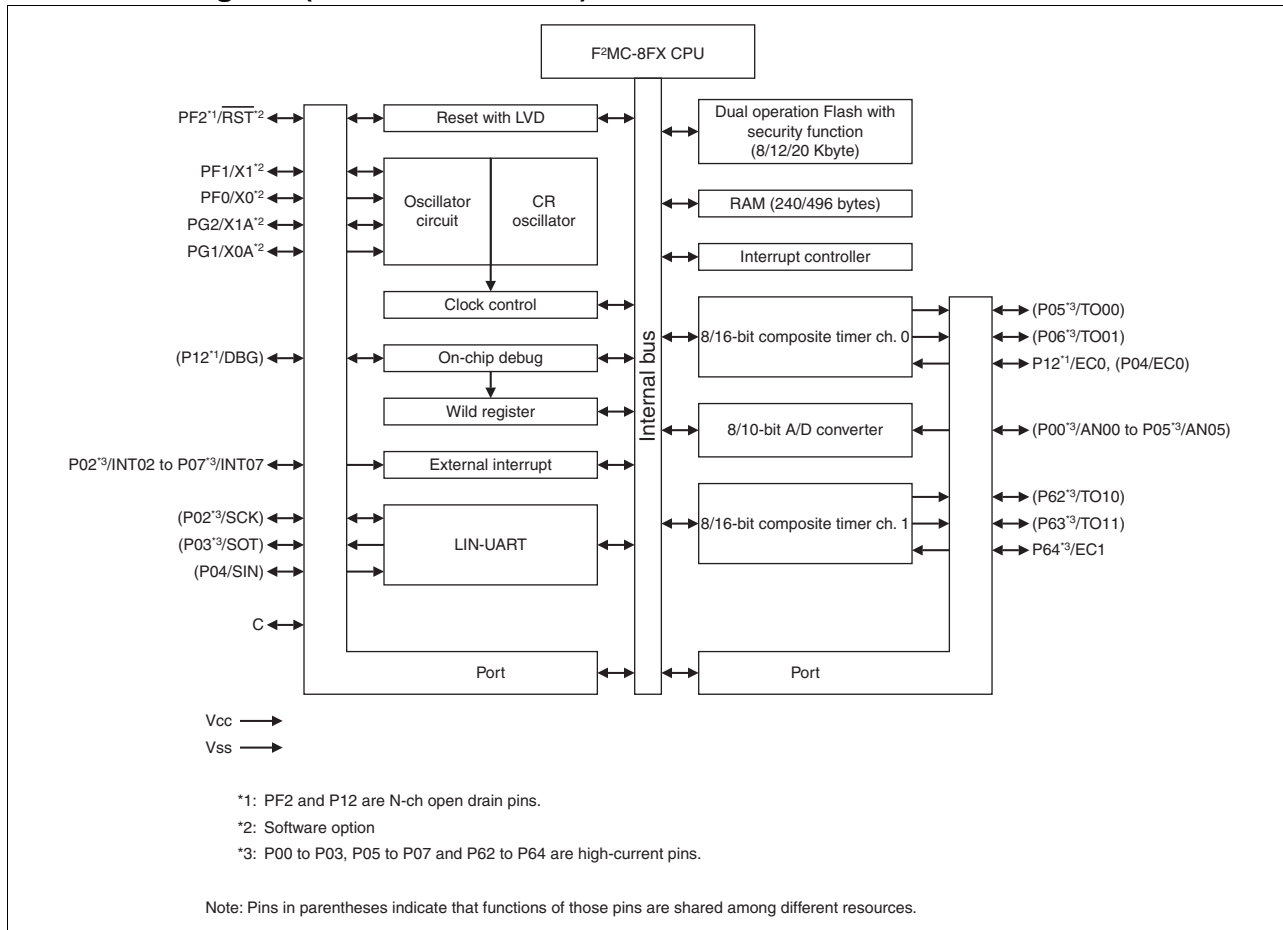
13. Pin Connection

- Treatment of unused pins
If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k Ω . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.
- Power supply pins
To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 μ F as a decoupling capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.
- DBG pin
Connect the DBG pin to an external pull-up resistor of 2 k Ω or above.
After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released.
The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.
- \overline{RST} pin
Connect the \overline{RST} pin to an external pull-up resistor of 2 k Ω or above.
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the \overline{RST} pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
The PF2/ \overline{RST} pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/ \overline{RST} pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.
- C pin
Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_s . For the connection to a decoupling capacitor C_s , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_s and the distance between C_s and the V_{SS} pin when designing the layout of a printed circuit board.

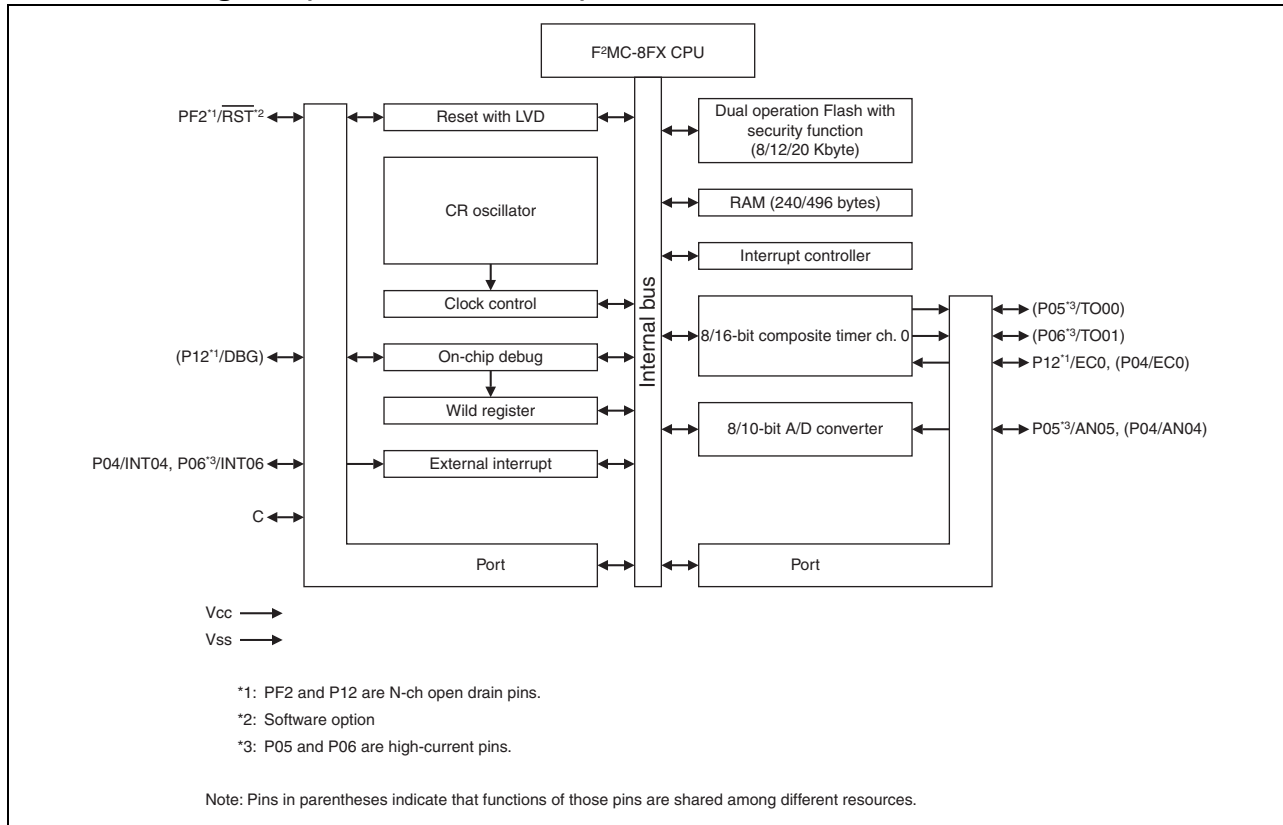
- $\overline{\text{DBG}}/\overline{\text{RST}}/\text{C}$ pins connection diagram



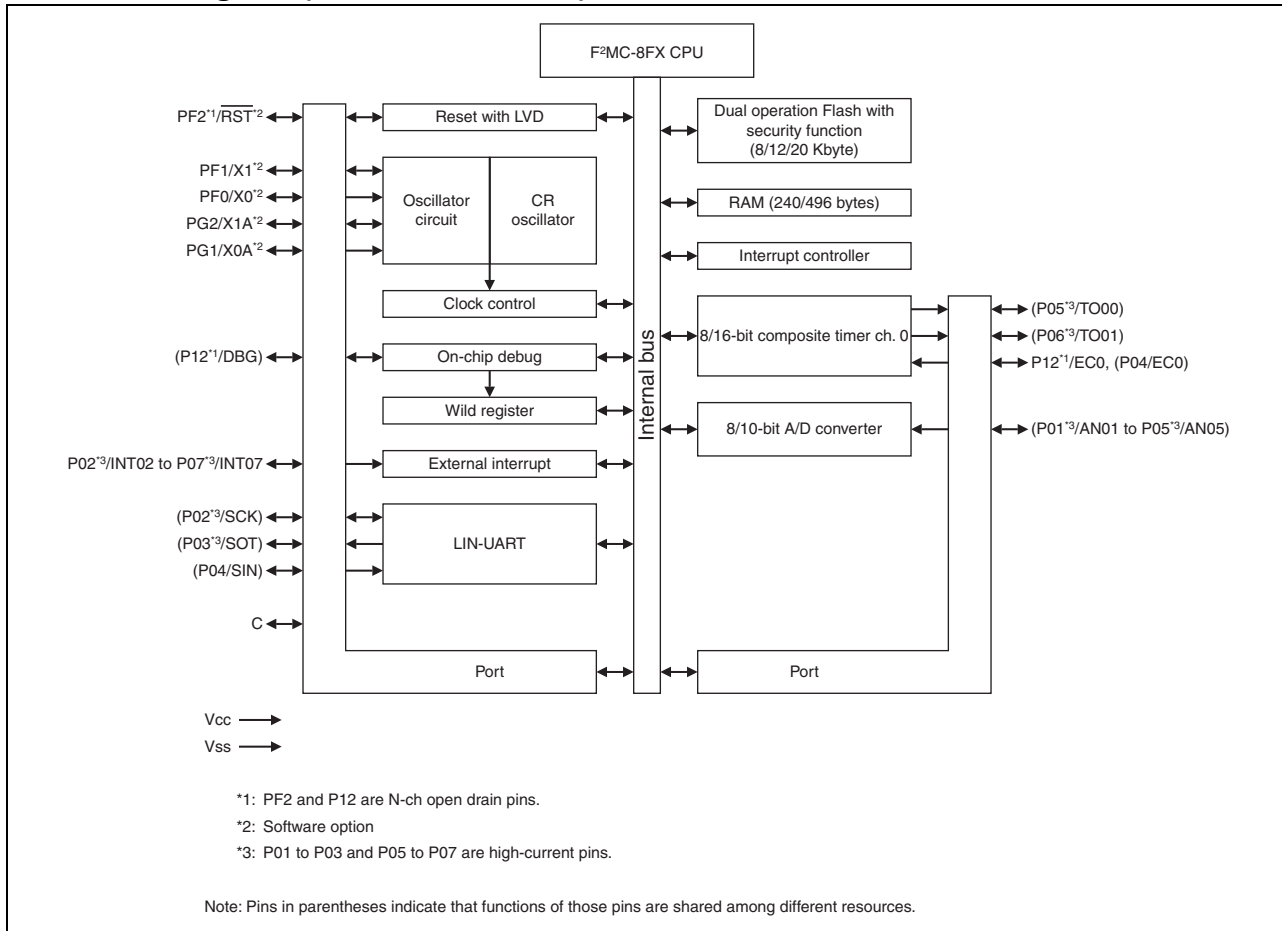
14. Block Diagram (MB95560H Series)



15. Block Diagram (MB95570H Series)



16. Block Diagram (MB95580H Series)



17. CPU Core

- Memory space

The memory space of the MB95560H/570H/580H is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95560H/570H/580H are shown below.8

- Memory maps

| MB95F562H/F562K/F572H/ F572K/F582H/F582K | MB95F563H/F563K/F573H/ F573K/F583H/F583K | MB95F564H/F564K/F574H/ F574K/F584H/F584K |
|---|---|---|
| 0000 _H | 0000 _H | 0000 _H |
| 0080 _H | 0080 _H | 0080 _H |
| 0090 _H | 0090 _H | 0090 _H |
| 0100 _H | 0100 _H | 0100 _H |
| 0180 _H | 0200 _H | 0200 _H |
| | 0280 _H | 0280 _H |
| 0F80 _H | 0F80 _H | 0F80 _H |
| 1000 _H | 1000 _H | 1000 _H |
| | | |
| B000 _H | B000 _H | B000 _H |
| C000 _H | C000 _H | |
| | | |
| F000 _H | E000 _H | |
| FFFF _H | FFFF _H | FFFF _H |



18. I/O Map (MB95560H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 000X0000 _B |
| 0007 _H | SYCC | System clock control register | R/W | XXX11011 _B |
| 0008 _H | STBC | Standby control register | R/W | 00000000 _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XXXX0011 _B |
| 000E _H | STBC2 | Standby control register 2 | R/W | 00000000 _B |
| 000F _H to 0015 _H | — | (Disabled) | — | — |
| 0016 _H | PDR6 | Port 6 data register | R/W | 00000000 _B |
| 0017 _H | DDR6 | Port 6 direction register | R/W | 00000000 _B |
| 0018 _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0032 _H | — | (Disabled) | — | — |
| 0033 _H | PUL6 | Port 6 pull-up register | R/W | 00000000 _B |
| 0034 _H | — | (Disabled) | — | — |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000 _B |
| 0038 _H | T11CR1 | 8/16-bit composite timer 11 status control register 1 | R/W | 00000000 _B |
| 0039 _H | T10CR1 | 8/16-bit composite timer 10 status control register 1 | R/W | 00000000 _B |
| 003A _H to 0048 _H | — | (Disabled) | — | — |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H , 004D _H | — | (Disabled) | — | — |
| 004E _H | LVDR | LVDR reset voltage selection ID register | R/W | 00000000 _B |
| 004F _H | — | (Disabled) | — | — |
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR | LIN-UART receive data register | R/W | 00000000 _B |
| | TDR | LIN-UART transmit data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 000XXXXX _B |
| 0075 _H | FSR4 | Flash memory status register 4 | R/W | 00000000 _B |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0F83 _H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000 _B |
| 0F97 _H | T11CR0 | 8/16-bit composite timer 11 status control register 0 | R/W | 00000000 _B |
| 0F98 _H | T10CR0 | 8/16-bit composite timer 10 status control register 0 | R/W | 00000000 _B |
| 0F99 _H | T11DR | 8/16-bit composite timer 11 data register | R/W | 00000000 _B |
| 0F9A _H | T10DR | 8/16-bit composite timer 10 data register | R/W | 00000000 _B |
| 0F9B _H | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register | R/W | 00000000 _B |
| 0F9C _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRTH | Main CR clock trimming register (upper) | R/W | 000XXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (lower) | R/W | 000XXXXX _B |
| 0FE6 _H | — | (Disabled) | — | — |
| 0FE7 _H | CRTDA | Main CR clock temperature dependent adjustment register | R/W | 000XXXXX _B |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R | 00000000 _B |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0FEB _H | WDTH | Watchdog timer selection ID register (upper) | R | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (lower) | R | XXXXXXXX _B |
| 0FED _H to 0FFF _H | — | (Disabled) | — | — |

• R/W access symbols

R/W : Readable / Writable

R : Read only

• Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.



19. I/O Map (MB95570H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 000X0000 _B |
| 0007 _H | SYCC | System clock control register | R/W | XXX11011 _B |
| 0008 _H | STBC | Standby control register | R/W | 00000000 _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XXXX0011 _B |
| 000E _H | STBC2 | Standby control register 2 | R/W | 00000000 _B |
| 000F _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H , 002B _H | — | (Disabled) | — | — |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0035 _H | — | (Disabled) | — | — |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000 _B |
| 0038 _H to 0049 _H | — | (Disabled) | — | — |
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H , 004D _H | — | (Disabled) | — | — |
| 004E _H | LVDR | LVDR reset voltage selection ID register | R/W | 00000000 _B |
| 004F _H to 006B _H | — | (Disabled) | — | — |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 000XXXXX _B |
| 0075 _H | FSR4 | Flash memory status register 4 | R/W | 00000000 _B |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H , 007C _H | — | (Disabled) | — | — |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000 _B |
| 0F97 _H to 0FC2 _H | — | (Disabled) | — | — |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0FC3 _H | AIDRL | A/D input disable register (lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRTH | Main CR clock trimming register (upper) | R/W | 000XXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (lower) | R/W | 000XXXXX _B |
| 0FE6 _H | — | (Disabled) | — | — |
| 0FE7 _H | CRTDA | Main CR clock temperature dependent adjustment register | R/W | 000XXXXX _B |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R | 00000000 _B |
| 0FEB _H | WDTH | Watchdog timer selection ID register (upper) | R | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (lower) | R | XXXXXXXX _B |
| 0FED _H to 0FFF _H | — | (Disabled) | — | — |

• R/W access symbols

R/W : Readable / Writable

R : Read only

• Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.



20. I/O Map (MB95580H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 000X0000 _B |
| 0007 _H | SYCC | System clock control register | R/W | XXX11011 _B |
| 0008 _H | STBC | Standby control register | R/W | 00000000 _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XXXX0011 _B |
| 000E _H | STBC2 | Standby control register 2 | R/W | 00000000 _B |
| 000F _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0034 _H | — | (Disabled) | — | — |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000 _B |
| 0038 _H to 0048 _H | — | (Disabled) | — | — |
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H , 004D _H | — | (Disabled) | — | — |
| 004E _H | LVDR | LVDR reset voltage selection ID register | R/W | 00000000 _B |
| 004F _H | — | (Disabled) | — | — |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR | LIN-UART receive data register | R/W | 00000000 _B |
| | TDR | LIN-UART transmit data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 000XXXXX _B |
| 0075 _H | FSR4 | Flash memory status register 4 | R/W | 00000000 _B |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | — | (Disabled) | — | — |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |



| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000 _B |
| 0F97 _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRT _H | Main CR clock trimming register (upper) | R/W | 000XXXXX _B |
| 0FE5 _H | CRT _L | Main CR clock trimming register (lower) | R/W | 000XXXXX _B |
| 0FE6 _H | — | (Disabled) | — | — |
| 0FE7 _H | CRT _{DA} | Main CR clock temperature dependent adjustment register | R/W | 000XXXXX _B |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R | 00000000 _B |
| 0FEB _H | WD _{TH} | Watchdog timer selection ID register (upper) | R | XXXXXXXX _B |
| 0FEC _H | WD _{TL} | Watchdog timer selection ID register (lower) | R | XXXXXXXX _B |
| 0FED _H to 0FFF _H | — | (Disabled) | — | — |

• R/W access symbols

R/W : Readable / Writable

R : Read only

• Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.



21. Interrupt Source Table (MB95560H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|--|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div> <div style="text-align: center;">↑</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Low</div> |
| External interrupt ch. 5 | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| 8/16-bit composite timer ch. 1 (upper) | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| 8/16-bit composite timer ch. 1 (lower) | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |



22. Interrupt Source Table (MB95570H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|--|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div> <div style="text-align: center;">↑</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Low</div> |
| — | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| — | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| — | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| — | | | | | |
| — | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| — | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| — | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| — | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| — | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |



23. Interrupt Source Table (MB95580H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|--|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div> <div style="text-align: center;">Low</div> |
| External interrupt ch. 5 | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| — | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| — | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |

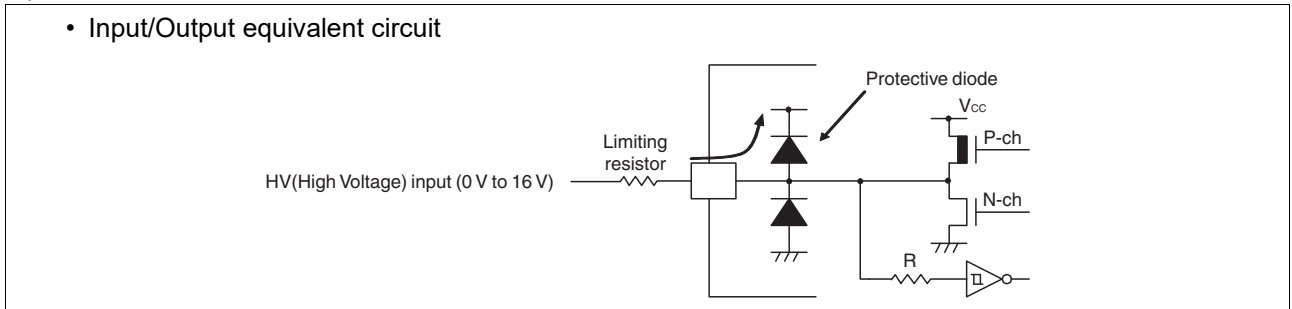
24. Electrical Characteristics

24.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|--------------------|----------------|--------------|------|---|
| | | Min | Max | | |
| Power supply voltage*1 | V_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | |
| Input voltage*1 | V_I | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | *2 |
| Output voltage*1 | V_O | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | *2 |
| Maximum clamp current | I_{CLAMP} | -2 | +2 | mA | Applicable to specific pins*3 |
| Total maximum clamp current | $\sum I_{CLAMP} $ | — | 20 | mA | Applicable to specific pins*3 |
| “L” level maximum output current | I_{OL} | — | 15 | mA | |
| “L” level average current | I_{OLAV1} | — | 4 | mA | Other than P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin) |
| | I_{OLAV2} | | 12 | | P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin) |
| “L” level total maximum output current | $\sum I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\sum I_{OLAV}$ | — | 50 | mA | Total average output current= operating current × operating ratio (Total number of pins) |
| “H” level maximum output current | I_{OH} | — | -15 | mA | |
| “H” level average current | I_{OHAV1} | — | -4 | mA | Other than P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin) |
| | I_{OHAV2} | | -8 | | P00 to P03, P05 to P07, P62 to P64*4 Average output current= operating current × operating ratio (1 pin) |
| “H” level total maximum output current | $\sum I_{OH}$ | — | -100 | mA | |
| “H” level total average output current | $\sum I_{OHAV}$ | — | -50 | mA | Total average output current= operating current × operating ratio (Total number of pins) |
| Power consumption | P_d | — | 320 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

- *2: V_i and V_o must not exceed $V_{CC} + 0.3$ V. V_i must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_i rating.
- *3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0, PF1, PG1, and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)
 - Use under recommended operating conditions.
 - Use with DC voltage (current).
 - The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
 - The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
 - When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
 - If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
 - If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
 - Do not leave the HV (High Voltage) input pin unconnected.
 - Example of a recommended circuit:



- *4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

24.2 Recommended Operating Conditions

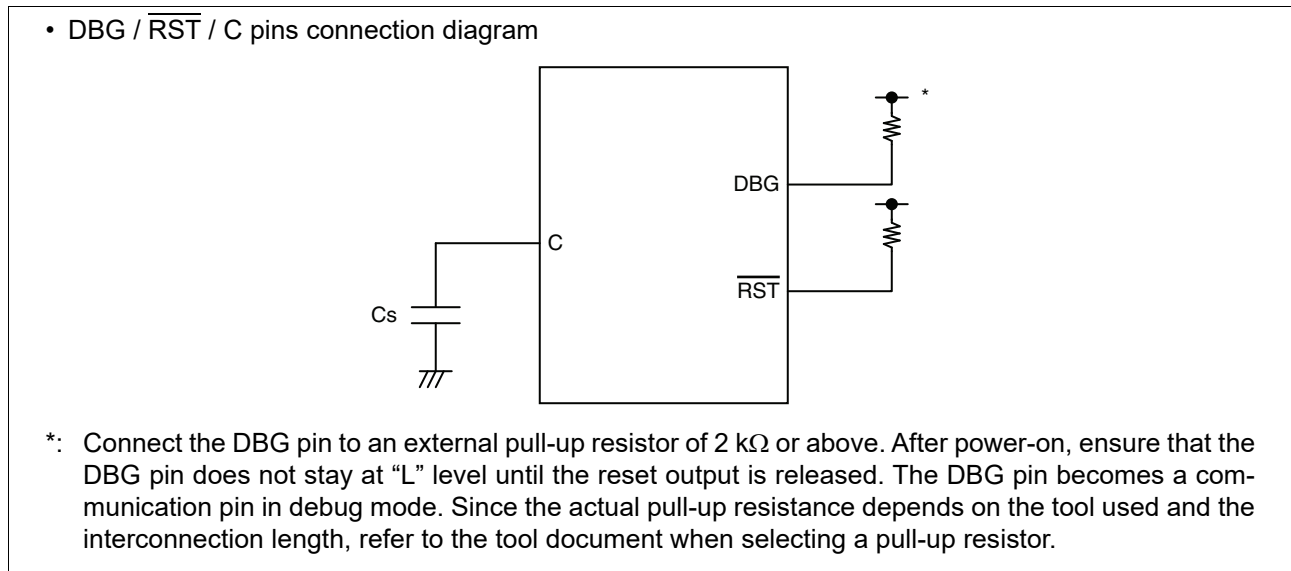
(V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|-----------------------|-----------------|-----------------------|-------------------|------|-------------------------------|-------------------------------|
| | | Min | Max | | | |
| Power supply voltage | V _{CC} | 2.4 ^{*1, *2} | 5.5 ^{*1} | V | In normal operation | Other than on-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| | | 2.9 | 5.5 | | In normal operation | On-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| Decoupling capacitor | C _s | 0.022 | 1 | μF | *3 | |
| Operating temperature | T _A | -40 | +85 | °C | Other than on-chip debug mode | |
| | | +5 | +35 | | On-chip debug mode | |

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_s. For the connection to a decoupling capacitor C_s, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_s and the distance between C_s and the V_{SS} pin when designing the layout of a printed circuit board.



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

24.3 DC Characteristics

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|--|-------------------------------|----------------|-----|----------------|---------------|--|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V_{IH} | P04 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHS} | P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P12, P62 to P64* ³ , PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2* ⁴ | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHM} | PF2 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| "L" level input voltage | V_{IL} | P04 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | Hysteresis input |
| | V_{ILS} | P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P12, P62 to P64* ³ , PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2* ⁴ | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILM} | PF2 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| Open-drain output application voltage | V_D | P12, PF2 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 5.5$ | V | |
| "H" level output voltage | V_{OH1} | P04, PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2 | $I_{OH} = -4\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| | V_{OH2} | P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P62 to P64* ³ | $I_{OH} = -8\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| "L" level output voltage | V_{OL1} | P04, P12, PF0 to PF2* ⁴ , PG1* ⁴ , PG2* ⁴ | $I_{OL} = 4\text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL2} | P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P62 to P64* ³ | $I_{OL} = 12\text{ mA}$ | — | — | 0.4 | V | |
| Input leak current (Hi-Z output leak current) | I_{LI} | All input pins | $0.0\text{ V} < V_I < V_{CC}$ | -5 | — | +5 | μA | When the internal pull-up resistor is disabled |
| Internal pull-up resistor | R_{PULL} | P00* ³ to P07* ⁴ , P62 to P64* ³ , PG1* ⁴ , PG2* ⁴ | $V_I = 0\text{ V}$ | 25 | 50 | 100 | k Ω | When the internal pull-up resistor is enabled |
| Input capacitance | C_{IN} | Other than V_{CC} and V_{SS} | $f = 1\text{ MHz}$ | — | 5 | 15 | pF | |

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks | |
|------------------------|---|---|---|---|-------|-------|----------------------|--|----------------------|
| | | | | Min | Typ*1 | Max*2 | | | |
| Power supply current*5 | I _{CC} | V _{CC} (External clock operation) | F _{CH} = 32 MHz F _{MP} = 16 MHz Main clock mode (divided by 2) | — | 3.5 | 4.4 | mA | Except during Flash memory programming and erasing | |
| | | | | — | 7.4 | 9.8 | mA | During Flash memory programming and erasing | |
| | | | | — | 5.1 | 6.4 | mA | At A/D conversion | |
| | I _{CCS} | | F _{CH} = 32 MHz F _{MP} = 16 MHz Main sleep mode (divided by 2) | — | 1.2 | 1.5 | mA | | |
| | I _{CCL} | | F _{CL} = 32 kHz F _{MPL} = 16 kHz Subclock mode (divided by 2) T _A = +25 °C | — | 65 | 71 | μA | | |
| | I _{CCLS} *6 | | F _{CL} = 32 kHz F _{MPL} = 16 kHz Subsleep mode (divided by 2) T _A = +25 °C | — | 5.4 | 7 | μA | In deep standby mode | |
| | I _{CCT} *6 | | F _{CL} = 32 kHz Watch mode T _A = +25 °C | — | 4.8 | 6.9 | μA | In deep standby mode | |
| | I _{CCMCR} | | V _{CC} | F _{CRH} = 4 MHz F _{MP} = 4 MHz Main CR clock mode | — | 1.1 | 1.4 | mA | |
| | I _{CCSCR} | | | Sub-CR clock mode (divided by 2) T _A = +25 °C | — | 58 | 64 | μA | |
| | I _{CCTS} | | V _{CC} (External clock operation) | F _{CH} = 32 MHz Time-base timer mode T _A = +25 °C | — | 290 | 340 | μA | In deep standby mode |
| I _{CCCH} | Main stop mode (single external clock product)/ Substop mode (dual external clock product) T _A = +25 °C | — | | 4.1 | 6.5 | μA | In deep standby mode | | |

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------------------|---------------------|-----------------|---|-------|-------------------|-------------------|------|---------|
| | | | | Min | Typ* ¹ | Max* ² | | |
| Power supply current* ⁵ | I _{LVD} | V _{CC} | Current consumption for the low-voltage detection circuit | — | 3.6 | 6.6 | μA | |
| | I _{CRH} | | Current consumption for the main CR oscillator | — | 220 | 280 | μA | |
| | I _{CRL} | | Current consumption for the sub-CR oscillator oscillating at 100 kHz | — | 5.1 | 9.3 | μA | |
| | I _{INSTBY} | | Current consumption difference between normal standby mode and deep standby mode T _A = +25 °C | — | 20 | 30 | μA | |

*1: V_{CC} = 5.0 V, T_A = + 25 °C

*2: V_{CC} = 5.5 V, T_A = + 85 °C (unless otherwise specified)

*3: P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*5: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

- See “24.4 AC Characteristics: Clock Timing” for F_{CH} and F_{CL}.
- See “24.4 AC Characteristics: Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

*6: In sub-CR clock mode, the power supply current value is the sum of adding I_{CRL} to I_{CCLS} or I_{CC}T. In addition, when the sub-CR clock mode is selected with F_{MPL} being 50 kHz, the current consumption increases accordingly.

24.4 AC Characteristics

24.4.1 Clock Timing

($V_{CC} = 2.4\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

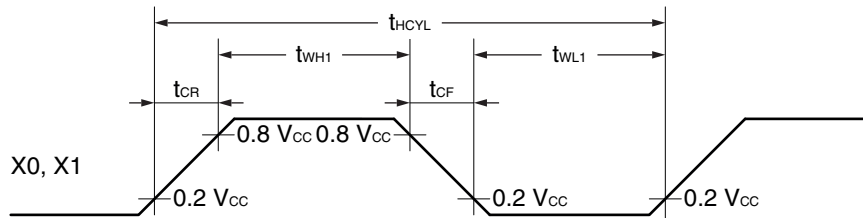
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks | |
|-----------------|---------------------|----------|-----------|-------|-------|--------|-------|---|--|
| | | | | Min | Typ | Max | | | |
| Clock frequency | F _{CH} | X0, X1 | — | 1 | — | 16.25 | MHz | When the main oscillation circuit is used | |
| | | X0 | X1: open | 1 | — | 12 | MHz | When the main external clock is used | |
| | | X0, X1 | * | 1 | — | 32.5 | MHz | When the main external clock is used | |
| | F _{CRH} | — | — | — | 3.92 | 4 | 4.08 | MHz | Operating conditions • The main CR clock is used. • $0\text{ }^\circ\text{C} \leq T_A \leq +70\text{ }^\circ\text{C}$ |
| | | | | | 3.8 | 4 | 4.2 | MHz | Operating conditions • The main CR clock is used. • $-40\text{ }^\circ\text{C} \leq T_A < 0\text{ }^\circ\text{C}$, $+70\text{ }^\circ\text{C} < T_A \leq +85\text{ }^\circ\text{C}$ |
| | F _{MCRPLL} | — | — | — | 7.84 | 8 | 8.16 | MHz | Operating conditions • PLL multiplication rate: 2 • $0\text{ }^\circ\text{C} \leq T_A \leq +70\text{ }^\circ\text{C}$ |
| | | | | | 7.6 | 8 | 8.4 | MHz | Operating conditions • PLL multiplication rate: 2 • $-40\text{ }^\circ\text{C} \leq T_A < 0\text{ }^\circ\text{C}$, $+70\text{ }^\circ\text{C} < T_A \leq +85\text{ }^\circ\text{C}$ |
| | | | | | 9.8 | 10 | 10.2 | MHz | Operating conditions • PLL multiplication rate: 2.5 • $0\text{ }^\circ\text{C} \leq T_A \leq +70\text{ }^\circ\text{C}$ |
| | | | | | 9.5 | 10 | 10.5 | MHz | Operating conditions • PLL multiplication rate: 2.5 • $-40\text{ }^\circ\text{C} \leq T_A < 0\text{ }^\circ\text{C}$, $+70\text{ }^\circ\text{C} < T_A \leq +85\text{ }^\circ\text{C}$ |
| | | | | | 11.76 | 12 | 12.24 | MHz | Operating conditions • PLL multiplication rate: 3 • $0\text{ }^\circ\text{C} \leq T_A \leq +70\text{ }^\circ\text{C}$ |
| | | | | | 11.4 | 12 | 12.6 | MHz | Operating conditions • PLL multiplication rate: 3 • $-40\text{ }^\circ\text{C} \leq T_A < 0\text{ }^\circ\text{C}$, $+70\text{ }^\circ\text{C} < T_A \leq +85\text{ }^\circ\text{C}$ |
| | | | | | 15.68 | 16 | 16.32 | MHz | Operating conditions • PLL multiplication rate: 4 • $0\text{ }^\circ\text{C} \leq T_A \leq +70\text{ }^\circ\text{C}$ |
| | | | | | 15.2 | 16 | 16.8 | MHz | Operating conditions • PLL multiplication rate: 4 • $-40\text{ }^\circ\text{C} \leq T_A < 0\text{ }^\circ\text{C}$, $+70\text{ }^\circ\text{C} < T_A \leq +85\text{ }^\circ\text{C}$ |
| | F _{CL} | X0A, X1A | — | — | — | 32.768 | — | kHz | When the suboscillation circuit is used |
| | | | | | — | 32.768 | — | kHz | When the sub-external clock is used |
| | F _{CRL} | — | — | — | 50 | 100 | 150 | kHz | When the sub-CR clock is used |

($V_{CC} = 2.4\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

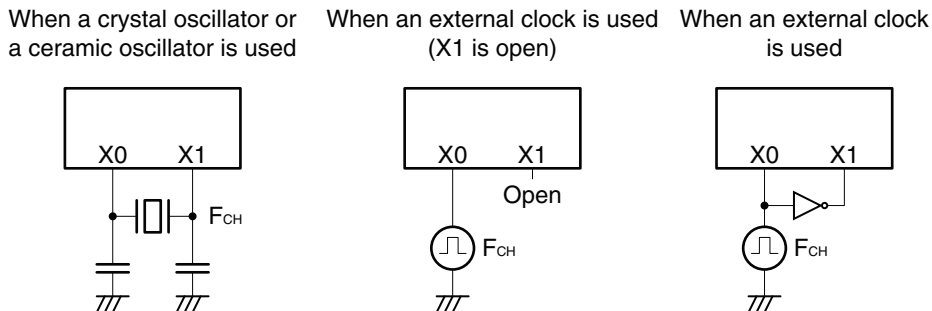
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--|--------------------------|---------------------|-----------|-------|------|------|---------------|--|
| | | | | Min | Typ | Max | | |
| Clock cycle time | t_{HCYL} | X0, X1 | — | 61.5 | — | 1000 | ns | When the main oscillation circuit is used |
| | | X0 | X1: open | 83.4 | — | 1000 | ns | When an external clock is used |
| | | X0, X1 | * | 30.8 | — | 1000 | ns | |
| | t_{LCYL} | X0A, X1A | — | — | 30.5 | — | μs | When the subclock is used |
| Input clock pulse width | t_{WH1} , t_{WL1} | X0 | X1: open | 33.4 | — | — | ns | When an external clock is used, the duty ratio should range between 40% and 60%. |
| | | X0, X1 | * | 12.4 | — | — | ns | |
| | t_{WH2} , t_{WL2} | X0A | — | — | 15.2 | — | μs | |
| Input clock rising time and falling time | t_{CR} , t_{CF} | X0, X0A | X1: open | — | — | 5 | ns | When an external clock is used |
| | | X0, X1, X0A, X1A | * | — | — | 5 | ns | |
| CR oscillation start time | t_{CRHWK} | — | — | — | — | 50 | μs | When the main CR clock is used |
| | t_{CRLWK} | — | — | — | — | 30 | μs | When the sub-CR clock is used |

*: The external clock signal is input to X0 and the inverted external clock signal to X1.

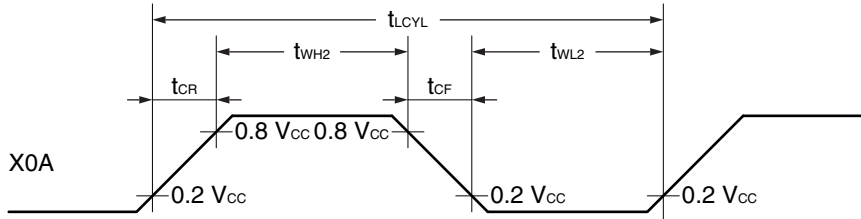
• Input waveform generated when an external clock (main clock) is used



• Figure of main clock input port external connection

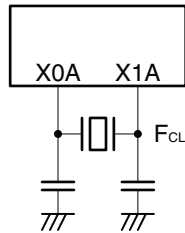


- Input waveform generated when an external clock (subclock) is used

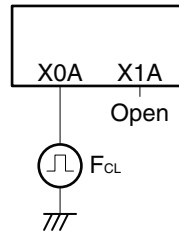


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When an external clock is used



24.4.2 Source Clock / Machine Clock

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|--|-------------------|----------|--------|-----|--------|---------------------------------------|---|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | t _{SCLK} | — | 61.5 | — | 2000 | ns | When the main external clock is used Min: F _{CH} = 32.5 MHz, divided by 2 Max: F _{CH} = 1 MHz, divided by 2 |
| | | | 62.5 | — | 1000 | ns | When the main CR clock is used Min: F _{CRH} = 4 MHz, multiplied by 4 Max: F _{CRH} = 4 MHz, divided by 4 |
| | | | — | 61 | — | μs | When the suboscillation clock is used F _{CL} = 32.768 kHz, divided by 2 |
| | | | — | 20 | — | μs | When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2 |
| Source clock frequency | F _{SP} | — | 0.5 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | — | 4 | — | MHz | When the main CR clock is used |
| | — | | 16.384 | — | kHz | When the suboscillation clock is used | |
| | F _{SPL} | | — | 50 | — | kHz | When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2 |
| — | | — | — | — | — | — | |
| Machine clock cycle time*2 (minimum instruction execution time) | t _{MCLK} | — | 61.5 | — | 32000 | ns | When the main oscillation clock is used Min: F _{SP} = 16.25 MHz, no division Max: F _{SP} = 0.5 MHz, divided by 16 |
| | | | 250 | — | 1000 | ns | When the main CR clock is used Min: F _{SP} = 4 MHz, no division Max: F _{SP} = 4 MHz, divided by 4 |
| | | | 61 | — | 976.5 | μs | When the suboscillation clock is used Min: F _{SPL} = 16.384 kHz, no division Max: F _{SPL} = 16.384 kHz, divided by 16 |
| | | | 20 | — | 320 | μs | When the sub-CR clock is used Min: F _{SPL} = 50 kHz, no division Max: F _{SPL} = 50 kHz, divided by 16 |
| Machine clock frequency | F _{MP} | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.25 | — | 16 | MHz | When the main CR clock is used |
| | F _{MPL} | | 1.024 | — | 16.384 | kHz | When the suboscillation clock is used |
| | | | 3.125 | — | 50 | kHz | When the sub-CR clock is used F _{CRL} = 100 kHz |

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

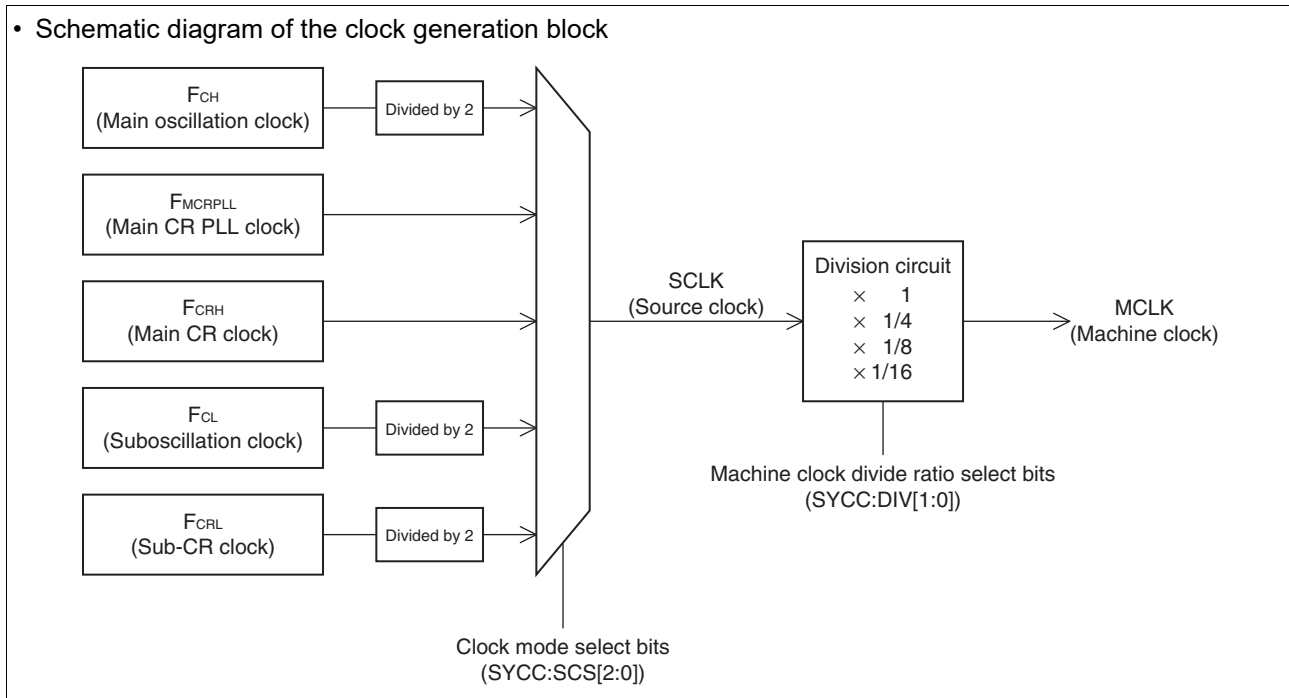
- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

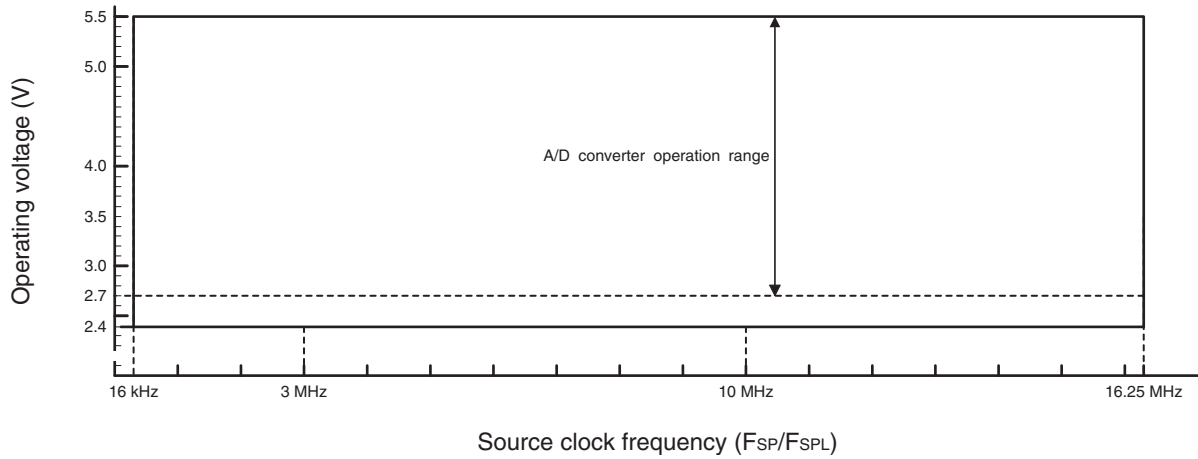


• Schematic diagram of the clock generation block

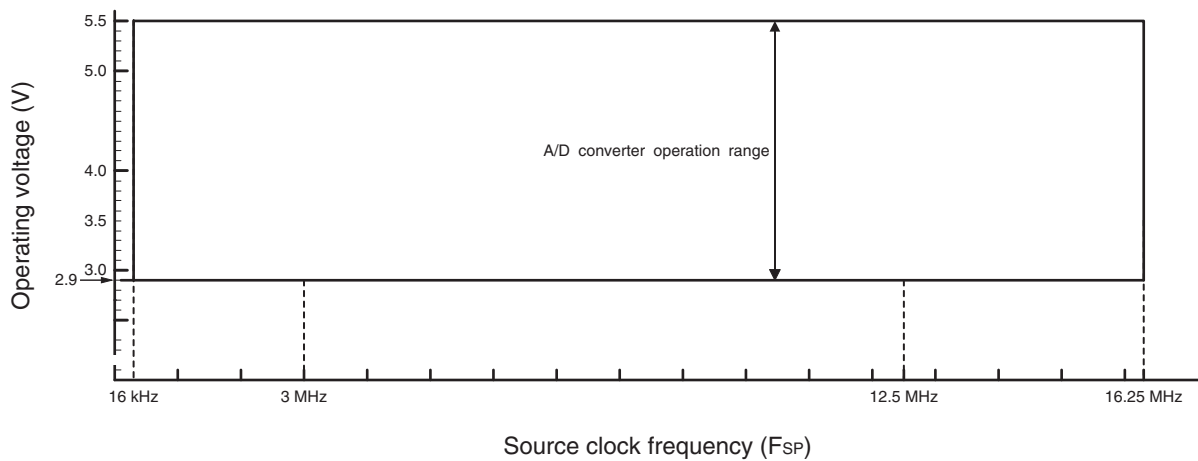




- Operating voltage - Operating frequency ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)
Without the on-chip debug function



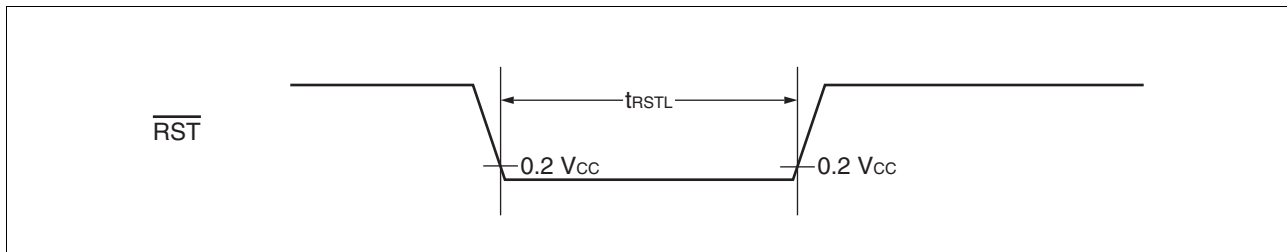
- Operating voltage - Operating frequency ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)
With the on-chip debug function



24.4.3 External Reset

 ($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

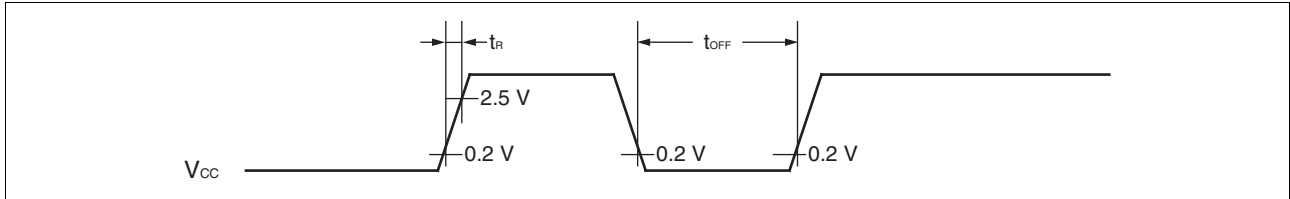
| Parameter | Symbol | Value | | Unit | Remarks |
|---------------------------|------------|-------------------|-----|------|---------------------|
| | | Min | Max | | |
| RST "L" level pulse width | t_{RSTL} | $2 t_{MCLK}^{*1}$ | — | ns | In normal operation |

 *1: See "Source Clock / Machine Clock" for t_{MCLK} .


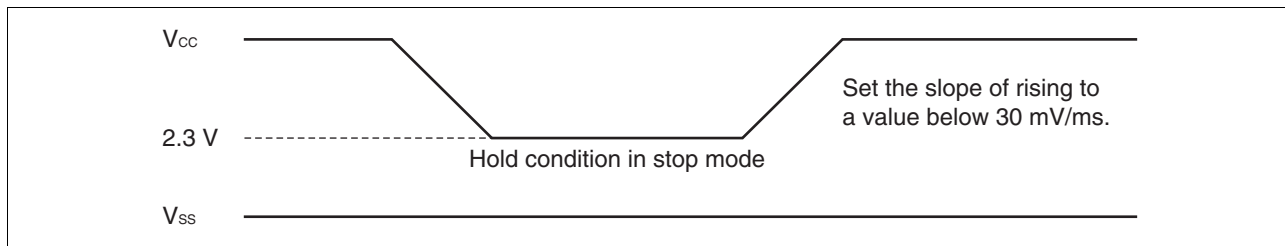
24.4.4 Power-on Reset

($V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|--------------------------|-----------|-----------|-------|-----|------|--------------------------|
| | | | Min | Max | | |
| Power supply rising time | t_R | — | — | 50 | ms | |
| Power supply cutoff time | t_{OFF} | — | 1 | — | ms | Wait time until power-on |



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



24.4.5 Peripheral Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

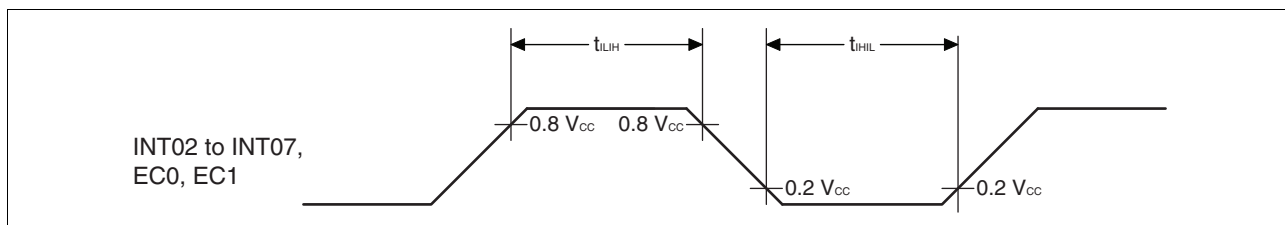
| Parameter | Symbol | Pin name | Value | | Unit |
|----------------------------------|----------|-----------------------------------|--------------------------|-----|------|
| | | | Min | Max | |
| Peripheral input "H" pulse width | t_{LH} | INT02 to INT07*1,*2, EC0*1, EC1*3 | $2\text{ }t_{MCLK}^{*4}$ | — | ns |
| Peripheral input "L" pulse width | t_{HL} | | $2\text{ }t_{MCLK}^{*4}$ | — | ns |

*1: INT04, INT06 and EC0 are available on all products.

*2: INT02, INT03, INT05 and INT07 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*3: EC1 is only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: See "Source Clock / Machine Clock" for t_{MCLK} .



24.4.6 LIN-UART Timing (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)

Sampling is executed at the rising edge of the sampling clock*¹, and serial clock delay is disabled*².
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

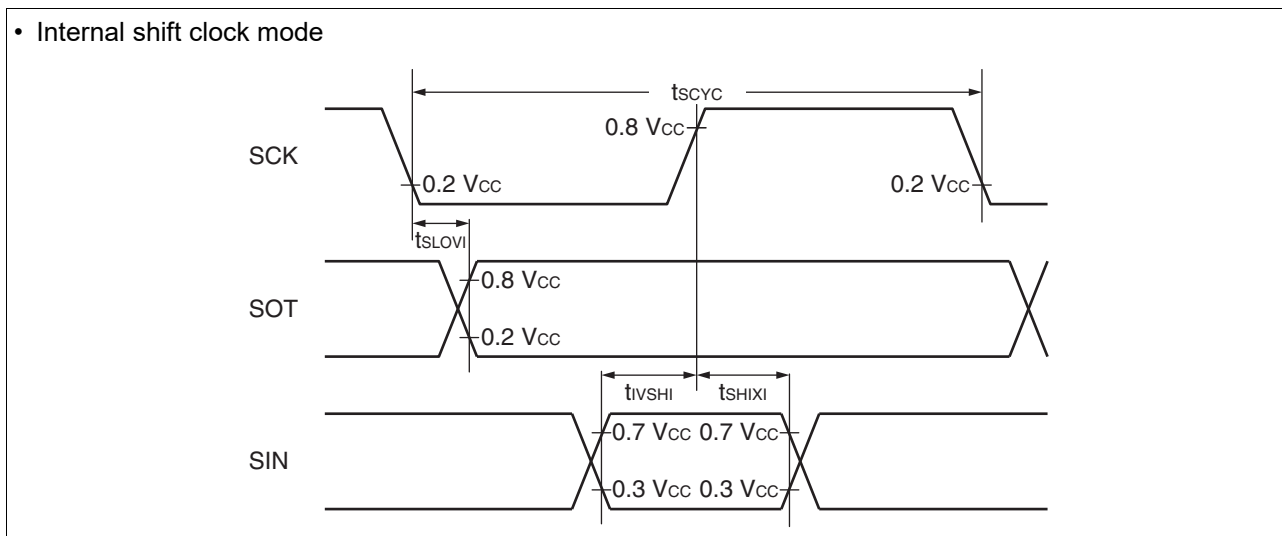
(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|------------------------------|--------------------|----------|--|---|---|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin: C _L = 80 pF + 1 TTL | 5 t _{MCLK} * ³ | — | ns |
| SCK ↓→ SOT delay time | t _{SLOVI} | SCK, SOT | | -50 | +50 | ns |
| Valid SIN → SCK ↑ | t _{IVSHI} | SCK, SIN | | t _{MCLK} * ³ + 80 | — | ns |
| SCK ↑→ valid SIN hold time | t _{SHIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "L" pulse width | t _{SLSH} | SCK | External clock operation output pin: C _L = 80 pF + 1 TTL | 3 t _{MCLK} * ³ - t _R | — | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK | | t _{MCLK} * ³ + 10 | — | ns |
| SCK ↓→ SOT delay time | t _{SLOVE} | SCK, SOT | | — | 2 t _{MCLK} * ³ + 60 | ns |
| Valid SIN → SCK ↑ | t _{IVSHE} | SCK, SIN | | 30 | — | ns |
| SCK ↑→ valid SIN hold time | t _{SHIXE} | SCK, SIN | | t _{MCLK} * ³ + 30 | — | ns |
| SCK fall time | t _F | SCK | | — | 10 | ns |
| SCK rise time | t _R | SCK | | — | 10 | ns |

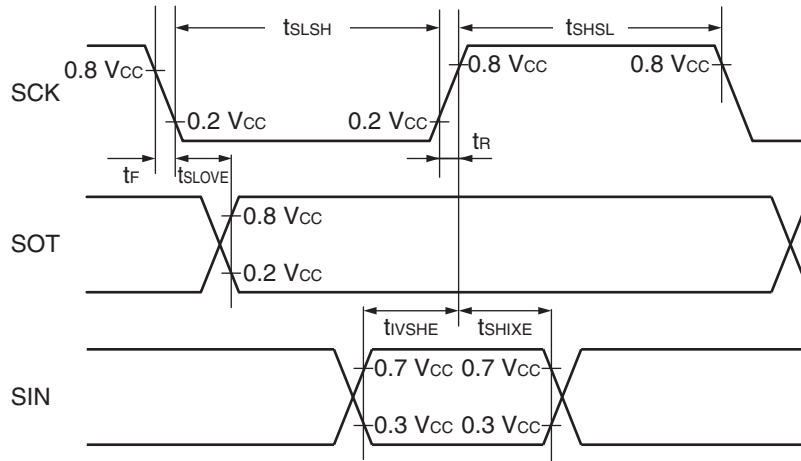
*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See "Source Clock / Machine Clock" for t_{MCLK}.



• External shift clock mode



Sampling is executed at the falling edge of the sampling clock*¹, and serial clock delay is disabled*².
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|---|--------------------------|-------------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$ | $5\ t_{MCLK}^{*3}$ | — | ns |
| SCK $\uparrow \rightarrow$ SOT delay time | t_{SHOVI} | SCK, SOT | | -50 | +50 | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLI} | SCK, SIN | | $t_{MCLK}^{*3} + 80$ | — | ns |
| SCK $\downarrow \rightarrow$ valid SIN hold time | t_{SLIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$ | $3\ t_{MCLK}^{*3} - t_R$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK | | $t_{MCLK}^{*3} + 10$ | — | ns |
| SCK $\uparrow \rightarrow$ SOT delay time | t_{SHOVE} | SCK, SOT | | — | $2\ t_{MCLK}^{*3} + 60$ | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLE} | SCK, SIN | | 30 | — | ns |
| SCK $\downarrow \rightarrow$ valid SIN hold time | t_{SLIXE} | SCK, SIN | | $t_{MCLK}^{*3} + 30$ | — | ns |
| SCK fall time | t_F | SCK | | — | 10 | ns |
| SCK rise time | t_R | SCK | | — | 10 | ns |

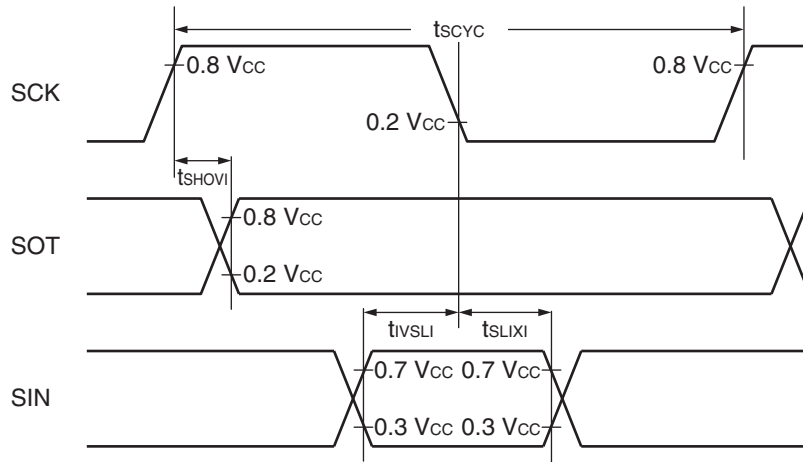
*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

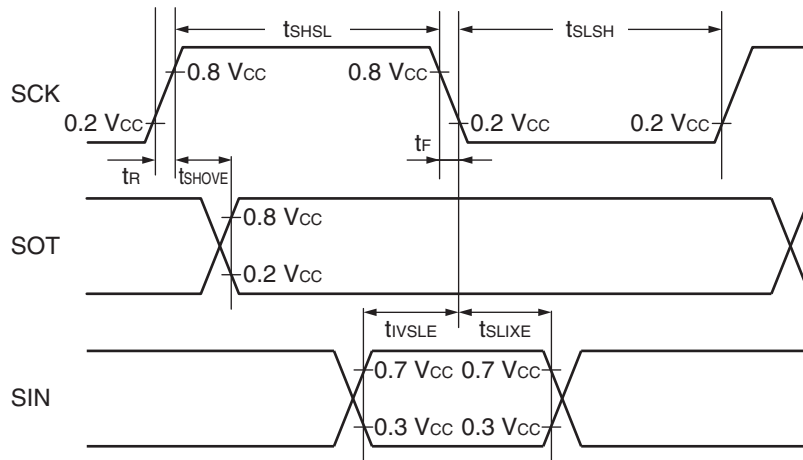
*3: See "Source Clock / Machine Clock" for t_{MCLK} .



• Internal shift clock mode



• External shift clock mode



Sampling is executed at the rising edge of the sampling clock*¹, and serial clock delay is enabled*².
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

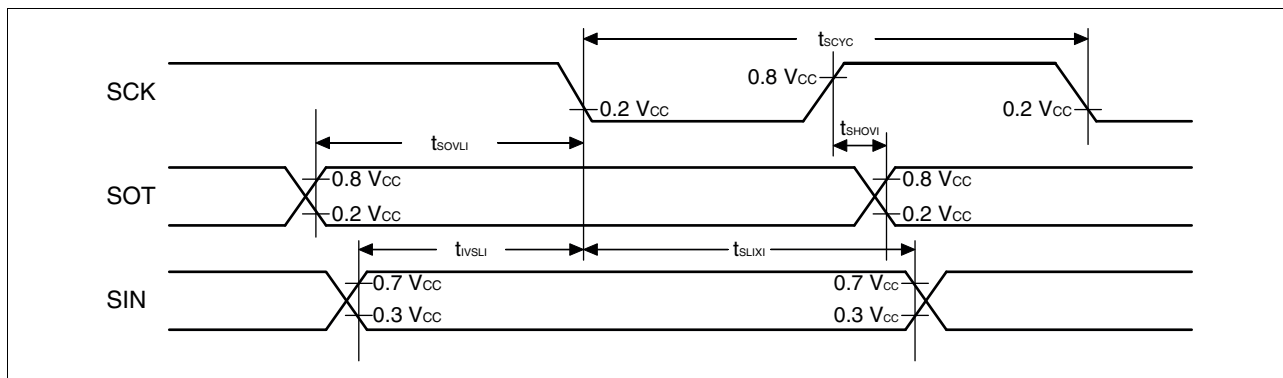
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|-----------------------------|--------------------|----------|---|---|-----|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operation output pin: C _L = 80 pF + 1 TTL | 5 t _{MCLK} * ³ | — | ns |
| SCK ↑ → SOT delay time | t _{SHOVI} | SCK, SOT | | -50 | +50 | ns |
| Valid SIN → SCK ↓ | t _{IVSLI} | SCK, SIN | | t _{MCLK} * ³ + 80 | — | ns |
| SCK ↓ → valid SIN hold time | t _{SLIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↓ delay time | t _{SOVLI} | SCK, SOT | | 3 t _{MCLK} * ³ - 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*¹, and serial clock delay is enabled*².
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

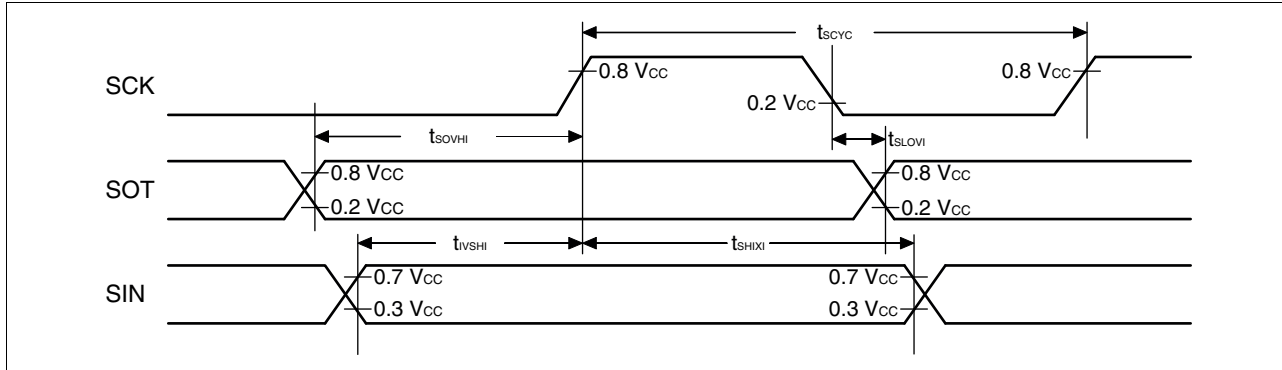
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|-----------------------------|--------------------|----------|---|---|-----|------|
| | | | | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK | Internal clock operating output pin: C _L = 80 pF + 1 TTL | 5 t _{MCLK} * ³ | — | ns |
| SCK ↓ → SOT delay time | t _{SLOVI} | SCK, SOT | | -50 | +50 | ns |
| Valid SIN → SCK ↑ | t _{IVSHI} | SCK, SIN | | t _{MCLK} * ³ + 80 | — | ns |
| SCK ↑ → valid SIN hold time | t _{SHIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↑ delay time | t _{SOVHI} | SCK, SOT | | 3 t _{MCLK} * ³ - 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.

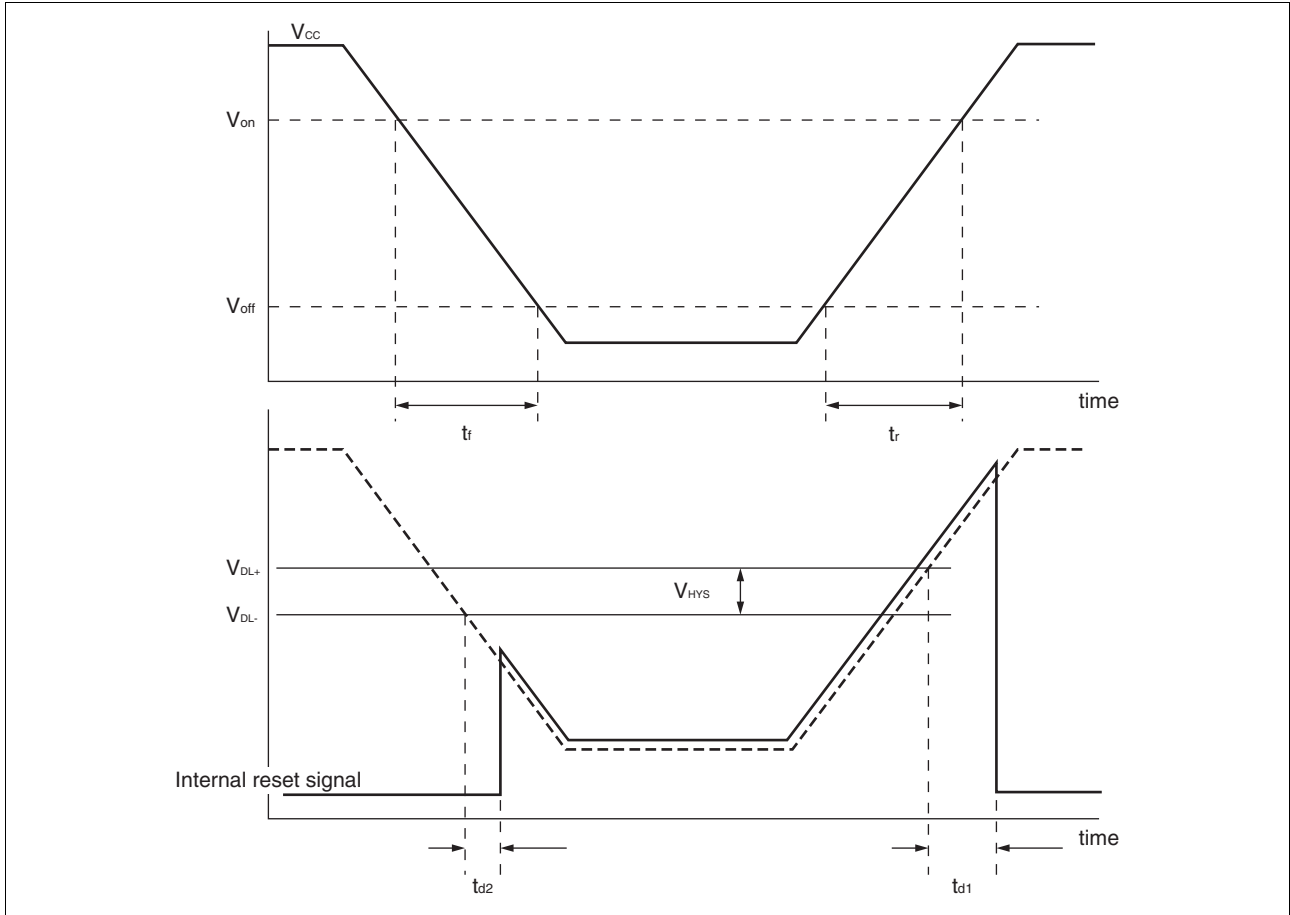


24.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|------------------|-------|-----|------|------|---|
| | | Min | Typ | Max | | |
| Release voltage* | V _{DL+} | 2.52 | 2.7 | 2.88 | V | At power supply rise |
| | | 2.61 | 2.8 | 2.99 | | |
| | | 2.89 | 3.1 | 3.31 | | |
| | | 3.08 | 3.3 | 3.52 | | |
| Detection voltage* | V _{DL-} | 2.43 | 2.6 | 2.77 | V | At power supply fall |
| | | 2.52 | 2.7 | 2.88 | | |
| | | 2.80 | 3 | 3.20 | | |
| | | 2.99 | 3.2 | 3.41 | | |
| Hysteresis width | V _{HYS} | — | 100 | — | mV | |
| Power supply start voltage | V _{off} | — | — | 2.3 | V | |
| Power supply end voltage | V _{on} | 4.9 | — | — | V | |
| Power supply voltage change time (at power supply rise) | t _r | 650 | — | — | μs | Slope of power supply that the reset release signal generates within the rating (V _{DL+}) |
| Power supply voltage change time (at power supply fall) | t _r | 650 | — | — | μs | Slope of power supply that the reset detection signal generates within the rating (V _{DL-}) |
| Reset release delay time | t _{d1} | — | — | 30 | μs | |
| Reset detection delay time | t _{d2} | — | — | 30 | μs | |
| LVD threshold voltage transition stabilization time | t _{stb} | 10 | — | — | μs | |

*: The release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDR register, refer to “CHAPTER 18 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95560H/570H/580H Hardware Manual”.



24.5 A/D Converter

24.5.1 A/D Converter Electrical Characteristics

($V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+85\text{ °C}$)

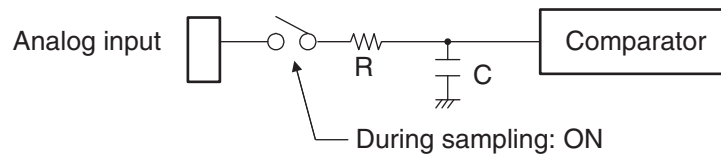
| Parameter | Symbol | Value | | | Unit | Remarks |
|-------------------------------|-----------|---------------------------|---------------------------|---------------------------|---------------|--|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | -3 | — | +3 | LSB | |
| Linearity error | | -2.5 | — | +2.5 | LSB | |
| Differential linearity error | | -1.9 | — | +1.9 | LSB | |
| Zero transition voltage | V_{0T} | $V_{SS} - 1.5\text{ LSB}$ | $V_{SS} + 0.5\text{ LSB}$ | $V_{SS} + 2.5\text{ LSB}$ | V | |
| Full-scale transition voltage | V_{FST} | $V_{CC} - 4.5\text{ LSB}$ | $V_{CC} - 2\text{ LSB}$ | $V_{CC} + 0.5\text{ LSB}$ | V | |
| Compare time | — | 1 | — | 10 | μs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ |
| | | 3 | — | 10 | μs | $2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$ |
| Sampling time | — | 0.6 | — | ∞ | μs | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, with external impedance $< 3.3\text{ k}\Omega$ |
| Analog input current | I_{AIN} | -0.3 | — | +0.3 | μA | |
| Analog input voltage | V_{AIN} | V_{SS} | — | V_{CC} | V | |

24.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

The A/D converter of the MB95560H/570H/580H has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μF to the analog input pin.

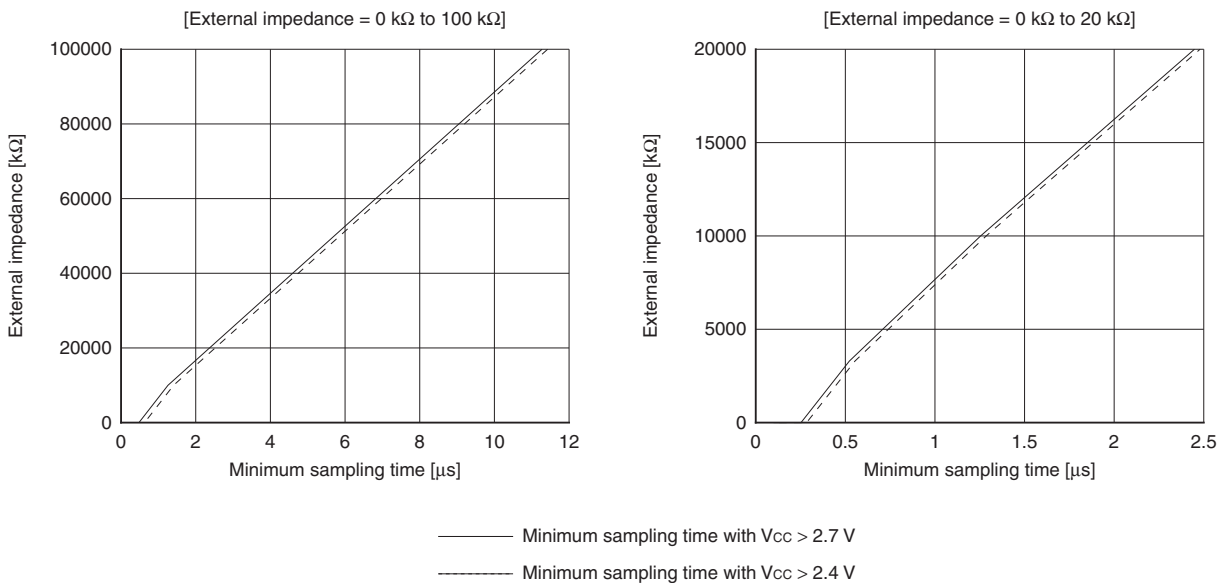
- Analog input equivalent circuit



| V _{CC} | R | C |
|---------------------------------|---------------|----------------|
| 4.5 V ≤ V _{CC} ≤ 5.5 V | 1.45 kΩ (Max) | 14.89 pF (Max) |
| 2.7 V ≤ V _{CC} < 4.5 V | 2.7 kΩ (Max) | 14.89 pF (Max) |

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time



- A/D conversion error

As $|V_{CC} - V_{SS}|$ decreases, the A/D conversion error increases proportionately.

24.5.3 Definitions of A/D Converter Terms

- Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

- Linearity error (unit: LSB)

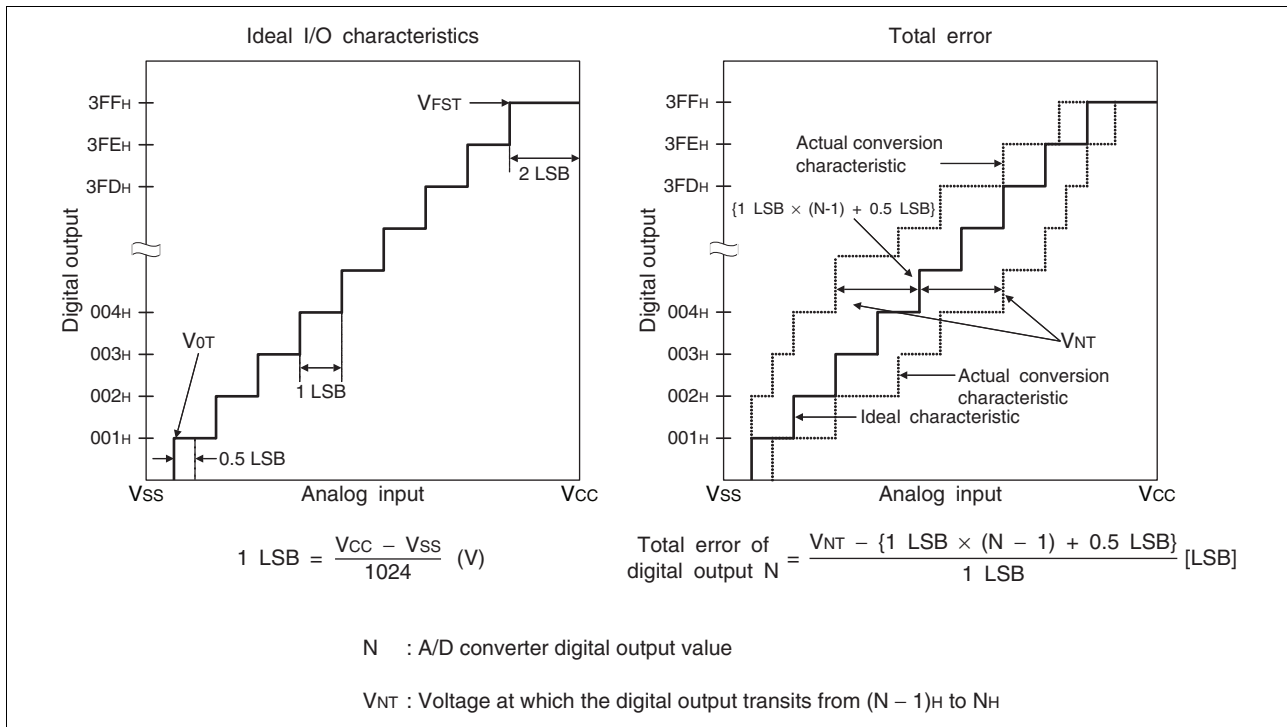
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“0000000000” ← → “0000000001”) of a device to the full-scale transition point (“1111111111” ← → “1111111110”) of the same device.

- Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

- Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.







24.6 Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|--|--------|-------|-------|-------|---|
| | Min | Typ | Max | | |
| Sector erase time (2 Kbyte sector) | — | 0.3*1 | 1.6*2 | s | The time of writing 00 _H prior to erasure is excluded. |
| Sector erase time (16 Kbyte sector) | — | 0.6*1 | 3.1*2 | s | The time of writing 00 _H prior to erasure is excluded. |
| Byte writing time | — | 17 | 272 | μs | System-level overhead is excluded. |
| Program/erase cycle | 100000 | — | — | cycle | |
| Power supply voltage at program/erase | 2.4 | — | 5.5 | V | |
| Flash memory data retention time | 5*3 | — | — | year | Average T _A = +85 °C |

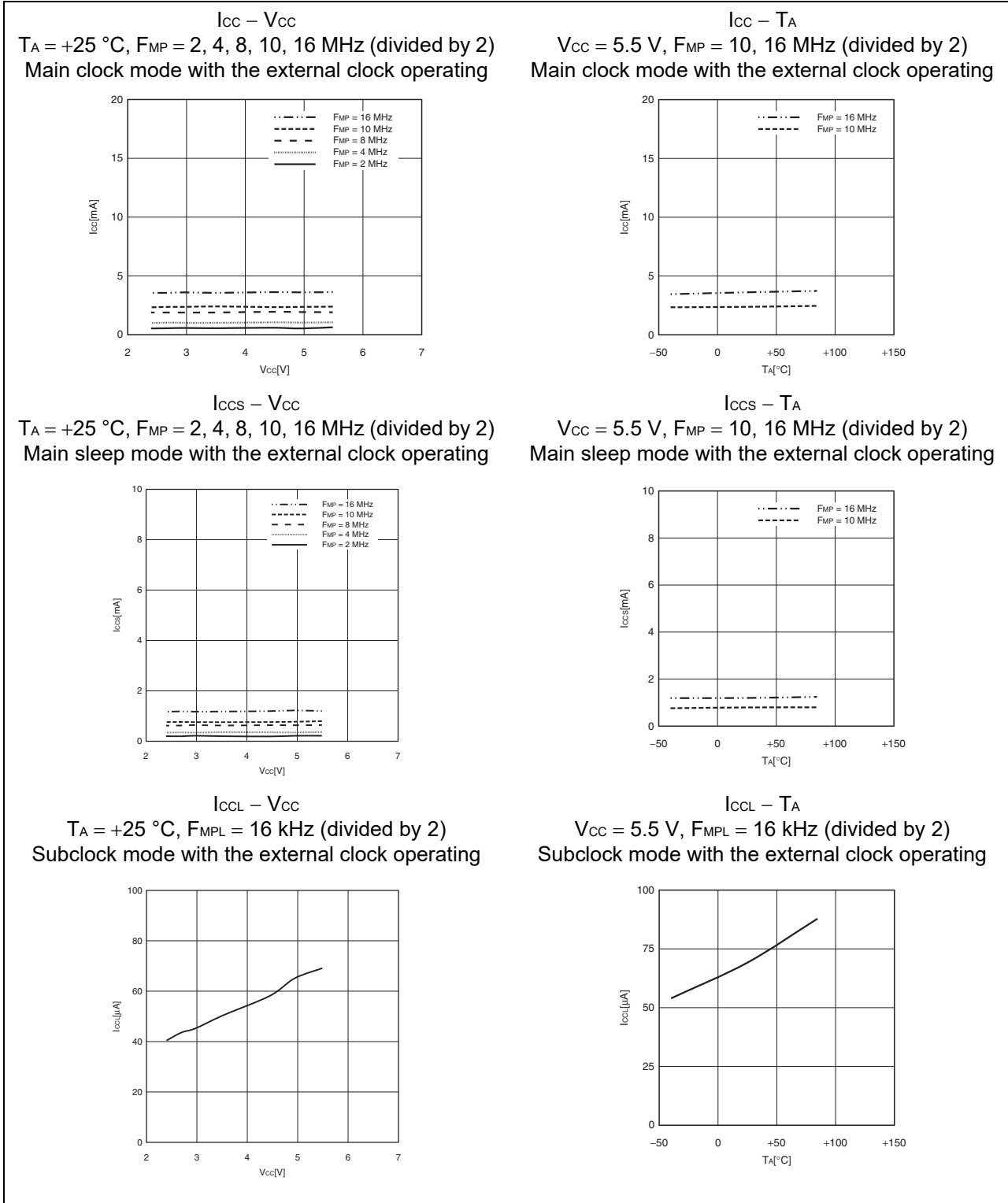
*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

*2: V_{CC} = 2.4 V, T_A = +85 °C, 100000 cycles

*3: This value was converted from the result of a technology reliability assessment. (The value was converted from the result of a high temperature accelerated test using the Arrhenius equation with an average temperature of +85 °C).

25. Sample Characteristics

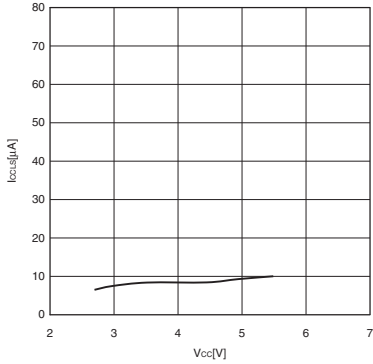
- Power supply current temperature characteristics





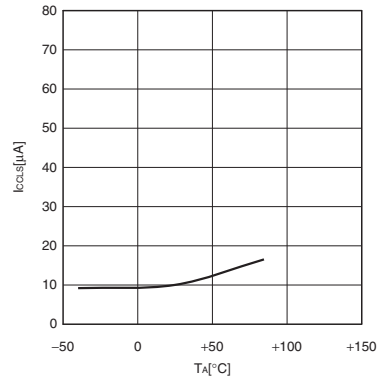
$I_{CCLS} - V_{CC}$

$T_A = +25\text{ }^\circ\text{C}$, $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



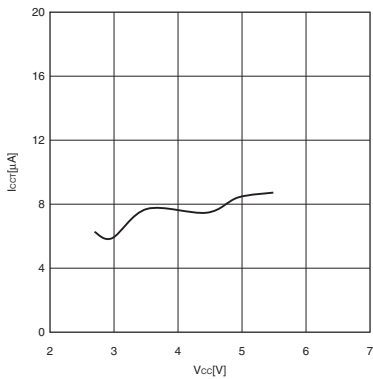
$I_{CCLS} - T_A$

$V_{CC} = 5.5\text{ V}$, $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



$I_{CCT} - V_{CC}$

$T_A = +25\text{ }^\circ\text{C}$, $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



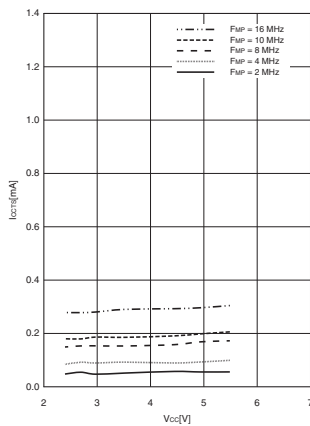
$I_{CCT} - T_A$

$V_{CC} = 5.5\text{ V}$, $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



$I_{CCTS} - V_{CC}$

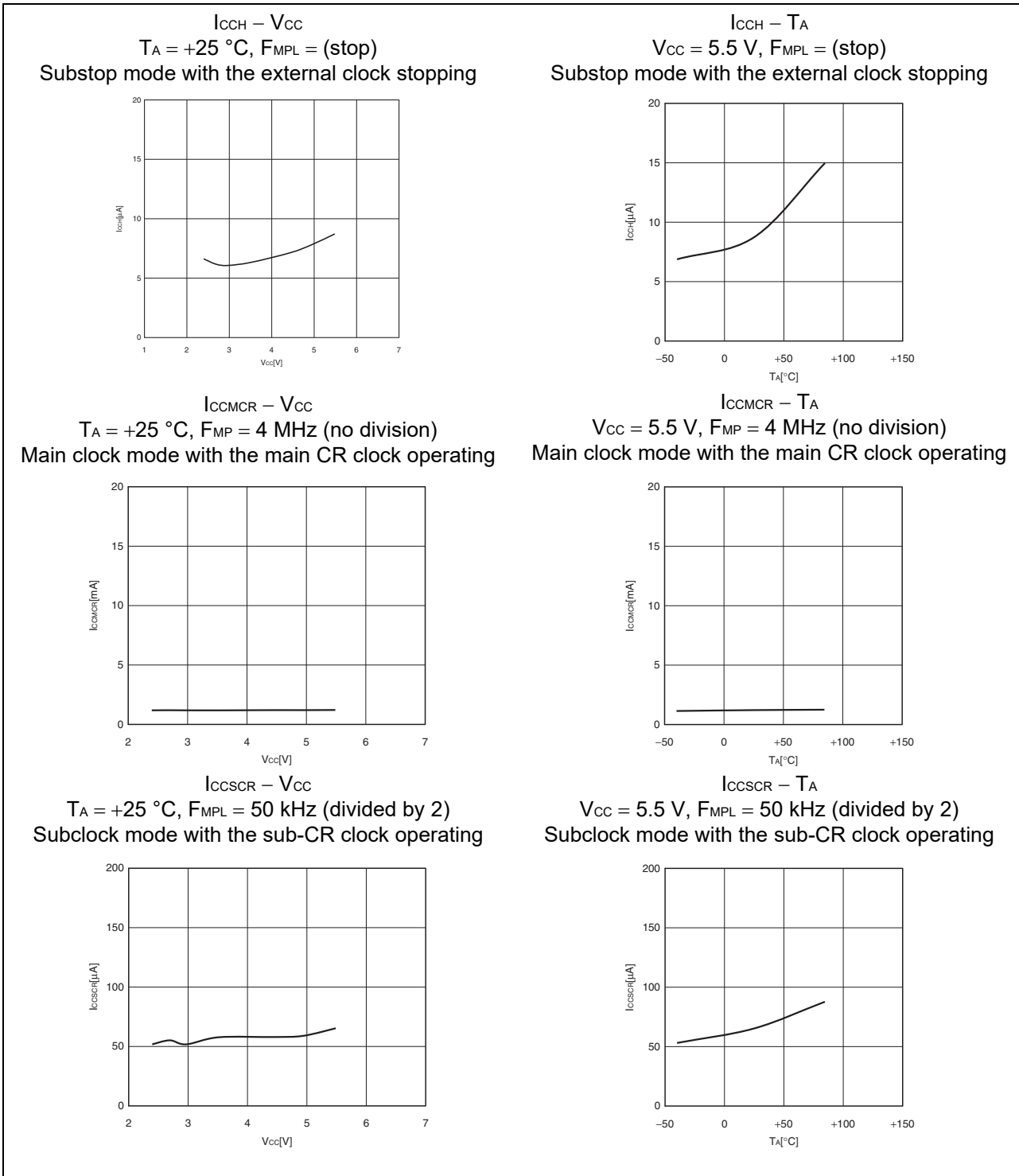
$T_A = +25\text{ }^\circ\text{C}$, $F_{MP} = 2, 4, 8, 10, 16\text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating



$I_{CCTS} - T_A$

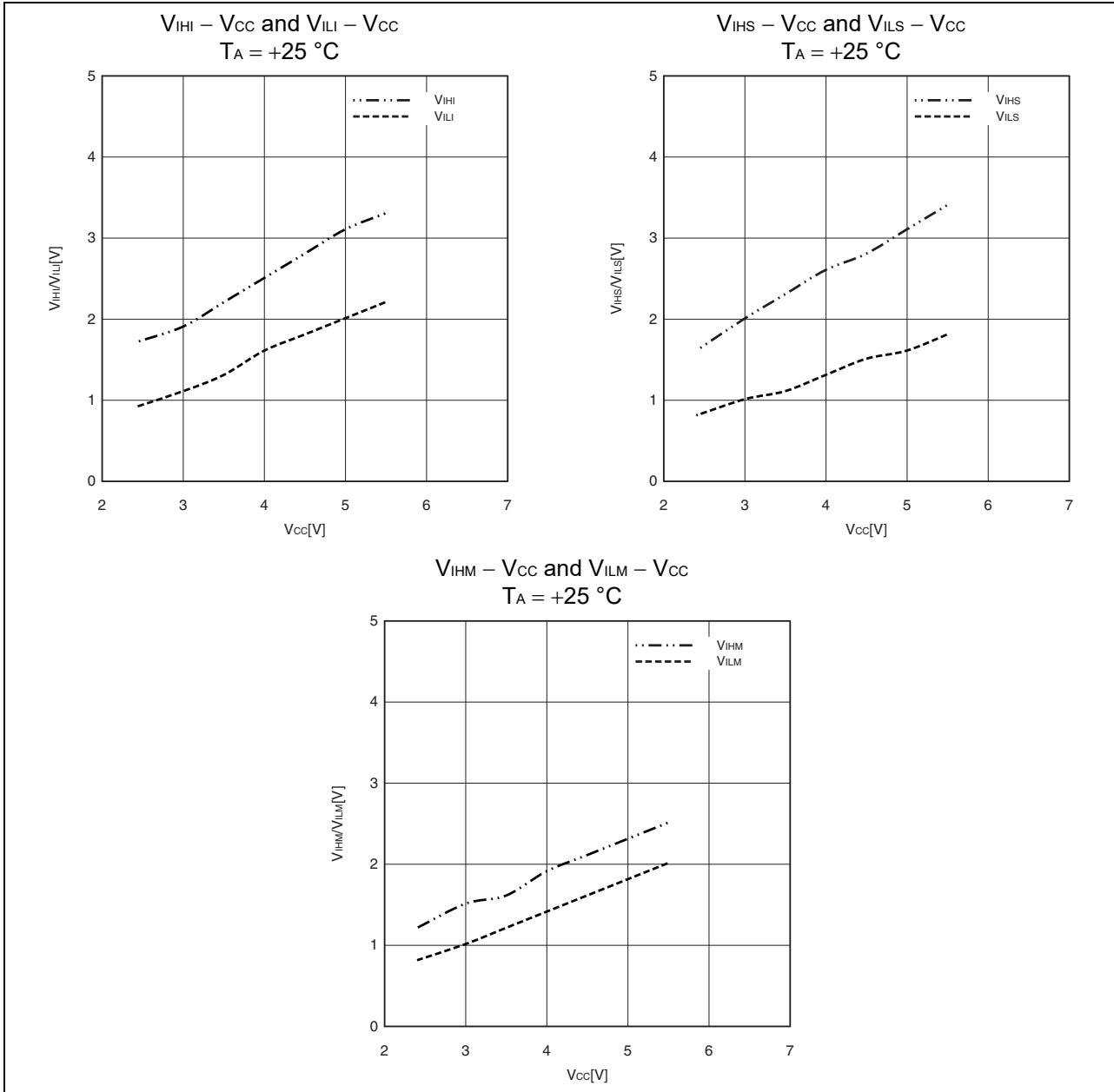
$V_{CC} = 5.5\text{ V}$, $F_{MP} = 10, 16\text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating



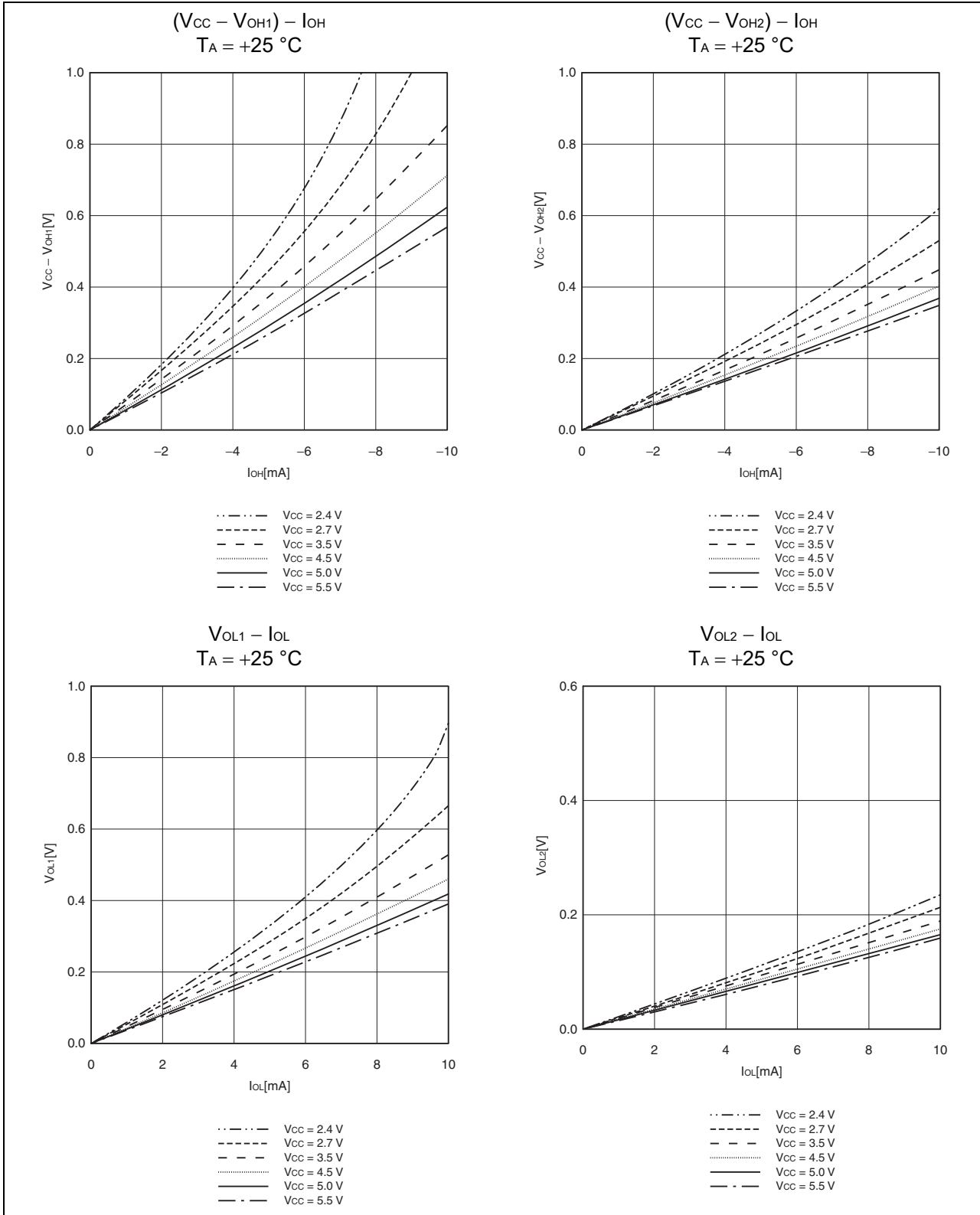




• Input voltage characteristics

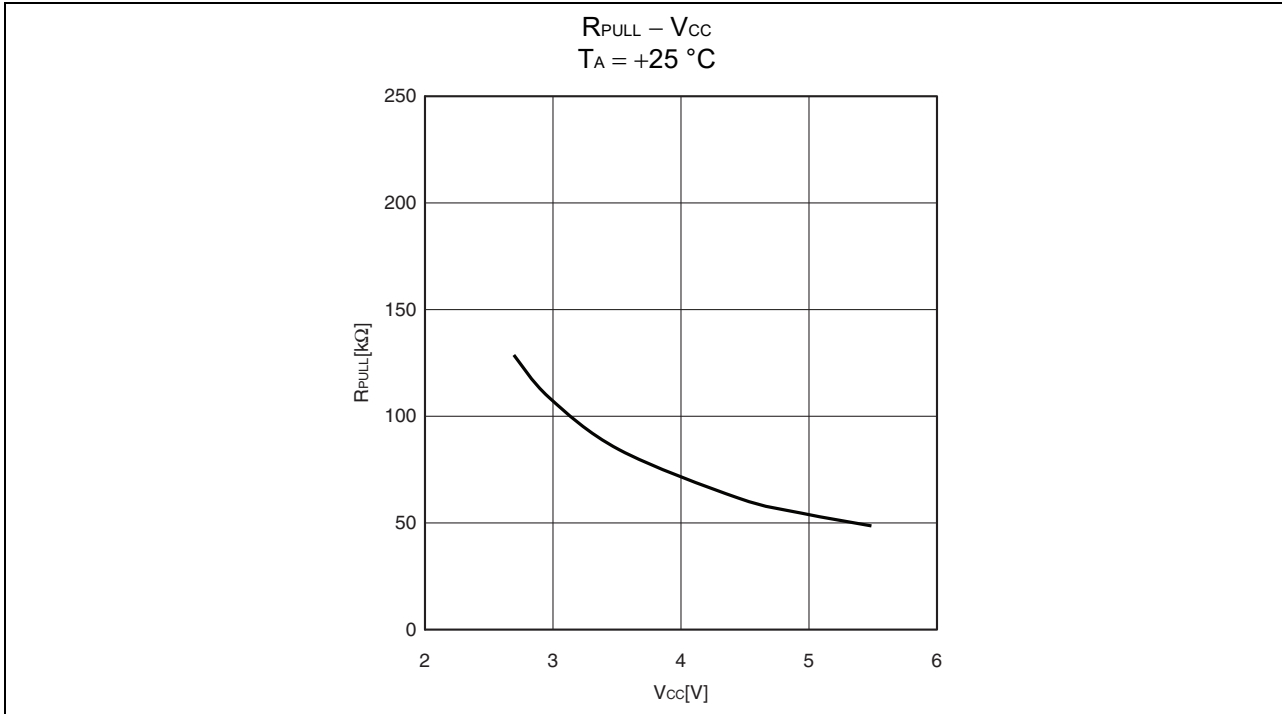


• Output voltage characteristics





• Pull-up characteristics



26. Mask Options

| No. | Part Number | MB95F562H | MB95F562K |
|-------------------------|-----------------------------|-------------------------------------|----------------------------------|
| | | MB95F563H | MB95F563K |
| | | MB95F564H | MB95F564K |
| | | MB95F572H | MB95F572K |
| | | MB95F573H | MB95F573K |
| | | MB95F574H | MB95F574K |
| | | MB95F582H | MB95F582K |
| | | MB95F583H | MB95F583K |
| | | MB95F584H | MB95F584K |
| Selectable/Fixed | | Fixed | |
| 1 | Low-voltage detection reset | Without low-voltage detection reset | With low-voltage detection reset |
| 2 | Reset | With dedicated reset input | Without dedicated reset input |

27. Ordering Information

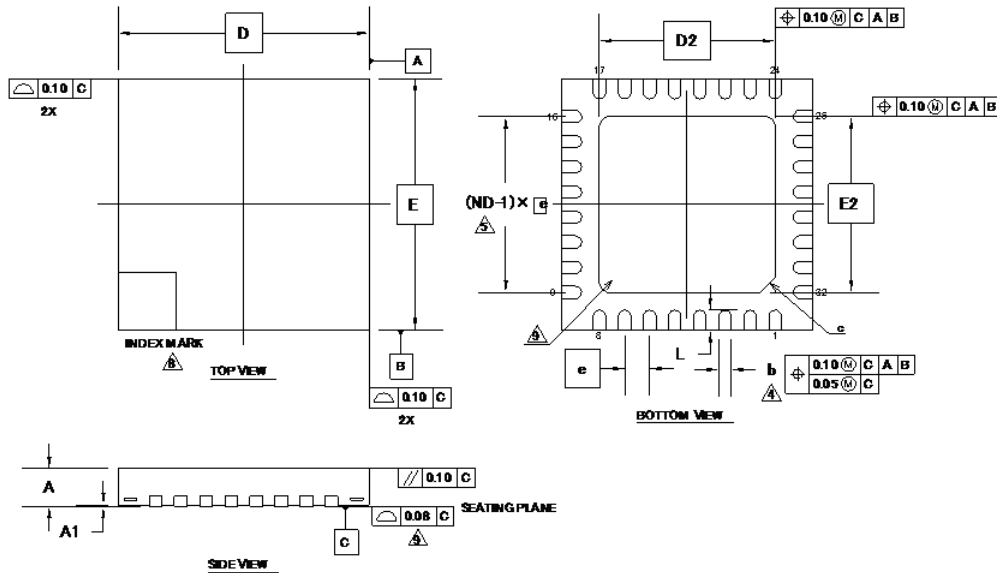
| Part number | Package | Packing |
|--|----------------------------------|---------|
| MB95F562HWQN-G-SNE1 MB95F562KWQN-G-SNE1 MB95F563HWQN-G-SNE1 MB95F563KWQN-G-SNE1 MB95F564HWQN-G-SNE1 MB95F564KWQN-G-SNE1 | 32-pin plastic QFN (WNP032) | Tray |
| MB95F562HWQN-G-SNERE1 MB95F562KWQN-G-SNERE1 MB95F563HWQN-G-SNERE1 MB95F563KWQN-G-SNERE1 MB95F564HWQN-G-SNERE1 MB95F564KWQN-G-SNERE1 | | Reel |
| MB95F562HPF-G-SNE2 MB95F562KPF-G-SNE2 MB95F563HPF-G-SNE2 MB95F563KPF-G-SNE2 MB95F564HPF-G-SNE2 MB95F564KPF-G-UNE2 | 20-pin plastic SOP (SOJ020) | Tube |
| MB95F562HPFT-G-SNE2 MB95F562KPFT-G-SNE2 MB95F563HPFT-G-SNE2 MB95F563KPFT-G-SNE2 MB95F564HPFT-G-SNE2 MB95F564KPFT-G-UNE2 | 20-pin plastic TSSOP (STG020) | Tube |
| MB95F562KPFT-G-UNERE2 MB95F563HPFT-G-UNERE2 MB95F563KPFT-G-UNERE2 MB95F564KPFT-G-UNERE2 | | Reel |
| MB95F582HWQN-G-SNE1 MB95F582KWQN-G-SNE1 MB95F583HWQN-G-SNE1 MB95F583KWQN-G-SNE1 MB95F584HWQN-G-SNE1 MB95F584KWQN-G-SNE1 | 32-pin plastic QFN (WNP032) | Tray |
| MB95F582HWQN-G-SNERE1 MB95F582KWQN-G-SNERE1 MB95F583HWQN-G-SNERE1 MB95F583KWQN-G-SNERE1 MB95F584HWQN-G-SNERE1 MB95F584KWQN-G-SNERE1 | | Reel |
| MB95F582HPFT-G-SNE2 MB95F582KPFT-G-SNE2 MB95F583HPFT-G-SNE2 MB95F583KPFT-G-SNE2 MB95F584HPFT-G-SNE2 MB95F584KPFT-G-SNE2 | 16-pin plastic TSSOP (STB016) | Tube |



| Part number | Package | Packing |
|--|-------------------------------|---------|
| MB95F582HPF-G-SNE2 MB95F582KPF-G-SNE2 MB95F583HPF-G-SNE2 MB95F583KPF-G-SNE2 MB95F584HPF-G-SNE2 MB95F584KPF-G-SNE2 | 16-pin plastic SOP (SO016) | Tube |
| MB95F572HPH-G-SNE2 MB95F572KPH-G-SNE2 MB95F573HPH-G-SNE2 MB95F573KPH-G-SNE2 MB95F574HPH-G-SNE2 MB95F574KPH-G-SNE2 | 8-pin plastic DIP (PDA008) | Tube |
| MB95F572HPF-G-SNE2 MB95F572KPF-G-SNE2 MB95F573HPF-G-SNE2 MB95F573KPF-G-SNE2 MB95F574HPF-G-SNE2 MB95F574KPF-G-SNE2 | 8-pin plastic SOP (SOD008) | Tube |

28. Package Dimension

| Package Type | Package Code |
|--------------|--------------|
| QFN 32 | WNP032 |



| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 0.80 |
| A1 | 0.00 | — | 0.05 |
| D | 5.00 BSC | | |
| E | 5.00 BSC | | |
| b | 0.18 | 0.25 | 0.30 |
| D2 | 3.50 BSC | | |
| E2 | 3.50 BSC | | |
| e | 0.50 BSC | | |
| c | 0.30 REF | | |
| L | 0.35 | 0.40 | 0.45 |

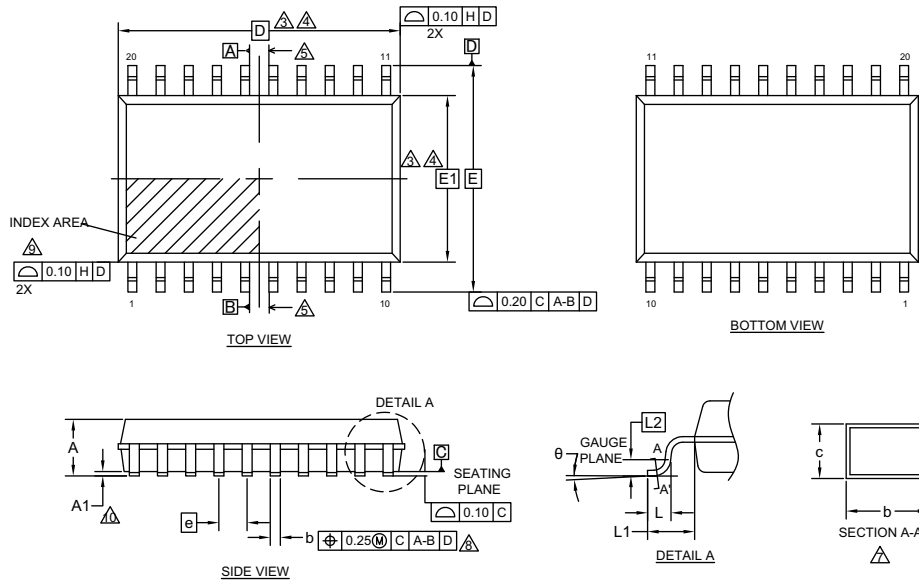
NOTE

- ALL DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
- N IS THE TOTAL NUMBER OF TERMINALS.
- Δ DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- Δ ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
- MAX. PACKAGE WARPAGE IS 0.05mm.
- MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
- Δ PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
- Δ BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE 32LEAD QFN
 5.000.000.8MM WNP032 3.53.3MM EPAD(S) ANV REV**

002-15160 **

| Package Type | Package Code |
|--------------|--------------|
| SOP 20 | SOJ020 |



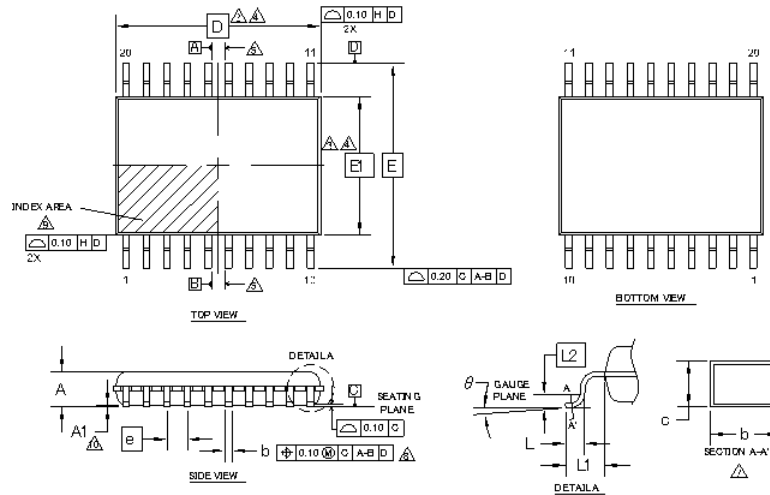
| SYMBOL | DIMENSIONS | | |
|----------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 2.65 |
| A1 | 0.05 | — | 0.20 |
| D | 12.70 BSC | | |
| E | 10.20 BSC | | |
| E1 | 7.50 BSC | | |
| θ | 0° | — | 8° |
| c | 0.22 | — | 0.32 |
| b | 0.35 | 0.40 | 0.49 |
| L | 0.50 | 0.80 | 1.27 |
| L 1 | 1.35 REF | | |
| L 2 | 0.25 BSC | | |
| e | 1.27 BSC | | |

NOTES

- ALL DIMENSIONS ARE IN MILLIMETER.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DATUMS A & B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
- DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- JEDEC SPECIFICATION NO. REF : N/A

002-16348 **

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| TSSOP 20 | STG020 |



| SYMBOL | DIMENSIONS | | |
|----------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| D | 6.50 BSC | | |
| E | 6.40 BSC | | |
| E1 | 4.40 BSC | | |
| θ | 0° | — | 8° |
| c | 0.10 | — | 0.19 |
| b | 0.20 | 0.24 | 0.28 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| e | 0.65 BSC | | |

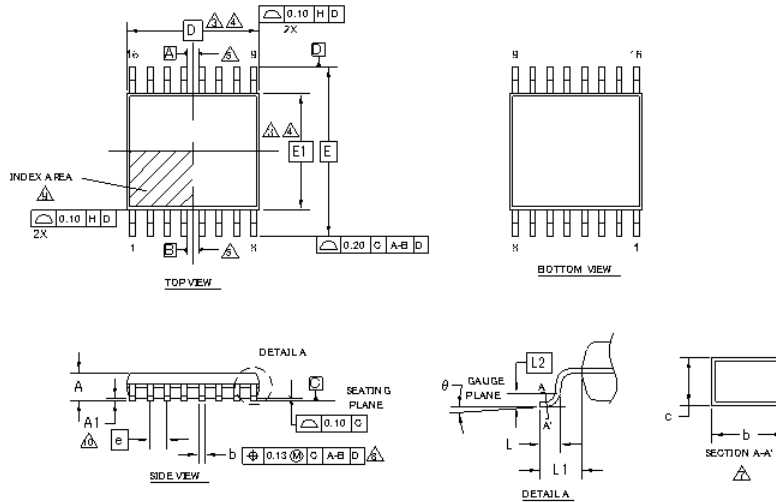
NOTES

- ALL DIMENSIONS ARE IN MILLIMETER.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- Δ DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERFAC FLASH OR PROTRUSION. INTERFAC FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- Δ THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- Δ DATUMS A & B TO BE DETERMINED AT DATUM H.
- Δ 'N' IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- Δ THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25 mm FROM THE LEAD TIP.
- Δ DIMENSION 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- Δ THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
- Δ 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CARRY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF: N/A

 PACKAGE OUTLINE, 20 LEAD TSSOP
 6-2008-40X1.20 MM STG020 REV04

002-15916 **

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| TSSOP 16 | STB016 |



| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| D | 4.36 BSC | | |
| E | 4.40 BSC | | |
| e | 0° | — | 8° |
| c | 0.10 | — | 0.19 |
| b | 0.16 | 0.24 | 0.32 |
| L | 0.45 | 0.60 | 0.75 |
| L 1 | 1.00 REF | | |
| L 2 | 0.25 BSC | | |
| e | 0.65 BSC | | |

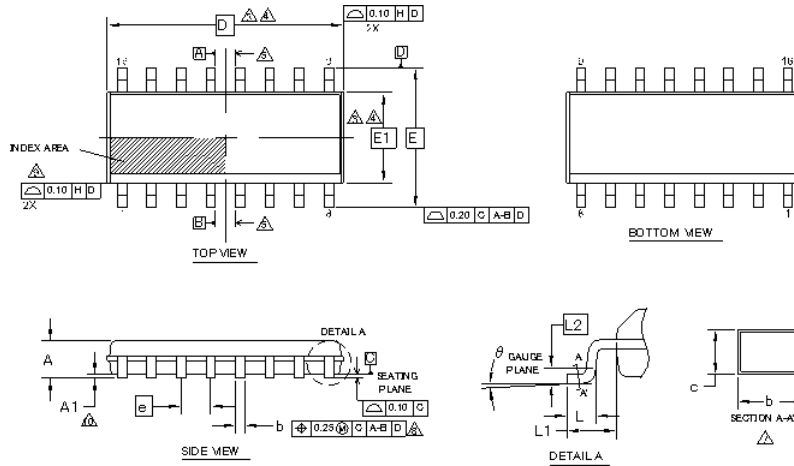
NOTES

- ALL DIMENSIONS ARE IN MILLIMETER.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- ⚠ DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERFAD FLASH OR PROTRUSION. INTERFAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- ⚠ THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- ⚠ DATUMS A & B TO BE DETERMINED AT DATUM H.
- ⚠ "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- ⚠ THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25 mm FROM THE LEAD TIP.
- ⚠ DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- ⚠ THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
- ⚠ "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND/OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF: N/A

 PACKAGE OUTLINE, 16 LEAD TSSOP
 4.9x8.40x1.20 MM STB016 REV**

002-15914 **

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| SOP 16 | SO016 |



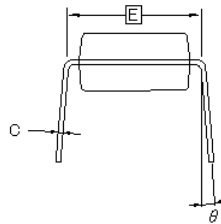
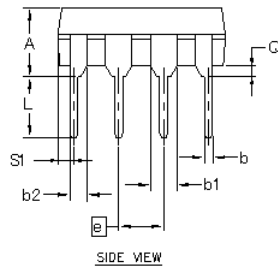
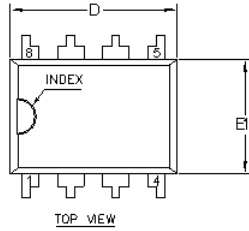
| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.75 |
| A1 | 0.10 | — | 0.25 |
| D | 3.95 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| θ | 0° | — | 8° |
| c | 0.13 | — | 0.20 |
| b | 0.36 | 0.40 | 0.51 |
| L | 0.45 | 0.60 | 0.80 |
| L1 | 1.05 REF | | |
| L2 | 0.25 BSC | | |
| e | 1.27 BSC | | |

- NOTES:**
- ALL DIMENSIONS ARE IN MILLIMETER.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
 - DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERFACIAL FLASH OR PROTRUSION. INTERFACIAL FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and C1 DIMENSION ARE DETERMINED AT DATUM H.
 - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUDING MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 - DATUMS A & B TO BE DETERMINED AT DATUM H.
 - "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
 - THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25 mm FROM THE LEAD TIP.
 - DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
 - THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
 - "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
 - JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 16 LEAD SOP
 59628-00X1.75 MM SO016 REV**

002-15861 **

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| DIP 8 | PDA008 |



| SYMBOL | DIMENSIONS | | |
|----------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 4.26 |
| L | 3.00 | — | — |
| D | 9.10 | 9.40 | 9.80 |
| E | 7.62 TYP | | |
| E1 | 6.10 | 6.35 | 6.60 |
| θ | — | — | 15° |
| c | 0.20 | 0.25 | 0.30 |
| b | 0.38 | 0.46 | 0.54 |
| b1 | — | 1.52 | 1.82 |
| b2 | — | 0.89 | 1.29 |
| e | 2.54 TYP | | |
| S1 | 0.59 | 0.89 | 1.24 |
| Q | 0.50 | — | — |

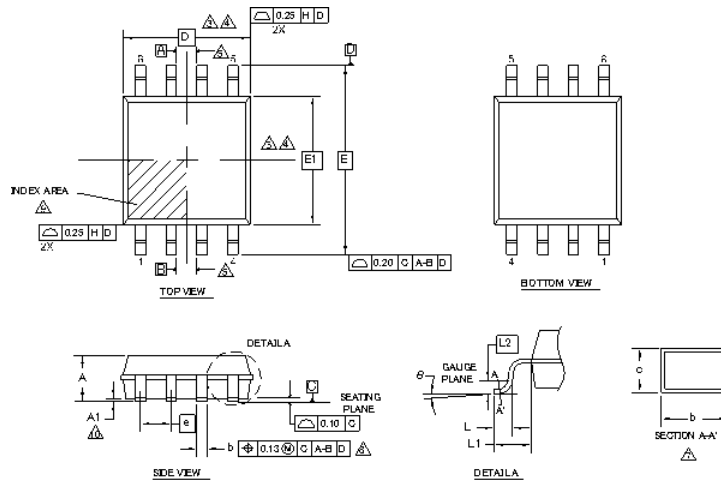
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. JEDEC SPECIFICATION NO. REF : N/A

PACKAGE OUTLINE & LEAD FOOT
 9-4008-15/12-98 MM PDA008 REV.4

002-16909 **

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| SOP 8 | SOD008 |



| SYMBOL | DIMENSION | | |
|--------|-----------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 2.10 |
| A1 | 0.05 | — | 0.25 |
| D | 5.24 BSC | | |
| E | 7.80 BSC | | |
| E1 | 5.30 BSC | | |
| θ | 0° | — | 8° |
| c | 0.15 | — | 0.25 |
| b | 0.38 | 0.43 | 0.48 |
| L1 | 1.25 REF | | |
| L2 | 0.25 BSC | | |
| e | 1.27 BSC | | |

- NOTES**
- ALL DIMENSIONS ARE IN MILLIMETER.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.5M '984.
 - DIMENSIONING D INCLUDE VOID FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERFAD FLASH OR PROTRUSION. INTERFAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
 - IHL PACKAGE TOP MAY BE SMALLER THAN IFL PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMITY OF THE PLASTIC BODY EXCLUDING VOID FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 - DATUMS A & B TO BE DETERMINED AT DATUM H.
 - N° 3 IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
 - THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.19mm TO 0.25mm FROM THE LEAD TIP.
 - DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.19mm TOTAL IN EXCESS OF "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
 - THE 3° CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
 - "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LEAD AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. UNLESS SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 8 LEAD SOP
 5240730/02, 10 MM SOD008 REV.0*

002-15858 **



29. Major Changes In This Edition

Spanion Publication Number: DS702-00010

| Page | Section | Details |
|------|--|---|
| — | — | <p>Changed the series name. MB95560H Series → MB95560H/570H/580H Series</p> <p>Added information on the MB95570H Series.</p> <p>Added information on the MB95580H Series.</p> |
| 27 | <p>■ PIN CONNECTION</p> <ul style="list-style-type: none"> • DBG pin | Revised details of “• DBG pin”. |
| | <ul style="list-style-type: none"> • $\overline{\text{RST}}$ pin | Revised details of “• $\overline{\text{RST}}$ pin”. |
| 28 | <ul style="list-style-type: none"> • C pin | <p>Corrected the following statement. The decoupling capacitor for the V_{CC} pin must have a capacitance larger than C_s. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_s.</p> |
| 39 | ■ I/O MAP (MB95570H Series) | <p>Corrected the R/W attribute of the CMDR register. R/W → R</p> <p>Corrected the R/W attribute of the WDTL register. R/W → R</p> <p>Corrected the R/W attribute of the WDTL register. R/W → R</p> |
| 42 | ■ I/O MAP (MB95580H Series) | <p>Corrected the R/W attribute of the CMDR register. R/W → R</p> <p>Corrected the R/W attribute of the WDTL register. R/W → R</p> <p>Corrected the R/W attribute of the WDTL register. R/W → R</p> |
| 46 | <p>■ ELECTRICAL CHARACTERISTICS</p> <p>1. Absolute Maximum Ratings</p> | <p>Corrected the rating of the parameter ““L” level total maximum output current”. 48 → 100</p> <p>Corrected the rating of the parameter ““H” level total maximum output current”. 48 → -100</p> |



| Page | Section | Details |
|------|---|---|
| 48 | 2. Recommended Operating Conditions | Revised note *2. The value is 2.88 V when the low-voltage detection reset is used. → The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used. |
| | | Corrected the following statement in note *3. The decoupling capacitor for the V _{CC} pin must have a capacitance larger than C _s . → The decoupling capacitor for the V _{CC} pin must have a capacitance equal to or larger than the capacitance of C _s . |
| | | Revised the remark in “• DBG/RST/C pins connection diagram”. |
| 49 | 3. DC Characteristics | Revised the remark of the parameter “Input leak current (Hi-Z output leak current)”. When pull-up resistance is disabled → When the internal pull-up resistor is disabled |
| | | Renamed the parameter “Pull-up resistance” to “Internal pull-up resistor”. |
| | | Revised the remark of the parameter “Internal pull-up resistor”. When pull-up resistance is enabled → When the internal pull-up resistor is enabled |
| 53 | 4. AC Characteristics (1) Clock Timing | Corrected the pin names of the parameter “Input clock rising time and falling time”. X0 → X0, X0A X0, X1 → X0, X1, X0A, X1A |



- Major changes from third edition to fourth edition

| Page | Section | Details |
|----------|---|---|
| 23 to 26 | ■ HANDLING PRECAUTIONS | New section |
| 35 | ■ I/O MAP (MB95560H Series) | Corrected the R/W attribute of the CMDR register. R/W → R |
| 52 | ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing | Corrected the operating conditions of F_{CRH} of the parameter "Clock frequency". $0\text{ }^{\circ}\text{C} \leq T_A < +70\text{ }^{\circ}\text{C}$ → $0\text{ }^{\circ}\text{C} \leq T_A \leq +70\text{ }^{\circ}\text{C}$ $+70\text{ }^{\circ}\text{C} \leq T_A < +85\text{ }^{\circ}\text{C}$ → $+70\text{ }^{\circ}\text{C} \leq T_A \leq +85\text{ }^{\circ}\text{C}$ |
| | | Corrected the operating conditions of F_{MCRPLL} of the parameter "Clock frequency". $0\text{ }^{\circ}\text{C} \leq T_A < +70\text{ }^{\circ}\text{C}$ → $0\text{ }^{\circ}\text{C} \leq T_A \leq +70\text{ }^{\circ}\text{C}$ $+70\text{ }^{\circ}\text{C} \leq T_A < +85\text{ }^{\circ}\text{C}$ → $+70\text{ }^{\circ}\text{C} < T_A \leq +85\text{ }^{\circ}\text{C}$ |
| 68 | 5. A/D Converter (1) A/D Converter Electrical Characteristics | Corrected the symbol of the parameter "Zero transition voltage". $V_{OT} \rightarrow V_{0T}$ |
| 69 | 5. A/D Converter (2) Notes on Using A/D Converter • Analog input equivalent circuit | Corrected the range of V_{CC} . $2.7\text{ V} \leq V_{CC} < 5.5\text{ V}$ → $2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$ |
| | | Corrected the values of R. $3.3\text{ k}\Omega \rightarrow 1.45\text{ k}\Omega$ $5.7\text{ k}\Omega \rightarrow 2.7\text{ k}\Omega$ |
| 70, 71 | 5. A/D Converter (3) Definitions of A/D Converter Terms | Corrected the symbol of the zero transition voltage. $V_{OT} \rightarrow V_{0T}$ |

NOTE: Please see "Document History" about later revised information.

Document History Page

| Document Title: MB95560H Series/MB95570H Series/MB95580H Series, New 8FX 8-bit Microcontrollers | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 002-04629 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | - | AKIH | 05/27/2013 | Migrated to Cypress and assigned document number 002-04629. No change to document contents or format. |
| *A | 5193921 | AKIH | 03/29/2016 | Updated 24.4.3 External Reset Added MB95F564KPF-G-UNE2, MB95F564KPFT-G-UNE2 in "Ordering Information". Updated to Cypress template. |
| *B | 5420206 | HTER | 02/06/2017 | Changed package code as the following in 1.Product Line-up (Page4, 6), 2.Packages And Corresponding Products (Page 7), 4.Pin Assignment (Page 9 to 10), 27.Ordering Information (Page 75 to 76) and 28.Package Dimensions (Page 77 to 83). "LCC-32P-M19" to "WNP032" "FPT-20P-M09" to "SOJ020" "FPT-20P-M10" to "STG020" "FPT-16P-M08" to "STB016" "FPT-16P-M23" to "SO016" "DIP-8P-M03" to "PDA008" "FPT-8P-M08" to "SOD008" Added Part number "MB95F564KPFT-G-UNERE2, MB95F562KPFT-G-UNERE2, MB95F563KPFT-G-UNERE2" in 27.Ordering Information (Page 75). Deleted Part number "MB95F564KPF-G-SNE2, MB95F564KPFT-G-SNE2" in 27.Ordering Information (Page 75). |
| *C | 5761469 | AESATP12 | 06/08/2017 | Updated logo and copyright. |
| *D | 5895915 | HUAL | 09/27/2017 | Added Part number "MB95F563HPFT-G-UNERE2" and Packing information in 27.Ordering Information (Page 75). |
| *E | 5972828 | HUAL | 11/21/2017 | Updated Package Dimension: Updated Diagram corresponding to "SOP 20". |



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