BUJD203AD

NPN power transistor with integrated diode

23 July 2018 Product data sheet

1. General description

High voltage, high speed, planar passivated NPN power switching transistor with integrated anti-parallel E-C diode in a SOT428 (DPAK) surface-mountable plastic package.

2. Features and benefits

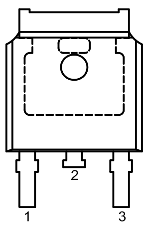
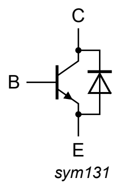
- Fast switching
- High voltage capability
- Integrated anti-parallel E-C diode
- Surface mountable package
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- Electronic lighting ballasts
- Inverters
- Motor control systems

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 DPAK (SOT428)	
2	C	collector[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

5. Ordering information

Table 2. Ordering information

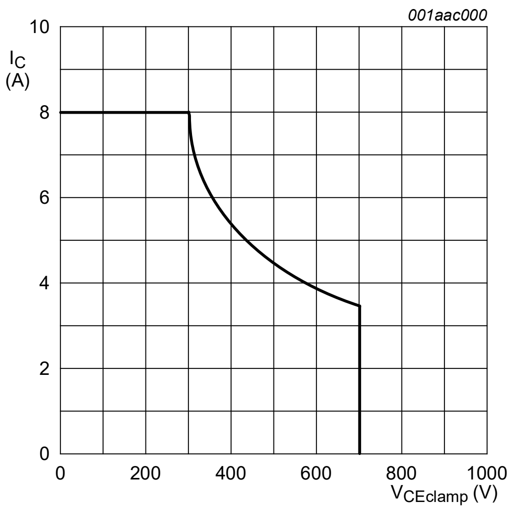
Type number	Package		
	Name	Description	Version
BUJD203AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

6. Limiting values

Table 3. Limiting values

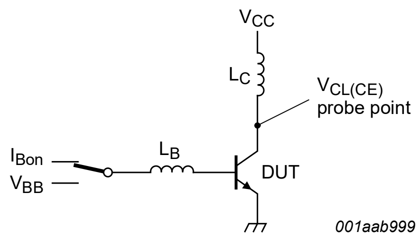
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	850	V
V_{CBO}	collector-base voltage	I_E = 0 A		-	850	V
V_{CEO}	collector-emitter voltage	I_B = 0 A		-	425	V
I_C	collector current	DC; Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{CM}	peak collector current	Fig. 1; Fig. 2; Fig. 3		-	8	A
I_B	base current	DC		-	2	A
I_{BM}	peak base current			-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq$ 25 °C; Fig. 4		-	80	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C



$T_j \leq T_{j(max)}$°C

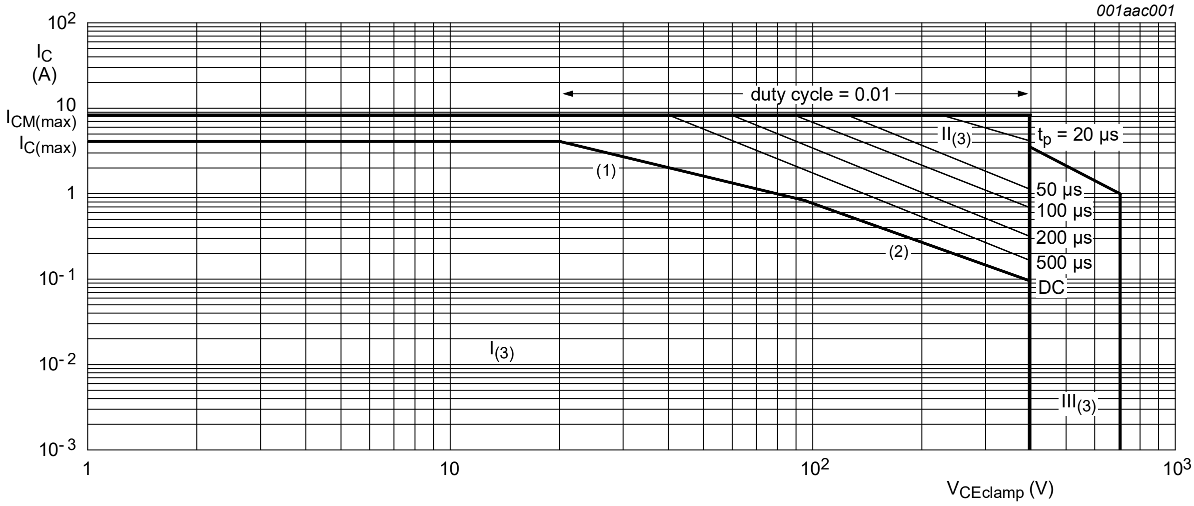
Fig. 1. Reverse bias safe operating area



$V_{CL(CE)} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V;

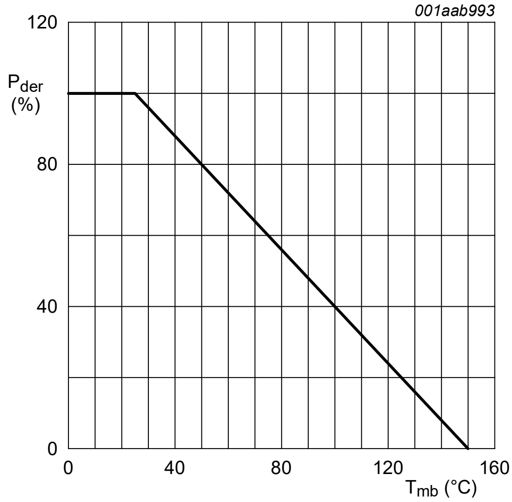
$L_B = 1$ μH; $L_C = 200$ μH

Fig. 2. Test circuit for reverse bias safe operating area



1)Ptot maximum and Ptot peak maximum lines
2)Second breakdown limits
3) I = Region of permissable DC operation
II = Extension for repetitive pulse operation
III = Extension during turn-on in single transistor converters
provided that RBE ≤ 100 Ω and tp ≤ 0.6 µs

Fig. 3. Forward bias safe operating area for Tmb ≤ 25 °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 4. Normalized total power dissipation as a function of mounting base temperature

7. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint; Fig. 6		-	75	-	K/W

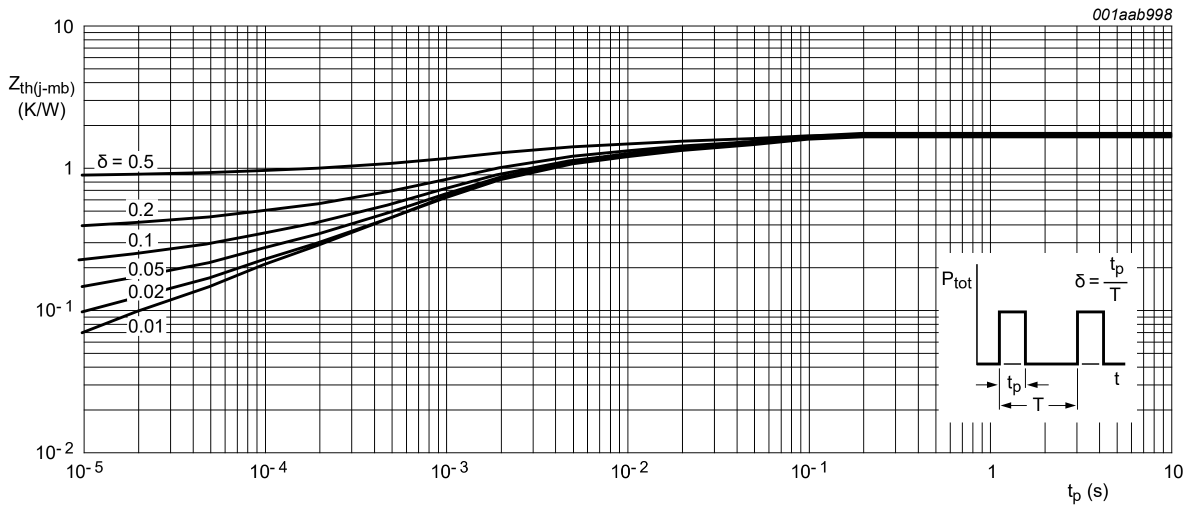


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse width

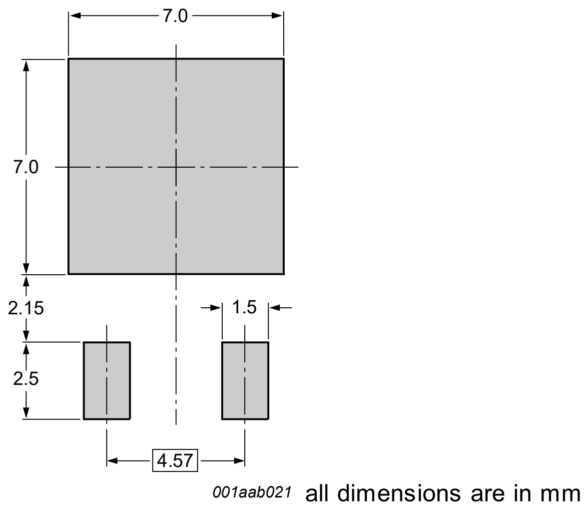


Fig. 6. Minimum footprint SOT428

8. Characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	V_{BE} = 0 V; V_{CE} = 850 V; T_j = 125 °C	[1]	-	-	2	mA
		V_{BE} = 0 V; V_{CE} = 850 V; T_j = 25 °C	[1]	-	-	1	mA
I_{CBO}	collector-base cut-off current (emitter open)	V_{CB} = 850 V; I_E = 0 A	[1]	-	-	1	mA
I_{CEO}	collector-emitter cut-off current (base open)	V_{CE} = 425 V; I_B = 0 A	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current (collector open)	V_{EB} = 7 V; I_C = 0 A		-	-	10	mA
V_{CEOsus}	collector-emitter sustaining voltage (base open)	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; Fig. 7; Fig. 8		400	450	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; Fig. 9; Fig. 10		-	0.29	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; Fig. 11		-	0.99	1.5	V
V_F	forward voltage	I_F = 2 A; T_j = 25 °C		-	1.04	1.5	V
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 12		10	15	32	
		I_C = 500 mA; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 12		13	21	32	
		I_C = 2 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 12		11	16	22	
		I_C = 3 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 12		-	12.5	-	
Dynamic characteristics							
t_{on}	turn-on time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 75 Ω; T_j = 25 °C; resistive load; Fig. 13; Fig. 14		-	0.52	0.6	μs
t_s	storage time			-	2.7	3.3	μs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 μH; T_j = 25 °C; inductive load; Fig. 15; Fig. 16		-	1.2	1.4	μs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 μH; T_j = 100 °C; inductive load; Fig. 15; Fig. 16		-	-	1.8	μs
t_f	fall time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 75 Ω; resistive load; Fig. 13; Fig. 14		-	0.3	0.35	μs
		I_C = 2 A; I_{Bon} = 0.4 A; V_{BB} = -5 V; L_B = 1 μH; inductive load; Fig. 15; Fig. 16		-	-	0.12	μs
				-	0.03	0.06	μs

[1] Measured with half-sine wave voltage (curve tracer)

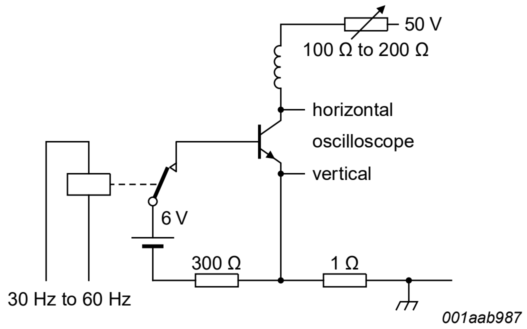


Fig. 7. Test circuit for collector-emitter sustaining voltage

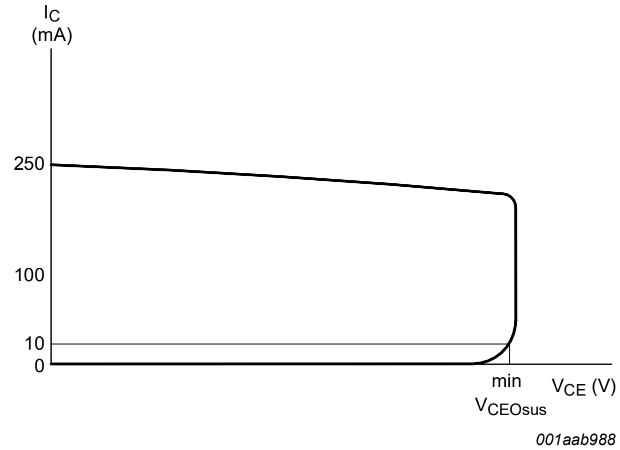


Fig. 8. Oscilloscope display for collector-emitter sustaining voltage test waveform

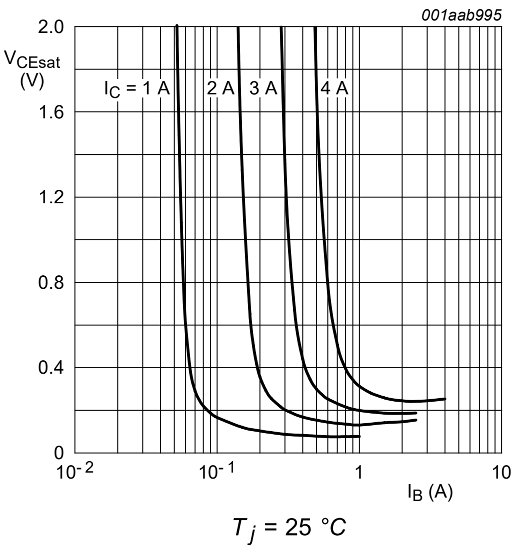


Fig. 9. Collector-emitter saturation voltage as a function of base current; typical values

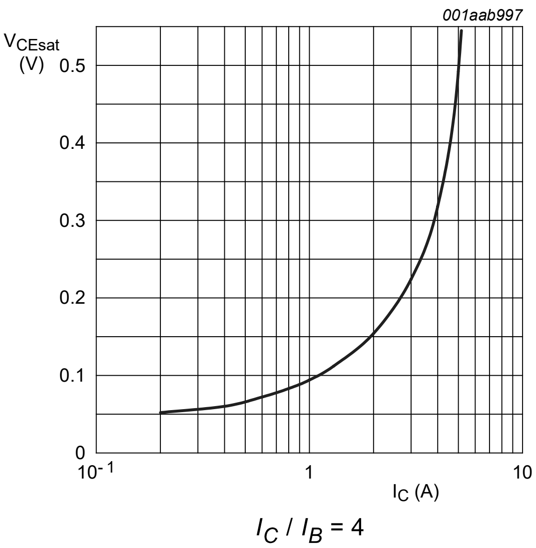
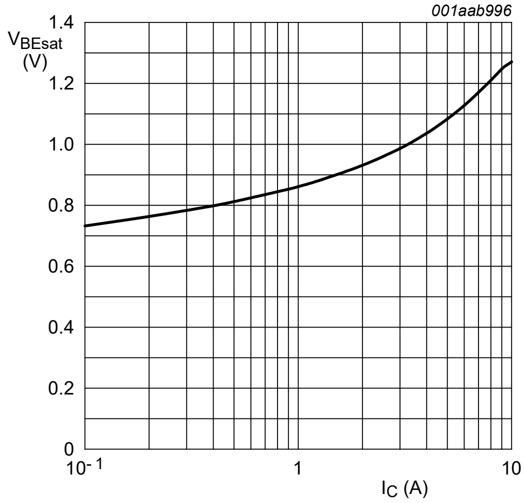
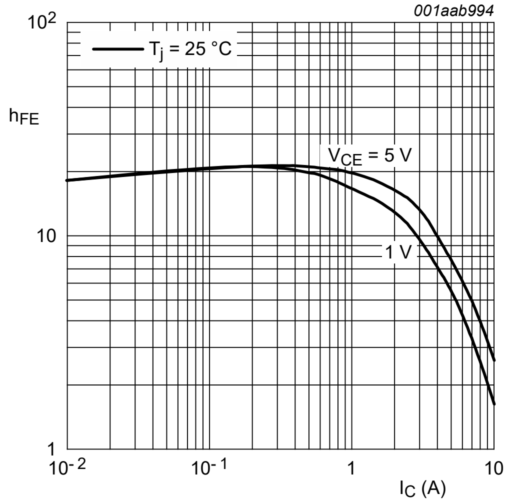


Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values



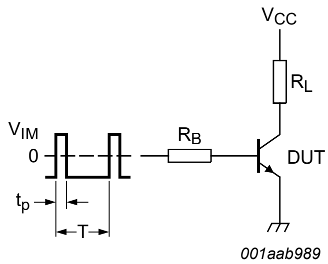
$I_C / I_B = 4$

Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values



$I_C / I_B = 4$

Fig. 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20$ μs; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 13. Test circuit for resistive load switching

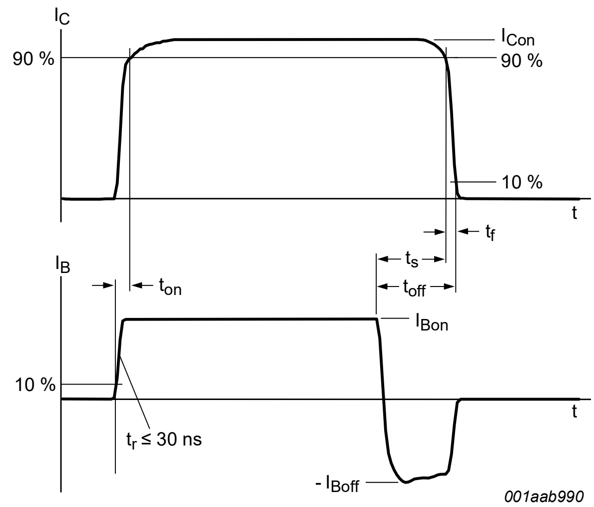
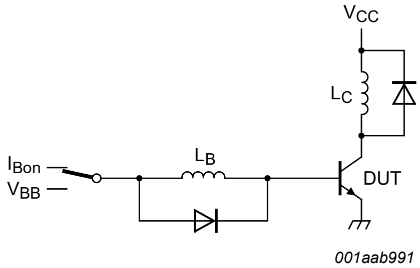


Fig. 14. Switching times waveforms for resistive load



$V_{CC} = 300\ V; V_{BB} = -5\ V; L_C = 200\ \mu H; L_B = 1\ \mu H$

Fig. 15. Test circuit for inductive load switching

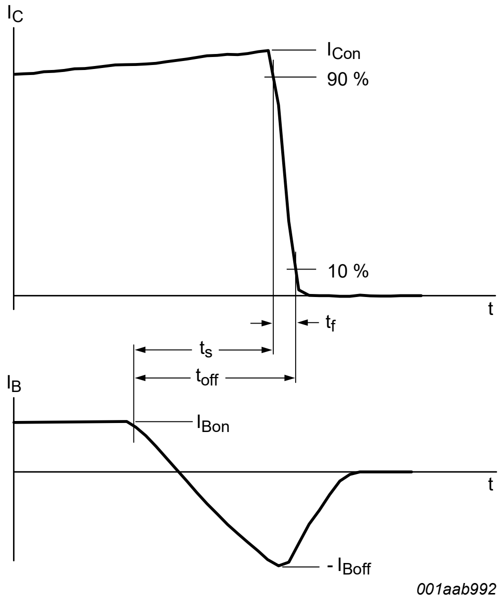
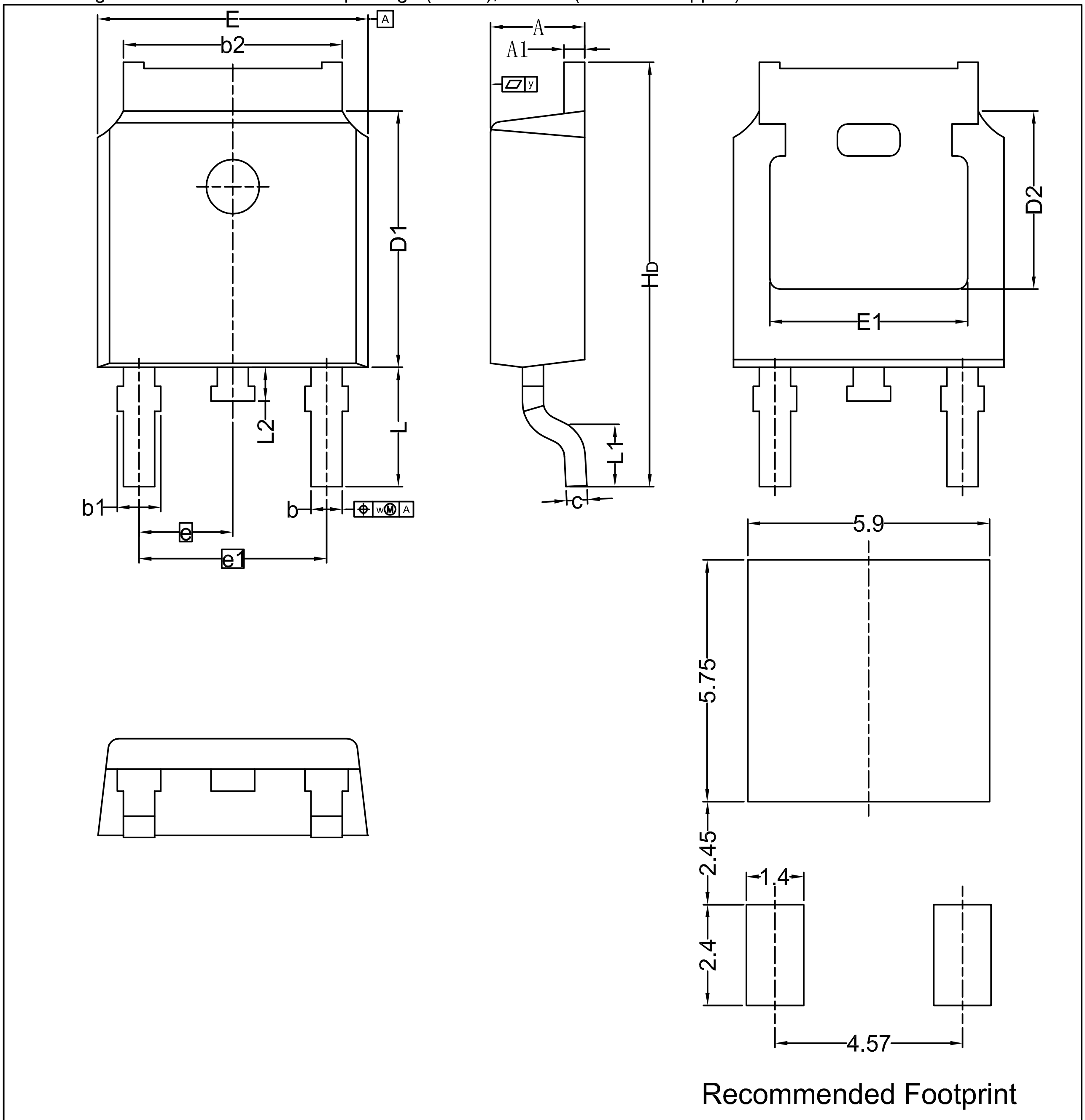


Fig. 16. Switching times waveforms for inductive load

9. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Unit		A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
mm	min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45			9.60		0.50	0.50		
	nom											2.285	4.57		2.90 (Ref.)			0.20	
	max	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		0.20

Fig. 17. Package outline DPAK (SOT428)

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Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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11. Contents

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Date of release: 23 July 2018

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