

74HC573-Q100; 74HCT573-Q100

Octal D-type transparent latch; 3-state

Rev. 5 — 10 March 2020

Product data sheet

1. General description

The 74HC573-Q100; 74HCT573-Q100 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable (\overline{OE}) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Input levels:
 - For 74HC573-Q100: CMOS level
 - For 74HCT573-Q100: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Multiple package options
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC573D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT573D-Q100				
74HC573DB-Q100	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT573DB-Q100				
74HC573PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT573PW-Q100				
74HC573BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HCT573BQ-Q100				

4. Functional diagram

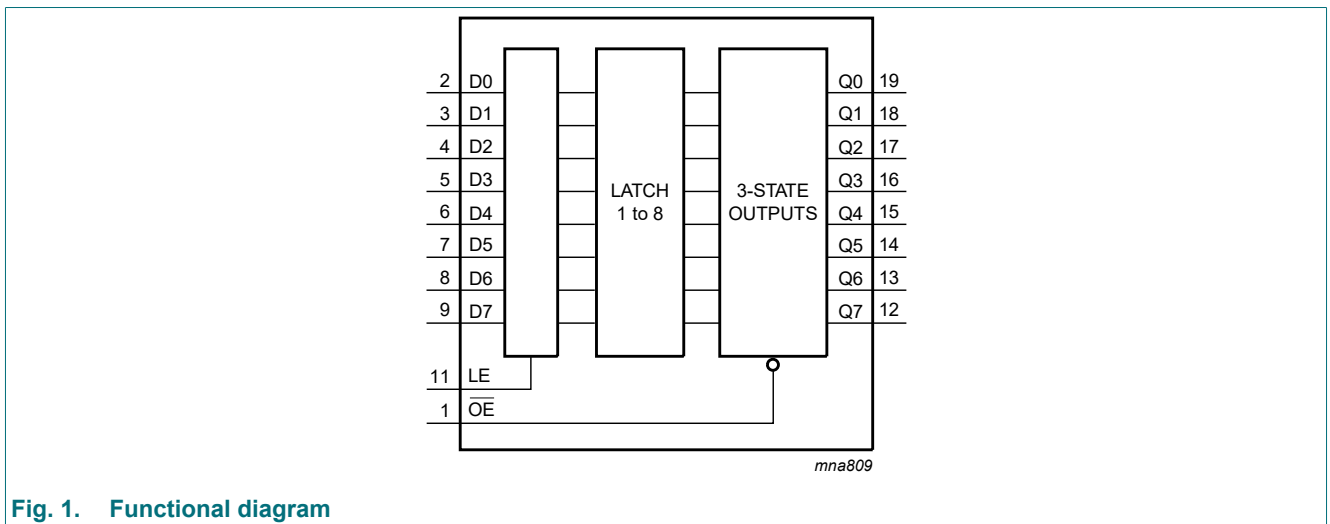


Fig. 1. Functional diagram

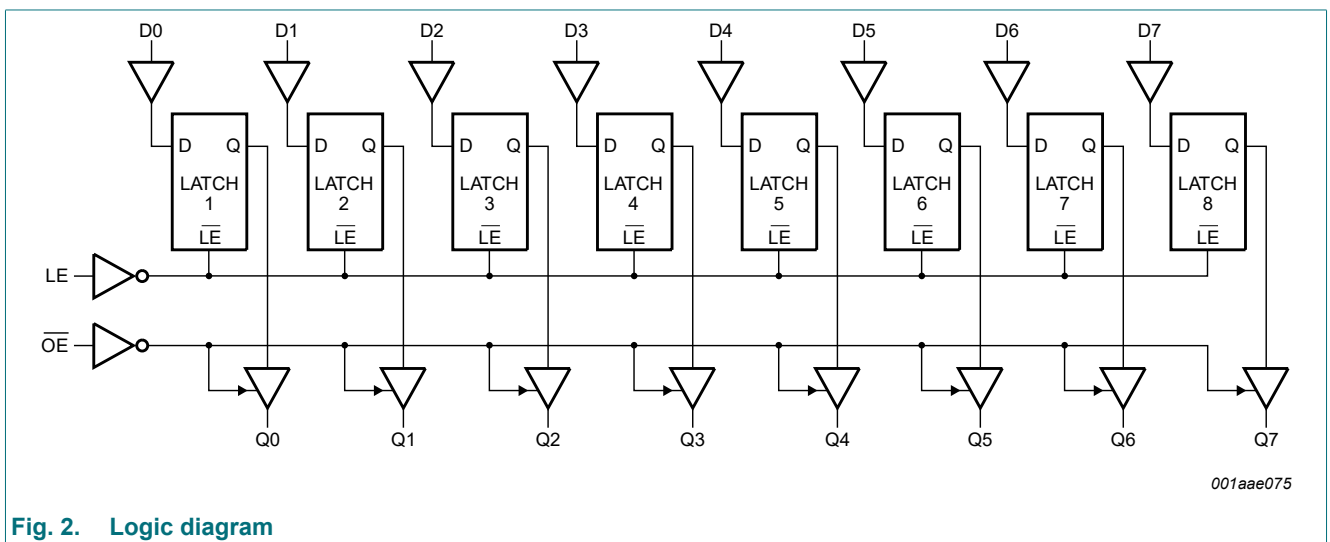


Fig. 2. Logic diagram

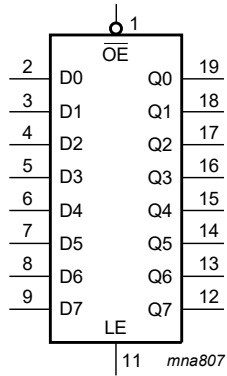


Fig. 3. Logic symbol

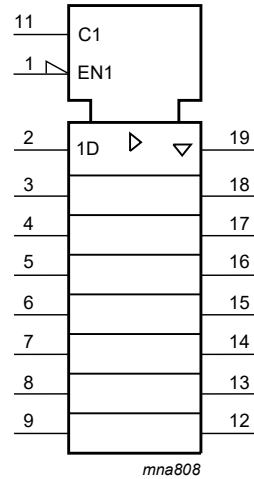


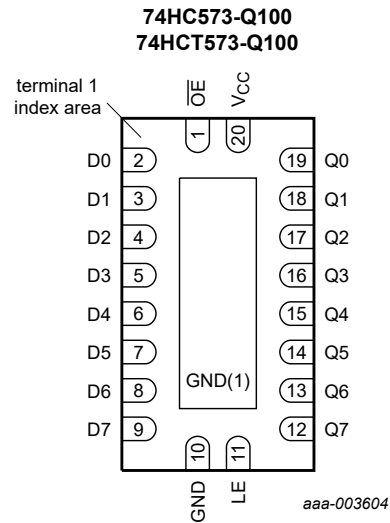
Fig. 4. IEC logic symbol

5. Pinning information

5.1. Pinning



Fig. 5. Pin configuration SOT163-1 (SO20), SOT339-1 (SSOP20) and SOT360-1 (TSSOP20)



Transparent top view
 (1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 6. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state latch output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

Operating mode	Control		Input	Internal latches	Output
	OE	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±35	mA
I _{CC}	supply current		-	+70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

- [1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
 For SOT339-1 (SSOP20) packages: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
 For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
 For SOT764-1 (DHFQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC573-Q100			74HCT573-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC573-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -6.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -7.8\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 7.8\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 6.0$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-					pF
74HCT573-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = -20$ µA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = 20$ µA	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0$ mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; Dn inputs	-	35	126	-	158	-	172	µA
		per input pin; LE input	-	65	234	-	293	-	319	µA
		per input pin; \overline{OE} input	-	125	450	-	563	-	613	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC573-Q100										
t_{pd}	propagation delay	Dn to Qn; see Fig. 7 [1]								
		$V_{CC} = 2.0$ V	-	47	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	17	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns
		LE to Qn; see Fig. 8 [1]								
		$V_{CC} = 2.0$ V	-	50	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	18	30	-	38	-	45	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
$V_{CC} = 6.0$ V	-	14	26	-	33	-	38	ns		
t_{en}	enable time	\overline{OE} to Qn; see Fig. 9 [2]								
		$V_{CC} = 2.0$ V	-	44	140	-	175	-	210	ns
		$V_{CC} = 4.5$ V	-	16	28	-	35	-	42	ns
		$V_{CC} = 6.0$ V	-	13	24	-	30	-	36	ns
t_{dis}	disable time	\overline{OE} to Qn; see Fig. 9 [3]								
		$V_{CC} = 2.0$ V	-	55	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	20	30	-	38	-	45	ns
		$V_{CC} = 6.0$ V	-	16	26	-	33	-	38	ns
t_t	transition time	Qn; see Fig. 7 [4]								
		$V_{CC} = 2.0$ V	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5$ V	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0$ V	-	4	10	-	13	-	15	ns
t_W	pulse width	LE HIGH; see Fig. 8								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
t_{su}	set-up time	Dn to LE; see Fig. 10								
		$V_{CC} = 2.0$ V	50	11	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V	10	4	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V	9	3	-	11	-	13	-	ns
t_h	hold time	Dn to LE; see Fig. 10								
		$V_{CC} = 2.0$ V	5	3	-	5	-	5	-	ns
		$V_{CC} = 4.5$ V	5	1	-	5	-	5	-	ns
		$V_{CC} = 6.0$ V	5	1	-	5	-	5	-	ns
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to V_{CC} [5]	-	26	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT573-Q100										
t _{pd}	propagation delay	Dn to Qn; see Fig. 7 [1]								
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		LE to Qn; see Fig. 8 [1]								
		V _{CC} = 4.5 V	-	18	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	ns	
t _{en}	enable time	OE to Qn; see Fig. 9 [2]								
		V _{CC} = 4.5 V	-	17	30	-	38	-	45	ns
t _{dis}	disable time	OE to Qn; see Fig. 9 [3]								
		V _{CC} = 4.5 V	-	18	30	-	38	-	45	ns
t _t	transition time	Qn; see Fig. 7 [4]								
		V _{CC} = 4.5 V	-	5	12	-	15	-	18	ns
t _w	pulse width	LE HIGH; see Fig. 8								
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
t _{su}	set-up time	Dn to LE; see Fig. 10								
		V _{CC} = 4.5 V	13	7	-	16	-	20	-	ns
t _h	hold time	Dn to LE; see Fig. 10								
		V _{CC} = 4.5 V	9	4	-	11	-	15	-	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [5]	-	26	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

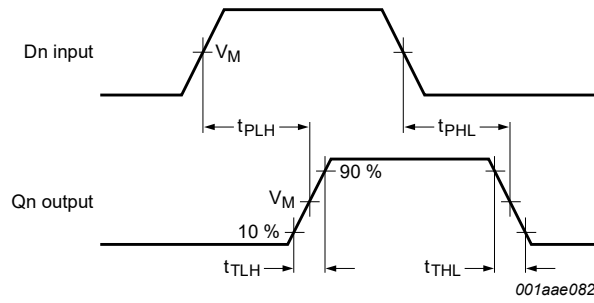
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

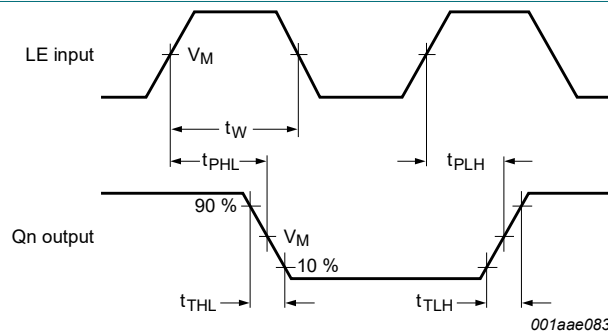
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms



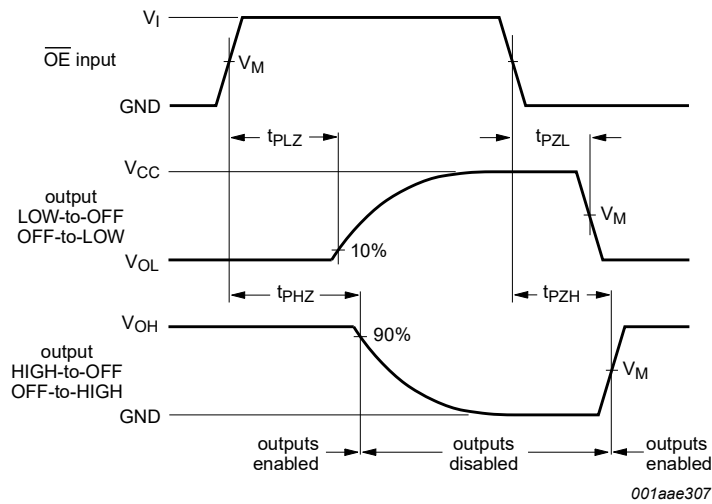
Measurement points are given in [Table 8](#).

Fig. 7. Propagation delay data input (Dn) to output (Qn) and output transition time



Measurement points are given in [Table 8](#).

Fig. 8. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. Enable and disable times



Table 8. Measurement points

Type	Input	Output
	V _M	V _M
74HC573-Q100	0.5V _{CC}	0.5V _{CC}
74HCT573-Q100	1.3 V	1.3 V



Table 9. Test data

Type	Input		Load		S1 position		
	V _I	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74HC573-Q100	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74HCT573-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

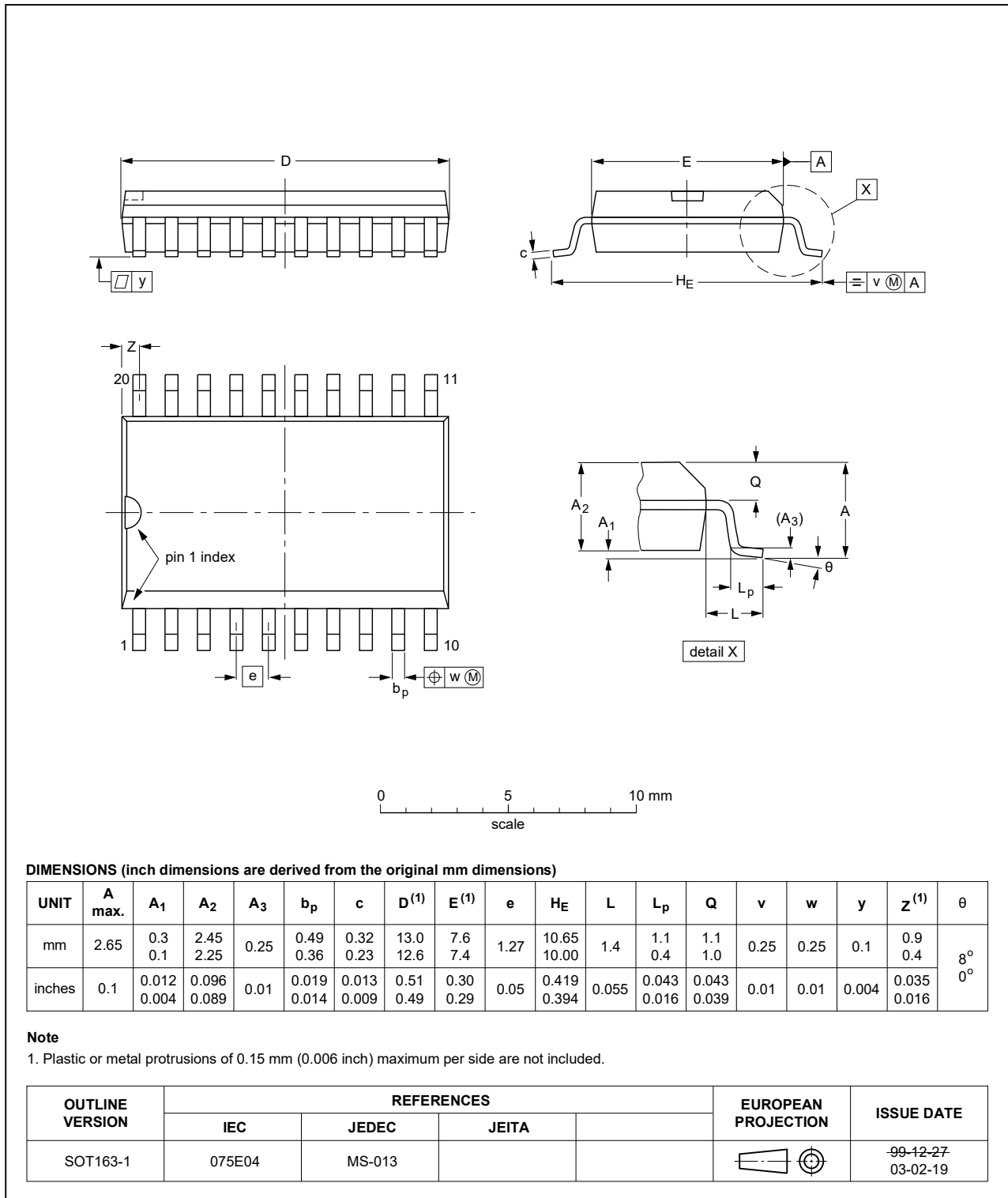


Fig. 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



Fig. 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 15. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT573_Q100 v.5	20200310	Product data sheet	-	74HC_HCT573_Q100 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 updated. Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT573_Q100 v.4	20150126	Product data sheet	-	74HC_HCT573_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Table 7: Power dissipation capacitance condition for 74HCT573-Q100 is corrected. 			
74HC_HCT573_Q100 v.3	20130305	Product data sheet	-	74HC_HCT573_Q100 v.2
Modifications:	<ul style="list-style-type: none"> 74HC573DB-Q100 and 74HCT573DB-Q100 added. 			
74HC_HCT573_Q100 v.2	20120816	Product data sheet	-	74HC_HCT573_Q100 v.1
74HC_HCT573_Q100 v.1	20120802	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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