

1. Overview

1.1 Features

The R8C/M11A Group and R8C/M12A Group of single-chip microcontrollers (MCUs) incorporate the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions on the same chip, including multifunction timer and serial interface, reduces the number of system components.

The R8C/M11A Group and R8C/M12A Group include data flash (1 KB × 2 blocks).

1.1.1 Applications

Home appliances, office equipment, audio equipment, consumer products, etc.

1.1.2 Differences between Groups

Table 1.1 lists the Specification Comparison between R8C/M11A Group and R8C/M12A Group. The explanations in 1.1.3 and subsequent sections apply to the R8C/M12A Group specifications only, unless otherwise specified.

Table 1.1 Specification Comparison between R8C/M11A Group and R8C/M12A Group

| Item | Function | R8C/M11A Group | R8C/M12A Group |
|---------------|------------------------------------|---|---|
| Interrupts | External interrupt inputs | 6 ($\overline{\text{INT}} \times 3$, key input $\times 3$) | 8 ($\overline{\text{INT}} \times 4$, key input $\times 4$) |
| I/O ports | Number of pins | 14 Non-provided pins: P1_0/AN0/TRCIOD/KI0 P3_3/IVCMP3/TRCCLK/INT3 P3_4/IVREF3/TRCIOC/INT2 P3_5/TRCIOD/KI2/VCOU3 P4_2/TRBO/TXD0/KI3 P4_5/INT0/ADTRG | 20 |
| | Number of CMOS I/O ports | 11 Non-provided ports: P1_0, P3_3, P3_4, P3_5, P4_2, P4_5 | 17 |
| | Number of high-current drive ports | 5 Non-provided ports: P3_3, P3_4, P3_5 | 8 |
| A/D converter | Number of A/D channels | 5 channels Non-provided port: AN0 | 6 channels |
| Comparator B | Number of channels | Comparator B1 | Comparator B1, comparator B3 |

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

| Related Function | Register Name | Address | Bit | Setting Method for Access |
|-------------------------|---------------|---------|------------------------------------|--|
| INT3 | INTEN | 00038h | INT3EN | Reserved bit. Set to 0. |
| | INTF0 | 0003Ah | INT3F0, INT3F1 | Reserved bits. Set to 0. |
| | ISCR0 | 0003Ch | INT3SA, INT3SB | Reserved bits. Set to 0. |
| | ILVLD | 0004Dh | ILVLD0, ILVLD1 | Reserved bits. Set to 0. |
| | IRR3 | 00053h | IRI3 | Reserved bit. Set to 0. |
| KI0 | KIEN | 0003Eh | KI0EN, KI0PL | Reserved bits. Set to 0. |
| Comparator B3 interrupt | ILVL2 | 00042h | ILVL24, ILVL25 | Reserved bits. Set to 0. |
| | IRR2 | 00052h | IRCMP3 | Reserved bit. Set to 0. |
| P1_0 | PD1 | 000A9h | PD1_0 | Reserved bit. Set to 0. |
| | P1 | 000AFh | P1_0 | Reserved bit. Set to 0. |
| | PUR1 | 000B5h | PU1_0 | Reserved bit. Set to 0. |
| | POD1 | 000C1h | POD1_0 | Reserved bit. Set to 0. |
| | PML1 | 000C8h | P10SEL0, P10SEL1 | Reserved bits. Set to 0. |
| P3_3, P3_4, P3_5 | PD3 | 000ABh | PD3_3, PD3_4, PD3_5 | Reserved bits. Set to 0. |
| | P3 | 000B1h | P3_3, P3_4, P3_5 | Reserved bits. Set to 0. |
| | PUR3 | 000B7h | PU3_3, PU3_4, PU3_5 | Reserved bits. Set to 0. |
| | DRR3 | 000BDh | DRR3_3, DRR3_4, DRR3_5 | Reserved bits. Set to 0. |
| | POD3 | 000C3h | POD3_3, POD3_4, POD3_5 | Reserved bits. Set to 0. |
| | PML3 | 000CCh | P33SEL0, P33SEL1 | Reserved bits. Set to 0. |
| | PMH3 | 000CDh | P34SEL0, P34SEL1, P35SEL0, P35SEL1 | Reserved bits. Set to 0. |
| P4_2, P4_5 | PD4 | 000ACh | PD4_2, PD4_5 | Reserved bits. Set to 0. |
| | P4 | 000B2h | P4_2, P4_5 | Reserved bits. Set to 0. |
| | PUR4 | 000B8h | PU4_2, PU4_5 | Reserved bits. Set to 0. |
| | POD4 | 000C4h | POD4_2, POD4_5 | Reserved bits. Set to 0. |
| | PML4 | 000CEh | P42SEL0, P42SEL1 | Reserved bits. Set to 0. |
| | PMH4 | 000CFh | P45SEL0, P45SEL1 | Reserved bits. Set to 0. |
| AN0 | ADINSEL | 0009Dh | CH0, ADGSEL0, ADGSEL1 | Do not set to 000. |
| Comparator B3 | WCMPR | 00180h | WCB3M0, WCB3OUT | Reserved bits. Set to 0. |
| | WCB3INTR | 00182h | All bits | Reserved register. No access is allowed. |

1.1.3 Specifications

Tables 1.3 and 1.4 outline the Specifications.

Table 1.3 Specifications (1)

| Item | Function | Description |
|-------------------|---------------------------|--|
| CPU | Central processing unit | R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ V to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ V to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, data flash | See Table 1.5 Product List . |
| Reset sources | | <ul style="list-style-type: none"> • Hardware reset by \overline{RESET} • Power-on reset • Watchdog timer reset • Software reset • Reset by voltage detection 0 |
| Voltage detection | Voltage detection circuit | Voltage detection with two check points: Voltage detection 0, voltage detection 1 (detection levels selectable) |
| Watchdog timer | | <ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start function selectable • Count source protection function selectable • Periodic timer function selectable |
| Clock | Clock generation circuits | <ul style="list-style-type: none"> • 3 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Clock frequency divider circuit integrated |
| Power control | | <ul style="list-style-type: none"> • Standard operating mode • Wait mode (CPU stopped, peripheral functions in operation) • Stop mode (CPU and peripheral functions stopped) |
| Interrupts | | <ul style="list-style-type: none"> • Number of interrupt vectors: 69 • External interrupt inputs: 8 ($\overline{INT} \times 4$, key input $\times 4$) • Priority levels: 2 |
| I/O ports | Programmable I/O ports | <ul style="list-style-type: none"> • CMOS I/O: 17 (pull-up resistor selectable) • High-current drive ports: 8 |
| Timer | Timer RJ2 | 16 bits \times 1 Timer mode, pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB2 | 8 bits \times 1 (with 8-bit prescaler) or 16 bits \times 1 (selectable) Timer mode, programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits \times 1 (with 4 capture/compare registers) Timer mode (output compare function, input capture function), PWM mode (3 outputs), PWM2 mode (1 PWM output) |
| Serial interface | UART0 | Clock synchronous serial I/O. Also used for asynchronous serial I/O. |
| A/D converter | | <ul style="list-style-type: none"> • Resolution: 10 bits \times 6 channels • Sample and hold function, sweep mode |
| Comparator B | | 2 circuits |

Table 1.4 Specifications (2)

| Item | Function | Description |
|--|----------|--|
| Flash memory | | <ul style="list-style-type: none"> • Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function |
| Operating frequency/ Power supply voltage | | f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V) |
| Temperature range | | -20 °C to 85 °C (N version) -40 °C to 85 °C (D version) ⁽¹⁾ |
| Package | | 14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A |

Note:

1. Specify the D version if it is to be used.

1.2 Product List

Table 1.5 lists the Product List. Figure 1.1 shows the Product Part Number Structure.

Table 1.5 Product List **Current of May 2012**

| Group Name | Part No. | Internal ROM Capacity | | Internal RAM Capacity | Package Type | Remarks | |
|----------------|--------------|-----------------------|-------------|-----------------------|--------------|-----------|-----------|
| | | Program ROM | Data Flash | | | | |
| R8C/M11A Group | R5F2M110ANSP | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PTSP0014JA-B | N version | |
| | R5F2M111ANSP | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M112ANSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |
| | R5F2M110ANDD | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PRDP0014AC-A | | |
| | R5F2M111ANDD | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M112ANDD | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |
| | R5F2M110ADSP | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PTSP0014JA-B | | D version |
| | R5F2M111ADSP | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M112ADSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |
| R8C/M12A Group | R5F2M120ANSP | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PLSP0020JB-A | N version | |
| | R5F2M121ANSP | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M122ANSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |
| | R5F2M120ANDD | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PRDP0020AD-A | | |
| | R5F2M121ANDD | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M122ANDD | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |
| | R5F2M120ADSP | 2 Kbytes | 1 Kbyte × 2 | 256 bytes | PLSP0020JB-A | | D version |
| | R5F2M121ADSP | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | | | |
| | R5F2M122ADSP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | | | |

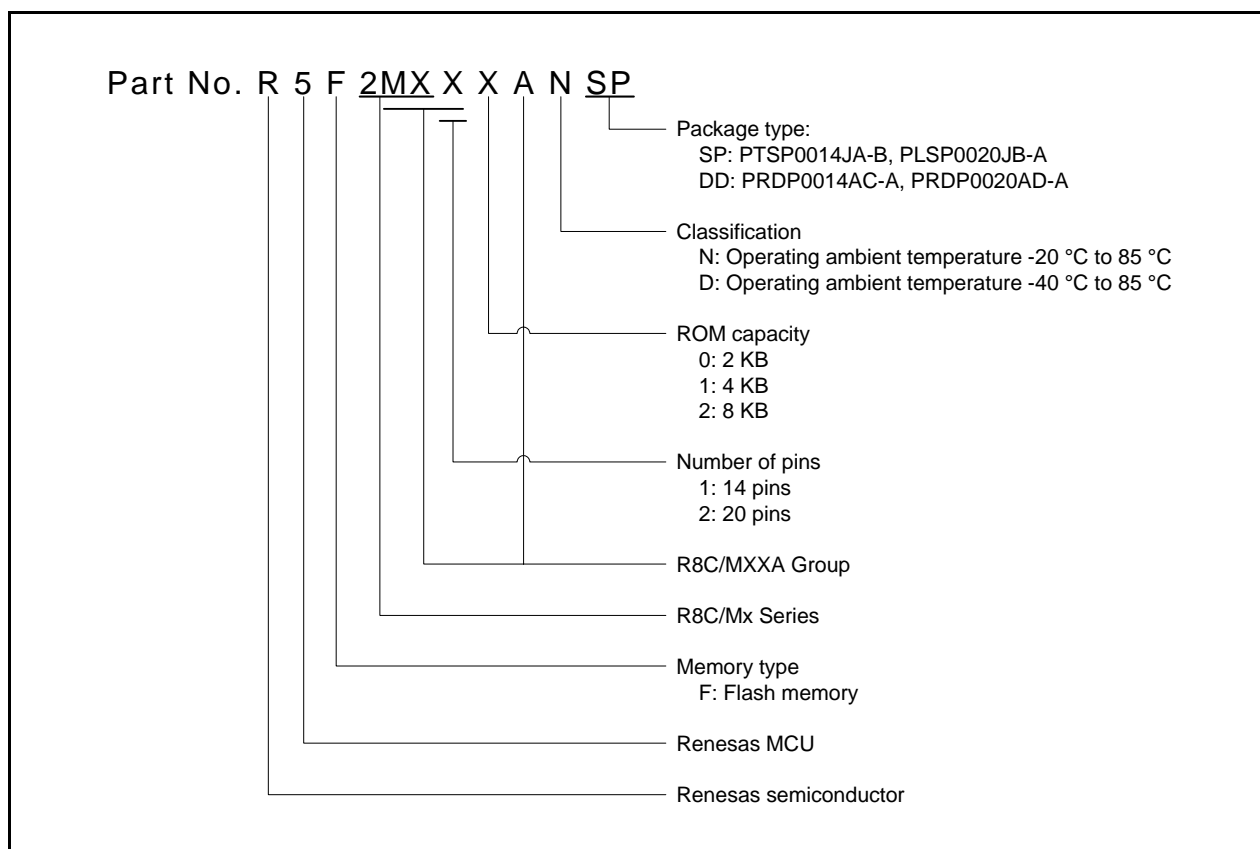


Figure 1.1 Product Part Number Structure

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

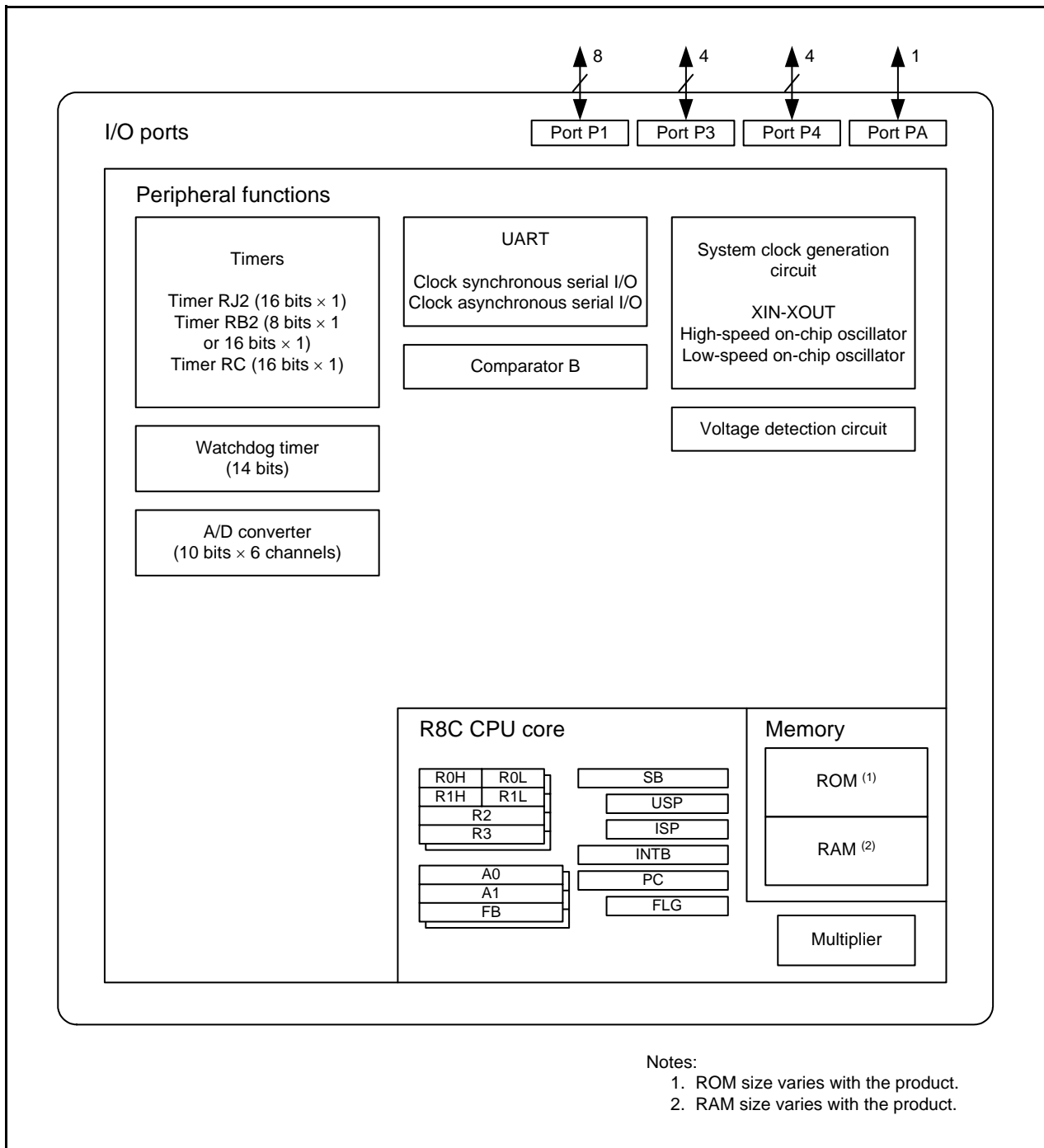


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.

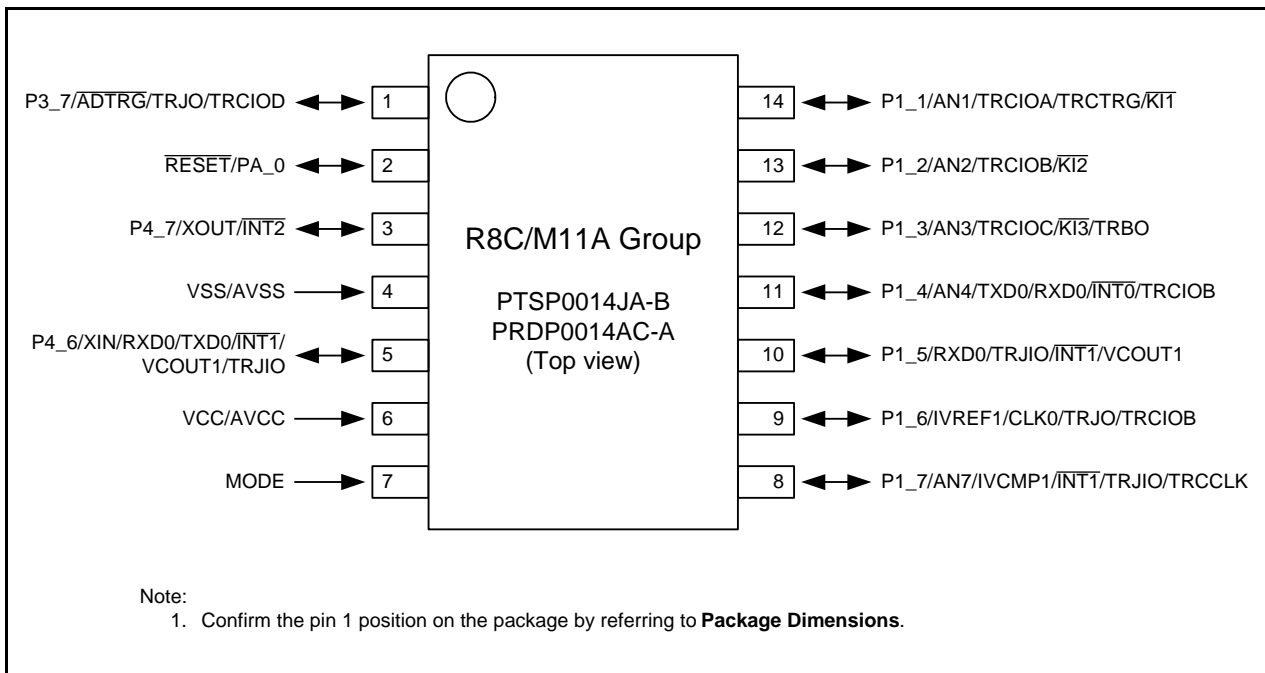


Figure 1.3 R8C/M11A Group Pin Assignment (Top View)

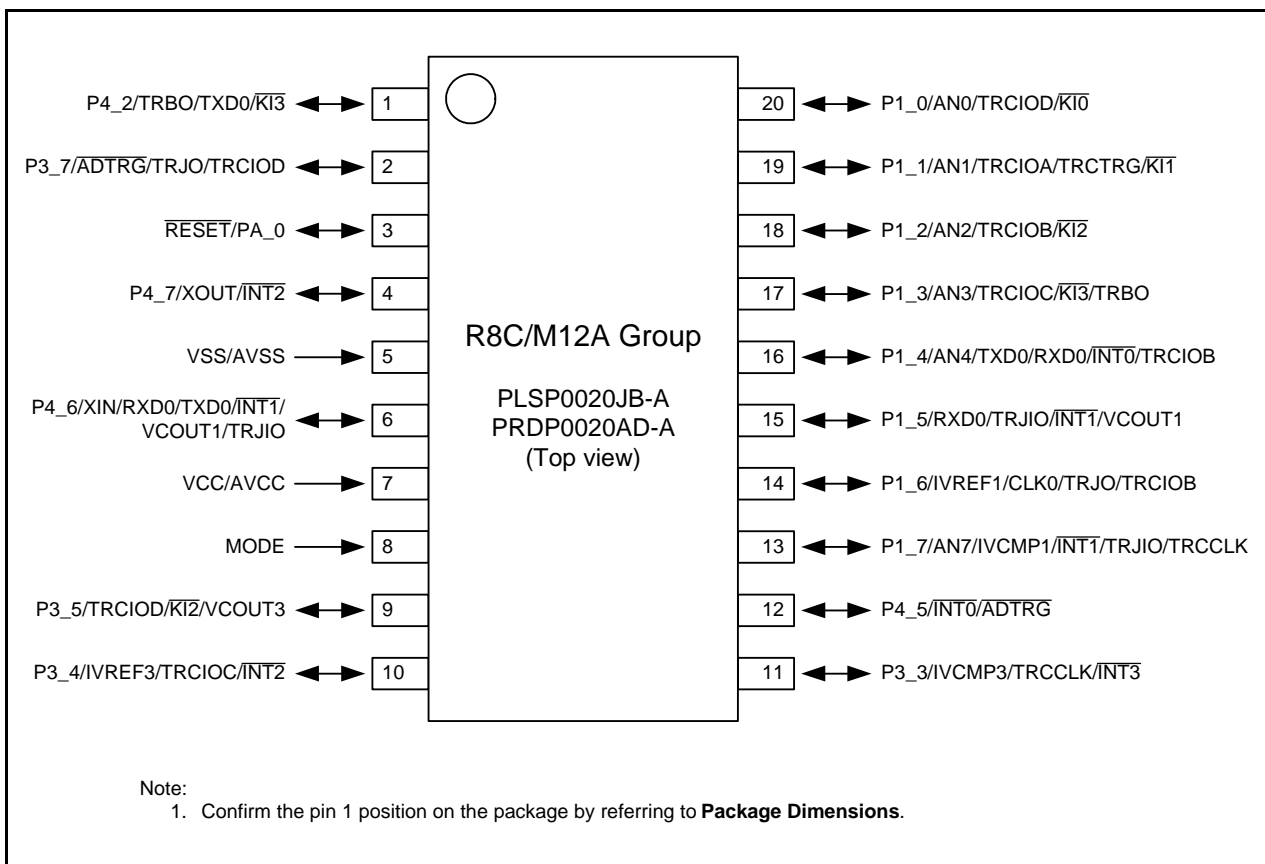


Figure 1.4 R8C/M12A Group Pin Assignment (Top View)

Table 1.6 Pin Name Information by Pin Number

| Pin Number | | Control Pin | Port | I/O Pins for Peripheral Functions | | | |
|----------------|----------------|--------------------|------|-----------------------------------|----------------|------------------|-----------------------------|
| R8C/M11A Group | R8C/M12A Group | | | Interrupt | Timer | Serial Interface | A/D Converter, Comparator B |
| | 1 | | P4_2 | $\overline{KI3}$ | TRBO | TXD0 | |
| 1 | 2 | | P3_7 | | TRJO/TRCIOD | | \overline{ADTRG} |
| 2 | 3 | \overline{RESET} | PA_0 | | | | |
| 3 | 4 | XOUT | P4_7 | $\overline{INT2}$ | | | |
| 4 | 5 | VSS/AVSS | | | | | |
| 5 | 6 | XIN | P4_6 | $\overline{INT1}$ | TRJIO | RXD0/TXD0 | VCOUT1 |
| 6 | 7 | VCC/AVCC | | | | | |
| 7 | 8 | MODE | | | | | |
| | 9 | | P3_5 | $\overline{KI2}$ | TRCIOD | | VCOUT3 |
| | 10 | | P3_4 | $\overline{INT2}$ | TRCIOC | | IVREF3 |
| | 11 | | P3_3 | $\overline{INT3}$ | TRCCLK | | IVCMP3 |
| | 12 | | P4_5 | $\overline{INT0}$ | | | \overline{ADTRG} |
| 8 | 13 | | P1_7 | $\overline{INT1}$ | TRJIO/TRCCLK | | AN7/IVCMP1 |
| 9 | 14 | | P1_6 | | TRJO/TRCIOB | CLK0 | IVREF1 |
| 10 | 15 | | P1_5 | $\overline{INT1}$ | TRJIO | RXD0 | VCOUT1 |
| 11 | 16 | | P1_4 | $\overline{INT0}$ | TRCIOB | RXD0/TXD0 | AN4 |
| 12 | 17 | | P1_3 | $\overline{KI3}$ | TRBO/TRCIOC | | AN3 |
| 13 | 18 | | P1_2 | $\overline{KI2}$ | TRCIOB | | AN2 |
| 14 | 19 | | P1_1 | $\overline{KI1}$ | TRCIOA/TRCTRGR | | AN1 |
| | 20 | | P1_0 | $\overline{KI0}$ | TRCIOD | | AN0 |

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

Table 1.7 Pin Functions

| Item | Pin Name | I/O | Description |
|---|---|-----|---|
| Power supply input | VCC, VSS | — | Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | — | Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Applying a low level to this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to the VCC pin via a resistor. |
| XIN clock input | XIN | I | I/O for the XIN clock generation circuit. |
| XIN clock output | XOUT | O | Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time. |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input. |
| I/O ports | P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0 | I/O | CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports. |
| Timer RJ2 | TRJIO | I/O | Timer RJ2 I/O. |
| | TRJO | O | Timer RJ2 output. |
| Timer RB2 | TRBO | O | Timer RB2 output. |
| Timer RC | TRCCLK | I | External clock input. |
| | TRCTRG | I | External trigger input. |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O. |
| Serial interface | CLK0 | I/O | Transfer clock I/O. |
| | RXD0 | I | Serial data input. |
| | TXD0 | O | Serial data output. |
| A/D converter | AN0 to AN4, AN7 | I | Analog input for the A/D converter. |
| | $\overline{\text{ADTRG}}$ | I | External trigger input for the A/D converter. |
| Comparator B | IVCMP1, IVCMP3 | I | Analog voltage input for comparator B. |
| | IVREF1, IVREF3 | I | Reference voltage input for comparator B. |
| | VCOU1, VCOU3 | O | Comparison result output for comparator B. |

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.

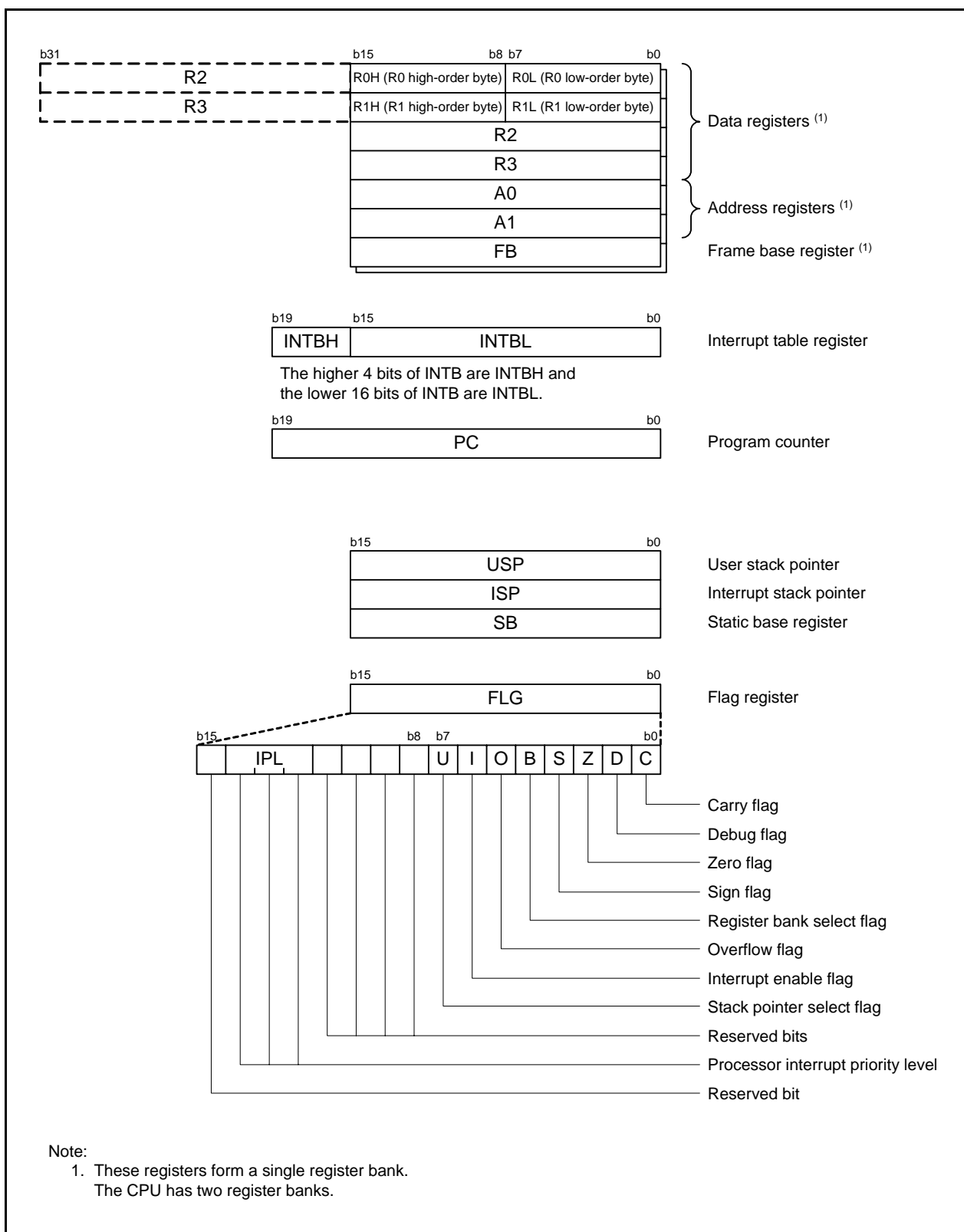


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.

R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled. If IPL is set to levels from 2 to 7, all maskable interrupt requests are disabled.

2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh. The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.

The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

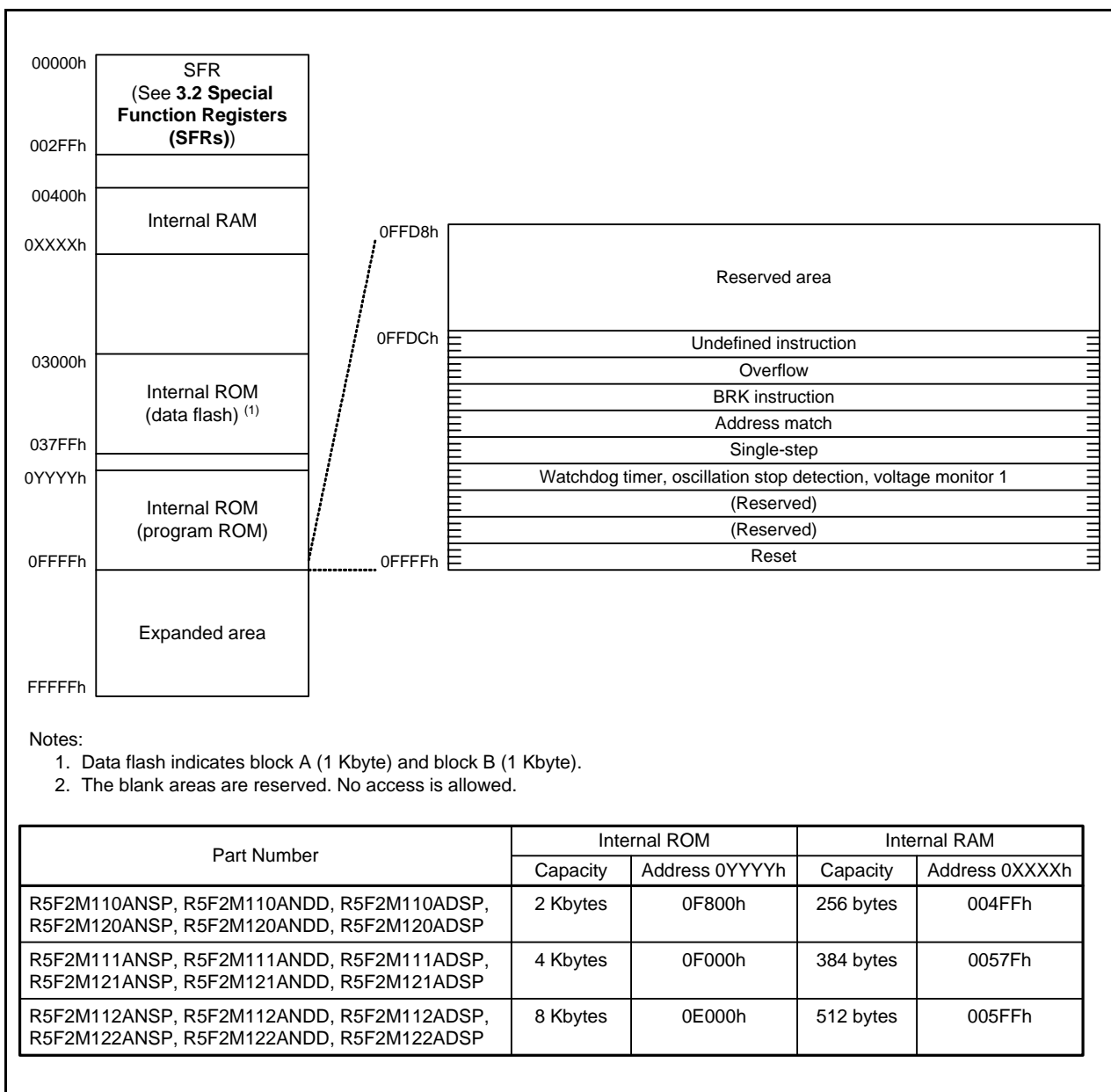


Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

| Address | Register Name | Symbol | After Reset |
|---------|--|--------|--------------------------|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | | | |
| 0005h | | | |
| 0006h | | | |
| 0007h | | | |
| 0008h | | | |
| 0009h | | | |
| 000Ah | | | |
| 000Bh | | | |
| 000Ch | | | |
| 000Dh | | | |
| 000Eh | | | |
| 000Fh | | | |
| 0010h | Processor Mode Register 0 | PM0 | 00h |
| 0011h | | | |
| 0012h | Module Standby Control Register | MSTCR | 00h (2) 01110111b (3) |
| 0013h | Protect Register | PRCR | 00h |
| 0014h | | | |
| 0015h | | | |
| 0016h | Hardware Reset Protect Register | HRPR | 00h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | | | |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | External Clock Control Register | EXCKCR | 00h |
| 0021h | High-Speed/Low-Speed On-Chip Oscillator Control Register | OCOCR | 00h |
| 0022h | System Clock f Control Register | SCKCR | 00h |
| 0023h | System Clock f Select Register | PHISEL | 00h |
| 0024h | Clock Stop Control Register | CKSTPR | 00h |
| 0025h | Clock Control Register When Returning from Modes | CKRSCR | 00h |
| 0026h | Oscillation Stop Detection Register | BAKCR | 00h |
| 0027h | | | |
| 0028h | | | |
| 0029h | | | |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h | Watchdog Timer Function Register | RISR | 1000000b (4) 00h (5) |
| 0031h | Watchdog Timer Reset Register | WDTR | XXh |
| 0032h | Watchdog Timer Start Register | WDTS | XXh |
| 0033h | Watchdog Timer Control Register | WDTC | 01XXXXXb |
| 0034h | Count Source Protection Mode Register | CSPR | 1000000b (4) 00h (5) |
| 0035h | Periodic Timer Interrupt Control Register | WDTIR | 00h |
| 0036h | | | |
| 0037h | | | |
| 0038h | External Input Enable Register | INTEN | 00h |
| 0039h | | | |

Notes:

1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.2 SFR Information (2) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---|--------|--------------------------------|
| 0003Ah | INT Input Filter Select Register 0 | INTF0 | 00h |
| 0003Bh | | | |
| 0003Ch | INT Input Edge Select Register 0 | ISCR0 | 00h |
| 0003Dh | | | |
| 0003Eh | Key Input Enable Register | KIEN | 00h |
| 0003Fh | | | |
| 00040h | Interrupt Priority Level Register 0 | ILVLO | 00h |
| 00041h | | | |
| 00042h | Interrupt Priority Level Register 2 | ILVL2 | 00h |
| 00043h | Interrupt Priority Level Register 3 | ILVL3 | 00h |
| 00044h | Interrupt Priority Level Register 4 | ILVL4 | 00h |
| 00045h | Interrupt Priority Level Register 5 | ILVL5 | 00h |
| 00046h | Interrupt Priority Level Register 6 | ILVL6 | 00h |
| 00047h | Interrupt Priority Level Register 7 | ILVL7 | 00h |
| 00048h | Interrupt Priority Level Register 8 | ILVL8 | 00h |
| 00049h | Interrupt Priority Level Register 9 | ILVL9 | 00h |
| 0004Ah | Interrupt Priority Level Register A | ILVLA | 00h |
| 0004Bh | Interrupt Priority Level Register B | ILVLB | 00h |
| 0004Ch | Interrupt Priority Level Register C | ILVLC | 00h |
| 0004Dh | Interrupt Priority Level Register D | ILVLD | 00h |
| 0004Eh | Interrupt Priority Level Register E | ILVLE | 00h |
| 0004Fh | | | |
| 00050h | Interrupt Monitor Flag Register 0 | IRR0 | 00h |
| 00051h | Interrupt Monitor Flag Register 1 | IRR1 | 00h |
| 00052h | Interrupt Monitor Flag Register 2 | IRR2 | 00h |
| 00053h | External Interrupt Flag Register | IRR3 | 00h |
| 00054h | | | |
| 00055h | | | |
| 00056h | | | |
| 00057h | | | |
| 00058h | Voltage Monitor Circuit Edge Select Register | VCAC | 00h |
| 00059h | | | |
| 0005Ah | Voltage Detect Register 2 | VCA2 | 00100100b (2) 00000100b (3) |
| 0005Bh | Voltage Detection 1 Level Select Register | VD1LS | 00000111b |
| 0005Ch | Voltage Monitor 0 Circuit Control Register | VW0C | 1100X011b (2) 1100X010b (3) |
| 0005Dh | Voltage Monitor 1 Circuit Control Register | VW1C | 10001010b |
| 0005Eh | | | |
| 0005Fh | Reset Source Determination Register | RSTFR | 0000XXXXb (4) |
| 00060h | | | |
| 00061h | | | |
| 00062h | | | |
| 00063h | | | |
| 00064h | High-Speed On-Chip Oscillator 18.432 MHz Control Register 0 | FR18S0 | Value when shipped |
| 00065h | High-Speed On-Chip Oscillator 18.432 MHz Control Register 1 | FR18S1 | Value when shipped |
| 00066h | | | |
| 00067h | High-Speed On-Chip Oscillator Control Register 1 | FRV1 | Value when shipped |
| 00068h | High-Speed On-Chip Oscillator Control Register 2 | FRV2 | Value when shipped |
| 00069h | | | |
| 0006Ah | | | |
| 0006Bh | | | |
| 0006Ch | | | |
| 0006Dh | | | |
| 0006Eh | | | |
| 0006Fh | | | |
| 00070h | | | |
| 00071h | | | |
| 00072h | | | |
| 00073h | | | |
| 00074h | | | |
| 00075h | | | |
| 00076h | | | |
| 00077h | | | |
| 00078h | | | |
| 00079h | | | |

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. The LVDAS bit in the OFS register is 0.
3. The LVDAS bit in the OFS register is 1.
4. The value after a reset differs depending on the reset source.

Table 3.3 SFR Information (3) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---|---------|-------------|
| 0007Ah | | | |
| 0007Bh | | | |
| 0007Ch | | | |
| 0007Dh | | | |
| 0007Eh | | | |
| 0007Fh | | | |
| 00080h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00081h | UART0 Bit Rate Register | U0BRG | XXh |
| 00082h | UART0 Transmit Buffer Register | U0TBL | XXh |
| 00083h | | U0TBH | XXh |
| 00084h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00085h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00086h | UART0 Receive Buffer Register | U0RBL | XXh |
| 00087h | | U0RBH | XXh |
| 00088h | UART0 Interrupt Flag and Enable Register | U0IR | 00h |
| 00089h | | | |
| 0008Ah | | | |
| 0008Bh | | | |
| 0008Ch | | | |
| 0008Dh | | | |
| 0008Eh | | | |
| 0008Fh | | | |
| 00090h | | | |
| 00091h | | | |
| 00092h | | | |
| 00093h | | | |
| 00094h | | | |
| 00095h | | | |
| 00096h | | | |
| 00097h | | | |
| 00098h | A/D Register 0 | AD0L | XXh |
| 00099h | | AD0H | 000000XXb |
| 0009Ah | A/D Register 1 | AD1L | XXh |
| 0009Bh | | AD1H | 000000XXb |
| 0009Ch | A/D Mode Register | ADMOD | 00h |
| 0009Dh | A/D Input Select Register | ADINSEL | 00h |
| 0009Eh | A/D Control Register 0 | ADCON0 | 00h |
| 0009Fh | A/D Interrupt Control Status Register | ADICSR | 00h |
| 000A0h | | | |
| 000A1h | | | |
| 000A2h | | | |
| 000A3h | | | |
| 000A4h | | | |
| 000A5h | | | |
| 000A6h | | | |
| 000A7h | | | |
| 000A8h | | | |
| 000A9h | Port P1 Direction Register | PD1 | 00h |
| 000AAh | | | |
| 000ABh | Port P3 Direction Register | PD3 | 00h |
| 000ACh | Port P4 Direction Register | PD4 | 00h |
| 000ADh | Port PA Direction Register | PDA | 00h |
| 000AEh | | | |
| 000AFh | Port P1 Register | P1 | 00h |
| 000B0h | | | |
| 000B1h | Port P3 Register | P3 | 00h |
| 000B2h | Port P4 Register | P4 | 00h |
| 000B3h | Port PA Register | PA | 00h |
| 000B4h | | | |
| 000B5h | Pull-Up Control Register 1 | PUR1 | 00h |
| 000B6h | | | |
| 000B7h | Pull-Up Control Register 3 | PUR3 | 00h |
| 000B8h | Pull-Up Control Register 4 | PUR4 | 00h |
| 000B9h | Port I/O Function Control Register | PINSR | 00h |
| 000BAh | | | |
| 000BBh | Drive Capacity Control Register 1 | DRR1 | 00h |
| 000BCh | | | |
| 000BDh | Drive Capacity Control Register 3 | DRR3 | 00h |
| 000BEh | | | |
| 000BFh | | | |

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---|---------|-------------|
| 000C0h | | | |
| 000C1h | Open-Drain Control Register 1 | POD1 | 00h |
| 000C2h | | | |
| 000C3h | Open-Drain Control Register 3 | POD3 | 00h |
| 000C4h | Open-Drain Control Register 4 | POD4 | 00h |
| 000C5h | Port PA Mode Control Register | PAMCR | 00010001b |
| 000C6h | | | |
| 000C7h | | | |
| 000C8h | Port 1 Function Mapping Register 0 | PML1 | 00h |
| 000C9h | Port 1 Function Mapping Register 1 | PMH1 | 00h |
| 000CAh | | | |
| 000CBh | | | |
| 000CCh | Port 3 Function Mapping Register 0 | PML3 | 00h |
| 000CDh | Port 3 Function Mapping Register 1 | PMH3 | 00h |
| 000CEh | Port 4 Function Mapping Register 0 | PML4 | 00h |
| 000CFh | Port 4 Function Mapping Register 1 | PMH4 | 00h |
| 000D0h | | | |
| 000D1h | Port 1 Function Mapping Expansion Register | PMH1E | 00h |
| 000D2h | | | |
| 000D3h | | | |
| 000D4h | | | |
| 000D5h | Port 4 Function Mapping Expansion Register | PMH4E | 00h |
| 000D6h | | | |
| 000D7h | | | |
| 000D8h | Timer RJ Counter Register | TRJ | FFh |
| 000D9h | | | FFh |
| 000DAh | Timer RJ Control Register | TRJCR | 00h |
| 000DBh | Timer RJ I/O Control Register | TRJIOC | 00h |
| 000DCh | Timer RJ Mode Register | TRJMR | 00h |
| 000DDh | Timer RJ Event Select Register | TRJISR | 00h |
| 000DEh | Timer RJ Interrupt Control Register | TRJIR | 00h |
| 000DFh | | | |
| 000E0h | Timer RB Control Register | TRBCR | 00h |
| 000E1h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 000E2h | Timer RB I/O Control Register | TRBIOC | 00h |
| 000E3h | Timer RB Mode Register | TRBMR | 00h |
| 000E4h | Timer RB Prescaler Register (2) Timer RB Primary/Secondary Register (Lower 8 Bits) (3) | TRBPRES | FFh |
| 000E5h | Timer RB Primary Register (2) Timer RB Primary Register (Higher 8 Bits) (3) | TRBPRES | FFh |
| 000E6h | Timer RB Secondary Register (2) Timer RB Secondary Register (Higher 8 Bits) (3) | TRBSC | FFh |
| 000E7h | Timer RB Interrupt Control Register | TRBIR | 00h |
| 000E8h | Timer RC Counter | TRCCNT | 00h |
| 000E9h | | | 00h |
| 000EAh | Timer RC General Register A | TRCGRA | FFh |
| 000EBh | | | FFh |
| 000ECh | Timer RC General Register B | TRCGRB | FFh |
| 000EDh | | | FFh |
| 000EEh | Timer RC General Register C | TRCGRC | FFh |
| 000EFh | | | FFh |
| 000F0h | Timer RC General Register D | TRCGRD | FFh |
| 000F1h | | | FFh |
| 000F2h | Timer RC Mode Register | TRCMR | 01001000b |
| 000F3h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 000F4h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 000F5h | Timer RC Status Register | TRCSR | 01110000b |
| 000F6h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 000F7h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 000F8h | Timer RC Control Register 2 | TRCCR2 | 00011000b |
| 000F9h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 000FAh | Timer RC Output Enable Register | TRCOER | 01111111b |
| 000FBh | Timer RC A/D Conversion Trigger Control Register | TRCADCR | 11110000b |
| 000FCh | Timer RC Waveform Output Manipulation Register | TRCOPR | 00h |
| 000FDh | | | |
| 000FEh | | | |
| 000FFh | | | |

Notes:

1. The blank areas are reserved. No access is allowed.
2. The TCNT16 bit in the TRBMR register is 0.
3. The TCNT16 bit in the TRBMR register is 1.

Table 3.5 SFR Information (5) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---------------|--------|-------------|
| 00100h | | | |
| 00101h | | | |
| 00102h | | | |
| 00103h | | | |
| 00104h | | | |
| 00105h | | | |
| 00106h | | | |
| 00107h | | | |
| 00108h | | | |
| 00109h | | | |
| 0010Ah | | | |
| 0010Bh | | | |
| 0010Ch | | | |
| 0010Dh | | | |
| 0010Eh | | | |
| 0010Fh | | | |
| 00110h | | | |
| 00111h | | | |
| 00112h | | | |
| 00113h | | | |
| 00114h | | | |
| 00115h | | | |
| 00116h | | | |
| 00117h | | | |
| 00118h | | | |
| 00119h | | | |
| 0011Ah | | | |
| 0011Bh | | | |
| 0011Ch | | | |
| 0011Dh | | | |
| 0011Eh | | | |
| 0011Fh | | | |
| 00120h | | | |
| 00121h | | | |
| 00122h | | | |
| 00123h | | | |
| 00124h | | | |
| 00125h | | | |
| 00126h | | | |
| 00127h | | | |
| 00128h | | | |
| 00129h | | | |
| 0012Ah | | | |
| 0012Bh | | | |
| 0012Ch | | | |
| 0012Dh | | | |
| 0012Eh | | | |
| 0012Fh | | | |
| 00130h | | | |
| 00131h | | | |
| 00132h | | | |
| 00133h | | | |
| 00134h | | | |
| 00135h | | | |
| 00136h | | | |
| 00137h | | | |
| 00138h | | | |
| 00139h | | | |
| 0013Ah | | | |
| 0013Bh | | | |
| 0013Ch | | | |
| 0013Dh | | | |
| 0013Eh | | | |
| 0013Fh | | | |

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---------------|--------|-------------|
| 00140h | | | |
| 00141h | | | |
| 00142h | | | |
| 00143h | | | |
| 00144h | | | |
| 00145h | | | |
| 00146h | | | |
| 00147h | | | |
| 00148h | | | |
| 00149h | | | |
| 0014Ah | | | |
| 0014Bh | | | |
| 0014Ch | | | |
| 0014Dh | | | |
| 0014Eh | | | |
| 0014Fh | | | |
| 00150h | | | |
| 00151h | | | |
| 00152h | | | |
| 00153h | | | |
| 00154h | | | |
| 00155h | | | |
| 00156h | | | |
| 00157h | | | |
| 00158h | | | |
| 00159h | | | |
| 0015Ah | | | |
| 0015Bh | | | |
| 0015Ch | | | |
| 0015Dh | | | |
| 0015Eh | | | |
| 0015Fh | | | |
| 00160h | | | |
| 00161h | | | |
| 00162h | | | |
| 00163h | | | |
| 00164h | | | |
| 00165h | | | |
| 00166h | | | |
| 00167h | | | |
| 00168h | | | |
| 00169h | | | |
| 0016Ah | | | |
| 0016Bh | | | |
| 0016Ch | | | |
| 0016Dh | | | |
| 0016Eh | | | |
| 0016Fh | | | |
| 00170h | | | |
| 00171h | | | |
| 00172h | | | |
| 00173h | | | |
| 00174h | | | |
| 00175h | | | |
| 00176h | | | |
| 00177h | | | |
| 00178h | | | |
| 00179h | | | |
| 0017Ah | | | |
| 0017Bh | | | |
| 0017Ch | | | |
| 0017Dh | | | |
| 0017Eh | | | |
| 0017Fh | | | |

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

| Address | Register Name | Symbol | After Reset |
|---------|--|----------|-------------|
| 00180h | Comparator B Control Register | WCMPR | 00h |
| 00181h | Comparator B1 Interrupt Control Register | WCB1INTR | 00h |
| 00182h | Comparator B3 Interrupt Control Register | WCB3INTR | 00h |
| 00183h | | | |
| 00184h | | | |
| 00185h | | | |
| 00186h | | | |
| 00187h | | | |
| 00188h | | | |
| 00189h | | | |
| 0018Ah | | | |
| 0018Bh | | | |
| 0018Ch | | | |
| 0018Dh | | | |
| 0018Eh | | | |
| 0018Fh | | | |
| 00190h | | | |
| 00191h | | | |
| 00192h | | | |
| 00193h | | | |
| 00194h | | | |
| 00195h | | | |
| 00196h | | | |
| 00197h | | | |
| 00198h | | | |
| 00199h | | | |
| 0019Ah | | | |
| 0019Bh | | | |
| 0019Ch | | | |
| 0019Dh | | | |
| 0019Eh | | | |
| 0019Fh | | | |
| 001A0h | | | |
| 001A1h | | | |
| 001A2h | | | |
| 001A3h | | | |
| 001A4h | | | |
| 001A5h | | | |
| 001A6h | | | |
| 001A7h | | | |
| 001A8h | | | |
| 001A9h | Flash Memory Status Register | FST | 10000000b |
| 001AAh | Flash Memory Control Register 0 | FMR0 | 00h |
| 001ABh | Flash Memory Control Register 1 | FMR1 | 00h |
| 001ACh | Flash Memory Control Register 2 | FMR2 | 00h |
| 001ADh | Flash Memory Refresh Control Register | FREFR | 00h |
| 001AEh | | | |
| 001AFh | | | |
| 001B0h | | | |
| 001B1h | | | |
| 001B2h | | | |
| 001B3h | | | |
| 001B4h | | | |
| 001B5h | | | |
| 001B6h | | | |
| 001B7h | | | |
| 001B8h | | | |
| 001B9h | | | |
| 001BAh | | | |
| 001BBh | | | |
| 001BCh | | | |
| 001BDh | | | |
| 001BEh | | | |
| 001BFh | | | |

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

| Address | Register Name | Symbol | After Reset |
|---------|---|---------|-------------|
| 001C0h | Address Match Interrupt Register 0 | AIADR0L | 00h |
| 001C1h | | AIADR0M | 00h |
| 001C2h | | AIADR0H | 00h |
| 001C3h | Address Match Interrupt Enable Register 0 | AIEN0 | 00h |
| 001C4h | Address Match Interrupt Register 1 | AIADR1L | 00h |
| 001C5h | | AIADR1M | 00h |
| 001C6h | | AIADR1H | 00h |
| 001C7h | Address Match Interrupt Enable Register 1 | AIEN1 | 00h |
| 001C8h | | | |
| 001C9h | | | |
| 001CAh | | | |
| 001CBh | | | |
| 001CCh | | | |
| 001CDh | | | |
| 001CEh | | | |
| 001CFh | | | |
| 001D0h | | | |
| 001D1h | | | |
| 001D2h | | | |
| 001D3h | | | |
| 001D4h | | | |
| 001D5h | | | |
| 001D6h | | | |
| 001D7h | | | |
| 001D8h | | | |
| 001D9h | | | |
| 001DAh | | | |
| 001DBh | | | |
| 001DCh | | | |
| 001DDh | | | |
| 001DEh | | | |
| 001DFh | | | |
| 001E0h | | | |
| 001E1h | | | |
| 001E2h | | | |
| 001E3h | | | |
| 001E4h | | | |
| 001E5h | | | |
| 001E6h | | | |
| 001E7h | | | |
| 001E8h | | | |
| 001E9h | | | |
| 001EAh | | | |
| 001EBh | | | |
| 001ECh | | | |
| 001EDh | | | |
| 001EEh | | | |
| 001EFh | | | |
| 001F0h | | | |
| 001F1h | | | |
| 001F2h | | | |
| 001F3h | | | |
| 001F4h | | | |
| 001F5h | | | |
| 001F6h | | | |
| 001F7h | | | |
| 001F8h | | | |
| 001F9h | | | |
| 001FAh | | | |
| 001FBh | | | |
| 001FCh | | | |
| 001FDh | | | |
| 001FEh | | | |
| 001FFh | | | |

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

| Address | Area Name | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| : | | | |
| 0FFDBh | Option Function Select Register 2 | OFS2 | (Note 1) |
| : | | | |
| 0FFDFh | ID1 | | (Note 2) |
| : | | | |
| 0FFE3h | ID2 | | (Note 2) |
| : | | | |
| 0FFEBh | ID3 | | (Note 2) |
| : | | | |
| 0FFEFh | ID4 | | (Note 2) |
| : | | | |
| 0FFF3h | ID5 | | (Note 2) |
| : | | | |
| 0FFF7h | ID6 | | (Note 2) |
| : | | | |
| 0FFFBh | ID7 | | (Note 2) |
| : | | | |
| 0FFFFh | Option Function Select Register | OFS | (Note 1) |

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

4. Electrical Characteristics

Table 4.1 Absolute Maximum Ratings

| Symbol | Parameter | | Condition | Rated Value | Unit |
|-----------------------------------|-------------------------------|------------|--|---|------|
| V _{cc} /AV _{cc} | Power supply voltage | | | -0.3 to 6.5 | V |
| V _i | Input voltage | XIN | XIN-XOUT oscillation on (oscillation circuit used) ⁽¹⁾ | -0.3 to 1.9 | V |
| | | | XIN-XOUT oscillation off (oscillation circuit not used) ⁽¹⁾ | -0.3 to V _{cc} + 0.3 | V |
| | | Other pins | | -0.3 to V _{cc} + 0.3 | V |
| V _o | Output voltage | XOUT | XIN-XOUT oscillation on (oscillation circuit used) ⁽¹⁾ | -0.3 to 1.9 | V |
| | | | XIN-XOUT oscillation off (oscillation circuit not used) ⁽¹⁾ | -0.3 to V _{cc} + 0.3 | V |
| | | Other pins | | -0.3 to V _{cc} + 0.3 | V |
| P _d | Power consumption | | -40 °C ≤ Topr ≤ 85 °C | 500 | mW |
| T _{opr} | Operating ambient temperature | | | -20 to 85 (N version)/ -40 to 85 (D version) | °C |
| T _{stg} | Storage temperature | | | -60 to 150 | °C |

Note:

- When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Table 4.2 Recommended Operating Conditions

| Symbol | Parameter | | Condition | Standard | | | Unit |
|-----------------------------------|--|---------------------------------------|--|----------------------|------|---------------------|------|
| | | | | Min. | Typ. | Max. | |
| V _{CC} /AV _{CC} | Power supply voltage | | | 1.8 | — | 5.5 | V |
| V _{SS} /AV _{SS} | Power supply voltage | | | — | 0 | — | V |
| V _{IH} | Input high voltage | Other than CMOS input | | 0.8 V _{CC} | — | V _{CC} | V |
| | | CMOS input | 4.0 V ≤ V _{CC} ≤ 5.5 V | 0.65 V _{CC} | — | V _{CC} | V |
| | | | 2.7 V ≤ V _{CC} < 4.0 V | 0.7 V _{CC} | — | V _{CC} | V |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | 0.8 V _{CC} | — | V _{CC} | V |
| V _{IL} | Input low voltage | Other than CMOS input | | 0 | — | 0.2 V _{CC} | V |
| | | CMOS input | 4.0 V ≤ V _{CC} ≤ 5.5 V | 0 | — | 0.4 V _{CC} | V |
| | | | 2.7 V ≤ V _{CC} < 4.0 V | 0 | — | 0.3 V _{CC} | V |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | 0 | — | 0.2 V _{CC} | V |
| I _{OH(sum)} | Peak sum output high current | Sum of all pins I _{OH(peak)} | | — | — | -160 | mA |
| I _{OH(sum)} | Average sum output high current | Sum of all pins I _{OH(avg)} | | — | — | -80 | mA |
| I _{OH(peak)} | Peak output high current | | When drive capacity is low | — | — | -10 | mA |
| | | | When drive capacity is high ⁽⁵⁾ | — | — | -40 | mA |
| I _{OH(avg)} | Average output high current | | When drive capacity is low | — | — | -5 | mA |
| | | | When drive capacity is high ⁽⁵⁾ | — | — | -20 | mA |
| I _{OL(sum)} | Peak sum output low current | Sum of all pins I _{OL(peak)} | | — | — | 160 | mA |
| I _{OL(sum)} | Average sum output low current | Sum of all pins I _{OL(avg)} | | — | — | 80 | mA |
| I _{OL(peak)} | Peak output low current | | When drive capacity is low | — | — | 10 | mA |
| | | | When drive capacity is high ⁽⁵⁾ | — | — | 40 | mA |
| I _{OL(avg)} | Average output low current | | When drive capacity is low | — | — | 5 | mA |
| | | | When drive capacity is high ⁽⁵⁾ | — | — | 20 | mA |
| f _(XIN) | XIN oscillation frequency | | 2.7 V ≤ V _{CC} ≤ 5.5 V | 2 | — | 20 | MHz |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | 2 | — | 5 | MHz |
| | XIN clock input oscillation frequency | | 2.7 V ≤ V _{CC} ≤ 5.5 V | 0 | — | 20 | MHz |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | 0 | — | 5 | MHz |
| f _{HOCO} | High-speed on-chip oscillator oscillation frequency ⁽³⁾ | | 1.8 V ≤ V _{CC} ≤ 5.5 V | — | 20 | — | MHz |
| f _{LOCO} | Low-speed on-chip oscillator oscillation frequency ⁽⁴⁾ | | 1.8 V ≤ V _{CC} ≤ 5.5 V | — | 125 | — | kHz |
| — | System clock frequency | | 2.7 V ≤ V _{CC} ≤ 5.5 V | — | — | 20 | MHz |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | — | — | 5 | MHz |
| f _s | CPU clock frequency | | 2.7 V ≤ V _{CC} ≤ 5.5 V | 0 | — | 20 | MHz |
| | | | 1.8 V ≤ V _{CC} < 2.7 V | 0 | — | 5 | MHz |

Notes:

1. V_{CC} = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

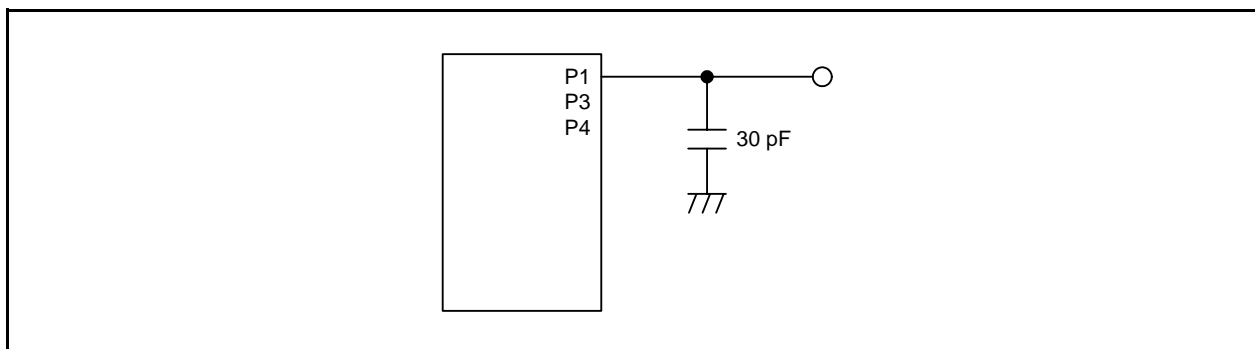
**Figure 4.1 Ports P1, P3, and P4 Timing Measurement Circuit**

Table 4.3 A/D Converter Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|-------------------------------------|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | — | — | 10 | Bit |
| — | Absolute accuracy | AVcc = 5.0 V AN0 to AN4, AN7 input | — | — | ±3 | LSB |
| | | AVcc = 3.0 V AN0 to AN4, AN7 input | — | — | ±5 | LSB |
| | | AVcc = 1.8 V AN0 to AN4, AN7 input | — | — | ±5 | LSB |
| — | A/D conversion clock | 4.0 V ≤ AVcc ≤ 5.5 V (2) | 2 | — | 20 | MHz |
| | | 3.2 V ≤ AVcc ≤ 5.5 V (2) | 2 | — | 16 | MHz |
| | | 2.7 V ≤ AVcc ≤ 5.5 V (2) | 2 | — | 10 | MHz |
| | | 1.8 V ≤ AVcc ≤ 5.5 V (2) | 2 | — | 5 | MHz |
| — | Permissible signal source impedance | | | 3 | | kΩ |
| tCONV | Conversion time | AVcc = 5.0 V, A/D conversion clock = 20 MHz | 2.20 | — | — | μs |
| tSAMP | Sampling time | A/D conversion clock = 20 MHz | 0.80 | — | — | μs |
| VIA | Analog input voltage | | 0 | — | AVcc | V |

Notes:

1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

Table 4.4 Comparator B Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--------------------|----------|------|-----------|------|
| | | | Min. | Typ. | Max. | |
| Vref | IVREF1, IVREF3 input reference voltage | | 0 | — | Vcc - 1.4 | V |
| Vi | IVCMP1, IVCMP3 input voltage | | -0.3 | — | Vcc + 0.3 | V |
| — | Offset | | — | 5 | 100 | mV |
| td | Comparator output delay time (2) | Vi = Vref ± 100 mV | — | 0.1 | — | μs |
| IcMP | Comparator operating current | Vcc = 5.0 V | — | 17.5 | — | μA |

Notes:

1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 4.5 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------------------|---|-----------------------------|-----------------------|------|--------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| — | Program/erase endurance ⁽²⁾ | | 10,000 ⁽³⁾ | — | — | times |
| — | Byte programming time (program/erase endurance ≤ 1,000 times) | | — | 80 | — | μs |
| — | Byte programming time (program/erase endurance > 1,000 times) | | — | 160 | — | μs |
| — | Block erase time | | — | 0.12 | — | s |
| t _d (SR-SUS) | Transition time to suspend | | — | — | 0.25 + CPU clock × 3 cycles | ms |
| — | Time from suspend until erase restart | | — | — | 30 + CPU clock × 1 cycle | μs |
| t _d (CMDRST READY) | Time from when command is forcibly terminated until reading is enabled | | — | — | 30 + CPU clock × 1 cycle | μs |
| — | Program/erase voltage | | 1.8 | — | 5.5 | V |
| — | Read voltage | | 1.8 | — | 5.5 | V |
| — | Program/erase temperature | | 0 | — | 60 | °C |
| — | Data hold time ⁽⁷⁾ | Ambient temperature = 85 °C | 10 | — | — | years |

Notes:

- V_{cc} = 2.7 V to 5.5 V and T_{opr} = 0 °C to 60 °C, unless otherwise specified.
- Definition of program/erase endurance
The number of program/erase cycles is defined on a per-block basis.
If the number of cycles is 10,000, each block can be erased 10,000 times.
For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
- This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
- In a system that executes multiple programming operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
- If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
- For information on the program/erase failure rate, contact a Renesas technical support representative.
- The data hold time includes the time that the power supply is off and the time the clock is not supplied.

Table 4.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------------------|---|-----------------------------|-----------------------|------|--------------------------------|-------|
| | | | Min. | Typ. | Max. | |
| — | Program/erase endurance ⁽²⁾ | | 10,000 ⁽³⁾ | — | — | times |
| — | Byte programming time | | — | 150 | — | μs |
| — | Block erase time | | — | 0.05 | 1 | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | — | — | 0.25 + CPU clock × 3 cycles | ms |
| — | Time from suspend until erase restart | | — | — | 30 + CPU clock × 1 cycle | μs |
| t _d (CMDRST-READY) | Time from when command is forcibly stopped until reading is enabled | | — | — | 30 + CPU clock × 1 cycle | μs |
| — | Program/erase voltage | | 1.8 | — | 5.5 | V |
| — | Read voltage | | 1.8 | — | 5.5 | V |
| — | Program/erase temperature | | -20 (N version) | — | 85 | °C |
| | | | -40 (D version) | — | 85 | °C |
| — | Data hold time ⁽⁷⁾ | Ambient temperature = 85 °C | 10 | — | — | years |

Notes:

- V_{cc} = 2.7 V to 5.5 V and T_{opr} = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
- Definition of program/erase endurance
The number of program/erase cycles is defined on a per-block basis.
If the number of cycles is 10,000, each block can be erased 10,000 times.
For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
- This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
- In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
- If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
- For information on the program/erase failure rate, contact a Renesas technical support representative.
- The data hold time includes the time that the power supply is off and the time the clock is not supplied.

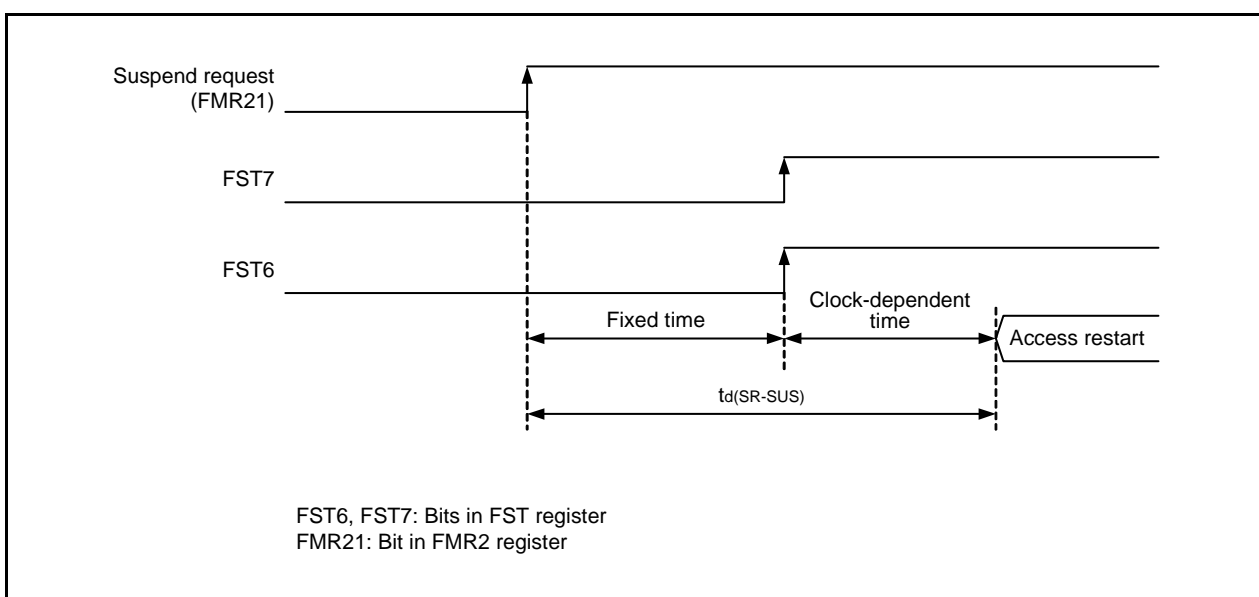


Figure 4.2 Transition Time until Suspend

Table 4.7 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------|---|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Vdet0 | Voltage detection level Vdet0_0 ⁽²⁾ | | 1.80 | 1.90 | 2.05 | V |
| | Voltage detection level Vdet0_1 ⁽²⁾ | | 2.15 | 2.35 | 2.50 | V |
| | Voltage detection level Vdet0_2 ⁽²⁾ | | 2.70 | 2.85 | 3.05 | V |
| | Voltage detection level Vdet0_3 ⁽²⁾ | | 3.55 | 3.80 | 4.05 | V |
| — | Voltage detection 0 circuit response time ⁽³⁾ | When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V | — | 30 | — | μs |
| — | Self power consumption in voltage detection circuit | VC0E = 1, Vcc = 5.0 V | — | 1.5 | — | μA |
| td(E-A) | Wait time until voltage detection circuit operation starts ⁽⁴⁾ | | — | — | 100 | μs |

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 4.8 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------|---|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Vdet1 | Voltage detection level Vdet1_1 ⁽²⁾ | When Vcc decreases | 2.15 | 2.35 | 2.55 | V |
| | Voltage detection level Vdet1_3 ⁽²⁾ | When Vcc decreases | 2.45 | 2.65 | 2.85 | V |
| | Voltage detection level Vdet1_5 ⁽²⁾ | When Vcc decreases | 2.75 | 2.95 | 3.15 | V |
| | Voltage detection level Vdet1_7 ⁽²⁾ | When Vcc decreases | 3.00 | 3.25 | 3.55 | V |
| | Voltage detection level Vdet1_9 ⁽²⁾ | When Vcc decreases | 3.30 | 3.55 | 3.85 | V |
| | Voltage detection level Vdet1_B ⁽²⁾ | When Vcc decreases | 3.60 | 3.85 | 4.15 | V |
| | Voltage detection level Vdet1_D ⁽²⁾ | When Vcc decreases | 3.90 | 4.15 | 4.45 | V |
| | Voltage detection level Vdet1_F ⁽²⁾ | When Vcc decreases | 4.20 | 4.45 | 4.75 | V |
| — | Hysteresis width at the rising of Vcc in voltage detection 1 circuit | Vdet1_1 to Vdet1_5 selected | — | 0.07 | — | V |
| | | Vdet1_7 to Vdet1_F selected | — | 0.10 | — | V |
| — | Voltage detection 1 circuit response time ⁽³⁾ | When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V | — | 60 | 150 | μs |
| — | Self power consumption in voltage detection circuit | VC1E = 1, Vcc = 5.0 V | — | 1.7 | — | μA |
| td(E-A) | Wait time until voltage detection circuit operation starts ⁽⁴⁾ | | — | — | 100 | μs |

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 4.9 Power-On Reset Circuit (2)

| Symbol | Parameter | Condition | Standard | | | Unit |
|-----------|----------------------------------|-----------|----------|------|--------|---------|
| | | | Min. | Typ. | Max. | |
| t_{rth} | External power Vcc rise gradient | | 0 | — | 50,000 | mV/msec |

Notes:

1. The measurement condition is $T_{opr} = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. To use the power-on reset function, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

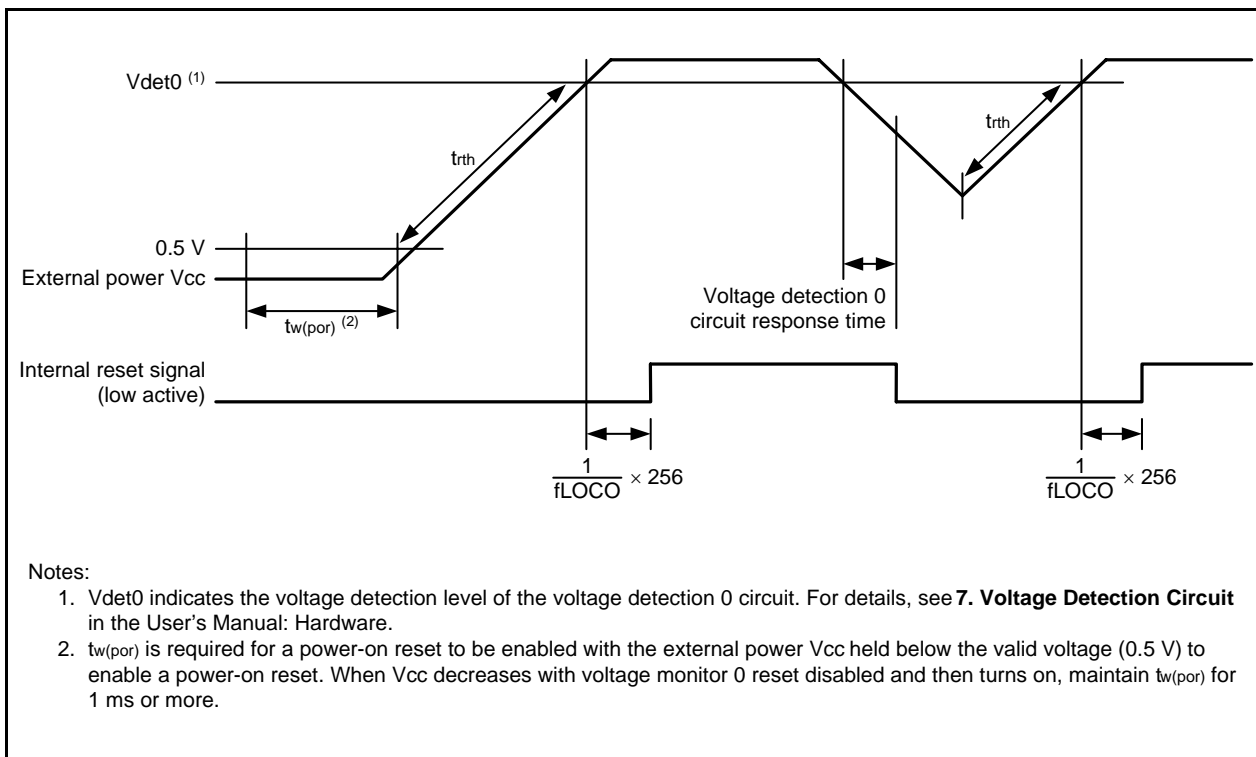


Figure 4.3 Power-On Reset Circuit Electrical Characteristics

Table 4.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Package | Condition | Standard | | | Unit |
|--------|--|------------------------------|--|----------|--------|--------|---------------|
| | | | | Min. | Typ. | Max. | |
| — | High-speed on-chip oscillator frequency after reset is cleared | 14-pin TSSOP 20-pin LSSOP | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $-20 \text{ }^\circ\text{C} \leq T_{opr} \leq 85 \text{ }^\circ\text{C}$ | 19.2 | 20.0 | 20.8 | MHz |
| | | 14-pin DIP 20-pin DIP | | 19.0 | 20.0 | 21.0 | MHz |
| | | 14-pin TSSOP 20-pin LSSOP | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $-40 \text{ }^\circ\text{C} \leq T_{opr} \leq 85 \text{ }^\circ\text{C}$ | 19.0 | 20.0 | 21.0 | MHz |
| — | High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register ⁽²⁾ | 14-pin TSSOP 20-pin LSSOP | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $-20 \text{ }^\circ\text{C} \leq T_{opr} \leq 85 \text{ }^\circ\text{C}$ | 17.694 | 18.432 | 19.169 | MHz |
| | | 14-pin DIP 20-pin DIP | | 17.510 | 18.432 | 19.353 | MHz |
| | | 14-pin TSSOP 20-pin LSSOP | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $-40 \text{ }^\circ\text{C} \leq T_{opr} \leq 85 \text{ }^\circ\text{C}$ | 17.510 | 18.432 | 19.353 | MHz |
| — | Oscillation stabilization time | — | | — | — | 30 | μs |
| — | Self power consumption at oscillation | — | $V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^\circ\text{C}$ | — | 530 | — | μA |

Notes:

- $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ }^\circ\text{C to } 85 \text{ }^\circ\text{C}$ (N version)/ $-40 \text{ }^\circ\text{C to } 85 \text{ }^\circ\text{C}$ (D version), unless otherwise specified.
- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

Table 4.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|--|--|----------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| f _{LOCO} | Low-speed on-chip oscillator frequency | | 60 | 125 | 250 | kHz |
| — | Oscillation stabilization time | | — | — | 35 | μs |
| — | Self power consumption at oscillation | $V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^\circ\text{C}$ | — | 2 | — | μA |

Note:

- $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ }^\circ\text{C to } 85 \text{ }^\circ\text{C}$ (N version)/ $-40 \text{ }^\circ\text{C to } 85 \text{ }^\circ\text{C}$ (D version), unless otherwise specified.

Table 4.12 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|---|-----------|----------|------|-------|---------------|
| | | | Min. | Typ. | Max. | |
| t _{d(P-R)} | Time for internal power supply stabilization during power-on ⁽²⁾ | | — | — | 2,000 | μs |

Notes:

- The measurement condition is $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ and $T_{opr} = 25 \text{ }^\circ\text{C}$.
- Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 4.13 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|------------------|---------------------|---|-----------------------------|-----------------------|-----------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| VOH | Output high voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | IOH = -20 mA | Vcc - 2.0 | — | Vcc | V |
| | | | When drive capacity is low | IOH = -5 mA | Vcc - 2.0 | — | Vcc | V |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | | IOH = -5 mA | Vcc - 2.0 | — | Vcc | V |
| VOL | Output low voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | IOL = 20 mA | — | — | 2.0 | V |
| | | | When drive capacity is low | IOL = 5 mA | — | — | 2.0 | V |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | | IOL = 5 mA | — | — | 2.0 | V |
| VT+-VT- | Hysteresis | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0 | Vcc = 5 V | | 0.1 | 1.2 | — | V |
| | | RESET | Vcc = 5 V | | 0.1 | 1.2 | — | V |
| IiH | Input high current | | | Vi = 5 V, Vcc = 5.0 V | — | — | 5.0 | μA |
| IiL | Input low current | | | Vi = 0 V, Vcc = 5.0 V | — | — | -5.0 | μA |
| RPULLUP | Pull-up resistance | | | Vi = 0 V, Vcc = 5.0 V | 25 | 50 | 100 | kΩ |
| RiXIN | Feedback resistance | XIN | | | — | 2.2 | — | MΩ |
| V _{RAM} | RAM hold voltage | | | In stop mode | 1.8 | — | — | V |

Notes:

- 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
- High drive capacity can also be used while the peripheral output function is used.

**Table 4.14 DC Characteristics (2) [4.0 V ≤ V_{CC} ≤ 5.5 V]
(Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)**

| Symbol | Parameter | | Condition | | | | | | | | | Unit |
|-----------------|--------------------------|------------------------------------|---------------------|--------------------|-----------|----------------|---|---|----------|----------|------|------|
| | | | Oscillation Circuit | On-Chip Oscillator | | CPU Clock | Low-Power-Consumption Setting | Other | Standard | | | |
| | | | XIN (2) | High-Speed | Low-Speed | | | | Min. | Typ. (3) | Max. | |
| I _{CC} | Power supply current (1) | High-speed clock mode | 20 MHz | Off | 125 kHz | No division | — | | — | 3 | 7.0 | mA |
| | | | 16 MHz | Off | 125 kHz | No division | — | | — | 2.5 | 6.0 | mA |
| | | | 10 MHz | Off | 125 kHz | No division | — | | — | 1.7 | — | mA |
| | | | 20 MHz | Off | 125 kHz | Division by 8 | — | | — | 1.5 | — | mA |
| | | | 16 MHz | Off | 125 kHz | Division by 8 | — | | — | 1.2 | — | mA |
| | | | 10 MHz | Off | 125 kHz | Division by 8 | — | | — | 1.0 | — | mA |
| | | High-speed on-chip oscillator mode | Off | 20 MHz | 125 kHz | No division | | | — | 3.5 | 7.5 | mA |
| | | | Off | 20 MHz | 125 kHz | Division by 8 | | | — | 2.0 | — | mA |
| | | | Off | 4 MHz (4) | 125 kHz | Division by 16 | MSTTRC = 1 | | — | 1.0 | — | mA |
| | | Low-speed on-chip oscillator mode | Off | Off | 125 kHz | Division by 8 | FMR27 = 1 LPE = 0 | | — | 60 | 270 | μA |
| | | Wait mode | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 | Peripheral clock supplied during WAIT instruction execution | — | 15 | 100 | μA |
| | | | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1 | Peripheral clock stopped during WAIT instruction execution | — | 4.0 | 90 | μA |
| | | Stop mode | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 25 °C Peripheral clock stopped | — | 1.0 | 4.0 | μA |
| | | | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 85 °C Peripheral clock stopped | — | 1.5 | — | μA |

Notes:

1. V_{CC} = 4.0 V to 5.5 V, single-chip mode, output pins are open, and other pins are connected to V_{SS}.
2. When the XIN input is a square wave.
3. V_{CC} = 5.0 V
4. Set the system clock to 4 MHz with the PHISEL register.

Timing Requirements ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Table 4.15 External Clock Input (XIN)

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | — | ns |
| $t_{WH(XIN)}$ | XIN input high width | 24 | — | ns |
| $t_{WL(XIN)}$ | XIN input low width | 24 | — | ns |

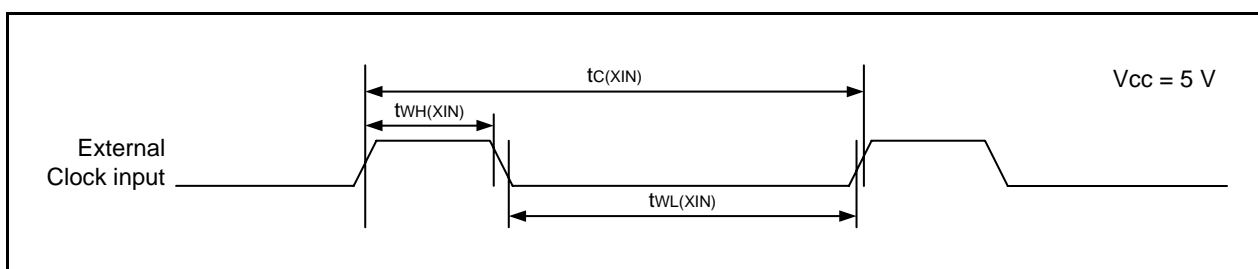


Figure 4.4 External Clock Input Timing When $V_{CC} = 5\text{ V}$

Table 4.16 TRJIO Input

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRJIO)}$ | TRJIO input cycle time | 100 | — | ns |
| $t_{WH(TRJIO)}$ | TRJIO input high width | 40 | — | ns |
| $t_{WL(TRJIO)}$ | TRJIO input low width | 40 | — | ns |

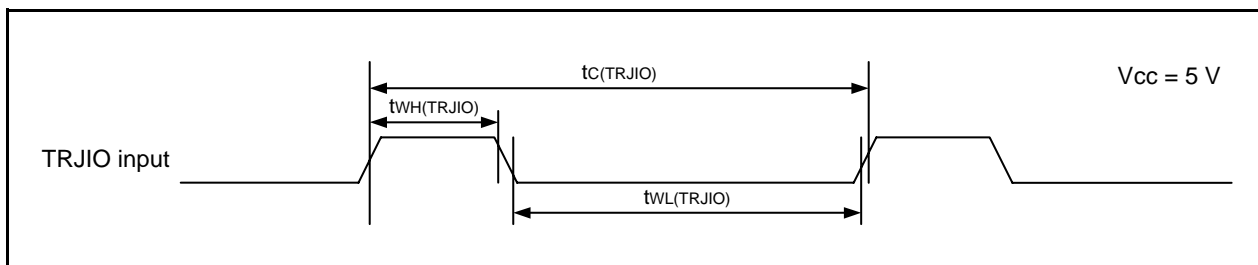


Figure 4.5 TRJIO Input Timing When $V_{CC} = 5\text{ V}$

Table 4.17 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|----------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{CK})$ | CLK0 input cycle time | 200 | — | ns |
| $t_w(\text{CKH})$ | CLK0 input high width | 100 | — | ns |
| $t_w(\text{CKL})$ | CLK0 input low width | 100 | — | ns |
| $t_d(\text{C-Q})$ | TXD0 output delay time | — | 50 | ns |
| $t_h(\text{C-Q})$ | TXD0 hold time | 0 | — | ns |
| $t_{su}(\text{D-C})$ | RXD0 input setup time | 50 | — | ns |
| $t_h(\text{C-D})$ | RXD0 input hold time | 90 | — | ns |

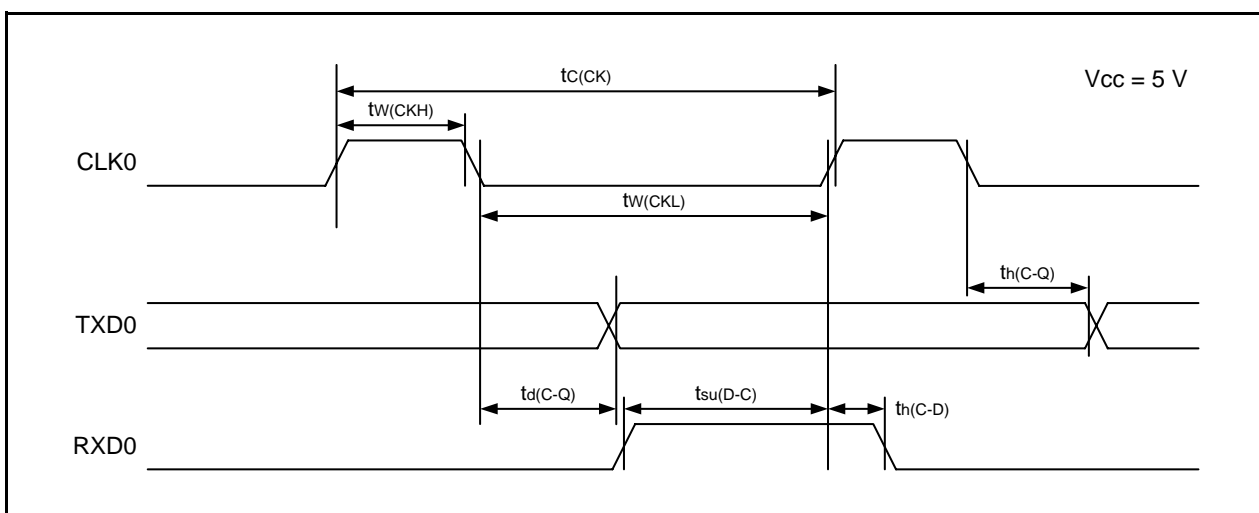


Figure 4.6 Serial Interface Timing When Vcc = 5 V

Table 4.18 External Interrupt $\overline{\text{INT}}_i$ Input, Key Input Interrupt $\overline{\text{K}}_i$ ($i = 0$ to 3)

| Symbol | Parameter | Standard | | Unit |
|-------------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_w(\text{INH})$ | $\overline{\text{INT}}_i$ input high width, $\overline{\text{K}}_i$ input high width | 250 (1) | — | ns |
| $t_w(\text{INL})$ | $\overline{\text{INT}}_i$ input low width, $\overline{\text{K}}_i$ input low width | 250 (2) | — | ns |

Notes:

1. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input high width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input low width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.

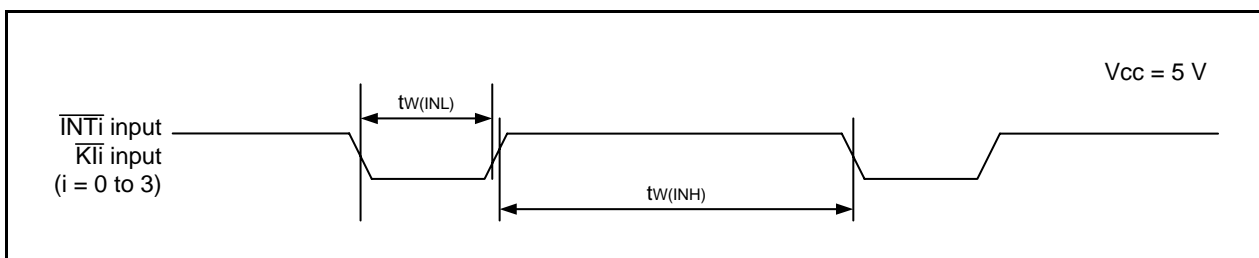


Figure 4.7 Timing for External Interrupt $\overline{\text{INT}}_i$ Input and Key Input Interrupt $\overline{\text{K}}_i$ When Vcc = 5 V

Table 4.19 DC Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.0\text{ V}$]

| Symbol | Parameter | | Condition | | Standard | | | Unit | | |
|----------------------------------|---------------------|---|-----------------------------|---|-----------------------|-----------------|-----------------|------|----|----|
| | | | | | Min. | Typ. | Max. | | | |
| V _{OH} | Output high voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | I _{OH} = -5 mA | V _{CC} - 0.5 | — | V _{CC} | V | | |
| | | | When drive capacity is low | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V | | |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V | | | |
| V _{OL} | Output low voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | I _{OL} = 5 mA | — | — | 0.5 | V | | |
| | | | When drive capacity is low | I _{OL} = 1 mA | — | — | 0.5 | V | | |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | I _{OL} = 1 mA | — | — | 0.5 | V | | | |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0 | V _{CC} = 3 V | | 0.1 | 0.4 | — | V | | |
| | | RESET | V _{CC} = 3 V | | 0.1 | 0.5 | — | V | | |
| I _{IH} | Input high current | | | V _I = 3 V, V _{CC} = 3.0 V | | — | — | 4.0 | μA | |
| I _{IL} | Input low current | | | V _I = 0 V, V _{CC} = 3.0 V | | — | — | -4.0 | μA | |
| R _{PULLUP} | Pull-up resistance | | | V _I = 0 V, V _{CC} = 3.0 V | | 42 | 84 | 168 | kΩ | |
| R _{iXIN} | Feedback resistance | XIN | | | | | — | 2.2 | — | MΩ |
| V _{RAM} | RAM hold voltage | | | In stop mode | | 1.8 | — | — | V | |

Notes:

1. $2.7\text{ V} \leq V_{CC} < 4.0\text{ V}$ and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

**Table 4.20 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]
(Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)**

| Symbol | Parameter | | Condition | | | | | | | | | Unit |
|-----------------|--------------------------|------------------------------------|---------------------|--------------------|-----------|----------------|---|---|----------|----------|------|------|
| | | | Oscillation Circuit | On-Chip Oscillator | | CPU Clock | Low-Power-Consumption Setting | Other | Standard | | | |
| | | | XIN (2) | High-Speed | Low-Speed | | | | Min. | Typ. (3) | Max. | |
| I _{CC} | Power supply current (1) | High-speed clock mode | 20 MHz | Off | 125 kHz | No division | — | | — | 3.0 | 7.0 | mA |
| | | | 16 MHz | Off | 125 kHz | No division | — | | — | 2.5 | 6.0 | mA |
| | | | 10 MHz | Off | 125 kHz | No division | — | | — | 1.6 | 5.0 | mA |
| | | | 20 MHz | Off | 125 kHz | Division by 8 | — | | — | 1.5 | — | mA |
| | | | 16 MHz | Off | 125 kHz | Division by 8 | — | | — | 1.2 | — | mA |
| | | | 10 MHz | Off | 125 kHz | Division by 8 | — | | — | 0.9 | 4.5 | mA |
| | | High-speed on-chip oscillator mode | Off | 20 MHz | 125 kHz | No division | | | — | 3.5 | 7.5 | mA |
| | | | Off | 20 MHz | 125 kHz | Division by 8 | | | — | 2.0 | — | mA |
| | | | Off | 10 MHz (4) | 125 kHz | No division | | | — | 2.2 | — | mA |
| | | | Off | 10 MHz (4) | 125 kHz | Division by 8 | | | — | 1.4 | — | mA |
| | | | Off | 4 MHz (4) | 125 kHz | Division by 16 | MSTTRC = 1 | | — | 1.0 | — | mA |
| | | Low-speed on-chip oscillator mode | Off | Off | 125 kHz | Division by 8 | FMR27 = 1 LPE = 0 | | — | 60 | 260 | μA |
| | | Wait mode | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 | Peripheral clock supplied during WAIT instruction execution | — | 15 | 90 | μA |
| | | | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1 | Peripheral clock stopped during WAIT instruction execution | — | 4.0 | 80 | μA |
| | | Stop mode | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 25 °C Peripheral clock stopped | — | 1.0 | 4.0 | μA |
| | | | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 85 °C Peripheral clock stopped | — | 1.5 | — | μA |

Notes:

1. V_{CC} = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to V_{SS}.
2. When the XIN input is a square wave.
3. V_{CC} = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

Timing Requirements ($V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Table 4.21 External Clock Input (XIN)

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | — | ns |
| $t_{WH(XIN)}$ | XIN input high width | 24 | — | ns |
| $t_{WL(XIN)}$ | XIN input low width | 24 | — | ns |

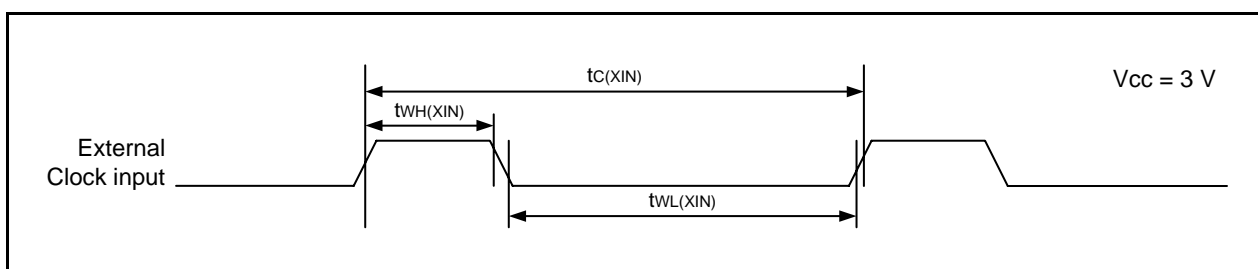
Figure 4.8 External Clock Input Timing When $V_{CC} = 3\text{ V}$

Table 4.22 TRJIO Input

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRJIO)}$ | TRJIO input cycle time | 300 | — | ns |
| $t_{WH(TRJIO)}$ | TRJIO input high width | 120 | — | ns |
| $t_{WL(TRJIO)}$ | TRJIO input low width | 120 | — | ns |

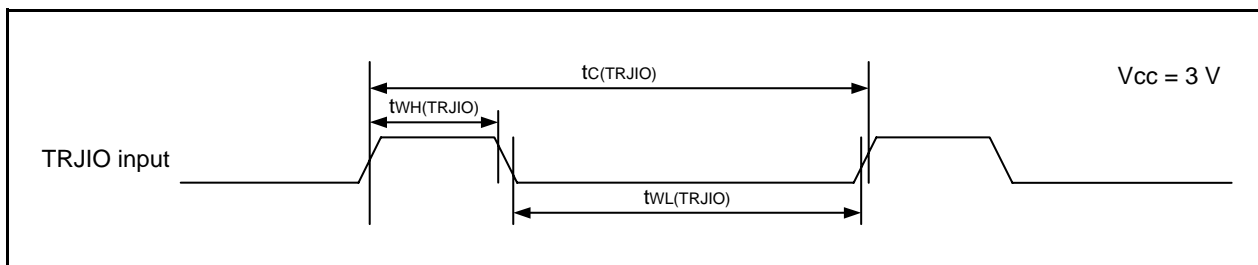
Figure 4.9 TRJIO Input Timing When $V_{CC} = 3\text{ V}$

Table 4.23 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|----------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{CK})$ | CLK0 input cycle time | 300 | — | ns |
| $t_w(\text{CKH})$ | CLK0 input high width | 150 | — | ns |
| $t_w(\text{CKL})$ | CLK0 input low width | 150 | — | ns |
| $t_d(\text{C-Q})$ | TXD0 output delay time | — | 80 | ns |
| $t_h(\text{C-Q})$ | TXD0 hold time | 0 | — | ns |
| $t_{su}(\text{D-C})$ | RXD0 input setup time | 70 | — | ns |
| $t_h(\text{C-D})$ | RXD0 input hold time | 90 | — | ns |

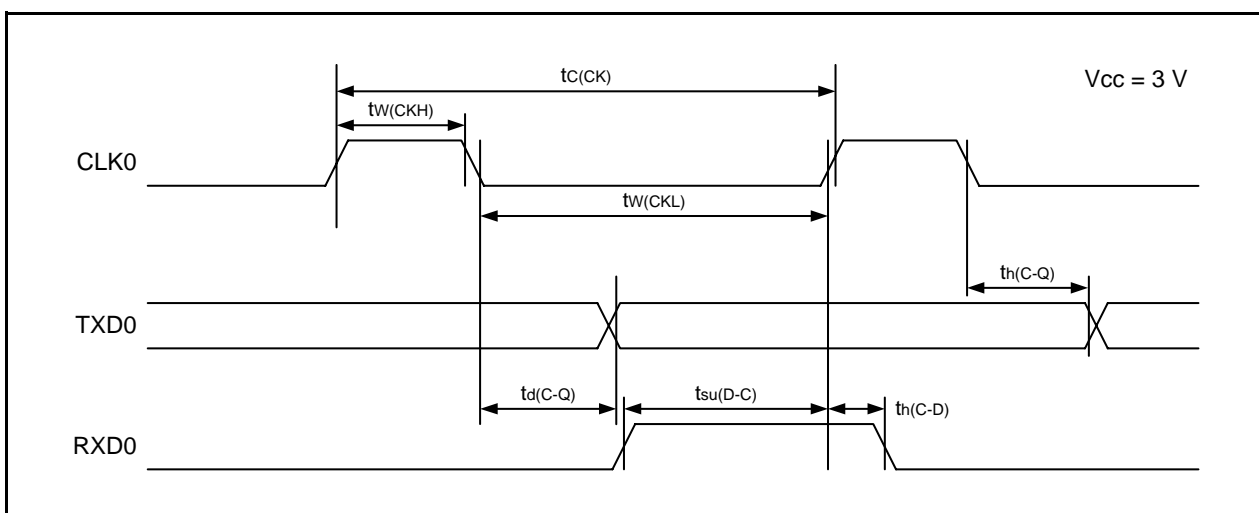


Figure 4.10 Serial Interface Timing When Vcc = 3 V

Table 4.24 External Interrupt $\overline{\text{INT}}_i$ Input, Key Input Interrupt $\overline{\text{K}}_i$ ($i = 0$ to 3)

| Symbol | Parameter | Standard | | Unit |
|-------------------|--|----------|------|------|
| | | Min. | Max. | |
| $t_w(\text{INH})$ | $\overline{\text{INT}}_i$ input high width, $\overline{\text{K}}_i$ input high width | 380 (1) | — | ns |
| $t_w(\text{INL})$ | $\overline{\text{INT}}_i$ input low width, $\overline{\text{K}}_i$ input low width | 380 (2) | — | ns |

Notes:

1. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input high width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input low width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.

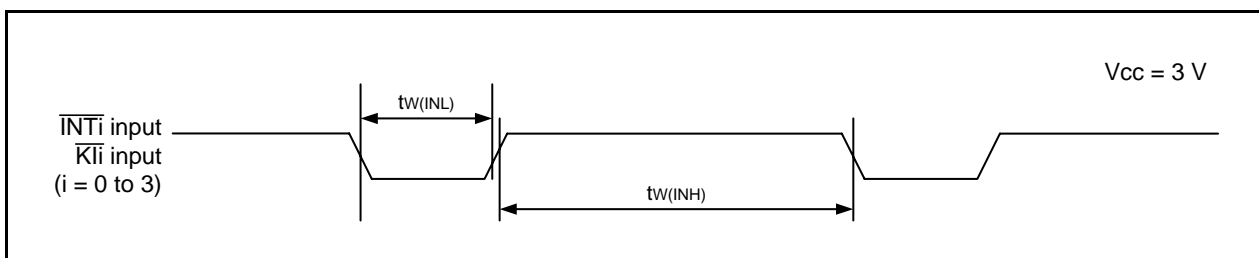


Figure 4.11 Timing for External Interrupt $\overline{\text{INT}}_i$ Input and Key Input Interrupt $\overline{\text{K}}_i$ When Vcc = 3 V

Table 4.25 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|--|-----------------------------|---|-----------------------|-----------------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output high voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | I _{OH} = -2 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| | | | When drive capacity is low | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | I _{OH} = -1 mA | V _{CC} - 0.5 | — | V _{CC} | V | |
| V _{OL} | Output low voltage | P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2) | When drive capacity is high | I _{OL} = 2 mA | — | — | 0.5 | V |
| | | | When drive capacity is low | I _{OL} = 1 mA | — | — | 0.5 | V |
| | | P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0 | I _{OL} = 1 mA | — | — | 0.5 | V | |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIO, TRCIOD, RXD0, CLK0 | V _{CC} = 2.2 V | | 0.05 | 0.20 | — | V |
| | | RESET | V _{CC} = 2.2 V | | 0.05 | 0.20 | — | V |
| I _{IH} | Input high current | | | V _I = 2.2 V, V _{CC} = 2.2 V | — | — | 4.0 | μA |
| I _{IL} | Input low current | | | V _I = 0 V, V _{CC} = 2.2 V | — | — | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | | V _I = 0 V, V _{CC} = 2.2 V | 70 | 140 | 300 | kΩ |
| R _{iXIN} | Feedback resistance | XIN | | | — | 2.2 | — | MΩ |
| V _{RAM} | RAM hold voltage | | | In stop mode | 1.8 | — | — | V |

Notes:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 4.26 DC Characteristics (6) [1.8 V ≤ V_{CC} < 2.7 V]
(Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

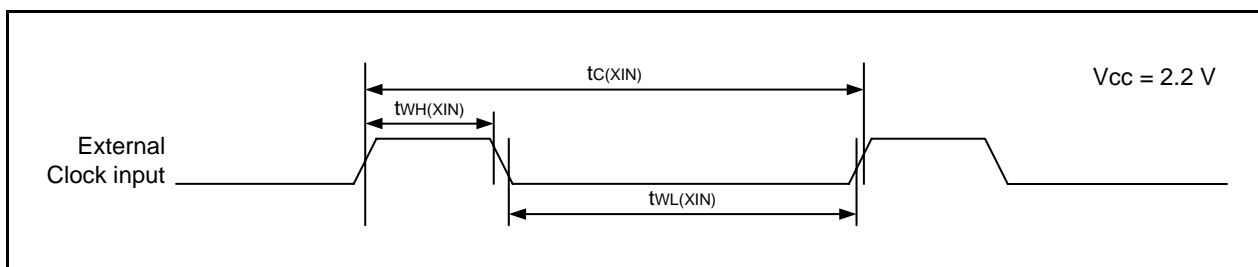
| Symbol | Parameter | | Condition | | | | | | | | | Unit |
|-----------------|--------------------------|------------------------------------|---------------------|--------------------|-----------|----------------|---|---|----------|----------|------|------|
| | | | Oscillation Circuit | On-Chip Oscillator | | CPU Clock | Low-Power-Consumption Setting | Other | Standard | | | |
| | | | XIN (2) | High-Speed | Low-Speed | | | | Min. | Typ. (3) | Max. | |
| I _{CC} | Power supply current (1) | High-speed clock mode | 5 MHz | Off | 125 kHz | No division | — | | — | 1.0 | — | mA |
| | | | 5 MHz | Off | 125 kHz | Division by 8 | — | | — | 0.6 | — | mA |
| | | High-speed on-chip oscillator mode | Off | 5 MHz (4) | 125 kHz | No division | | | — | 1.6 | 6.5 | mA |
| | | | Off | 5 MHz (4) | 125 kHz | Division by 8 | | | — | 1.1 | — | mA |
| | | | Off | 4 MHz (4) | 125 kHz | Division by 16 | MSTTRC = 1 | | — | 1.0 | — | mA |
| | | Low-speed on-chip oscillator mode | Off | Off | 125 kHz | Division by 8 | FMR27 = 1 LPE = 0 | | — | 60 | 200 | μA |
| | | Wait mode | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 | Peripheral clock supplied during WAIT instruction execution | — | 15 | 90 | μA |
| | | | Off | Off | 125 kHz | — | VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1 | Peripheral clock stopped during WAIT instruction execution | — | 4.0 | 80 | μA |
| | | Stop mode | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 25 °C Peripheral clock stopped | — | 1.0 | 4.0 | μA |
| | | | Off | Off | Off | — | VC1E = 0 VC0E = 0 STPM = 1 | Topr = 85 °C Peripheral clock stopped | — | 1.5 | — | μA |

Notes:

1. V_{CC} = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to V_{SS}.
2. When the XIN input is a square wave.
3. V_{CC} = 2.2 V
4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.

Timing Requirements ($V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)**Table 4.27 External Clock Input (XIN)**

| Symbol | Parameter | Standard | | Unit |
|---------------|----------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 200 | — | ns |
| $t_{WH(XIN)}$ | XIN input high width | 90 | — | ns |
| $t_{WL(XIN)}$ | XIN input low width | 90 | — | ns |

**Figure 4.12 External Clock Input Timing When $V_{CC} = 2.2\text{ V}$** **Table 4.28 TRJIO Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(TRJIO)}$ | TRJIO input cycle time | 500 | — | ns |
| $t_{WH(TRJIO)}$ | TRJIO input high width | 200 | — | ns |
| $t_{WL(TRJIO)}$ | TRJIO input low width | 200 | — | ns |

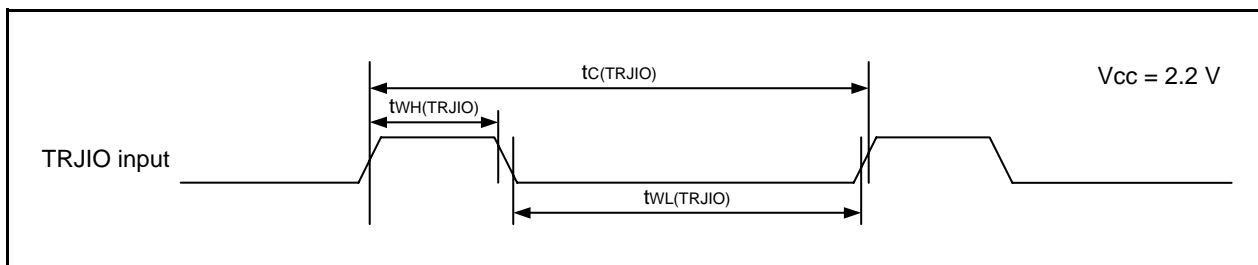
**Figure 4.13 TRJIO Input Timing When $V_{CC} = 2.2\text{ V}$**

Table 4.29 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|----------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_c(\text{CK})$ | CLK0 input cycle time | 800 | — | ns |
| $t_w(\text{CKH})$ | CLK0 input high width | 400 | — | ns |
| $t_w(\text{CKL})$ | CLK0 input low width | 400 | — | ns |
| $t_d(\text{C-Q})$ | TXD0 output delay time | — | 200 | ns |
| $t_h(\text{C-Q})$ | TXD0 hold time | 0 | — | ns |
| $t_{su}(\text{D-C})$ | RXD0 input setup time | 150 | — | ns |
| $t_h(\text{C-D})$ | RXD0 input hold time | 90 | — | ns |

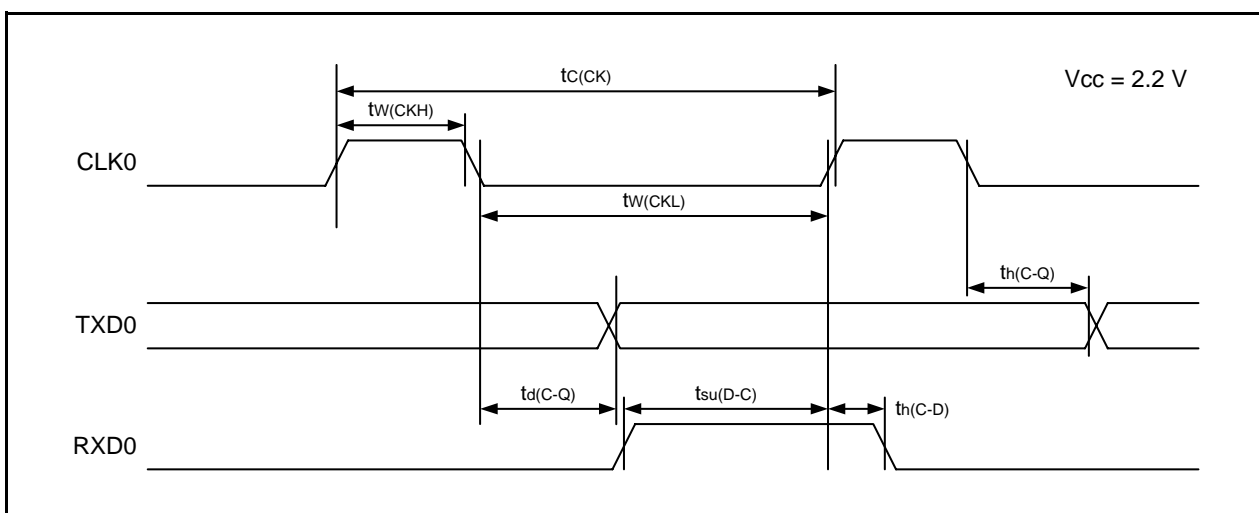


Figure 4.14 Serial Interface Timing When Vcc = 2.2 V

Table 4.30 External Interrupt $\overline{\text{INT}}_i$ Input, Key Input Interrupt $\overline{\text{K}}_i$ ($i = 0$ to 3)

| Symbol | Parameter | Standard | | Unit |
|-------------------|--|-----------|------|------|
| | | Min. | Max. | |
| $t_w(\text{INH})$ | $\overline{\text{INT}}_i$ input high width, $\overline{\text{K}}_i$ input high width | 1,000 (1) | — | ns |
| $t_w(\text{INL})$ | $\overline{\text{INT}}_i$ input low width, $\overline{\text{K}}_i$ input low width | 1,000 (2) | — | ns |

Notes:

1. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input high width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{\text{INT}}_i$ input filter select bit, the $\overline{\text{INT}}_i$ input low width is $(1/\text{digital filter clock frequency} \times 3)$ or the minimum value of the standard, whichever is greater.

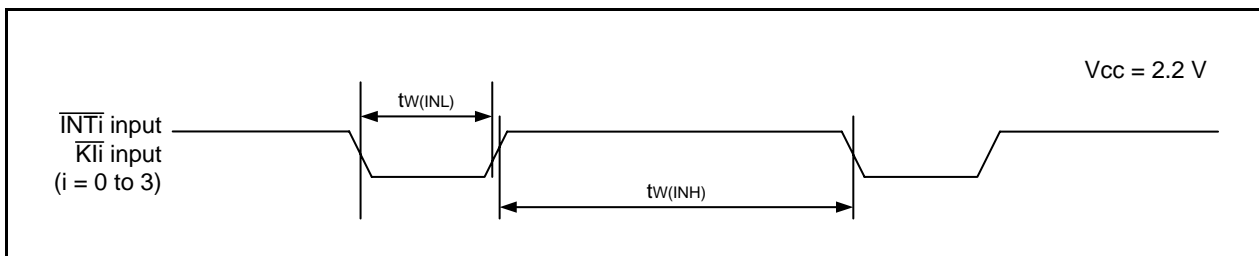


Figure 4.15 Timing for External Interrupt $\overline{\text{INT}}_i$ Input and Key Input Interrupt $\overline{\text{K}}_i$ When Vcc = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

| | | | |
|--|------------------------------|---------------------------|---------------------|
| JEITA Package Code P-TSSOP14-4.4x5-0.65 | RENASAS Code PTSP0014JA-B | Previous Code TTP-14DV | MASS[Typ.] 0.05g |
|--|------------------------------|---------------------------|---------------------|

NOTE)

- DIMENSIONS **1 (Nom)*AND**2 DO NOT INCLUDE MOLD FLASH.
- DIMENSION**3* DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section
(Ni/Pd/Au plating)

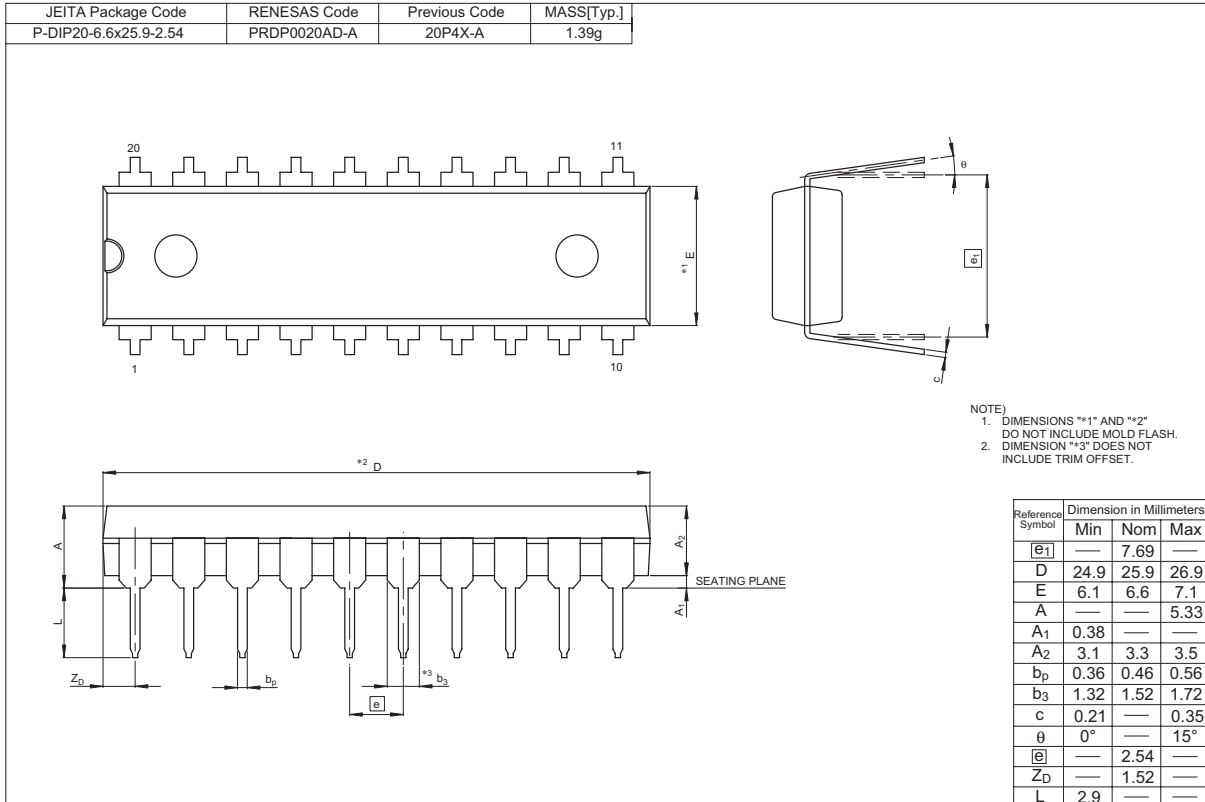
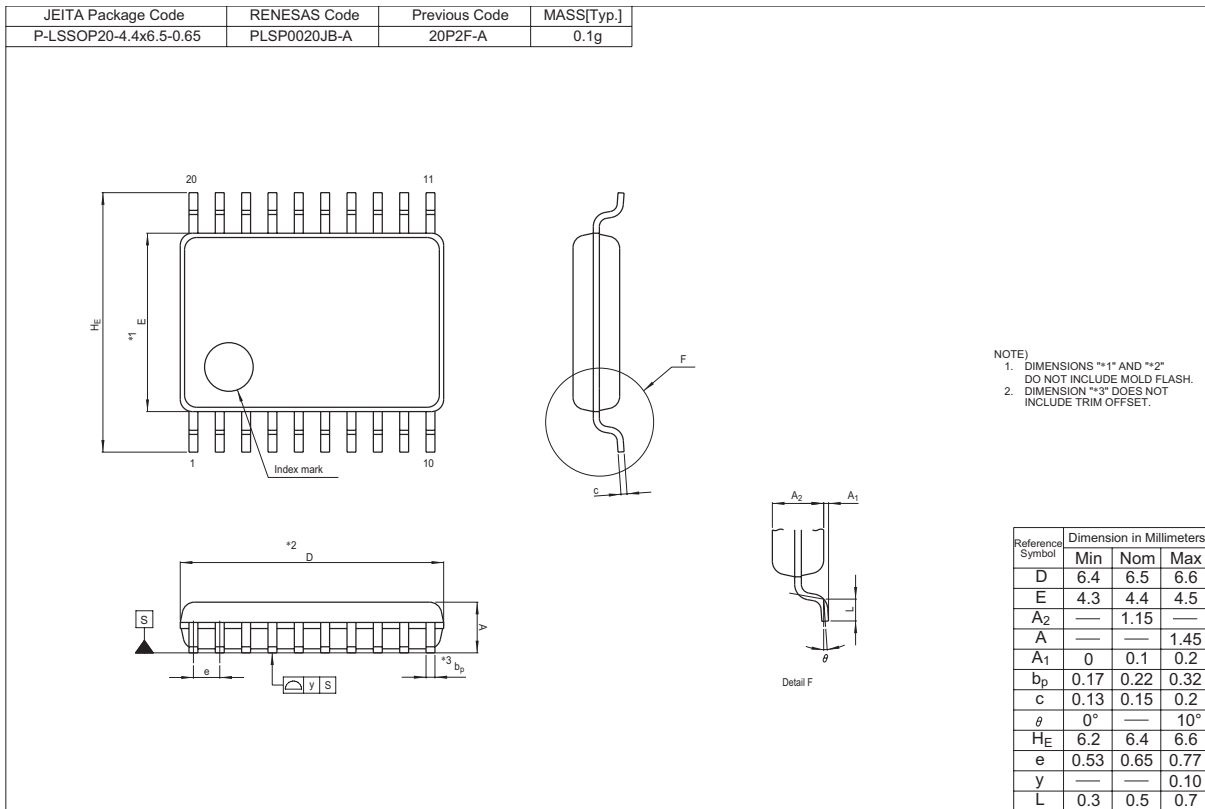
| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | — | 5.00 | 5.30 |
| E | — | 4.40 | — |
| A ₂ | — | — | — |
| A ₁ | 0.03 | 0.07 | 0.10 |
| A | — | — | 1.10 |
| b _p | 0.15 | 0.20 | 0.25 |
| b ₁ | — | — | — |
| c | 0.10 | 0.15 | 0.20 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 6.20 | 6.40 | 6.60 |
| ⓔ | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| Z | — | — | 0.83 |
| L | 0.4 | 0.5 | 0.6 |
| L ₁ | — | 1.0 | — |

| | | | |
|--|------------------------------|--------------------------|---------------------|
| JEITA Package Code P-DIP14-6.35x19.3-2.54 | RENASAS Code PRDP0014AC-A | Previous Code 14P4X-A | MASS[Typ.] 0.94g |
|--|------------------------------|--------------------------|---------------------|

NOTE)

- DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| ⓔ ₁ | — | 7.69 | — |
| D | 19.2 | 19.3 | 19.4 |
| E | 6.25 | 6.35 | 6.45 |
| A | — | — | 4.8 |
| A ₁ | 0.5 | — | — |
| A ₂ | 3.05 | 3.25 | 3.45 |
| b _p | 0.38 | — | 0.55 |
| b ₃ | 1.47 | 1.52 | 1.57 |
| c | 0.21 | — | 0.35 |
| θ | 0° | — | 15° |
| ⓔ | — | 2.54 | — |
| Z _D | — | 2.03 | — |
| L | 2.92 | — | — |



REVISION HISTORY
R8C/M11A Group, R8C/M12A Group Datasheet

| Rev. | Date | Description | |
|------|--------------|--|--|
| | | Page | Summary |
| 0.01 | Jan 14, 2010 | — | First Edition issued |
| 0.10 | Aug 25, 2010 | — 2, 3 4 5 6 8 9 11 to 43 | Document No. "REJ03B0308" → "R01DS0010EJ" 1.1.2 Differences between Groups added Table 1.3 "Reset by voltage detection 0" deleted Table 1.4 "... ROM: VCC = 2.7 V to 5.5 V" → "... ROM: VCC = 1.8 V to 5.5 V", "1,000 times (program ROM)" → "10,000 times (program ROM)", Note 1 added Table 1.5 revised Figures 1.3 and 1.4 revised Table 1.6 revised 2. Central Processing Unit (CPU), 3. Address Space, 4. Electrical Characteristics added |
| 1.00 | May 31, 2012 | All pages 1 3 4 5 6 10 15 18 23 26 31 45 | "Preliminary" and "Under development" deleted 1.1 revised Table 1.2 revised Table 1.3 revised Table 1.4 Note 1 revised Table 1.5 revised Table 1.7 revised Table 3.1 revised Table 3.4 revised Table 3.9 Notes 1 and 2 revised Table 4.3 revised Table 4.10 and 4.11 revised, Note3 deleted Package added |
| 2.00 | May 31, 2012 | 4 9 26 | "Under development" deleted Table 1.6 "Voltage detection circuit" deleted Table 4.3 revised |

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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