

# SN54ABT2244, SN74ABT2244 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS106B – JANUARY 1991 – REVISED JULY 1994

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT2240 and 'ABT2241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

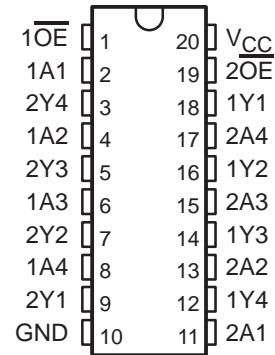
The outputs, which are designed to sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

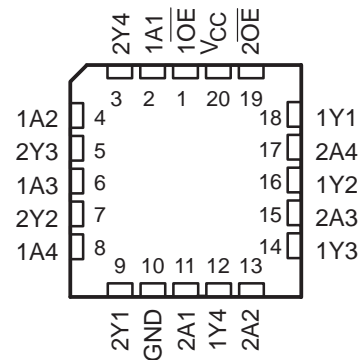
The SN74ABT2244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2244 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT2244 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT2244 . . . J PACKAGE  
SN74ABT2244 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT2244 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

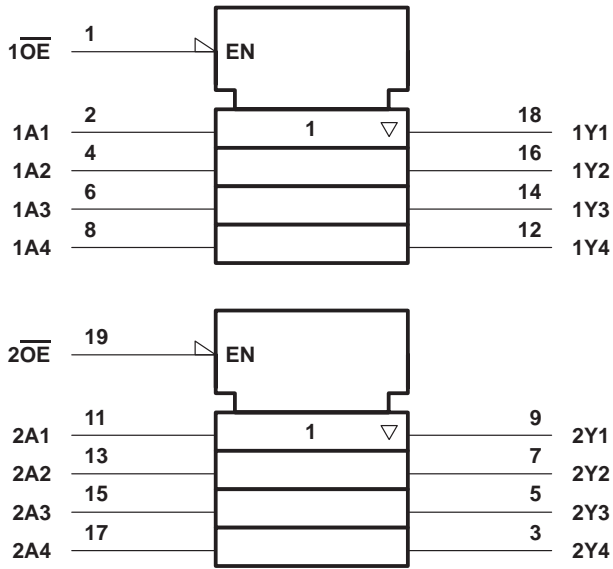
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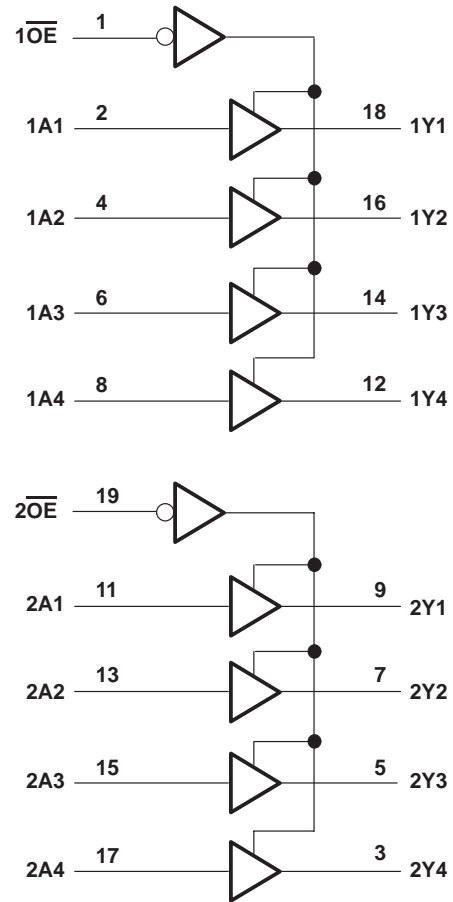
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## logic symbol†

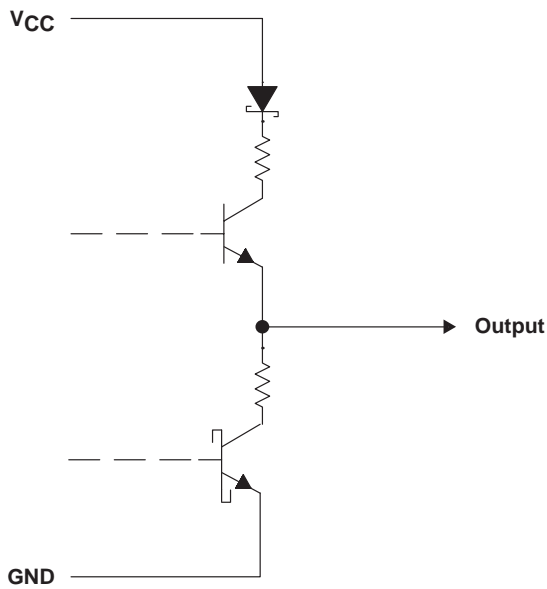


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematic of Y outputs



# SN54ABT2244, SN74ABT2244 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package .....	0.6 W
DW package .....	1.6 W
N package .....	1.3 W
PW package .....	0.7 W
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

		SN54ABT2244		SN74ABT2244		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s}/\text{V}$
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.



# SN54ABT2244, SN74ABT2244 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT2244		SN74ABT2244		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2			-1.2		-1.2		V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5			2.5		2.5		V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3			3		3			
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2			2					
I <sub>OH</sub> = -32 mA		2*					2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA		0.8			0.8		0.8		V	
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1			±1		±1		μA	
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{OE} = X$		±50			±50		±50		μA	
I <sub>OZPD</sub>	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{OE} = X$		±50			±50		±50		μA	
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V		10			10		10		μA	
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V		-10			-10		-10		μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V		±100					±100		μA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V		Outputs high		50		50		50		μA
I <sub>O‡</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		Outputs high		1 250		250		250		μA
			Outputs low		24 30		30		30		mA
			Outputs disabled		0.5 250		250		250		μA
ΔI <sub>CC</sub> §	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		Data inputs		Outputs enabled		1.5		1.5		mA
					Outputs disabled		0.05		0.05		
			Control inputs				1.5		1.5		1.5
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V		3							pF	
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V		8.5							pF	

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

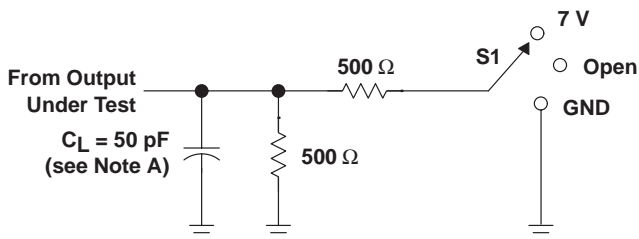
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

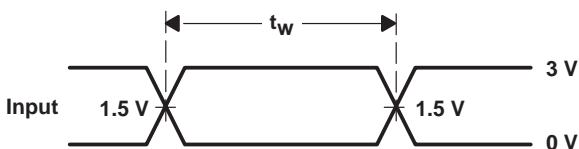
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT2244		SN74ABT2244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1	3.4	4.3	1	5.3	1	4.7	ns
t <sub>PHL</sub>			1	4.5	5.3	1	6.8	1	5.6	
t <sub>PZH</sub>	$\overline{OE}$	Y	1.1	3.8	4.8	1.1	6.5	1.1	5.5	ns
t <sub>PZL</sub>			2.1	6.3	7.3	2.1	10.2	2.1	8.3	
t <sub>PHZ</sub>	$\overline{OE}$	Y	2.1	4.5	5.6	2.1	7	2.1	6.6	ns
t <sub>PLZ</sub>			1.7	4.3	5.3	1.7	7.4	1.7	5.8	

PARAMETER MEASUREMENT INFORMATION

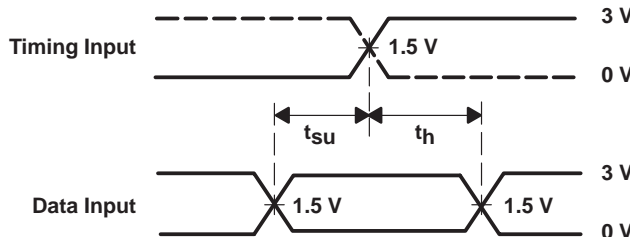


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

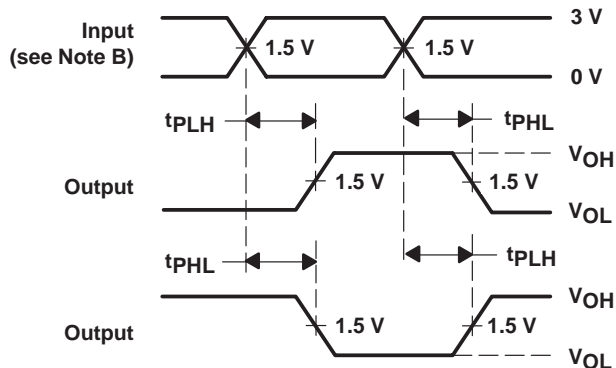
LOAD CIRCUIT FOR OUTPUTS



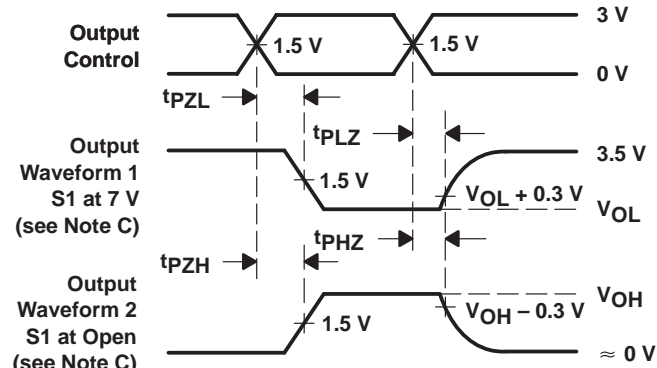
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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