KLI-4104

Linear CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KLI−4104 Image Sensor is a multi-spectral, linear solid-state image sensor for color scanning applications where fast operation and high resolution are required. The imager consists of three parallel linear photodiode arrays, each with 4,080 active photosites for the output of red, green and blue (R, G, and B) signals. The sensor contains a fourth channel for luminance information. This array has 8,160 pixels segmented to transfer out data through one of four luminance outputs. This device offers high sensitivity, high data rates, low noise and negligible lag. Individual electronic exposure control for each of the Chroma and the Luma channel is provided, allowing the KLI−4104 sensor to be used under a variety of illumination conditions.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Total Number of Pixels	3 × 4134 (Chroma), 1 × 8292 (Luma)
Number of Effective Pixels	3 × 4128 (Chroma), 1 × 8276 (Luma)
Number of Active Pixels	3 × 4080 (Chroma), 1 × 8160 (Luma)
Pixel Size	10 μm (H) × 10 μm (V) (Chroma), 5 μm (H) × 5 μm (V) (Luma)
Pixel Pitch	10 μm (Chroma), 5 μm (Luma)
Inter-Array Spacing G to R R to B B to L	 90 μm (9 Lines Effective) 90 μm (9 Lines Effective) 122.5 μm (12.25 Lines Effective)
Chip Size	50.5 mm (H) × 1.1 mm (V)
Saturation Signal	121,000 e^- (Chroma), 110,000 e^- (Luma)
Quantum Efficiency	62% (B), 62% (G), 80% (R), 85% (L)
Output Sensitivity	14 μV/e^- (Chroma), 11 μV/e^- (Luma)
Responsivity (R/G/B/L)	17 (B), 20 (G), 32 (R), 27 (L) V/μJ/cm^2
Total Read Noise	120 e^-
Dark Current	0.007 pA/Pixel (Chroma), 0.0008 pA/Pixel (Luma)
Dark Current Doubling Temp.	9°C
Dynamic Range @ 30 MHz Data Rate	60 dB (Chroma), 60 dB (Luma)
Charge Transfer Efficiency	0.999999/Transfer
Photoresponse Non-Uniformity	5% Peak to Peak

NOTE: All Parameters are specified at T = 25°C unless otherwise noted.

Figure 1. KLI−4104 Linear CCD Image Sensor

Features

- Quad-Linear Array (G, R, B, L)
- High Resolution: Luma (Monochrome) Array with 5 μm Pixels with 8,160 Count
- Luma Channel has 4 Outputs Approaching 120 MHz Data Rate
- High Resolution: Color (RGB) Array with 10 μm Pixels with 4,080 Count
- Each Color Channel has 1 Output Approaching 30 MHz Data Rate
- No Image Lag
- Two-Phase Register Clocking
- On-Ship Dark Reference
- Electronic Exposure Control

Application

- Machine Vision

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KLI−4104 IMAGE SENSOR

Part Number	Description	Marking Code
KLI−4104−AAA−CB−AA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade	KLI−4104−A Lot Number Serial Number
KLI−4104−AAA−CB−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	
KLI−4104−AAA−CP−AA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	
KLI−4104−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	
KLI−4104−DAA−CB−AA	Color (RGB), No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade	KLI−4104−D Lot Number Serial Number
KLI−4104−DAA−CB−AE	Color (RGB), No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	
KLI−4104−DAA−CP−AA	Color (RGB), No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	
KLI−4104−DAA−CP−AE	Color (RGB), No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KLI−4104−12−30−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

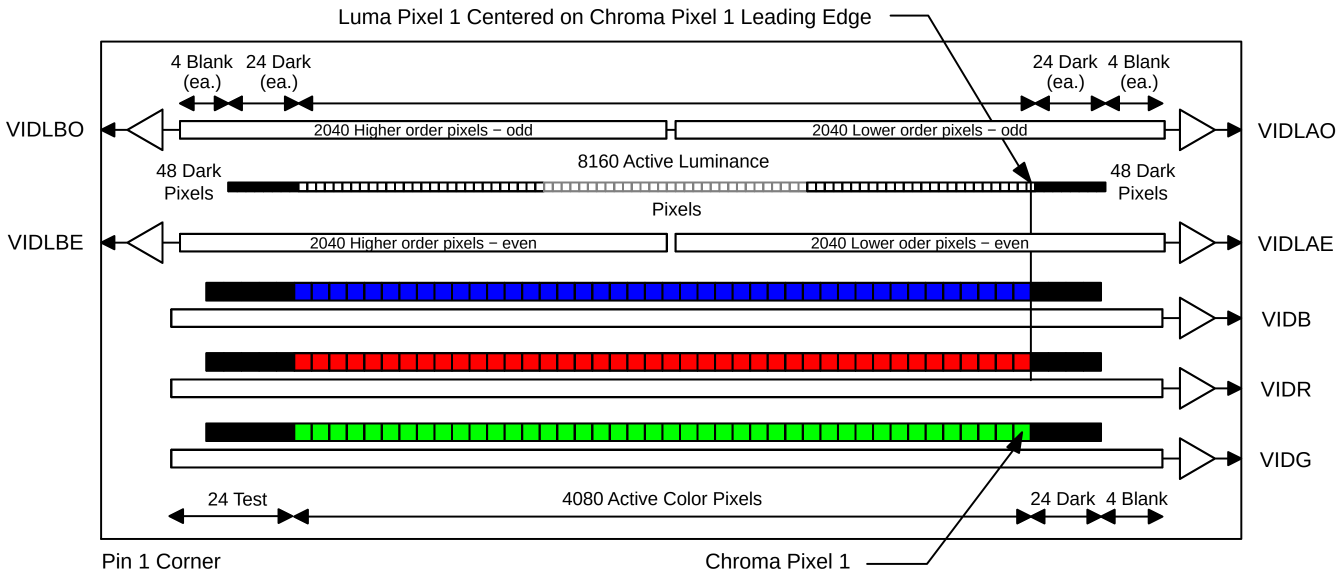


Figure 2. Block Diagram

The KLI−4104 Image Sensor is a high resolution, quadri-linear array designed for high-speed color scanning applications. Each device contains 3 rows of 4,080 active photoelements, consisting of high performance ‘pinned diodes’ for improved sensitivity, lower noise and the elimination of lag. Each row is selectively covered with a red, green or blue integral filter stripe for unparalleled spectral separation. The pixel height and pitch is 10 micron and the center-to-center spacing between color channels is 90 microns, giving an effective nine line delay between adjacent channels during imaging.

Each device also contains 1 row of 8,160 active photoelements. This channel has a monochrome response. The pixel height and pitch is 5 micron and the center-to-center spacing between this luminance channel and the blue color channel is 122.5 microns, giving an effective 12 1/4 line delay.

Readout of the pixel data for each color channel is accomplished through the use of a single CCD shift register allowing for a single output per channel with no multiplexing artifacts. Twenty-four light shielded photoelements are supplied at the start of each channel to act as a dark reference. After the 4,080 active pixels, the trailing region contains 24 pixels dedicated for test. Only the first 16 pixels in this trailing group are configured to be dark reference pixels. The remaining pixels are used for internal testing. See the block diagram in Figure 2.

Readout of the pixel data for the luminance channel is accomplished through the use of four CCD shift registers in an odd/even and left/right readout configuration. Forty-eight light shielded photoelements are supplied at the beginning of each output channel to act as its dark reference. In other words, twenty-four dark reference pixels are on the leading edge of each luma output, none trailing. See the block diagram in Figure 2.

The devices are manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies.

The architecture of the KLI−4104 provides the ability to achieve high-resolution color scans (600 dpi) by utilizing information from all 4 channels. The edge data from the luminance channel (which provides the image “detail”) can be combined with the chroma data and the result is a full resolution color image. In this design there are 4 outputs on the luminance channel to match the read out rate of the chroma channels. Both resolution and throughput are thereby maximized.

The die size is 50.50 × 1.10 mm and is housed in a custom 46-pin, 0.400″ wide, dual in line package. The die center is located between the blue and red channels and the color channels are centered in the long direction of the die. The blue channel center line is displaced +30 μm along the short dimension of the die from the die center, with pin 1 in the lower left corner.

Why High-Resolution Luma/Low-Resolution Chrominance?

The human visual system uses more luminance information than chrominance information. Based on this, we know that high spatial frequency luminance data represents the “details” in an image. To achieve a full resolution (8,160 pixels) color scan, the chrominance data can be of lower resolution (4,080 pixels) as long as the “edge/detail” information is sampled at the higher frequency.

Notice that each chroma pixel covers 4 times the area of a single luma pixel. An advantage to having larger pixel sizes is increased responsivity. This is especially useful in the chroma channels where some light is absorbed by the color filter material. Please refer to Figure 12: Typical Responsivity for the responsivity data.

Image Processing

By utilizing the data from all 4 channels, a high-resolution color scan can be achieved. The luminance channel can be used to provide the edge detail in the image.

Chroma Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the ϕ1 and ϕ2 gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photodiode into the TG1 storage region. As TG1 is turned back 'off' charge is transferred through TG2 and into the ϕ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

Luma Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode and an accumulation region adjacent to the photodiode. This transfer occurs with the bias applied to TG1L. The accumulation storage region is isolated from the CCD shift registers during the integration period by the transfer gate TG2, which is held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the ϕ1Lx and ϕ2Lx gates (x = A or B) being held in a 'high' and 'low' state respectively. Next, the TG2 gate is turned 'on' causing the charge to drain from the accumulation region into ϕ1 storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

Charge Transport and Sensing

In either the chroma or luma cases, readout of the signal charge is accomplished by two-phase, complementary clocking of the ϕ1 and ϕ2 gates, (labeled ϕ1Cx/ϕ2Cx or ϕ1Lx/ϕ2Lx, where x = A or B). The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (7.25 Vp-p min) clock swings for reduced power dissipation at 30 MHz thereby, lowering clock noise and simplifying the driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the H2 clocks. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta VFD = \Delta Q / C_{FD}$, where ΔVFD is the change in potential on the floating diffusion, ΔQ is the amount of charge, and C_{FD} is the capacitance of the floating diffusion node. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR.

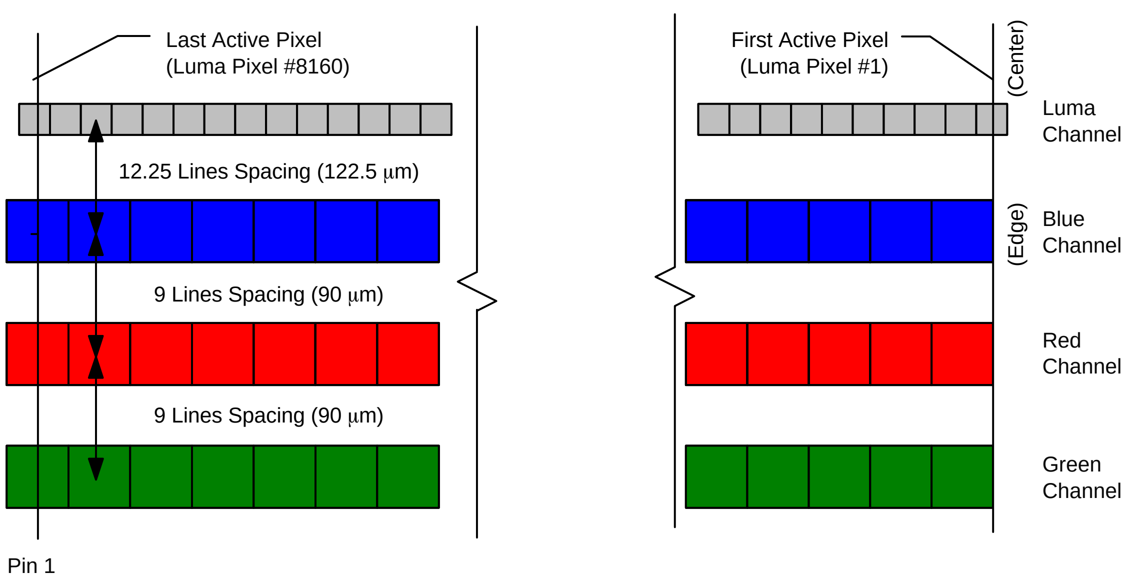


Figure 3. Channel Alignment Diagram

Zero re-phasing errors, in the final color image, is accomplished by having effectively center-aligned sampling apertures (pixels) in the luminance and chroma channels.

Even though the luminance and chroma channels are physically edge-aligned vertically, when scan motion is introduced it has a “center-weighted” sampling effect at the full resolution scan speed.

The following pixel alignment diagram explains in more detail the reason for being edge-aligned in the vertical direction and how the 12.25 line spacing (122.5 μm) works out to achieve zero re-phasing errors at full resolution.

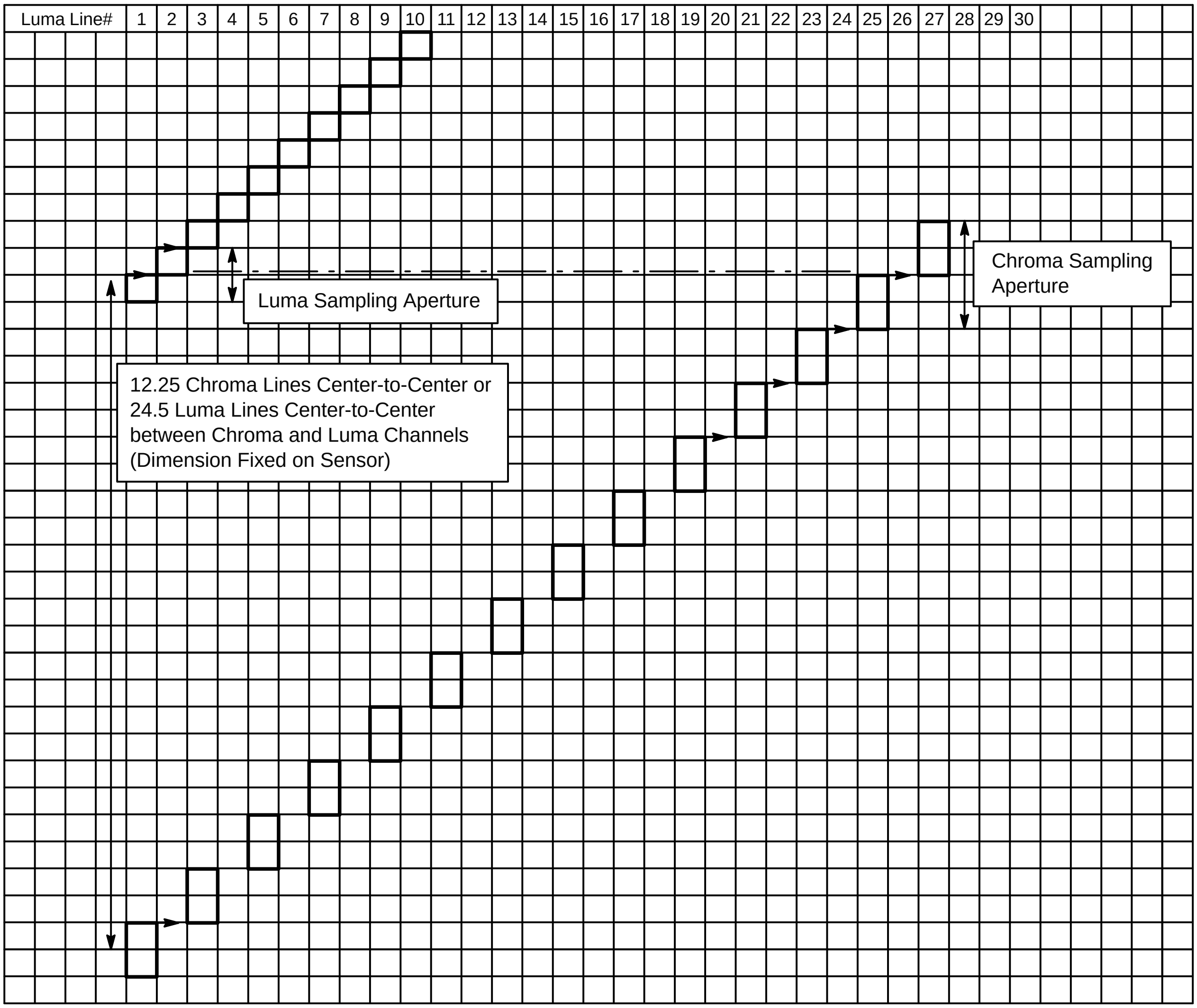


Figure 4. Pixel Alignment Diagram

The y-axis of the diagram is the direction of scanning motion (luminance-leading scan in this case). Note on the x-axis, that the luminance sampling rate (represented by the arrows) is 2× that of the chroma channel. Also note the horizontal dotted line, showing that the arrows are synchronized, depicting the effective center-aligned sampling of luminance and chroma channels after 25 luminance lines have been acquired.

This equates to zero re-phasing error between luminance and chroma signals at full resolution.

If scan speed is changed to lower the vertical resolution, a small re-phasing error may be introduced.

High Speed Scanning

The KLI−4104 sensor is ideal for applications such as high-speed document scanning.

High data throughput is achieved by having a total of 7 outputs, 4 outputs on the luminance channel (4 · 30 MHz = 120 MHz total data rate), and 1 output per chroma channel (30 MHz each).

Readout of the pixel data for the luminance channel is accomplished through the use of two CCD shift registers in an odd/even pixel readout configuration (4 outputs total).

A system can be designed with the KLI−4104 to achieve high-resolution color scans (600 dpi), when scanning the longer length side of A4 paper size at over 150 pages per minute.

Pin Description and Physical Orientation

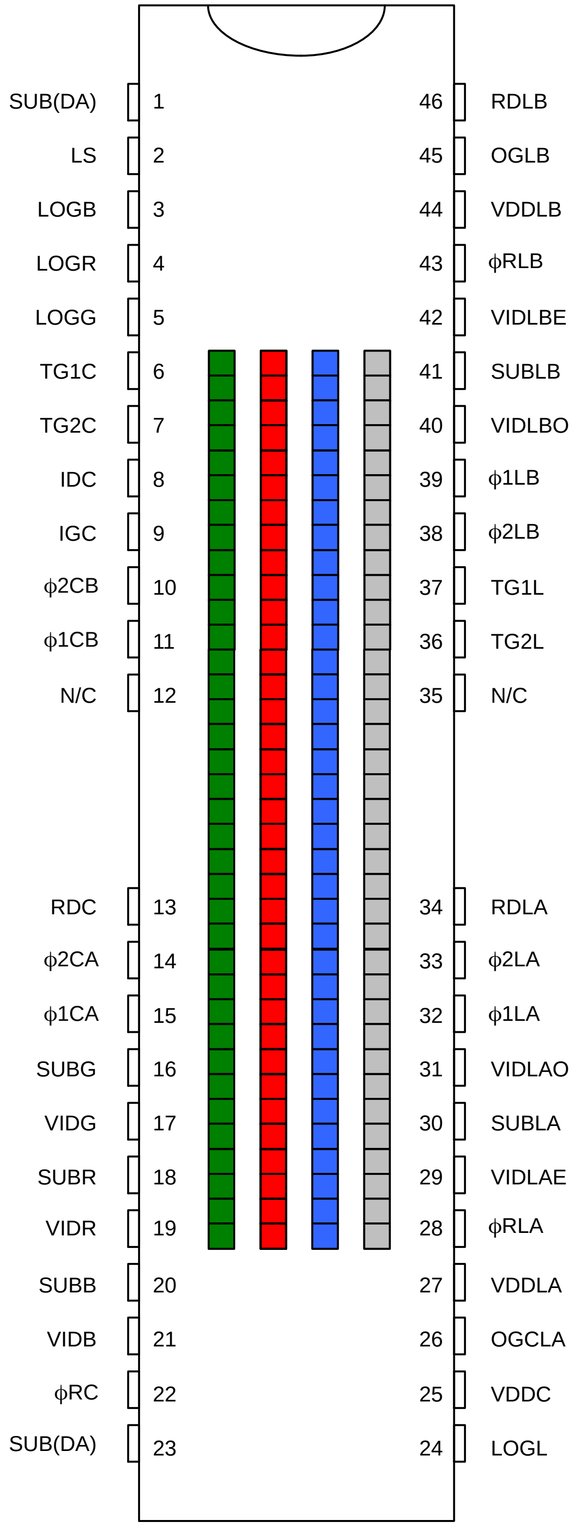


Figure 5. Pinout Diagram

Table 4. PACKAGE PIN DESCRIPTION

Pin	Name	Description
1	SUB(DA)	Substrate/Ground
2	LS	Light Shield/Exposure Drain
3	LOGB	Exposure Control, Blue
4	LOGR	Exposure Control, Red
5	LOGG	Exposure Control, Green
6	TG1C	Transfer Gate 1 Clock, Chroma
7	TG2C	Transfer Gate 2 Clock, Chroma
8	IDC	Test Input, Input Diode, Chroma
9	IGC	Test Input, Input Gate, Chroma
10	ϕ2CB	Phase 2 CCD Clock, Chroma
11	ϕ1CB	Phase 1 CCD Clock, Chroma
12	N/C	No Connection (Recommended these Pins at Ground)
13	RDC	Reset Drain Chroma
14	ϕ2CA	Phase 2 CCD Clock, Chroma
15	ϕ1CA	Phase 1 CCD Clock, Chroma
16	SUBG	Ground Reference, Green
17	VIDG	Output Video, Green
18	SUBR	Ground Reference, Red
19	VIDR	Output Video, Red
20	SUBB	Ground Reference, Blue
21	VIDB	Output Video, Blue
22	ϕRC	Reset Clock, Chroma
23	SUB(DA)	Substrate/Ground
24	LOGL	Exposure Control, Luma
25	VDDC	Amplifier Supply, Chroma
26	OGCLA	Output Gate, Chroma and Low Pixels Luma
27	VDDLA	Amplifier Supply, Low-High Pixels, Luma
28	ϕRLA	Reset Clock, Luma
29	VISLAE	Output Video, Luma Low Pixels, Even Channel
30	SUBLA	Ground Reference, Low-High Pixels, Luma
31	VIDLAO	Output Video, Luma Low Pixels, Odd Channel
32	ϕ1LA	Phase 1 CCD Clock, Luma
33	ϕ2LA	Phase 2 CCD Clock, Luma
34	RDLA	Reset Drain, Low-High Pixels, Luma
35	N/C	No Connection (Recommended these Pins at Ground)
36	TG2L	Transfer Gate 2 Clock, Luma
37	TG1L	Transfer Gate 1 Bias, Luma
38	ϕ2LB	Phase 2 CCD Clock, Luma
39	ϕ1LB	Phase 1 CCD Clock, Luma
40	VIDLBO	Output Video, Luma High Pixels, Odd Channel
41	SUBLB	Ground Reference, Low-High Pixels, Luma
42	VIDLBE	Output Video, Luma High Pixels, Even Channel
43	ϕRLB	Reset Clock, Luma
44	VDDLB	Amplifier Supply, Low-High Pixels, Luma
45	OGLB	Output Gate, High Pixels, Luma
46	RDLB	Reset Drain, Low-High Pixels, Luma

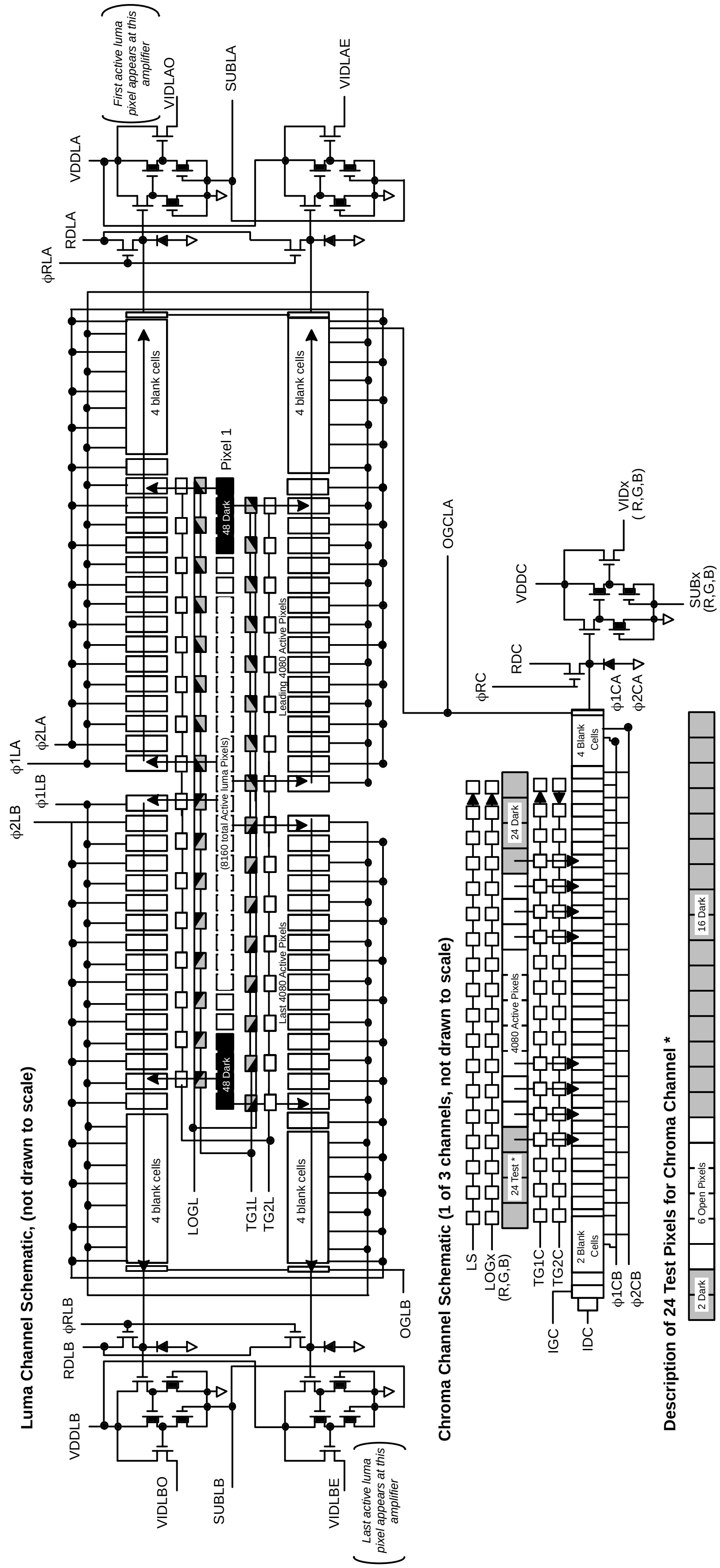


Figure 6. Device Schematic

Table 5. PIXEL CLOCK VIDEO OUTPUT

	Pixel Clock Cycle	VIDR	VIDG	VIDB	VIDLAO	VIDLAE	VIDLBO	VIDBLE
Leading Blanks (4)	1	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)	Blank(1)
	2	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)	Blank(2)
	3	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)	Blank(3)
	4	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)	Blank(4)
Leading DARK Pixels (24)	5	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)
	6	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)
	7	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)	Dark(3)
	8	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)	Dark(4)
	9	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)	Dark(5)
	…	…	…	…	…	…	…	…
	26	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)	Dark(22)
	27	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)	Dark(23)
	28	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)	Dark(24)
ACTIVE Pixels	29	Active(1)	Active(1)	Active(1)	Active(1)	Active(2)	Active(8159)	Active(8160)
	30	Active(2)	Active(2)	Active(2)	Active(3)	Active(4)	Active(8157)	Active(8158)
	31	Active(3)	Active(3)	Active(3)	Active(5)	Active(6)	Active(8155)	Active(8156)
	32	Active(4)	Active(4)	Active(4)	Active(7)	Active(8)	Active(8153)	Active(8154)
	…	…	…	…	…	…	…	…
	2066	Active(2038)	Active(2038)	Active(2038)	Active(4075)	Active(4076)	Active(4085)	Active(4086)
	2067	Active(2039)	Active(2039)	Active(2039)	Active(4077)	Active(4078)	Active(4083)	Active(4084)
	2068	Active(2040)	Active(2040)	Active(2040)	Active(4079)	Active(4080)	Active(4081)	Active(4082)
	Clock Hold during Luma Transfer Transition to Minimize Noise Feedthru							
	2069	Active(2041)	Active(2041)	Active(2041)	Active(1)	Active(2)	Active(8159)	Active(8160)
	2070	Active(2042)	Active(2042)	Active(2042)	Active(3)	Active(4)	Active(8157)	Active(8158)
	2080	Active(2043)	Active(2043)	Active(2043)	Active(5)	Active(6)	Active(8155)	Active(8156)
	…	…	…	…	…	…	…	…
	4105	Active(4077)	Active(4077)	Active(4077)	Active(4073)	Active(4074)	Active(4087)	Active(4088)
	4106	Active(4078)	Active(4078)	Active(4078)	Active(4075)	Active(4076)	Active(4085)	Active(4086)
	4107	Active(4079)	Active(4079)	Active(4079)	Active(4077)	Active(4078)	Active(4083)	Active(4084)
	4108	Active(4080)	Active(4080)	Active(4080)	Active(4079)	Active(4080)	Active(4081)	Active(4082)
TEST Group Lagging DARK Pixels (24)	4109	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)	Dark(1)
	4110	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)	Dark(2)
	…	…	…	…	…	…	…	…
	4123	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)	Dark(15)
	4124	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)	Dark(16)
	4125	Open(1)	Open(1)	Open(1)	Dark(17)	Dark(17)	Dark(17)	Dark(17)
	4126	Open(2)	Open(2)	Open(2)	Dark(18)	Dark(18)	Dark(18)	Dark(18)
	4127	Open(3)	Open(3)	Open(3)	Dark(19)	Dark(19)	Dark(19)	Dark(19)
	4128	Open(4)	Open(4)	Open(4)	Dark(20)	Dark(20)	Dark(20)	Dark(20)
	4129	Open(5)	Open(5)	Open(5)	Dark(21)	Dark(21)	Dark(21)	Dark(21)
	4130	Open(6)	Open(6)	Open(6)	Dark(22)	Dark(22)	Dark(22)	Dark(22)
	4131	Dark(17)	Dark(17)	Dark(17)	Dark(23)	Dark(23)	Dark(23)	Dark(23)
	4132	Dark(18)	Dark(18)	Dark(18)	Dark(24)	Dark(24)	Dark(24)	Dark(24)
Blanks (2) Chroma	4133	Blank(1)	Blank(1)	Blank(1)	OVERCLOCK FOR SYMMETRY			
	4134	Blank(2)	Blank(2)	Blank(2)				

NOTE: 2 lines of Luma channels per every Chroma channel.

IMAGING PERFORMANCE

Imaging Performance Operational Conditions

Specifications given under nominally specified operating conditions for the given mode of operation at 25°C, f_{CLK} = 1 MHz, AR cover glass, color filters where applicable, no exposure control (line time = integration time), and an active load as shown in Figure 14, unless otherwise specified. See notes for further descriptions.

Table 6. IMAGING PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
CHROMA CHANNELS							
Saturation Output Voltage	V_{SAT}	1.5	1.7	−	Vp-p	1, 8, 9, 17	Die[21]
Output Sensitivity	$\Delta V_O/\Delta N_e$	−	14	−	μV/e⁻	8, 9	Design[22]
Saturation Signal Charge	$N_{e,sat}$	−	121 k	−	e⁻	1, 8, 9	Design[22]
Responsitivity Blue @ 460 nm Green @ 550 nm Red @ 650 nm	R	 − − −	 17 20 32	 − − −	V/μJ/cm^2	2, 8, 9 ±10% ±10% ±10%	Design[22]
Dynamic Range	DR	−	60	−	dB	3	Design[22]
Dark Signal Non-Uniformity	DSNU	−	2	16	mV		Die[21]
DC Gain, Amplifier	ADC	−	0.74	−			Design[22]
Dark Current, @ 40°C	I_{DARK}	−	0.007	2	pA/Pixel	14, 17	Die[21]
Charge Transfer Efficiency @ 30 MHz Data Rate @ 2 MHz Data Rate	CTE	 0.999995 0.999995	 0.999992 0.999997	 − −		4, 19	 Design[22] Die[21]
Lag @ 30 MHz Data Rate @ 2 MHz Data Rate	L	 − −	 1 0.005	 − −	%	15	 Design[22] Die[21]
DC Output, Offset	V_{ODC}	−	8.6	−	V	8, 9	Design[22]
Photoresponse Non-Uniformity, Low Frequency	PRNU, Low	−	4	15	% p-p	5, 19	Die[21]
Photoresponse Non-Uniformity, Medium Frequency	PRNU, Medium	−	4	15	% p-p	6, 19	Die[21]
Photoresponse Non-Uniformity, High Frequency	PRNU, High	−	4	15	% p-p	7, 19	Die[21]
Smear @ 450 nm @ 500 nm @ 550 nm @ 600 nm @ 650 nm	Smear	 − − − − −	 0.03 0.05 0.1 0.2 0.3	 − − − − −	%		Design[22]
Response Non-Linearity	RNL	−	3	−	%	16	Design[22]
Darkfield Defect, Chroma Brightpoint	Dark Def	−	−	0	Allowed	11, 17	Die[21]
Brightfield Defect, Chroma Dark or Bright	Bfld Def	−	−	3	Allowed	10, 12, 19	Die[21]
Exposure Control Defects, Chroma Channels	Exp Def	−	−	64	Allowed	10, 13, 20 Figure 11	Die[21]
LUMA CHANNELS							
Saturation Output Voltage	V_{SAT}	1.0	1.3	−	Vp-p	1, 8, 9, 17	Die[21]
Output Sensitivity	$\Delta V_O/\Delta N_e$	−	11.5	−	μV/e⁻	8, 9	Design[22]
Saturation Signal Charge	$N_{e,sat}$	−	110 k	−	e⁻	1, 8, 9	Design[22]
Responsitivity, @ 550 nm	R	−	6.5	−	V/μJ/cm^2	2, 8, 9 ±10%	Design[22]

Table 6. IMAGING PERFORMANCE SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
LUMA CHANNELS							
Dynamic Range	DR	−	60	−	dB	3	Design[22]
Dark Signal Non-Uniformity	DSNU	−	2	16	mV	17	Die[21]
DC Gain, Amplifier	ADC	−	0.74	−			Design[22]
Dark Current, @ 40°C	I_{DARK}	−	0.0008	0.02	pA/Pixel	14, 17	Die[21]
Charge Transfer Efficiency @ 30 MHz Data Rate @ 2 MHz Data Rate	CTE	 0.999995 0.999995	 0.999997 0.999997	 − −		4, 19	 Design[22] Die[21]
Lag @ 30 MHz Data Rate @ 2 MHz Data Rate	L	 − −	 1 0.03	 − −	%	15	 Design[22] Die[21]
DC Output, Offset	V_{ODC}	−	8.6	−	V	8, 9	Design[22]
Photoresponse Non-Uniformity, Low Frequency	PRNU, Low	−	4	10	% p-p	5, 19	Die[21]
Photoresponse Non-Uniformity, Medium Frequency	PRNU, Medium	−	4	10	% p-p	6, 19	Die[21]
Photoresponse Non-Uniformity, High Frequency	PRNU, High	−	4	10	% p-p	7, 19	Die[21]
Smear @ 550 nm	Smear	−	0.12	−	%		Design[22]
Response Non-Linearity	RNL	−	3.4	−	%	16	Design[22]
Darkfield Defect, Luma Brightpoint	Dark Def	−	−	0	Allowed	11, 17	Die[21]
Brightfield Defect, Luma Dark or Bright	Bfld Def	−	−	6	Allowed	17, 18, 19	Die[21]
Exposure Control Defects, Luma Channels	Exp Def	−	−	128	Allowed	13, 20 Figure 11	Die[21]

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See Figure 12.
3. As measured at 30 MHz data rate. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between ϕ1 and ϕ2 phases must be maintained to minimize clock noise.
4. Measured per transfer. For a Chroma line: (0.99999) · 8268 = 0.92065. For a Luma line: (0.99999) · 2092 = 0.97930.
5. Low frequency response is measured across the entire array with a 1000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
6. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
7. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array. Zero individual defects allowed per this specification.
8. Increasing the current load (nominally 4.7 mA) to improve signal bandwidth will decrease these parameters.
9. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity.
10. Defective pixels will be separated by at least one non-defective pixel within and across the color channels.
11. Pixels whose response is greater than the average response by the specified threshold, (16 mV). See Figure 11.
12. Pixels whose response is greater or less than the average response by the specified threshold, (±15%). See Figure 11.
13. Pixels whose response deviates from the average pixel response by the specified threshold, (4.5 mV for Chroma, 5.5 mV for Luma), when operating in exposure control mode with an integration time that is 50% of the line time. See Figure 11. If dark pattern correction is used with exposure control, the dark pattern acquisition should be completed with exposure control actuated. Dark current tends to suppress the magnitude of these defects as observed in typical applications, hence line rate changes may affect perceived defect magnitude. Measured at 1 MHz data rate.
14. Dark current doubles approximately every +9°C.
15. Residual charge in the first field after transfer is used to determine lag measurement.
16. Nominal value was measured at an output of 1.5 V signal level at 30 MHz. Expect linearity to be better than 10% over the entire range.
17. As measured at 1 MHz data rate.
18. Pixels whose response is greater or less than the average response by the specified threshold, (±10%). See Figure 11.
19. As measured at 1 MHz data rate and with an average output level of 70% V_{SAT}.
20. As measured at 1 MHz data rate and with an average output level of 100 mV. With the exposure control active − the timing is adjusted so exposure time = 50% · integration time.
21. A parameter that is measured on every sensor during production testing.
22. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

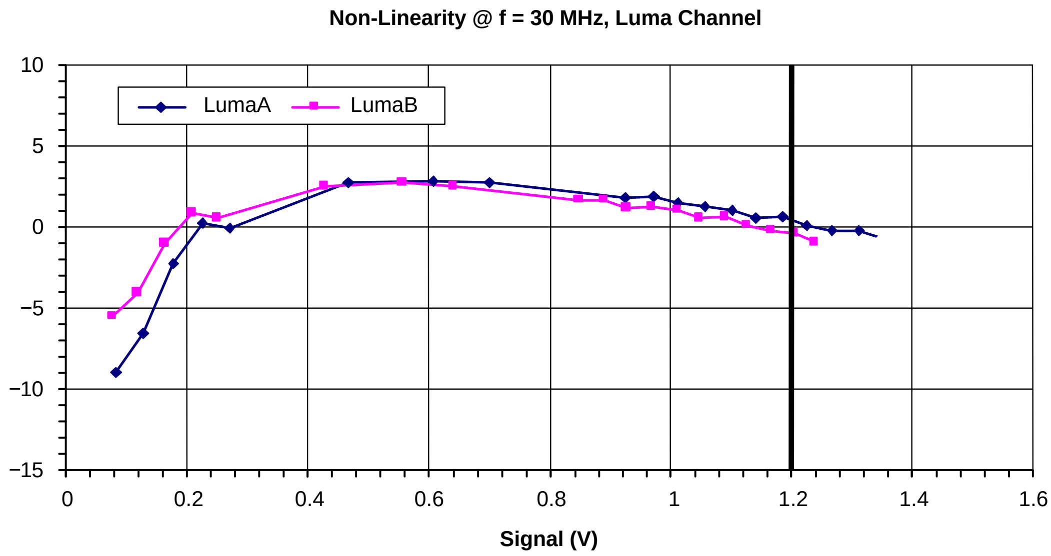


Figure 7. Typical Response Non-Linearity (%), Luma

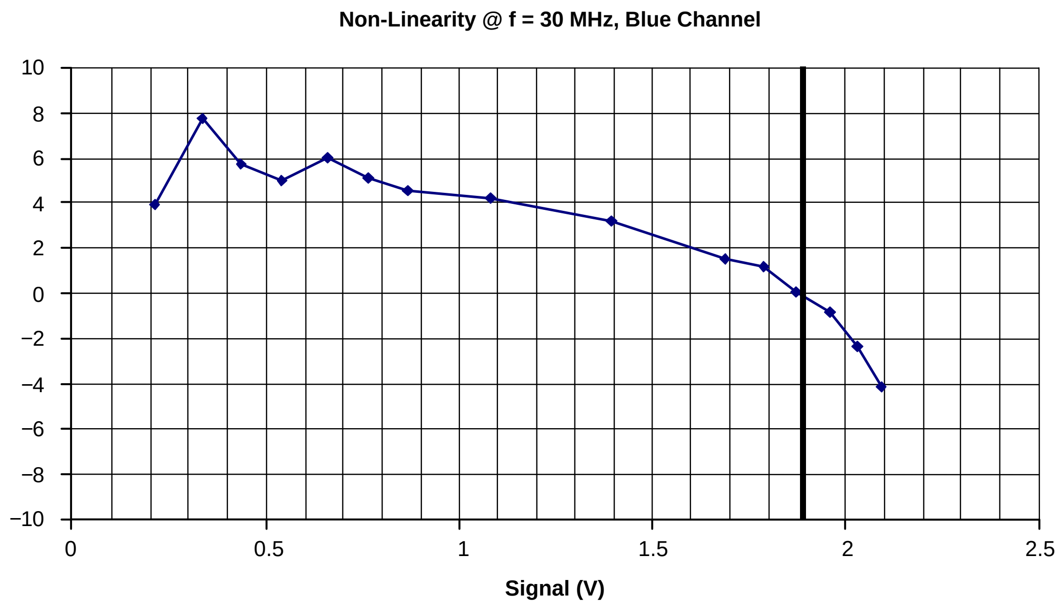


Figure 8. Typical Response Non-Linearity (%), Blue

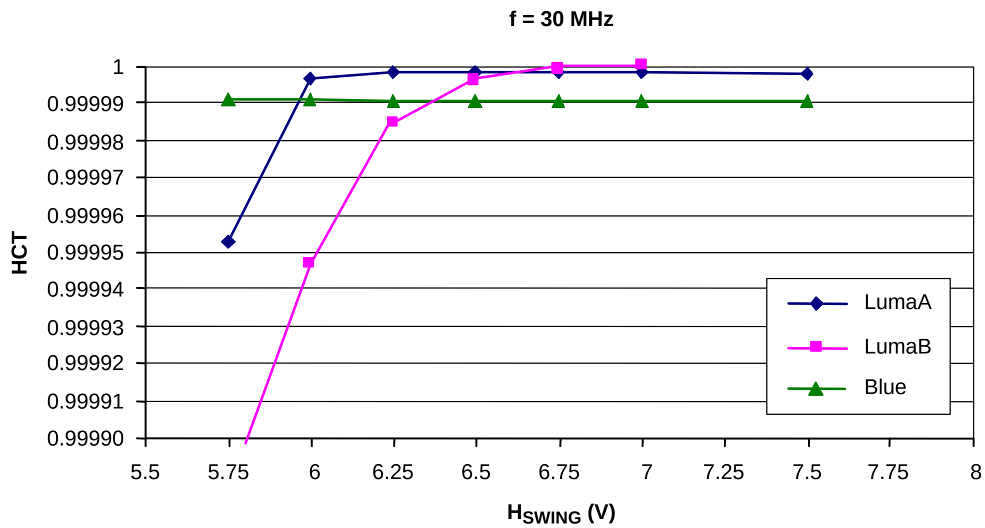


Figure 9. Typical CTE Performance vs. H Clock Levels

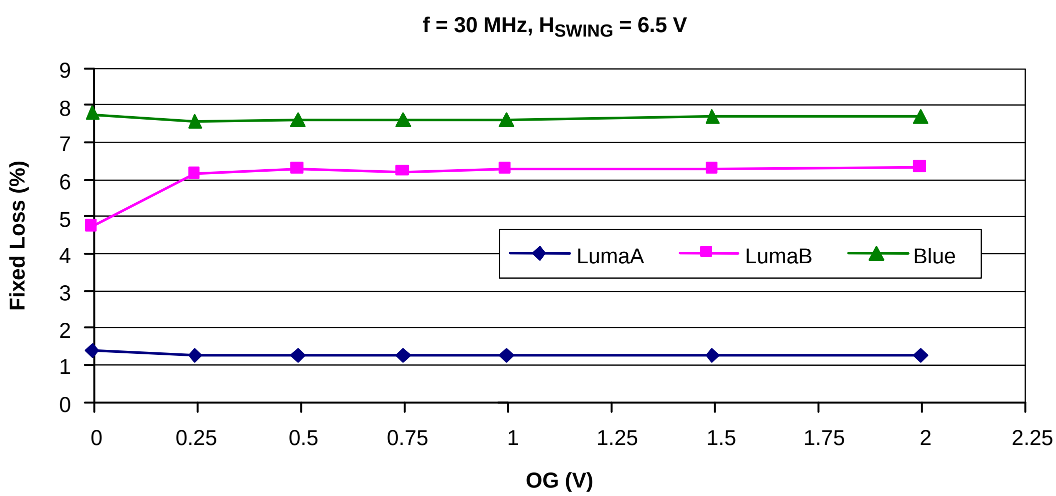


Figure 10. Typical Fixed Charge Loss vs. OG at 30 MHz

DEFECT DEFINITIONS

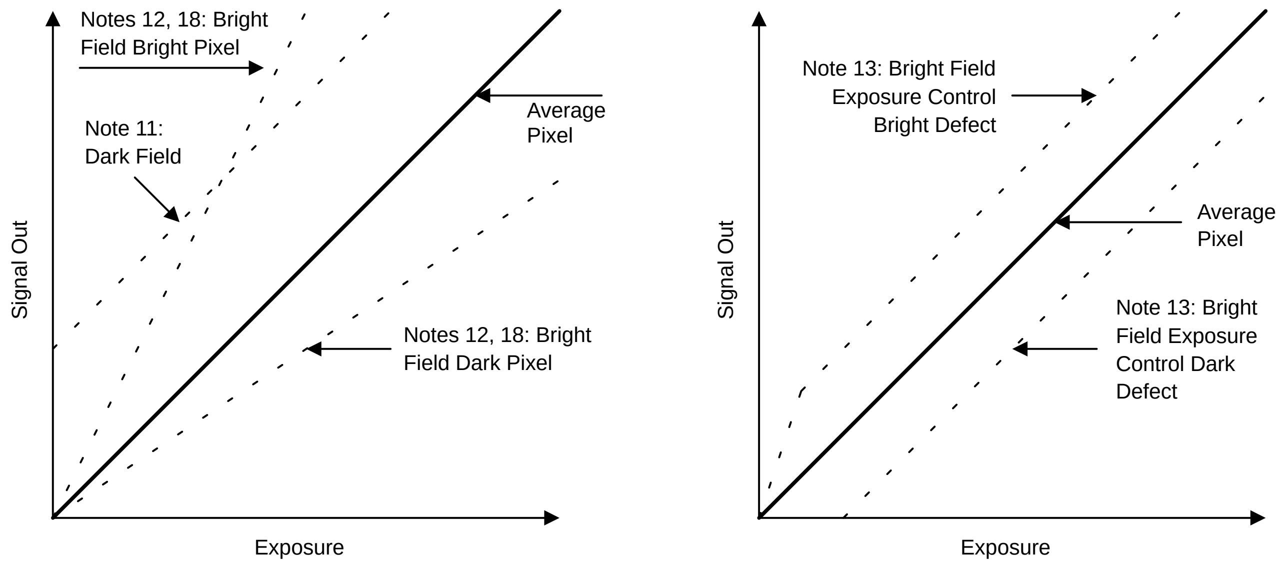


Figure 11. Defect Pixel Classification

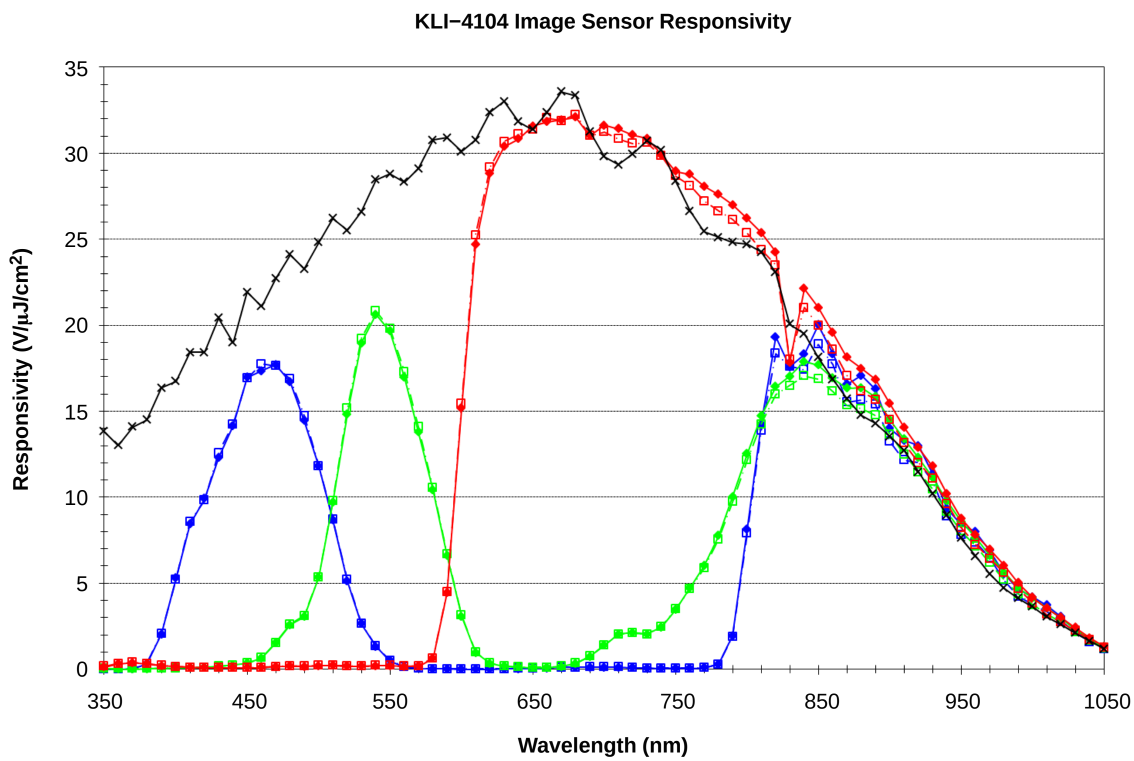


Figure 12. Typical Responsivity

OPERATION

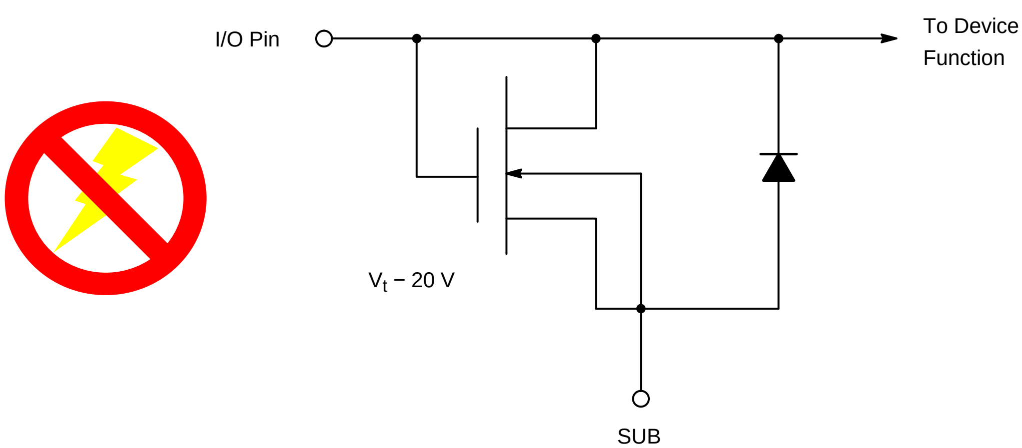
Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit	Notes
Gate Pin Voltage	V_{GATE}	0	16	V	1, 2
Pin-to-Pin Voltage	$V_{PIN-PIN}$	–	16	V	1, 3
Diode Pin Voltage	V_{DIODE}	−0.5	16	V	1, 4
Output Bias Current	I_{DD}	−2	−8	mA	5
Output Load Capacitance	$C_{VID,Load}$	–	10	pF	7
CCD Clocking Frequency	f_{CLK}	–	30	MHz	6

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to substrate voltage.
2. Includes pins: ϕ1CA, ϕ1CB, ϕ2CA, ϕ2CB, ϕ1LA, ϕ1LB, ϕ2LA, ϕ2LB, TG1C, TG2C, TG1L, TG2L, ϕRC, ϕRLA, ϕRLB, OGCLA, OGLB, IGC, LOGR, and LOGG.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDR, VIDG, VIDB, VIDLAO, VIDLAE, VIDLBO, VIDLBE, SUB(DA), SUBR, SUBG, SUBB, SUBLA, SUBLB, RDC, RDLA, RDLB, VDDC, VDDLA, VDDLB, LS and IDC.
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDR, VIDG, VIDB, VIDLAO, VIDLAE, VIDLBO, and VIDLBE load current values may need to be adjusted as well.
7. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
8. The absolute maximum ratings indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions where the design should operate the device. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Imaging Performance section.

Device Input ESD Protection Circuit (Schematic)



CAUTION: To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!

Figure 13. Device Input ESD Protection Circuit

DC Bias Operating Conditions

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Substrate	V_{SUBR}, V_{SUBG}, V_{SUBB}, V_{SUBLA}, V_{SUBLB}, $V_{SUB(DA)}$	−	0	−	V	
Accumulation Phase Bias, Luma	V_{TG1L}	−	0	0.5	V	2, 3
Reset Drain Bias	V_{RDC}, V_{RDLA}, V_{RDLB}	10.5	11	11.5	V	2
Output Buffer Supply	V_{VDDC}, V_{VDDLA}, V_{VDDLB}	14.5	15	15.5	V	2
Output Bias Current/Channel	I_{IDDC}, I_{IDDLA}, I_{IDDLB}	−2	−4.7	−8	mA	1, 2
Output Gate Bias	V_{OGCLA}, V_{OGLB}	0.5	0.7	0.9	V	2, 3
Light Shield/Drain Bias	V_{LS}	12	15	15.5	V	2
Test Pin − Input Gate	V_{IGC}	−	0	−	V	2, 3
Test Pin − Input Diode	V_{IDC}	12	15	15.5	V	2

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. RX serves as the load bias for the on-chip amplifiers. The values of RX and RL should be chosen to optimize performance for a given operating frequency. The values shown in Figure 14 below represent just one solution.
2. Referenced to substrate voltage.
3. Do not exceed absolute maximum levels for diode pins voltage.

Typical Output Bias/Buffer Circuit

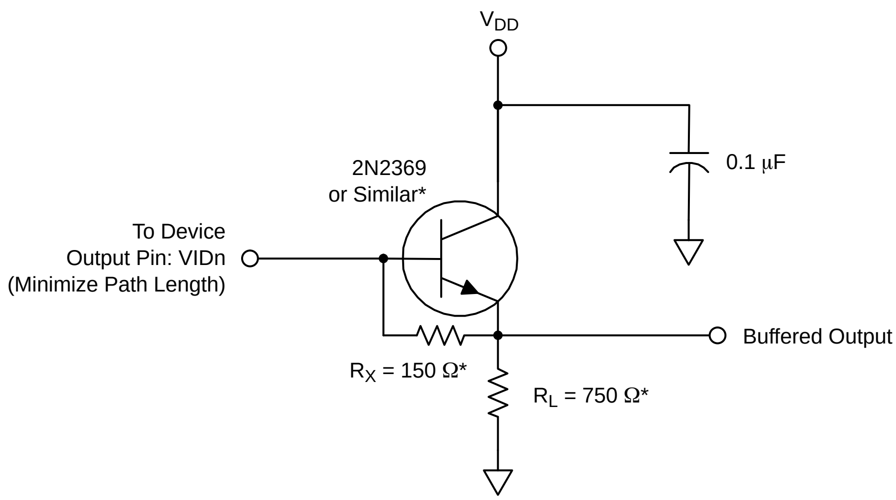


Figure 14. Typical Output Bias/Buffer Circuit

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	30 MHz Operation	1 MHz Operation	Max.	Unit	Notes
CCD Element Duration	1e (= $1/f_{CLK}$)	0.033	1	−	μs	3, 1e Count
Line/Integration Period Chroma Luma	1L (= t_{INT})	 138.4 68.9	 4,156 2,087	 − −	μs	3, 4 4,156e Counts 2,086e Counts
PD-CCD Transfer Period Chroma Luma	t_{PD}	 0.533 0.566	 16 17	 − −	μs	3, 5 16e Counts 17e Counts
Transfer Gate 1 Clear	t_{TG1}	0.033	1	−	μs	3, 1e Count
Transfer Gate 2 Clear	t_{TG2}	0.033	1	−	μs	3, 1e Count
Charge Drain Duration as % of Line Time Chroma Luma	t_{DR}	 − −	 − −	 90 90	%	2
Clamp to ϕ2 Delay	t_{CD}	5	−	−	ns	1
Sample to Reset Edge Delay	t_{SD}	5	−	−	ns	1
LOG Rise Time	$t_{LOGRISE}$	0.066	2	−	μs	3, 2e Count
LOG Fall Time	$t_{LOGFALL}$	0.066	2	−	μs	3, 2e Count

1. Recommended delays for Correlated Double Sampling (CDS) of output.
2. Maximum value stated ensures proper linearity performance. Integration times shorter than 10% of the line time increase device non-linearity.
3. Where noted as a multiple of CCD element durations, scale the appropriate times listed if the clock element time changes.
4. This value represents the shortest line period. Integration time can be shorter than a line period with the use of electronic exposure control or by extending the line period with horizontal overclocking.
5. If the application uses values less than those listed here expect degradation in lag and/or exposure control performance, where appropriate.

ELECTRICAL CHARACTERISTICS AC

Table 10. CLOCK LEVEL CONDITIONS FOR OPERATION

Description	Symbol	Min.	1 MHz Operation	30 MHz Operation	Max.	Unit	Notes
CCD Readout Clocks High	Vϕ1xH, Vϕ2xH	6.25	6.5	7.25	9.0	V	3, 7
CCD Readout Clocks Low	Vϕ1xL, Vϕ2xL	−0.1	0.0	0.0	0.1	V	1, 3
Transfer Clocks High						V	
Chroma	VTGxCH	6.25	6.5	7.25	9.0		4, 7
Luma	VTGxLH	7.00	7.5	8.00	10.0		7
Transfer Clocks Low	VTGxL	−0.1	0.0	0.0	0.1	V	1, 4
Reset Clock High (Normal Mode)	VϕRxH	6.25	6.5	7.25	9.0	V	5, 7
Reset Clock Low	VϕRxL	−0.1	0.0	0.0	0.1	V	1, 5
Exposure Clocks High	VLOGxH	6.25	6.5	7.25	9.0	V	2, 6, 7
Exposure Clocks Low	VLOGxL	−0.1	0.0	0.0	0.1	V	1, 2, 6

1. Care should be taken to insure that low rail overshoot does not exceed −0.5 VDC. Exceeding this value may result in non-photogenerated charged being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.
3. Where “x” can be “CA”, “CB”, “LA”, or “LB”.
4. Where “x” can be “1” or “2”.
5. Where “x” can be “C”, “LA”, or “LB”.
6. Where “x” can be “R”, “G”, or “B”.
7. For high level clocks at 30 MHz operation, use the values found in the “30 MHz Operation” column. This value represents the recommended setting for operation. Operating ranges for the high level clocks should be held to a variation range of ±0.25. Clock levels below this range will result in loss of charge transfer efficiency and other performance degradations.

Table 11. CLOCK VOLTAGE DETAIL CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
TG1C High-Level Variation	V1HH	−	0.50	1	V	High-Level Coupling
TG1C Low-Level Variation	V1LL	−	0.14	1	V	Low-Level Coupling
TG2x High-Level Variation	V2HL	−	0.28	1	V	High-Level Coupling
TG2x Low-Level Variation	V2LH	−	0.46	1	V	Low-Level Coupling
ϕ1x High-Level Variation	ϕ1HH	−	0.30	1	V	
ϕ1x High-Level Variation	ϕ1HL	−	0.07	1	V	
ϕ1x Low-Level Variation	ϕ1LH	−	0.16	1	V	
ϕ1x Low-Level Variation	ϕ1LL	−	0.25	1	V	
ϕ2x High-Level Variation	ϕ2HH	−	0.40	1	V	
ϕ2x High-Level Variation	ϕ2HL	−	0.06	1	V	
ϕ2x Low-Level Variation	ϕ2LH	−	0.10	1	V	
ϕ2x Low-Level Variation	ϕ2LL	−	0.27	1	V	
ϕ1x − ϕ2x Cross-Over	ϕ1CR1	40	50	60	%	Rising Side of ϕ1
ϕ1x − ϕ2x Cross-Over	ϕ1CR2	40	50	60	%	Falling Side of ϕ1
ϕRx High-Level Variation	RGHH	−	0.19	1	V	
ϕRx High-Level Variation	RGHL	−	0.20	1	V	
ϕRx Low-Level Variation	RGLH	−	0.11	1	V	
ϕRx Low-Level Variation	RGLL	−	0.30	1	V	
TG1C Rise Time	t_{V1R}	−	0.26	1	μs	2
TG2x Rise Time	t_{V2R}	−	0.55	1	μs	2
TG1C Fall Time	t_{V1F}	−	0.43	1	μs	2
TG2x Fall Time	t_{V2F}	−	0.31	1	μs	2
ϕ1 Rise Time	t_{H1R}	−	9.0	10	ns	2
ϕ2 Rise Time	t_{H2R}	−	6.9	10	ns	2

Table 11. CLOCK VOLTAGE DETAIL CHARACTERISTICS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
ϕ1 Fall Time	t_{H1F}	−	5.8	10	ns	2
ϕ2 Fall Time	t_{H2F}	−	5.4	10	ns	2
ϕRx Rise Time	t_{RGR}	−	2.0	4	ns	2
ϕRx Fall Time	t_{RGF}	−	2.2	4	ns	2
Reset Pulse Width	t_{RGW}	−	5.0	−	ns	

1. ϕ1, ϕ2 clock frequency: 30 MHz. The maximum and minimum values in this table are supplied for reference. Testing against the device performance specifications is performed using the nominal values.
2. Longer times will degrade noise performance.

Table 12. CLOCK LINE CAPACITANCE

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
CHROMA						
Phase 1 Clock Capacitance	$C_{\phi 1CA}$, $C_{\phi 1CB}$	−	330	−	pF	1
Phase 2 Clock Capacitance	$C_{\phi 2CA}$, $C_{\phi 2CB}$	−	270	−	pF	1
Transfer Gate 1 Capacitance	C_{TG1C}	−	185	−	pF	
Transfer Gate 2 Capacitance	C_{TG2C}	−	320	−	pF	
Exposure Gate Capacitance	C_{LOGR}, C_{LOGG}, C_{LOGB}	−	33	−	pF	
Reset Gate Capacitance	$C_{\phi RC}$	−	10	−	pF	
LUMA						
Phase 1 Clock Capacitance	$C_{\phi 1LA}$, $C_{\phi 1LB}$	−	400	−	pF	
Phase 2 Clock Capacitance	$C_{\phi 2LA}$, $C_{\phi 2LB}$	−	300	−	pF	
Transfer Gate 2 Capacitance	C_{TG2L}	−	230	−	pF	
Exposure Gate Capacitance	C_{LOGL}	−	75	−	pF	
Reset Gate Capacitance	$C_{\phi RLA}$, $C_{\phi RLB}$	−	6	−	pF	

1. The value listed is the effective value, or equal to 1/2 the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the total load capacitance per horizontal drive function is approximately twice the value listed. These values were calculated from design targets. These values do not take into account the device package.

TIMING

Edge Alignment

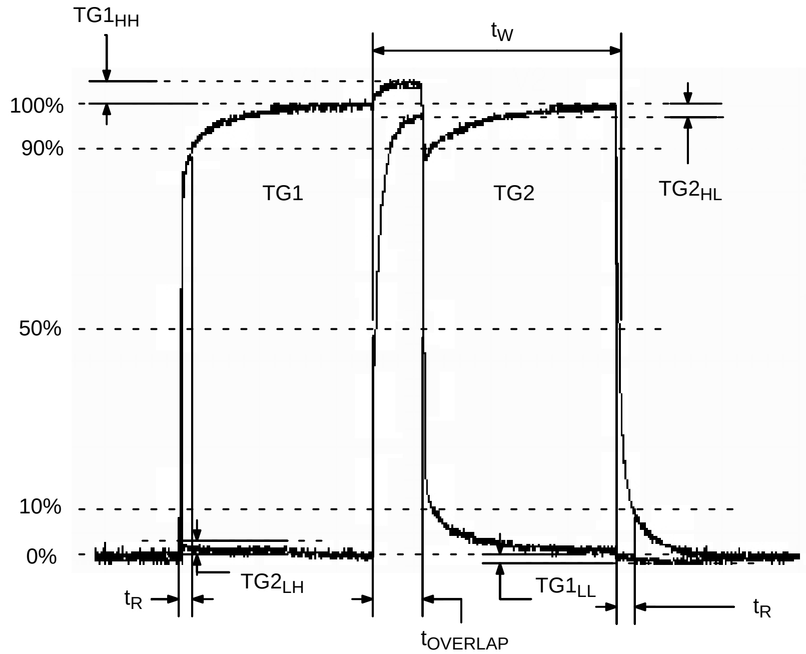


Figure 15. Transfer Timing Edge Alignment

Pixel Timing

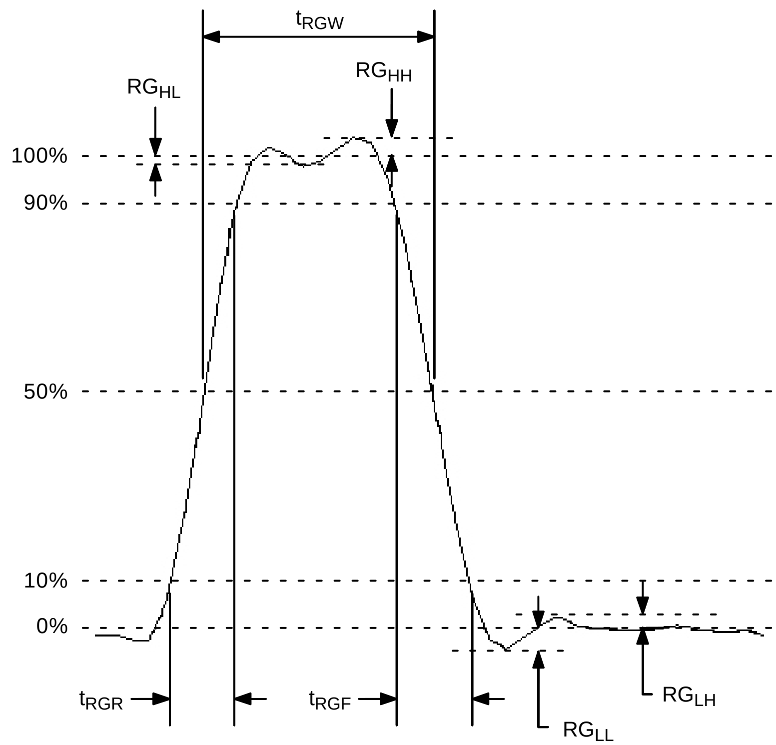


Figure 16. Pixel Timing Detail

Pixel Timing Edge Alignment

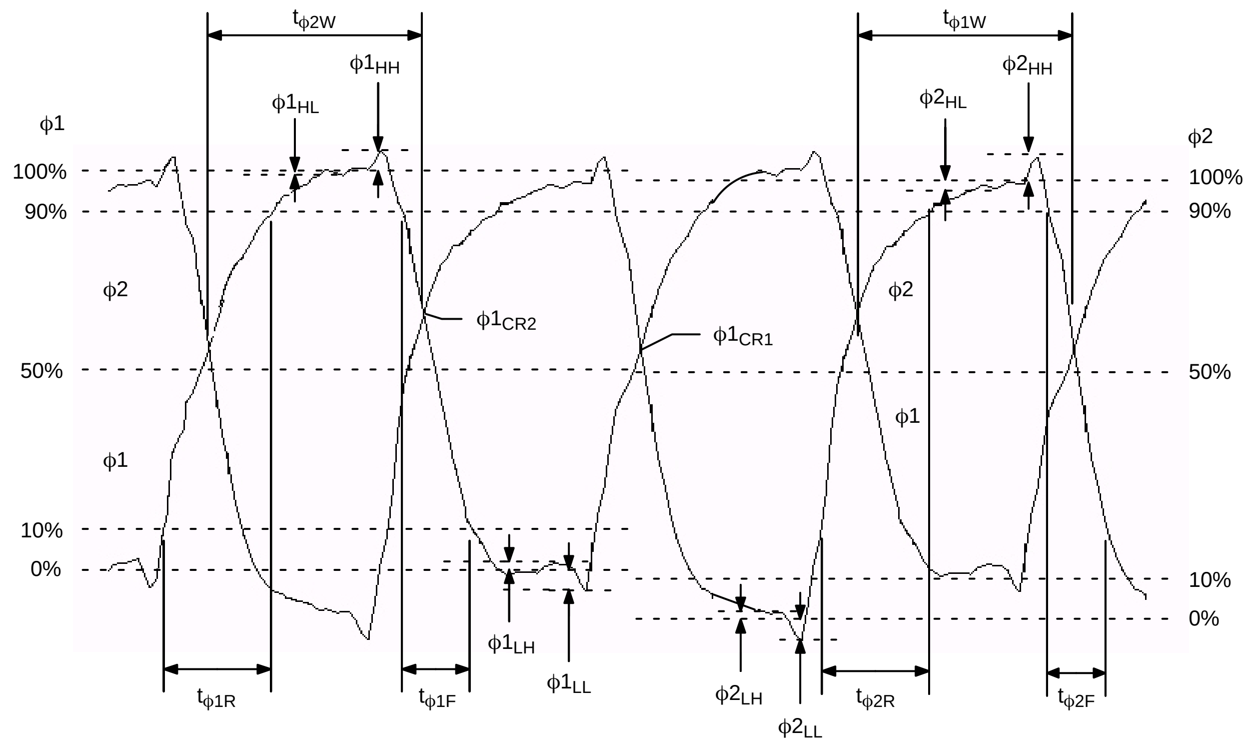
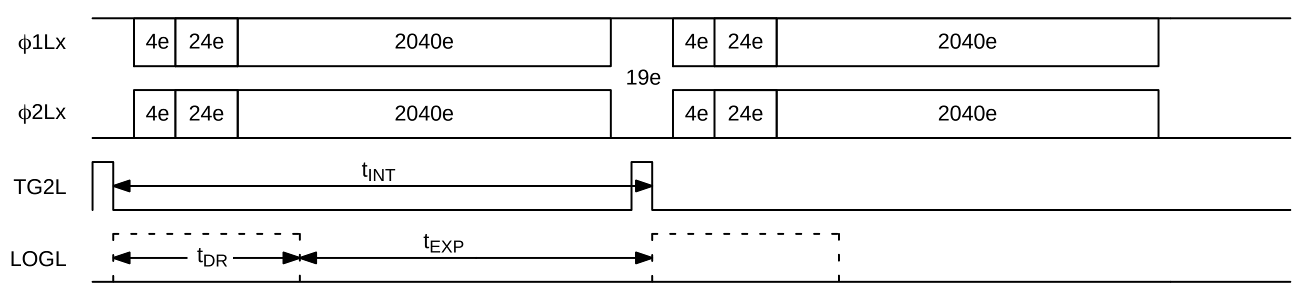


Figure 17. φ1 and φ2 Edge Alignment

Line Timing

Line Timing, Luma



Line Timing, Chroma

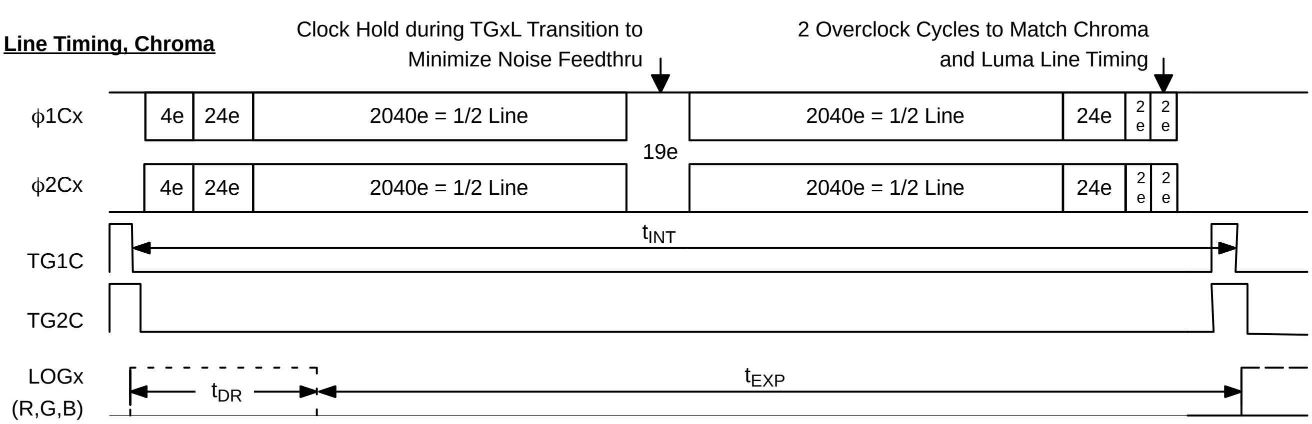
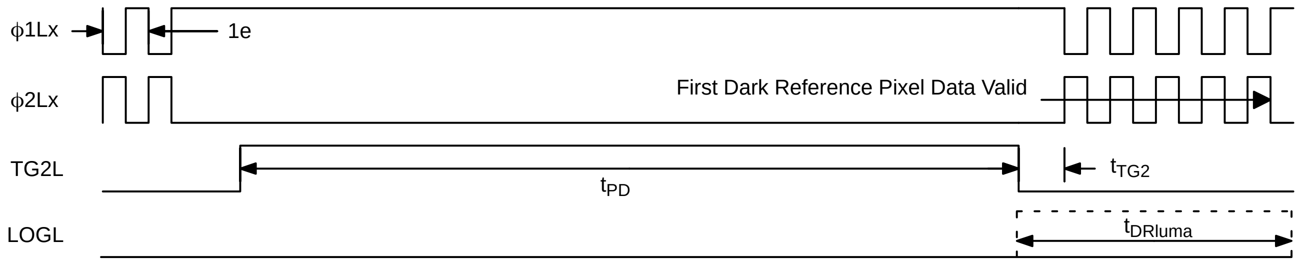


Figure 18. Line Timing Diagram

Luma Accumulation Gate-to-Gate Transfer Timing



Chroma Photodiode-to-CCD Transfer Timing

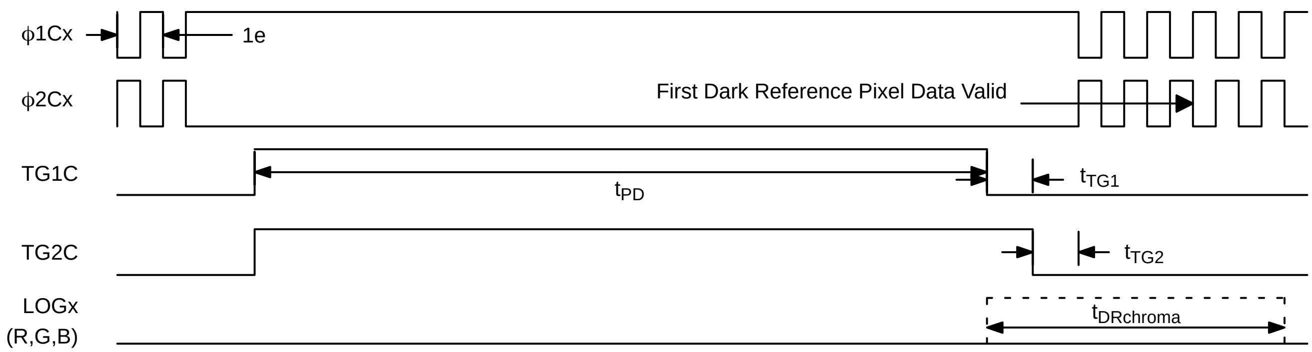
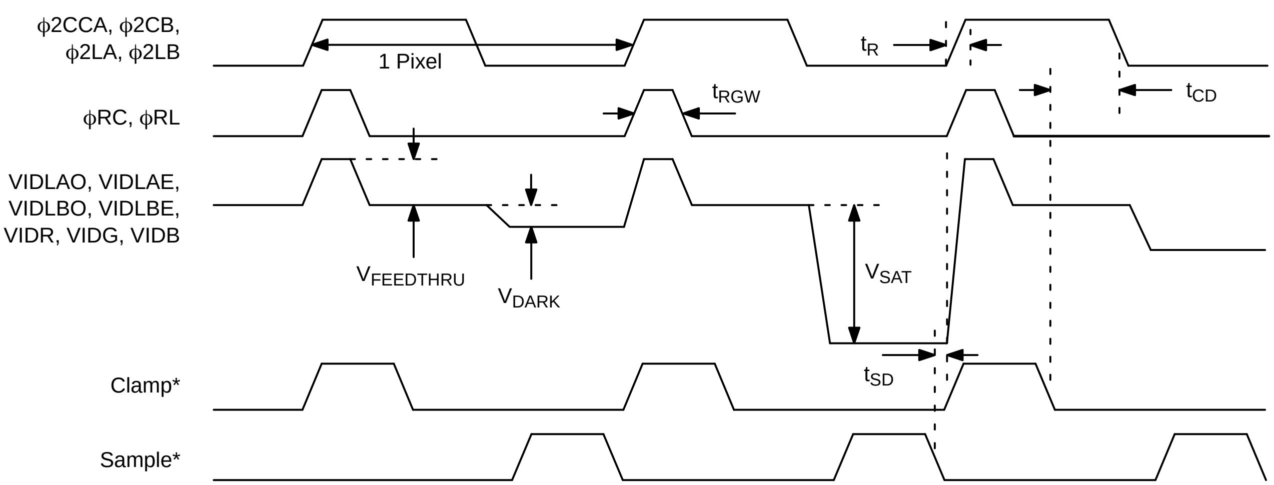


Figure 19. Transfer Timing Diagram

Output Timing



*Required for Optional Off-Chip, Analog, Correlated Double Sampling (CDS) Signal Processing

Figure 20. Output Timing Diagram

STORAGE AND HANDLING

Table 13. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_{ST}	−25	80	°C	2
Humidity	RH	5	90	%	1
Operating Temperature	T_{OP}	0	70	°C	3
Guaranteed Temperature of Performance	T_{SP}	25	40	°C	4

1. T = 25°C. Excessive humidity will degrade MTTF.
2. Long-term storage toward the maximum temperature may accelerate color filter degradation.
3. Noise performance will degrade at higher temperatures.
4. See section for Imaging Performance Specifications.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

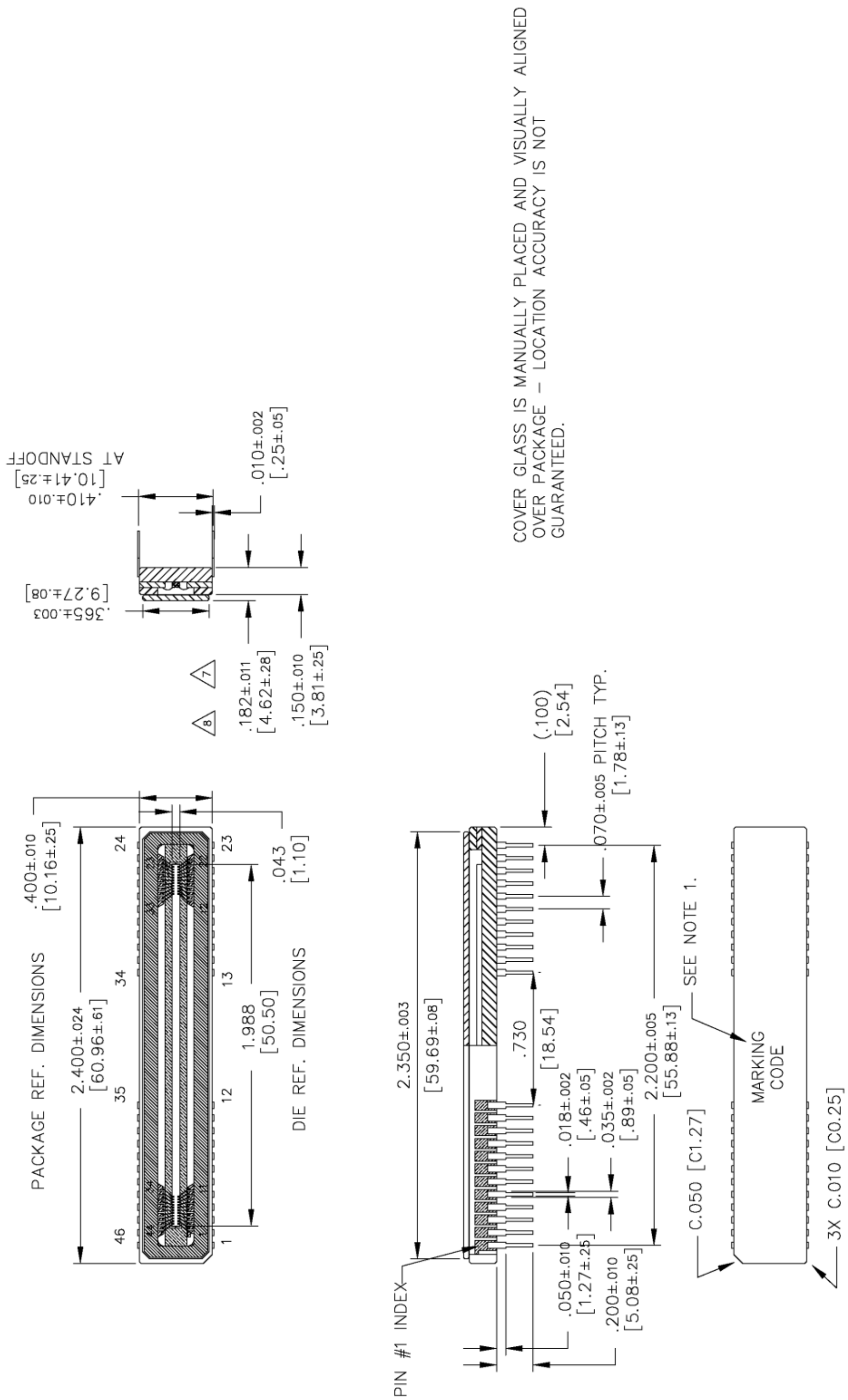


Figure 21. Completed Assembly

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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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«FORSTAR» (основан в 1998 г.)

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