



N-Channel Depletion-Mode DMOS FET

Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and low C_{ISS}
- ▶ ESD gate protection

General Description

The LND150 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND150 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

Applications

- ▶ Solid state relays
- ▶ Normally-on switches
- ▶ Converters
- ▶ Power supply circuits
- ▶ Constant current sources
- ▶ Input protection circuits

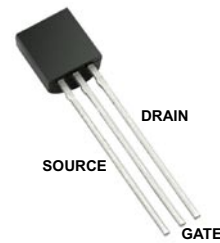
Ordering Information

Device	Package Options			BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (K Ω)	I_{DSS} (min) (mA)
	TO-236AB (SOT-23)	TO-92	TO-243AA (SOT-89)			
LND150	LND150K1-G	LND150N3-G	LND150N8-G	500	1.0	1.0

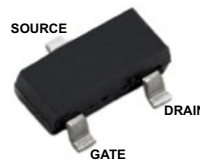
-G indicates package is RoHS compliant ('Green')



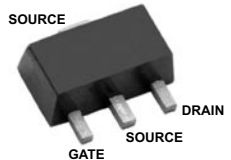
Pin Configurations



TO-92 (N3)



TO-236AB (SOT-23) (K1)



TO-243AA (SOT-89) (N8)

Absolute Maximum Ratings

Parameter	Value
Drain-to-source	BV_{DSX}
Drain-to-gate	BV_{DGX}
Gate-to-source	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Product Marking

NDEW W = Code for Week Sealed
_____ = "Green" Packaging

TO-236AB (SOT-23) (K1)

D150YYWW YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

TO-92 (N3)

LN1EW W = Code for Week Sealed
_____ = "Green" Packaging

TO-243AA (SOT-89) (N8)

Packages may or may not include the following marks: Si or

Thermal Characteristics

Package	I _D (continuous) [†] (mA)	I _D (pulsed) (mA)	Power Dissipation @T _A = 25°C (W)	θ _{jc} (°C/W)	θ _{ja} (°C/W)	I _{DR} (mA)	I _{DRM} [†] (mA)
TO-236AB (SOT-23)	13	30	0.36	200	350	13	30
TO-92	30	30	0.74	125	170	30	30
TO-243AA (SOT-89)	30	30	1.6 [‡]	15	78	30	30

Notes:

- [†] I_D (continuous) is limited by max rated T_J.
- [‡] Mounted on FR4 board, 25mm x 25mm x 1.57mm

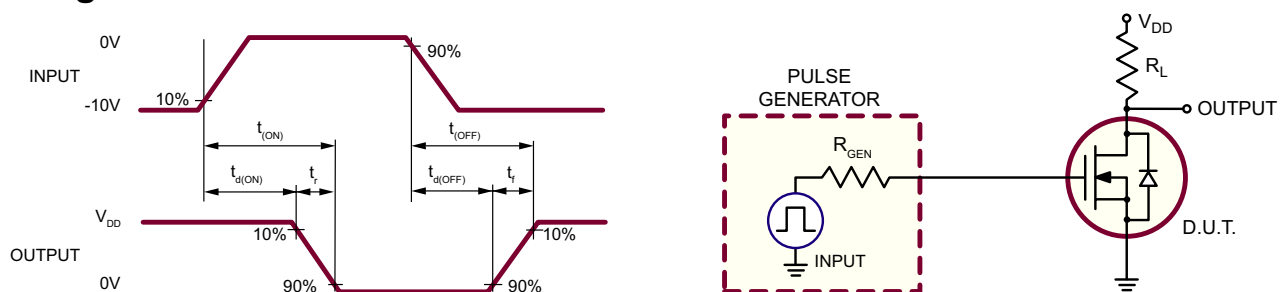
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV _{DSX}	Drain-to-source breakdown voltage	500	-	-	V	V _{GS} = -10V, I _D = 1.0mA
V _{GS(OFF)}	Gate-to-source off voltage	-1.0	-	-3.0	V	V _{GS} = 25V, I _D = 100nA
ΔV _{GS(OFF)}	Change in V _{GS(OFF)} with temperature	-	-	5.0	mV/°C	V _{GS} = 25V, I _D = 100nA
I _{GSS}	Gate body leakage current	-	-	100	nA	V _{GS} = ± 20V, V _{DS} = 0V
I _{D(OFF)}	Drain-to-source leakage current	-	-	100	nA	V _{GS} = -10V, V _{DS} = 450V
		-	-	100	μA	V _{DS} = 0.8V Max Rating, V _{GS} = -10V, T _A = 125°C
I _{DSS}	Saturated drain-to-source current	1.0	-	3.0	mA	V _{GS} = 0V, V _{DS} = 25V
R _{DS(ON)}	Static drain-to-source on-state resistance	-	850	1000	Ω	V _{GS} = 0V, I _D = 0.5mA
ΔR _{DS(ON)}	Change in R _{DS(ON)} with temperature	-	-	1.2	%/°C	V _{GS} = 0V, I _D = 0.5mA
G _{FS}	Forward transconductance	1.0	2.0	-	mΩ	V _{DS} = 0V, I _D = 1.0mA
C _{ISS}	Input capacitance	-	7.5	10	pF	V _{GS} = -10V, V _{DS} = 25V, f = 1.0MHz
C _{OSS}	Common source output capacitance	-	2.0	3.5		
C _{RSS}	Reverse transfer capacitance	-	0.5	1.0		
t _{d(ON)}	Turn-on delay time	-	0.09	-	μs	V _{DD} = 25V, I _D = 1.0mA, R _{GEN} = 25Ω
t _r	Rise time	-	0.45	-		
t _{d(OFF)}	Turn-off delay time	-	0.1	-		
t _f	Fall time	-	1.3	-		
V _{SD}	Diode forward voltage drop	-	-	0.9	V	V _{GS} = -10V, I _{SD} = 1.0mA
t _{rr}	Reverse recovery time	-	200	-	ns	V _{GS} = -10V, I _{SD} = 1.0mA

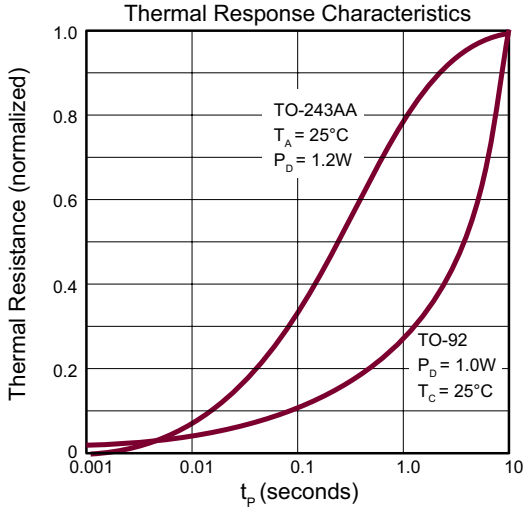
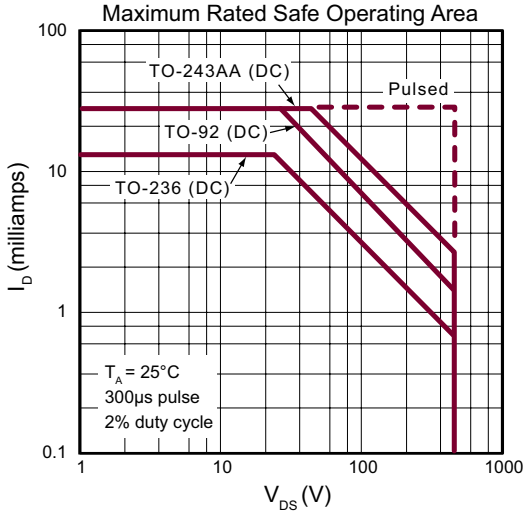
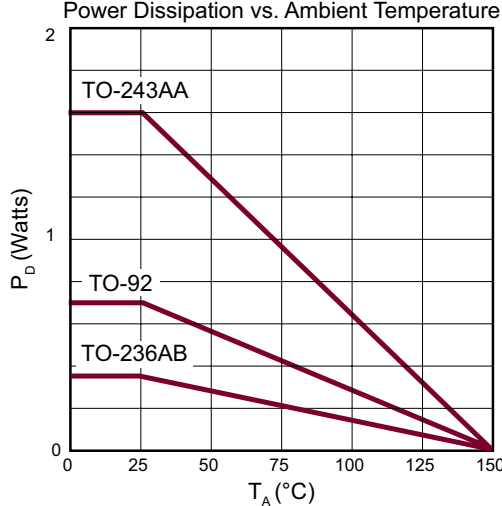
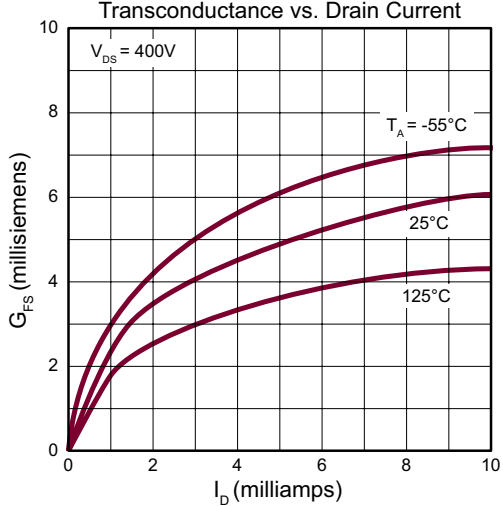
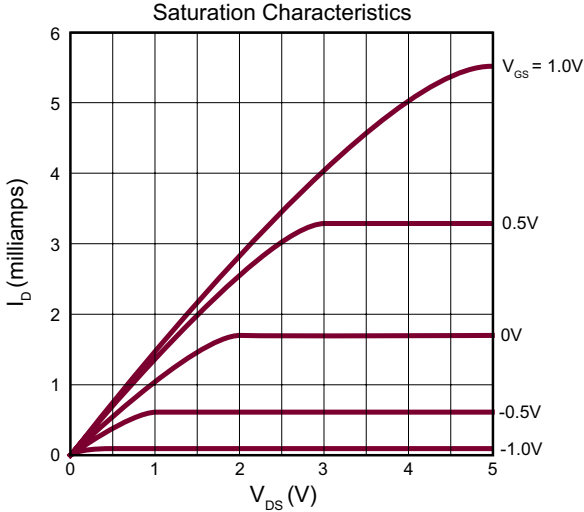
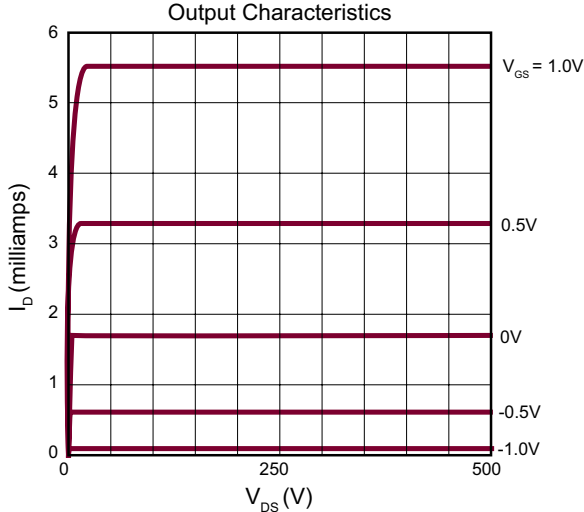
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

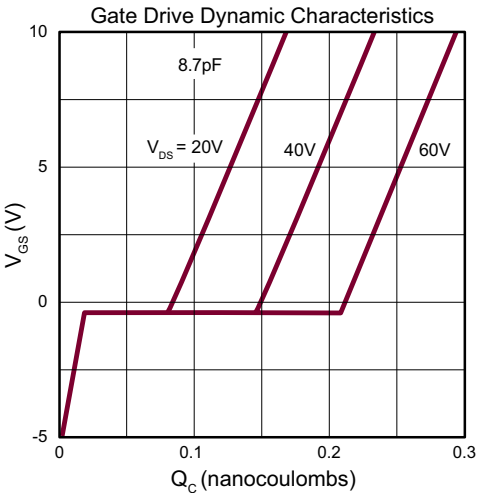
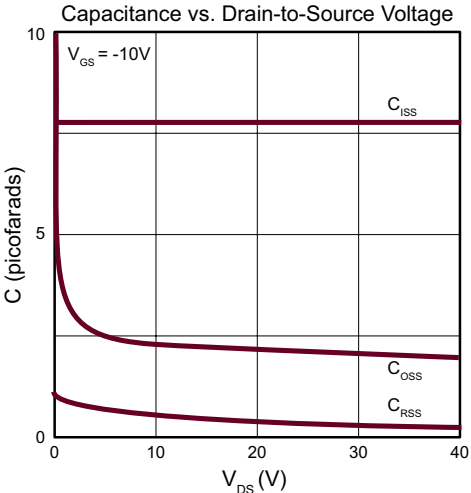
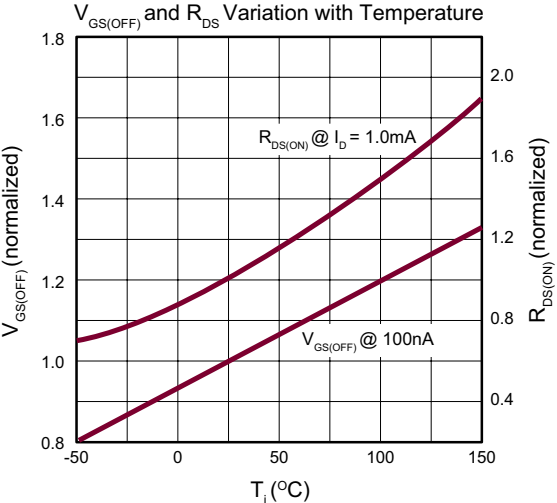
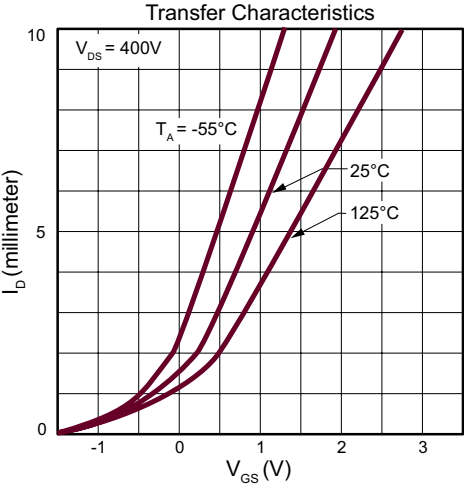
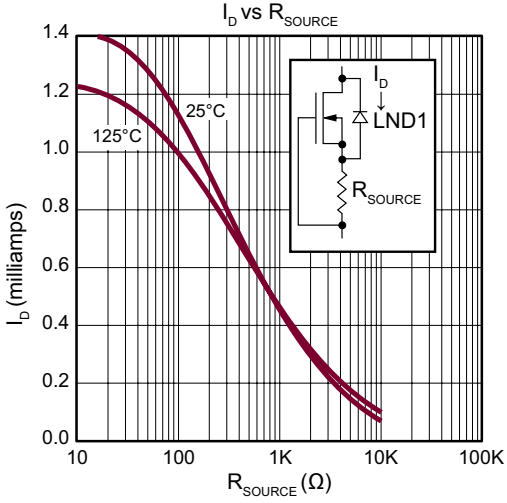
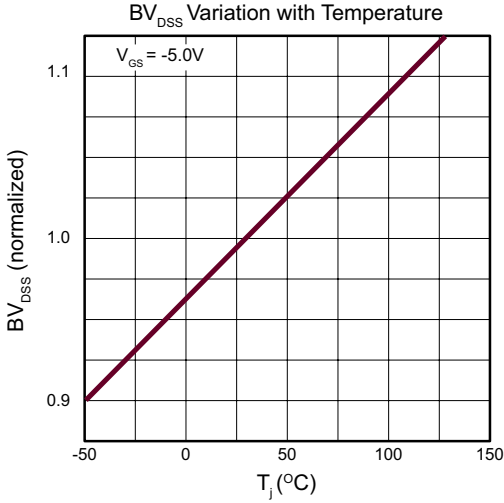
Switching Waveforms and Test Circuit



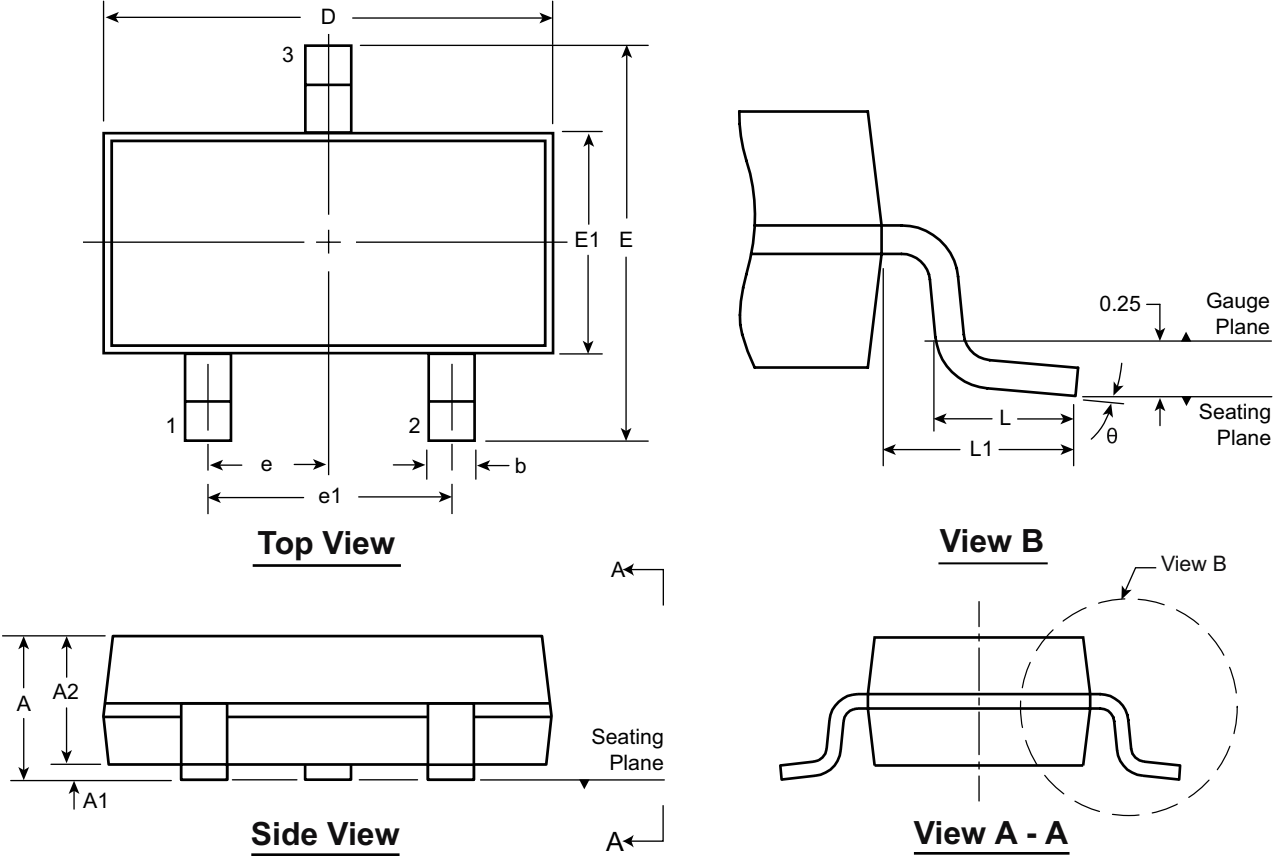
Typical Performance Curves



Typical Performance Curves (cont.)



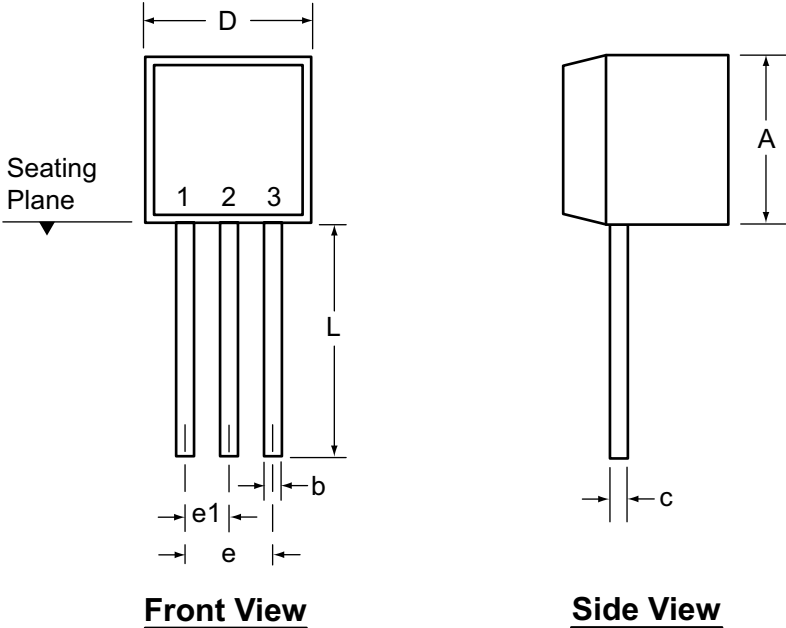
3-Lead TO-236AB (SOT-23) Package Outline (K1) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Symbol	A	A1	A2	b	D	E	E1	e	e1	L	L1	θ	
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30					-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40					0.60

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
[†] This dimension differs from the JEDEC drawing.
 Drawings not to scale.
 Supertex Doc.#: DSPD-3TO236ABK1, Version C041309.

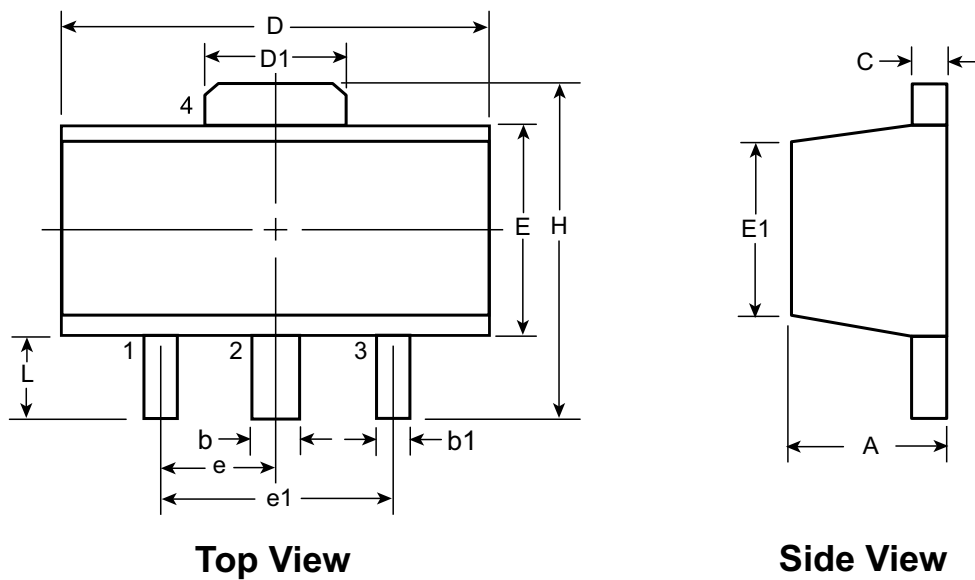
3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
 * This dimension is not specified in the JEDEC drawing.
 † This dimension differs from the JEDEC drawing.
Drawings not to scale.
 Supertex Doc.#: DSPD-3TO92N3, Version E041009.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version E051509.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А