Micro Circuit Engineering

technology applied

SINGLE CHANNEL ARINC DECODER

- 16/24 bit parallel interface
- Automatic address recognition option on 8/10 bits
- Single 5V supply with low power consumption < 50mW
- Full MIL operating range
- Built in parity and word length error detection
- HIGH/LOW speed programmable

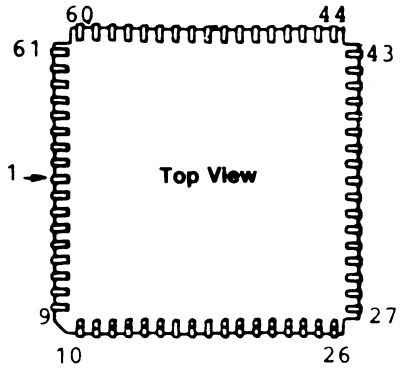
PIN CONFIGURATION

VDD	1	64	NRTDATRDY
D1/D17	2	63	DATA RDY
D2/D18	3	62	ONE DET
D3/D19	4	61	ZERO DET
D4/D20	5	60	NC
D5/D21	6	59	NTAGEN
D6/D22	7	58	ADD REC
D7/D23	8	57	PHI IN
NC	9	56	NC
NC	10	55	NC
NC	11	54	FAST/SLOW
NC	12	53	NRESET
NC	13	52	OVERRUN
D8/D24	14	51	TRANFLT
D9/D25	15	50	TAG VAL
D10/D26	16	49	MODE
D11/D27	17	48	IDENT
D12/D28	18	47	T1
D13/D29	19	46	T2
D14/D30	20	45	T3
D15/D31	21	44	NC
D16/D32	22	43	T4
D9	23	42	T5
D10	24	41	T6
D11	25	40	T7
NC	26	39	T8
NC	27	38	T9
D12	28	37	T10
D13	29	36	16/24 SEL
D14	30	35	DATMUX
D15	31	34	NDATEN
D16	32	33	VSS

Top View

NC NOT CONNECTED

64 PIN DIL PACKAGE



1	VDD	24	D9	47	NC
2	D1/D17	25	D10	48	T3
3	D2/D18	26	NC	49	T2
4	D3/D19	27	D11	50	T1
5	D4/D20	28	NC	51	IDENT
6	D5/D21	29	NC	52	MODE
7	D6/D22	30	D12	53	TAG VAL
8	D7/D23	31	D13	54	TRANFLT
9	NC	32	D14	55	OVERRUN
10	NC	33	D15	56	NRESET
11	NC	34	D16	57	FAST/SLOW
12	NC	35	VSS	58	NC
13	NC	36	NDATEN	59	NC
14	NC	37	DATMUX	60	NC
15	D8/D24	38	16/24 SEL	61	PHI IN
16	D9/D25	39	T10	62	ADD REC
17	D10/D26	40	T9	63	NTAGEN
18	D11/D27	41	T8	64	NC
19	D12/D28	42	T7	65	ZERO DET
20	D13/D29	43	NC	66	ONE DET
21	D14/D30	44	T6	67	DATA RDY
22	D15/D31	45	T5	68	NRTDATRDY
23	D16/D32	46	T4		

68 PIN J LEAD
SURFACE MOUNT PACKAGE.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	- 65ºC to +150ºC
Temperature (Ambient) under Bias	- 55ºC to +125ºC
Supply Voltage VDD	-0.3V to + 7V
DC Input Voltage	-0.3 to VDD +0.3V
Output Current (Single O/P)	10mA
Output Current (Total O/P)	20mA

ELECTRICAL CHARACTERISTICS over operating range

PARAMETER	DESCRIPTION	TEST CONDITIONS		MIN	TYP	MAX	UNITS
IOH	Output High Current	VOH=2.8V	VDD= 4.5V	1.0			mA
IOL	Output Low Current	VOL=0.4V		3.2			mA
VIH	Input High Voltage			2.4		VCC	Volts
VIL	Input Low Voltage			-0.3		0.8	Volts
IIL	Input Load Current	VSS				0.45	mA
IOZ	Output Leakage Current	0.4V‹VO‹VCC Output Disabled		-40		40	uA
CI	Input Capacitance	Test Frequency = 1.0 MHZ			2	2.6	pF
CI/O	I/O Capacitance				7	9	pF
ICC	Supply Current	VCC = MAX. All inputs HIGH, All outputs open.				1.5	mA

Switching Characteristics

Note Unless otherwise stated output loading assumes 50 pF capacitive plus static current within the limits of IOH_{MIN} and IOL_{MAX}

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
tRI & tFI	Input rise and fall times		50	ns
	Clock ∅ period	0.9	1.0	us
tHI	Clock ∅ HI time	0.45	0.55	us
tLO	NOT RESET LO time	200		ns
tLO	NOT RESET DATA READY LO time	100		ns
tRO; tFO	Output rise and fall times		200	ns
	Output Tristates delays relative to changes on NOT TAG EN or NOT DATA ENABLE.			
tAZ	Tristate OFF from NOT ENABLE ↑		300	ns
tAZ	Tristate ON from NOT ENABLE ↓ (includes worst case output edge time).		500	ns
tPLH	DATA READY from NOT RESET DATA READY ↓.	+0.05 2 -0.1	2 +0.2 2 +0.1	us us
tLO	DATA READY ↑ from DATA READY ↓.			
	16 bit bus option; data access incomplete; NOT DATA ENABLE LO; LO pulse on NOT RESET DATA READY ‹)		2 +0.2	

tPLH	DATA READY ↑ from RESET DATA READY ↑			us
	(16 bit bus option; data access incomplete; NOT DATA ENABLE LO; LO pulse on NOT RESET DATA READY >2)			
tPLH	DATA READY ↑ from TAG VALID (NOT DATA ENABLE LO; sequence operation)			us
tPLH	DATA READY ↑ from NOT DATA ENABLE ↓ (TAG VALID HI; NOT RESET DATA READY HI)			us
tPLH	DATA READY ↓ from NOT DATA ENABLE ↑			us
tPLH	TAG VALID ↓ from NOT RESET DATA READY ↑ (Data access completed)			us
	ADDRESS RECOGNITION times			
	ADDRESS RECOGNISED settling time from TAG VALID) (external recognition MODE SELECT HI)) TAG INPUTS settling time from TAG VALID (internal) recognition MODE SELECT LO))		4 -0.3	us
	ADDRESS RECOGNISED end of hold time from TAG) VALID)	6		us
	TAG INPUTS end of hold time from TAG VALID			

General

This circuit receives serial data from a buffered ARINC 429 bus into a 32 bit shift register. At the end of transmission the received word is checked. It is only considered to be “good” if the overall parity is ODD and the length is 32 bits. If the word fails these checks a TRANSMISSION FAULT flag is set. If the word is ‘good’ the tag bits are loaded into a tag latch and a TAG VALID flag is set. Either internal or external address recognition can be selected according to the state of MODE SELECT.

If the address is recognised within 4 us time window a 32 bit word latch is updated from the shift register. Thus the word latch only contains a “good” word whose address has been recognised. The contents of the word latch can be accessed whenever DATA READY flag is HI. It is available on a parallel trio-state output highway which is either 16 or 24 bits wide according to the state of 16/24 BUS SELECT. In the former, the 32 bit word is output in 2 halves and the state of output DATAMUX indicates which half is present. In the latter case bits 1 to 8 (the tag bits) are not available but the remaining 24 bits are presented together.

The user signals his receipt of the ARINC word by pulsing NOT RESET DATA READY low indicating that data access is complete which cancels TAG VALID and DATA READY.

The user has a whole word transmission time to access the word latch without entering an overrun condition.

When ‘end of word’ is detected an internal sequencer is initiated. Firstly, TAG VALID is examined. If this is still HI an OVERRUN flag is set. Next the data access logic is initialized and both TAG VALID and TRANSMISSION FAULT are cancelled.

Once set, the OVERRUN flag is only cancelled by a ‘data access complete’ signal. Thus the presence of an OVERRUN flag signals that the rate of servicing the word latch is slower than the transmission rate. Note that DATA READY and DATA MUX always refer to the status of the output data available from the word latch which cannot be updated unless the user requests it, whereas TAG VALID and TRANSMISSION FAULT always refer the the latest received word. The tag latch is always updated when TAG VALID is set but unless this tag is recognised the contents of the trag latch will bear no relationship to the contents of the word latch.

Arinc 429 Word Structure

An Arinc 429 word is 32 bits long. The first part of the word to be transmitted is the lable (tag) of which bit 1 is the most significant and bit 8 the least significant. Bits 9 and 10 are reserved for the source/destination identifier in some formats otherwise they are used as data pad bits. When circuit input IDENTIFIER is wired HI bits 9 & 10 are treated as extra tag bits and contribute to address recognition but when IDENTIFIER is wired LO bits 9 & 10 are excluded from address recognition.

Bits 11 to 29 are the data field of which bit 11 is the least significant, Bits 30 and 31 are reserved for the sign/status matrix and bit 32 is the parity bit.
µ
For high speed operation the bit rate must be 100 Kilobits per second ± 1% and circuit input FAST/SLOW SELECT must be wired LO. For low speed operation the bit rate must be in the range 12.0 to 14.5 Kilobits per second and the selected rate should be maintained within 1%. FAST/SLOW SELECT must then be wired HI.

Internal Timing

This is determined by a 1 Mhz clock applied to ∅ IN. this clock is asynchronous with the bit rate and should be maintained within ± 10%.

Word Synchronisation

The digital word is synchronised by reference to a gap of 4 bit times (minimum) between words. The beginning of the first transmitted bit following the gap signifies the beginning of the next word.

Spike Rejection (Timing asumes clock period = 1 µs)

The circuit incorporates pulse rejection filters on both inputs. This will reject pulses less than 2 µs duration and accept pulses greater than 3 µs duration.

Internal Address Recognition

If MODE SELECT is wired LO internal address recognition is performed during the sequencer period. during the sequencer period. If IDENTIFIER is LO the states input on T1 to T8 are internally compared with bits 1 to 8 of the tag latch and only if they are equivalent within 4 µs of TAG VALID being set is the address recognised. Although the states on T9 and T10 are ignored, these inputs should be held at good logic levels otherwise the circuit supply current could increase.

If IDENTIFIER is HI then T9 and T10 are also compared against 9 & 10 of the tag latch.

With MODE SELECT held LO the conditions on input pins ADDRESS RECOGNISED and TAG ENABLE are ignored. Since these pins have internal pull-up transistors they need not be connected if not required.

External Address Recognition (Timing assumes clock period = 1µs)

If MODE SELECT is wired HI the internal address comparator is inhibited. T1 to T10 respond as tri-state output ports enabled whenever NOTTAG ENABLE is LO. Then the contents of the tag latch are presented to the tag output bus.

The normal sequence of operations in this mode is for TAG VALID to be set at the end of a good word. The user takes this as a singla to interrogate the tag latch by enabling the tristates. Within 4 µs of TAG VALID going HI a decision is taken whether or not to load the word latch via ADDRESS RECOGNISED.

If either mode of operation is an address recognition signal is not detected within 4 μs of TAG VALID being set this flag is automatically cancelled and the word latch is not updated. Conversely, if an address recognition signal is detected within 4 μs of TAG VALID being set and is held for at least until 6 μs after the rising edge of TAG VALID then the word latch is updated. TAG VALID then stays HI until cancelled either by data access complete or the detection of the end of the next received word.

Data Bus

The contents of the word latch is output onto a data bus enabled by a LO on NOT DATA ENABLE. The status of the output bus is indicated by DATA READY. This flag is automatically held LO whenever DATA ENABLE ia HI. DATA READY is held LO for the duration of the internal sequence, whilst NOT RESET DATA READY is held LO and whilst DATA MUX and the output date are settling. Otherwise DATA READY is set soon after the word latch has been updated and cancelled when data access is complete.

24 Bit Option

For the 24 bit format 16/24 BUS SELECT is wired LO. DATA MUX is always HI to indicate that bits 17 to 32 are output on D1/17 and D16/32 respectively and in addition bits 9 to 16 are output on D9 to D16. Data access is complete when the user pulses NOT RESET DATA READY with a single LO pulse of width greater than 100 ns.

16 Bit Option

16/24 BUS SELECT is wired HI. DATA MUX is reset by the sequencer at the end of word. When DATA READY is set, bits 1 to 16 are available on D1/17 to D1/32 respectively. The user signals acceptance of the first half by pulsing NOT RESET DATA READY LO. Then DATA READY cancels whilst DATA MUX and DATA READY has been taken HI, DATA READY re-appears. DATA MUX is now HI and bits 17 to 32 available on D1/17 to D16/32. Data access is complete when NOT RESET DATA READY is pulsed LO for a second time.

End of Word Detection

This is detected by a gap counter which times out whilst ‘O’ DETECT and ‘1’ DETECT are LO for a time equivalent to 2 bit periods. Having timed out it generates an end of word signal which sets OVERRUN if TAG VALID is still HI and triggers the control sequencer.

Bit Counter

This counts the number of shift pulses applied to the shift register. It is not allowed to count past state 33 and is reset by the control sequencer. For a good word to be detected it must be in state 32 at the end of the word.

Parity Checker

This is reset along with the bit counter. It toggles whenever a logic ‘1’ is shifted into the register. For a good word to be detected it must be in a HI state at the end of the word.

Circuit Initialisation

The circuit can be initialised at any time by holding NOT RESET LO. This pin has an internal pull-up transistor. All the flags are immediately cleared and the circuit is locked whilst NOT RESET is LO. The minimum duration of LO is 200 ns. The removal of the reset condition occurs on a rising edge of ∅ IN following NOT RESET going HI.

APPLICATIONS

Instrument Displays

It is anticipated that the 24 bit data bus option will be required and that the data tri-states will be permanently enabled by wiring NOT DATA ENABLE LO.

If only one specific label is of interest this can be hard wired onto the tag ports conditioned as inputs by wiring MODE SELECT LO. Then internal address recognition will be performed.

If a range of labels is of interest then MODE SELECT can be wired HI. The tag ports are then conditioned as outputs. By wiring NOT TAG ENABLE LO and by using some simple external 'acceptable label' decode to drive ADDRESS RECOGNISED only the required transmissions are loaded. Note that in this mode if ADDRESS RECOGNISED is not connected then every good transmission is loaded into the word latch irrespective of its label since this input has an 'on chip' pull-up transistor.

Several of the pins may not be of interest e.g. OVERRUN, TRANSMISSION FAULT, TAG VALID, DATA READY, NOT RESET DATA READY, DATA MUX, in which case they need not be connected. This will not impair the basic function since a good, recognised transmission will be maintained in the word latch until overwritten by the next good, recognised transmission.

General Processor Systems

It is anticipated that the 16 bit data highway option will be required.

Many users will wire MODE SELECT HI and employ a label identification P.R.O.M. to generate the address recognition signal. A Direct Memory Access can be performed to transfer wanted data from the word latch into memory.

If the user requires an indication of the word transmission rate he can externally 'OR' TRANSMISSION FAULT with TAG VALID. The rising edge of such a waveform could be used to trigger a timer.

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