AT91EB55 Evaluation Board

User Guide



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Section 1

Overview

1.1 Scope

The AT91EB55 Evaluation Board enables real-time code development and evaluation. It supports the AT91M55800A.

This user guide focuses on the AT91 Evaluation Board as an evaluation and demonstration platform:

- Section 1 provides an overview.
- Section 2 describes how to setup the evaluation board.
- Section 3 describes the on-board software.
- Section 4 contains a description of the circuit board.

Appendixes A and B cover configuration straps and schematics including pin connectors.

1.2 Deliverables

The evaluation board is supplied with a DB9 plug to DB9 socket straight through serial cable to connect the target evaluation board to a PC. There is also a bare power lead with a 2.1 mm jack on one end for connection to a bench power supply.

The evaluation board is also delivered with a CD-ROM that contains an evaluation version of Software Development Toolkit and the documentation that outlines the AT91 microcontroller family.

The evaluation board is capable of supporting different kinds of debugging systems using an ICE interface or the on-board Angel Debug Monitor. Refer to the EB55 “Getting Started” tutorial documents for recommendations on using the evaluation board in a full debugging environment.

1.3 The AT91EB55 Evaluation Board

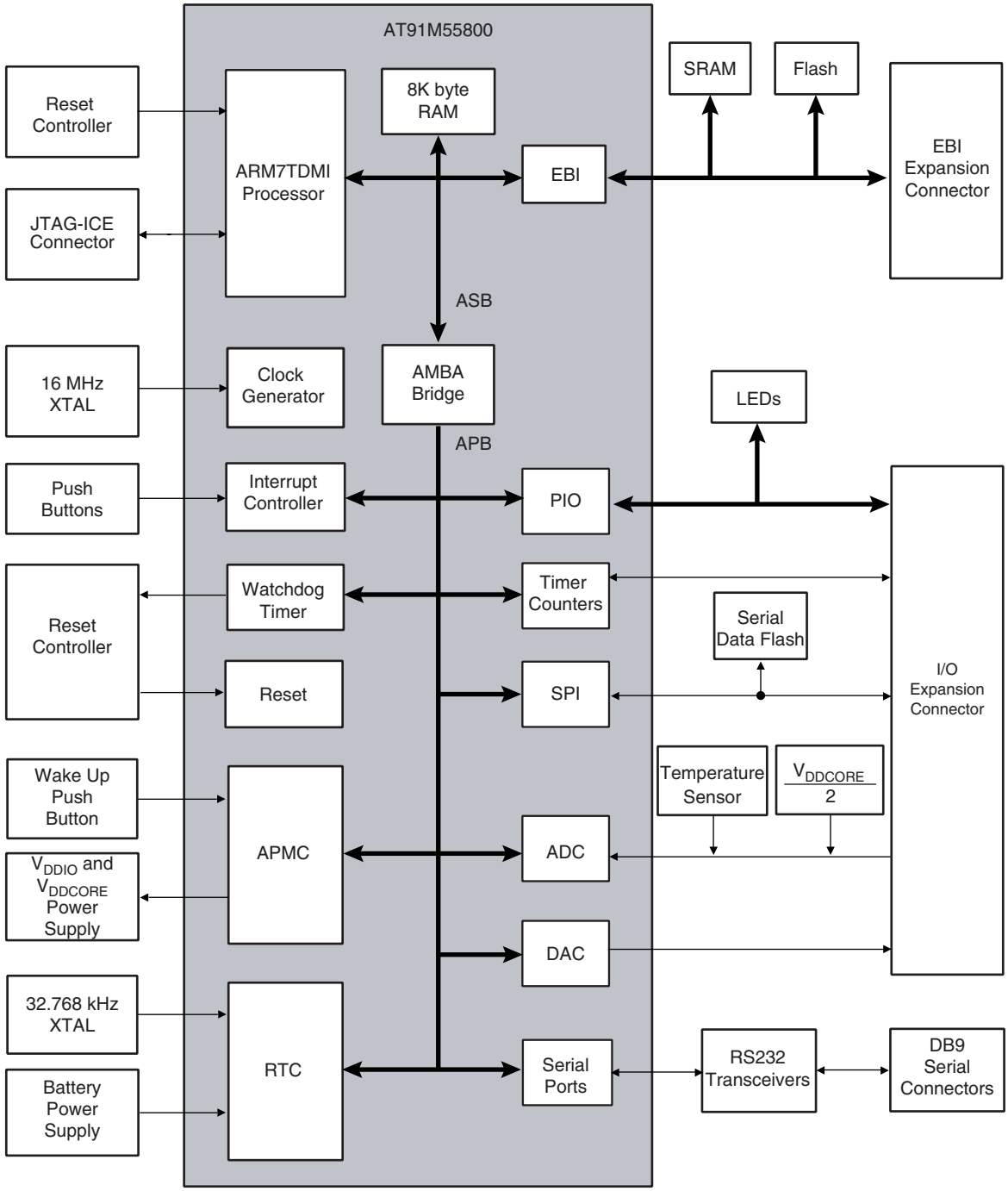
The board consists of an AT91M55800A, together with several peripherals:

- Two serial ports
- Reset push button
- An indicator which memorizes a reset appearance
- Memory clear for the reset indicator
- Four user-defined push buttons

- Eight LEDs
- 256K byte of 16-bit SRAM (upgradable to 1 MB)
- 2M bytes of 16-bit Flash (of which 1 MB is available for user software)
- 4M bytes of Serial Data Flash (upgradeable to 16 MB)
- 2 x 32 pin EBI expansion connector
- 3 x 32 pin I/O expansion connector
- 20-pin JTAG interface connector

If required, user-defined peripherals can also be added to the board. See “Appendix A” for details.

Figure 1-1. AT91EB55 Block Diagram



Section 2

Setting Up the AT91EB55 Evaluation Board

2.1 Electrostatic Warning

The AT91EB55 Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

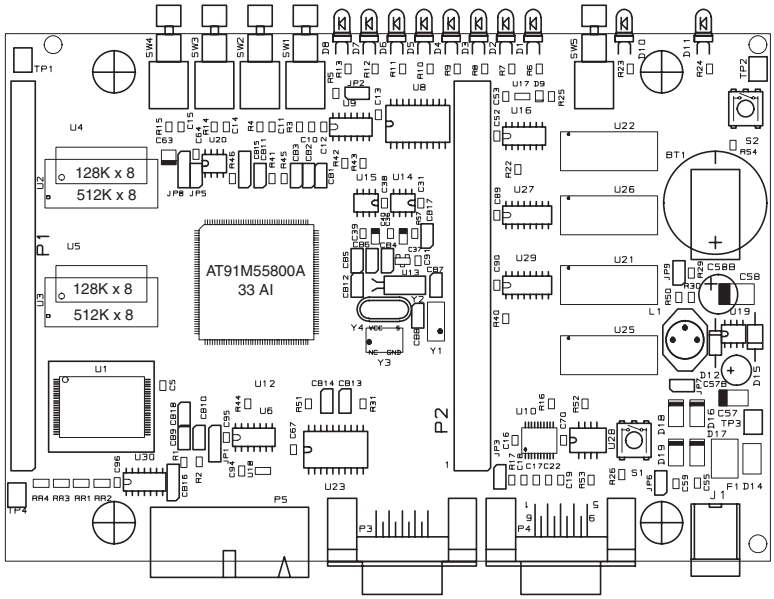
Requirements in order to set up the AT91EB55 Evaluation Board are:

- The AT91EB55 Evaluation Board itself
- DC power supply capable of supplying 7V to 12V @ 1 A (not supplied)

2.3 Layout

Figure 2-1 shows the layout of the AT91EB55 Evaluation Board.

Figure 2-1. Layout of the AT91EB55 Evaluation Board



2.4 Jumper Settings

JP1 is used to boot on standard or user programs. For standard operations, set it in the STD position.

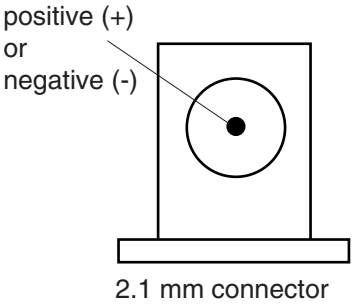
JP8 is used to select the core power supply of the AT91M55800A. Operations at 2V are not supported on the current silicon.

For more information about jumpers and other straps, see Appendix A.

2.5 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1) shown below in Figure 2-2. The polarity of the power supply is not critical. The minimum voltage required is 7V.

Figure 2-2. 2.1 mm Socket



The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to be from 7V to 12V. When you switch the power on, the red LED marked "POWER" will light up. If it does not, switch off and check the power supply connections.

The battery BT1 provides a 3V power supply to the Advanced Power Management Controller and the Real Time Clock (V_{DDBU}). In order to power up this module, the user must first close the JP9 jumper.

2.6 Measuring Current Consumption on the AT91M55800A

The board is designed to generate the power for the AT91 product only through the jumpers JP5 (V_{DDIO}), JP8 (V_{DDCORE}) and JP9 (V_{DDBU}). This feature enables measurements to be made on the current consumption of the AT91 product. See Appendix A for further details.

2.7 Testing the AT91EB55 Evaluation Board

In order to test the AT91EB55 Evaluation board, the following procedure should be performed:

1. Hold down the SW1 button and power up the board or generate a reset and wait for the light sequence on each LED to complete. All the LEDs light once and the D1 LED remains lit.
2. Release the SW1 button. The LEDs D1 to D7 light up in sequential order. If an error is detected, all the LEDs will light up twice.

The LEDs represent the following devices:

- D1 for the internal SRAM
- D2 for the external SRAM

- D3 for the external Flash
- D4 reserved
- D5 for the SPI data flash
- D6 reserved
- D7 for the USART
- D8 for the ADC and DAC

If a test is not carried out, the corresponding LED remains unlit and the test sequence restarts.

Section 3

The On-board Software

3.1 AT91EB55 Evaluation Board

The AT91EB55 Evaluation Board contains an AT49BV162A Flash device programmed with default software. Only the lowest eight 8-Kbyte sectors are used. The remaining sectors are user-definable and can be programmed using one of the Flash downloader solutions offered in the AT91 library.

When delivered, the Flash device contains:

- The Boot Software Program
- The Functional Test Software
- The Angel Debug Monitor
- A Default User Boot with a Default Application

The boot and FTS and are in sectors 0 and 1 of the Flash. These sectors are not locked for an easy on-board upgrade. The user must avoid overwriting this sector.

3.2 The Boot Software Program

The Boot Software Program configures the AT91M55800A and thus controls the memory and other board devices.

The Boot Software Program is started at reset if JP1 is in the STD position. If JP1 is in the USER position, the AT91M55800A boots from address 0x01010000 in the Flash, which must have a user-defined boot.

The Boot Software Program first initializes the master clock frequency at 32 MHz, the EBI, then executes the REMAP and checks the state of the buttons as described below.

As long as the SW1 button is pressed:

- All the LEDs light together
- The D1 LED remains lit until SW1 is released
- The Functional Test Software (FTS) is started

When the SW2 button is pressed:

- Reserved
- When the SW4 button is pressed:
- The shutdown function from AT91M55800A is activated. The power-up can be achieved by pressing the S1 push button only (Wake-up function)

When no buttons are pressed:

- Branch at address 0x01006000
- The Angel Debug Monitor starts from this address by recopying itself in external SRAM

3.3 Programmed Default Memory Mapping

The following table defines the mapping defined by the boot program.

Table 3-1. Memory Map

Part Name	Start Address	End Address	Size	Device
U1	0x01000000	0x011FFFFF	2-Mbyte	Flash AT49BV162A
U2 - U3	0x02000000	0x0203FFFF	256-Kbyte	SRAM

The Boot Software Program and FTS and are in sectors 0 and 1 of the Flash device. Sectors 3 to 7 support the Angel Debug Monitor

Sector 24 at address 0x01100000 must be programmed with a boot sequence to be debugged. This sector can be mapped at address 0x01000000 (or 0x0 after a reset) when the jumper JP1 is in the USER position.

3.4 The Angel Debug Monitor

The Angel Debug Monitor is located in the flash from 0x01006000 up to 0x0100FFFF. The boot program starts it if no button is pressed.

When Angel starts, it recopies itself in SRAM in order to run faster. The SRAM used by Angel is from 0x02020000 to 0x0203FFFF, i.e., the highest half part of the SRAM.

The Angel on the AT91EB55 can be upgraded regardless of the version programmed on it.

Note: If the debugger is started through ICE while the Angel monitor is on, the Advanced Interrupt Controller (AIC) and the USART channel are enabled.

Section 4

Circuit Description

4.1 AT91M55800A Processor

Figure 6-1 in “Appendix B – Schematics” shows the AT91M55800A. The footprint is for a 176-pin TQFP package.

Strap CB15 enables the user to choose between the standard ICE debug mode and the JTAG boundary scan mode of operation.

The operating mode is defined by the state of the JTAGSEL input detected at reset.

Jumper JP5 can be removed by the user to allow measurement of the current demand by the whole microcontroller (V_{DDIO} and V_{DDCORE}). Jumper JP8 can be removed to measure the core microcontroller consumption (V_{DDCORE}). See Figure 6-8. in “Appendix B – Schematics.”

Jumper JP9 can be removed by the user to allow measurement of the current demand by the APMC and RTC microcontroller modules (V_{DDBU}). See Figure 6-8. in “Appendix B – Schematics.”

4.2 Expansion Connectors and JTAG Interface

The two expansion connectors (I/O expansion connector and EBI expansion connector) and the JTAG Interface are described below.

The I/O and EBI expansion connectors pin-outs and positions are compatible with the other evaluation boards (except for the I/O expansion connector pin-out and position of the EB40) so that users can connect their prototype daughter boards to any of these evaluation boards. For the I/O expansion connector, rows A and B are position and pinout compatible.

4.2.1 I/O Expansion Connector

The I/O expansion connector makes the general purpose I/O (GPIO) lines, VCC3V3 and Ground available to the user. Configuration straps CB2, CB3, CB4, CB5, CB6, CB13, CB14 and CB17 are used to select between the I/O lines being used by the evaluation board or by the user via the I/O expansion connector. The connector is not fitted at the factory; however, the user can fit any 32 x 3 connector on a 0.1" (2.54 mm) pitch.

4.2.2 EBI Expansion Connector

The schematic illustrated in Figure 6-4 in "Appendix B - Schematics" also shows the Bus expansion connector, which, like the I/O expansion connector, is not fitted at the factory. The user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch to gain access to the data, address, chip select, read/write, oscillator output and wait request pins. VCC3V3 and Ground are also available on this connector. Configuration strap CB1, when open, allows the user to connect the EBI expansion connector to the MPI expansion connector of an AT91EB63 evaluation board without fearing any conflict problem.

4.2.3 JTAG Interface

An ARM-standard 20-pin box header (P5) is provided to enable connection of an ICE to the JTAG inputs on the AT91. This allows code to be developed on the board without using system resources such as memory and serial ports.

4.3 Memories

The schematics in Figure 6-3 and Figure 6-9 in "Appendix B – Schematics" show one AT49BV162A 2-Mbyte 16-bit Flash, one AT24C512 64-Kbyte EEPROM, one AT25256 32-Kbyte EEPROM, two 128K/512K x 8 SRAM devices and four AT45DB321 4-Mbyte serial data Flash devices.

The SPI devices are accessible through a 4 to 16 line decoder and by using the Chip Select Decode feature of the AT91 SPI peripheral (PCSDEC bit of the SPI Mode Register).

Note: The AT91EB55 is fitted with two 128K x 8 SRAM devices and one AT45DB321 serial DataFlash device (U21)AT24C512. The AT24C512 64-Kbyte EEPROM, and AT25256 32-Kbyte EEPROM are not fitted.

Strap JP1 shown on the schematic is used to select which part of 1-Mbyte of the flash is to be accessed. This is to enable users to flash download their application in the second part of the flash and to boot on it.

4.4 ADC and DAC Peripheral Connections

Two of the ADC and DAC channels are loop-backed together: DA0 on AD4 and DA1 on AD0.

Two 2.5V voltage reference devices are fitted on the board and connected to the DAVREF and ADVREF inputs, See Figure 6-6 in "Appendix B – Schematics". The user can fit other voltage reference value devices from this family (REF19x from Analog Devices) as the footprints are compatible.

A temperature sensor (LM61: Figure 6-6 in "Appendix B – Schematics") is connected to the AD1 input and is placed near the 32.768 kHz crystal quartz. It enables the user to take into account the frequency drift due to temperature evolutions using a software program.

The V_{DDCORE} with a resistor bridge (10 kΩ) provides the following value:

$$\frac{VDDCORE}{2}c$$

This voltage can be measured by AD2 input and allows the user to select the running clock accordingly.

4.5 Power and Crystal Quartz

The board features two quartz crystals: a 32.768 kHz one connected to the RTC low-power oscillator of the AT91M55800A and a 16 MHz one connected to the main oscillator.

The AT91M55800A Master Clock can be derived from the 32.768 kHz crystal quartz or the 16 MHz crystal quartz depending on the programming of the APMC registers. The on-chip oscillators together with one PLL-based frequency multiplier and the prescaler results in a programmable Master Clock between 500 Hz and 33 MHz.

Components for the PLL filter are fitted by default on the board (Figure 6-6 in "Appendix B – Schematics"). They are calculated to provide a 32 MHz (multiplier factor of 2 and settling time of 160 µs) Master Clock frequency.

The Voltage Regulator provides 3.3V to the board and will light the red POWER LED (D11) when operating.

This Voltage Regulator can be turned off by using the APMC shutdown feature when the JP7 jumper is closed. See Figure 6-8 in "Appendix B – Schematics." A wake-up push button (S1) is provided to exit this mode. Alternatively, the user can program a RTC alarm to awake the voltage regulator.

Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode rectifying circuit. Another regulator allows the user to power the AT91M55800A core with 3.3V or 2V by the mean of the JP8 jumper.

A 3V battery is provided on-board (Figure 6-8 in "Appendix B – Schematics") to power the RTC and APMC (V_{DDBU}). It has been provided to ensure the power supply for approximately 1 year.

4.6 Push Buttons, LEDs, Reset and Serial Interface

The IRQ0, TIOA0, PB17 and PB19 switches are debounced and buffered.

A supervisory circuit has been included in the design to detect and, consequently, reset the board when the 3.3V supply voltage drops below a typical 3.0V threshold. Note that the threshold can change, depending on the board production series. The supervisory circuit also provides a debounced reset signal. This device can also generate the reset signal in case of watchdog timeout as the pin NWDOVF of the AT91M55800A is connected on its input $\overline{MR}$.

The assertion of this reset signal will light the red RESET LED D10 and if the CLEAR RESET push button is pressed the LED D10 will unlight.

Another supervisory circuit separately initializes the microcontroller embedded JTAG/ICE interface when the 3.3V supply voltage drops below a typical 3.0V threshold. Note that this voltage can change depending on the board production series. The separated reset lines allow the user to reset the board without resetting the JTAG/ICE interface while debugging. bill

An RC device has been fitted on-board to ensure a correct power-on reset for the battery power supply modules (V_{DDBU}) first power up or when V_{DDBU} has been disconnected. This RC network has been calculated to generate a valid 300 ms minimum pulse width NRSTBU signal.

The schematic, Figure 6-5 in "Appendix B - Schematics" also shows eight general-purpose LEDs connected to Port B PIO pins PB8 to PB15.

Two 9-way D-type connectors P3/4 are provided for serial port connection.

Serial Port A (P3) is used primarily for host PC communication and is a DB9 female connector. TXD and RXD are swapped so that a straight through cable can be used. CTS and RTS are connected together as are DCD, DSR and DTR.

Serial Port B (P4) is a DB9 male connector with TXD and RXD obeying the standard RS-232 pin-out. Apart from TXD, RXD and Ground, the other pins are not connected.

A MAX3223 device U10 and associated bulk storage capacitors provide RS-232 level conversion.

4.7 Layout Drawing

The layout diagram schematic shows an approximate floorplan for the board. This has been designed to give the lowest board area, while still providing access to all test points, jumpers and switches on the board. See Figure 6-1 in “Appendix B – Schematics.”

The board is provided with four mounting holes, one at each corner, into which feet are attached. The board has two signal layers and two power planes.

Section 5

Appendix A – Configuration Straps

5.1 Configuration Straps (CB1 – 15, JP1 – 9)

By adding the I/O and EBI expansion connectors, users can connect their own peripherals to the evaluation board. These peripherals may require more I/O lines than available while the board is in its default state. Extra I/O lines can be made available by disabling some of the on-board peripherals or features. This is done using the configuration straps detailed below. Some of these straps present a default wire (notified by the default mention) that must be cut before soldering the strap.

CB1	On-board NCS4 Signal
Closed(1)	NCS4 signal is connected to the EBI expansion connector (P1 – B21)
Open	NCS4 signal is not connected to the EBI expansion connector (P1 – B21). This authorizes users to connect the EBI expansion connector of this board to the MPI expansion connector of an AT91EB63 evaluation board without conflict problems.

CB2	ADC0 Trigger Input Command
Closed(1)	ADC0 trigger input (AD0TRIG) is controlled by the PA4 PIO line.
Open	ADC0 trigger input (AD0TRIG) is not connected to the PA4 PIO line. This authorizes users to connect the corresponding lines to their own resources via the I/O expansion connector.

CB3	ADC1 Trigger Input Command
Closed(1)	ADC1 trigger input (AD1TRIG) is controlled by the PA7 PIO line.
Open	ADC1 trigger input (AD1TRIG) is not connected to the PA7 PIO line. This authorizes users to connect the corresponding lines to their own resources via the I/O expansion connector.

CB4	Temperature Sensor Enabling
Closed(1)	The temperature sensor device is connected to the ADC channel 1 (AD1) input.
Open	The temperature sensor device is not connected to the ADC channel 1 (AD1) input. This authorizes users to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

CB5	Analog Converter Peripherals Loopback
Closed(1)	DAC Channel 0 is connected to ADC Channel 4 for test purposes.
Open	DAC Channel 0 is not connected to ADC Channel 4. This authorizes users to connect the corresponding Analog Channels to their own resources via the I/O expansion connector.

CB6	Analog Converters Peripherals Loopback
Closed(1)	DAC Channel 1 is connected to ADC Channel 0 for test purposes.
Open	DAC Channel 1 is not connected to ADC Channel 0. This authorizes users to connect the corresponding Analog Channels to their own resources via the I/O expansion connector.

CB9	On-board Boot Chip Select
Closed(1)	NCS0 select signal is connected to the Flash memory.
Open	NCS0 select signal is not connected to the Flash memory. This authorizes users to connect the corresponding select signal to their own resources via the EBI expansion connector.

CB10	Flash Reset
Closed(1)	The on-board reset signal is connected to the Flash $\overline{\text{RESET}}$ input.
Open	The on-board reset signal is not connected to the Flash $\overline{\text{RESET}}$ input.

CB11	Boot Mode Strap Configuration
Open(1)	The BMS MCU input pin is set for the microcontroller to boot on an external 16-bit memory at reset.
Closed	The BMS MCU input pin is set for the microcontroller to boot on an external 8-bit memory at reset.

CB13, CB14	I^2C EEPROM Enabling
Closed(1)	E^2PROM communication is enabled.
Open	E^2PROM communication is disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

CB15	JTAGSEL
1 – 2(1)	The MCU standard ICE debug feature is enabled.
2 – 3	IEEE 1149.1 JTAG boundary scan feature is enabled.

CB16	R(eturn) TCK ICE Signal Synchronization
1 – 2	The TCK signal from the JTAG interface can be synchronized with MCKO signal and returns to the JTAG interface. (RTCK)
2 – 3(1)	The TCK and RTCK ICE signals are not synchronized with MCKO.

CB17	V_{DDCORE} Voltage Measurement
Closed(1)	The V_{DDCORE} power supply is connected to the ADC Channel 2 (AD2) input through a resistor bridge (divisor ratio 1/2).
Open	The V_{DDCORE} power supply is not connected to the ADC Channel 2 (AD2) input. This authorizes users to connect the corresponding ADC Channel to their own resources via the I/O expansion connector.

CB18	Flash Configuration
Open	Should be open when an AT49BV162A is fitted on the board.
Closed	Should not be closed when an AT49BV162A is fitted on the board.

JP1	User or Standard Boot Selection
2 – 3	The first half of the Flash memory is accessible at its base address.
1 – 2	The second half of the Flash memory is accessible at its base address. This authorizes users to download their own application software in this part and to boot on it.

JP2	Push Button Enabling
Open	SW1-4 inputs to the AT91 are valid.
Closed	SW1-4 inputs to the AT91 are not valid. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP3	RS-232 Driver Enabled
Open	The RS-232 transceivers are enabled.
Closed	The RS-232 transceivers are disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP7	Power Shut-down Feature
Open	The power supply shut-down feature is disabled.
Closed	The power supply shut-down feature is enabled. The user may shut-down the board main power supply by using the APMC shut-down feature. The system may be awakened by pushing the S1 Wake-Up push button or by programming an alarm in the RTC module.

JP8	Core Power Supply Selection
2 – 3	The MCU core is powered by a 3.3V power supply.
1 – 2	Not supported on the current microcontroller revision.

Note: 1. Hardwired default position: To cancel this default configuration, cut (or place) the wire (a jumper) on the board.

5.2 Power Consumption Measurement Straps (JP5, JP9)

The JP5 strap enables the user to connect an ammeter to measure the AT91M55800A global consumption (V_{DDCORE} and V_{DDIO}) when V_{DDCORE} power supply is derived from V_{DDIO} (JP8 in 3V3 position). The user can measure the core consumption by connecting another ammeter between JP8 1 – 2 or 2 – 3 depending on the power supply used to power the core.

The JP9 strap enables the user to connect an ammeter to measure the AT91M55800A APMC and RTC modules battery backup consumption (V_{DDBU}).

5.3 Ground Links (JP6)

The JP6 strap allows the user to connect the electrical and mechanical ground.

5.4 Increasing Memory Size

The AT91EB55 evaluation board is supplied with two 128K bytes x 8 SRAM memories. If, however, the user needs more than 256K bytes of memory, the devices can be replaced with two 512K x 8, 3.3V, 10/15 ns SRAMs, giving in total 1024K bytes.

The AT91EB55 evaluation board is supplied with one 4-MB Serial Data Flash. If the user needs more storage memory, 3 additional footprints are provided to fit AT45DB321 devices giving a total of 16M bytes.

Section 6

Appendix B – Schematics

6.1 Schematics

The following schematics are appended:

- Figure 6-1 PCB Layout
- Figure 6-2 AT91EB55 Blocks Synopsis
- Figure 6-3 EBI Memories
- Figure 6-4 I/O and EBI Expansion Connectors
- Figure 6-5 Push Buttons, LEDs and Serial Interface
- Figure 6-6 AT91M55800A
- Figure 6-7 Reset and JTAG Interface
- Figure 6-8 Power Supply
- Figure 6-9 SPI and I^2C Memories

The pin connectors are indicated on the schematics:

- P1 = EBI Expansion – External Bus Interface (Figure 6-4)
- P2 = I/O Expansion Connector (Figure 6-4)
- P3 = Serial A - Serial Interface (Figure 6-5)
- P4 = Serial B– Serial Interface (Figure 6-5)
- P5 = JTAG Interface (Figure 6-7)

Figure 6-1. PCB Layout

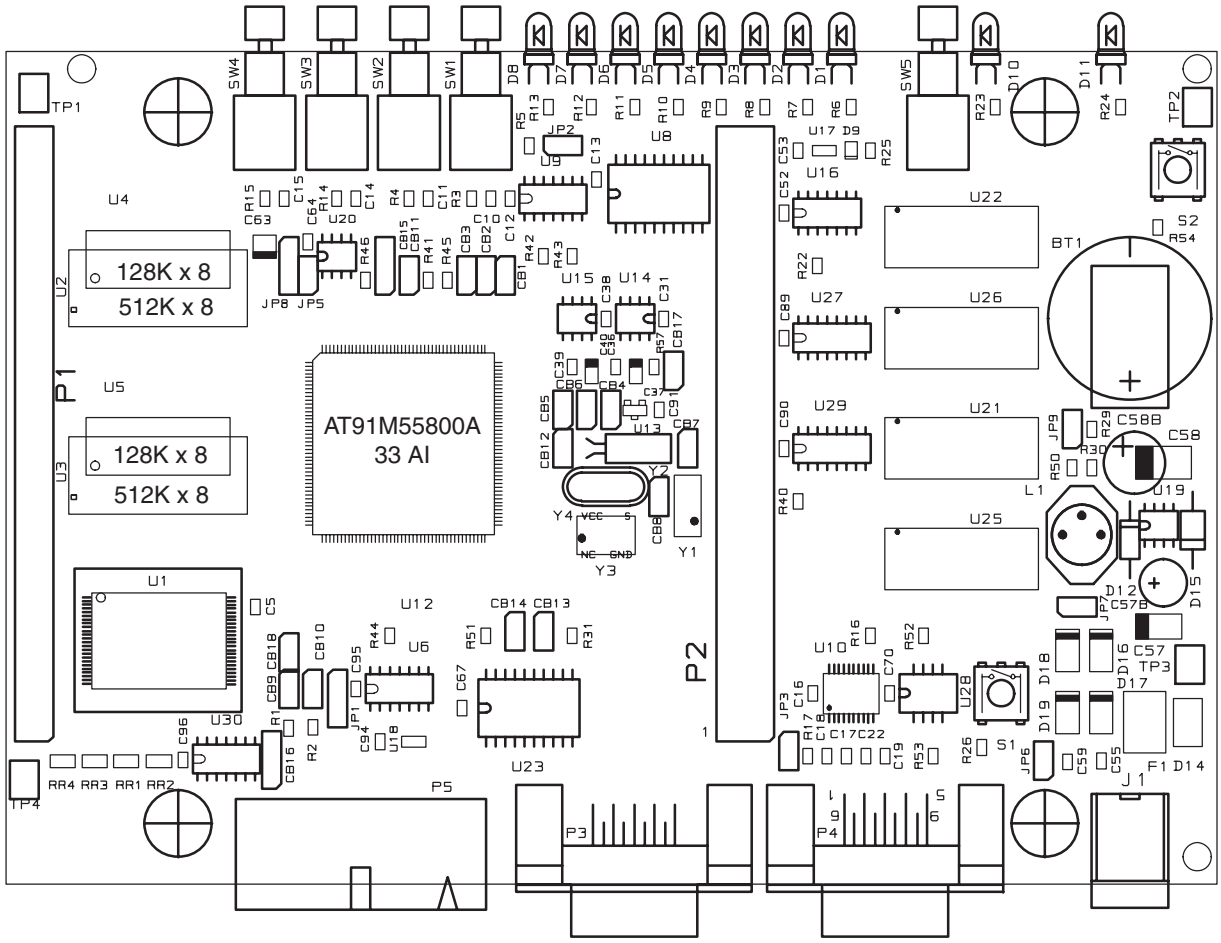


Figure 6-2. AT91EB55 Blocks Synopsis

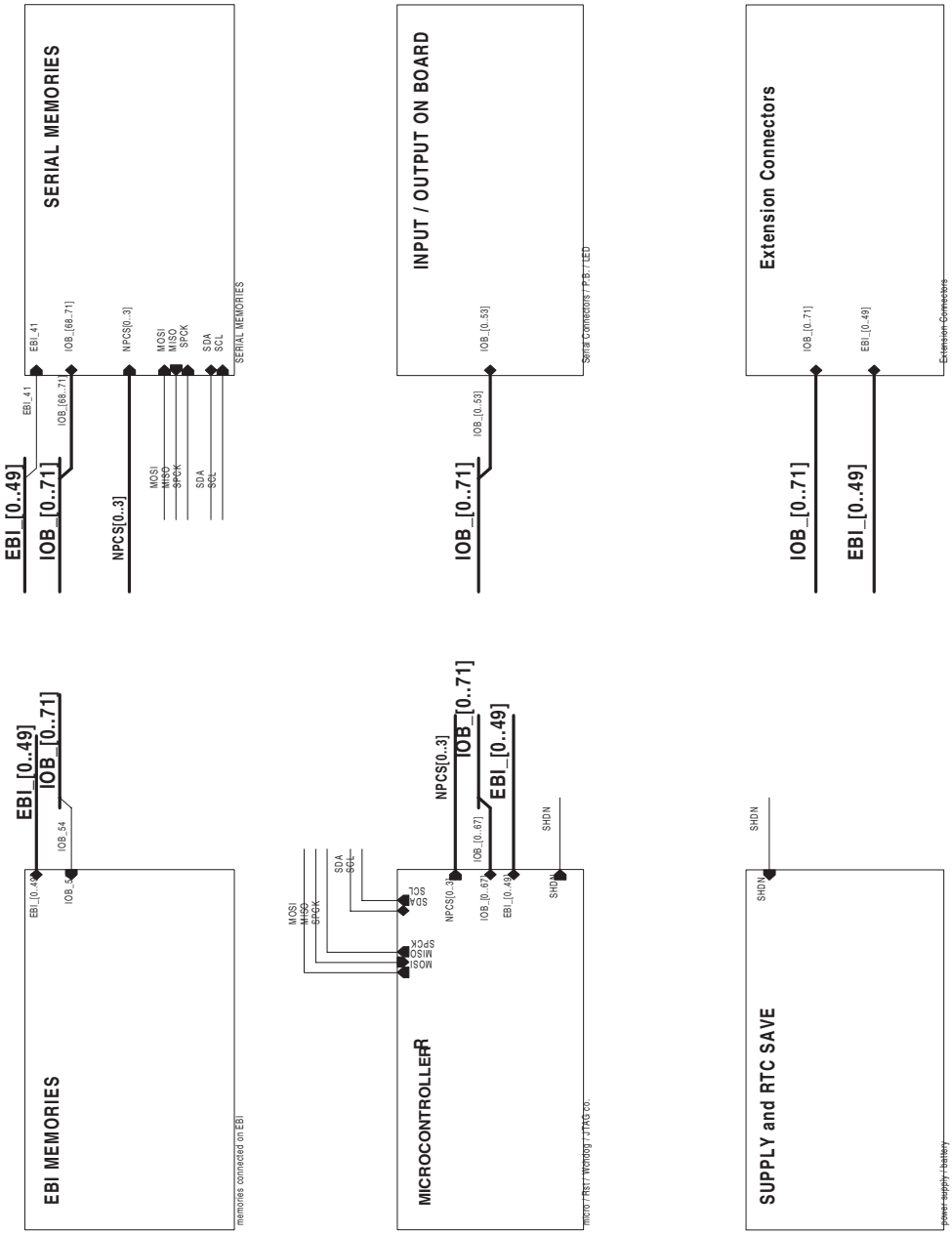


Figure 6-3. EBI Memories

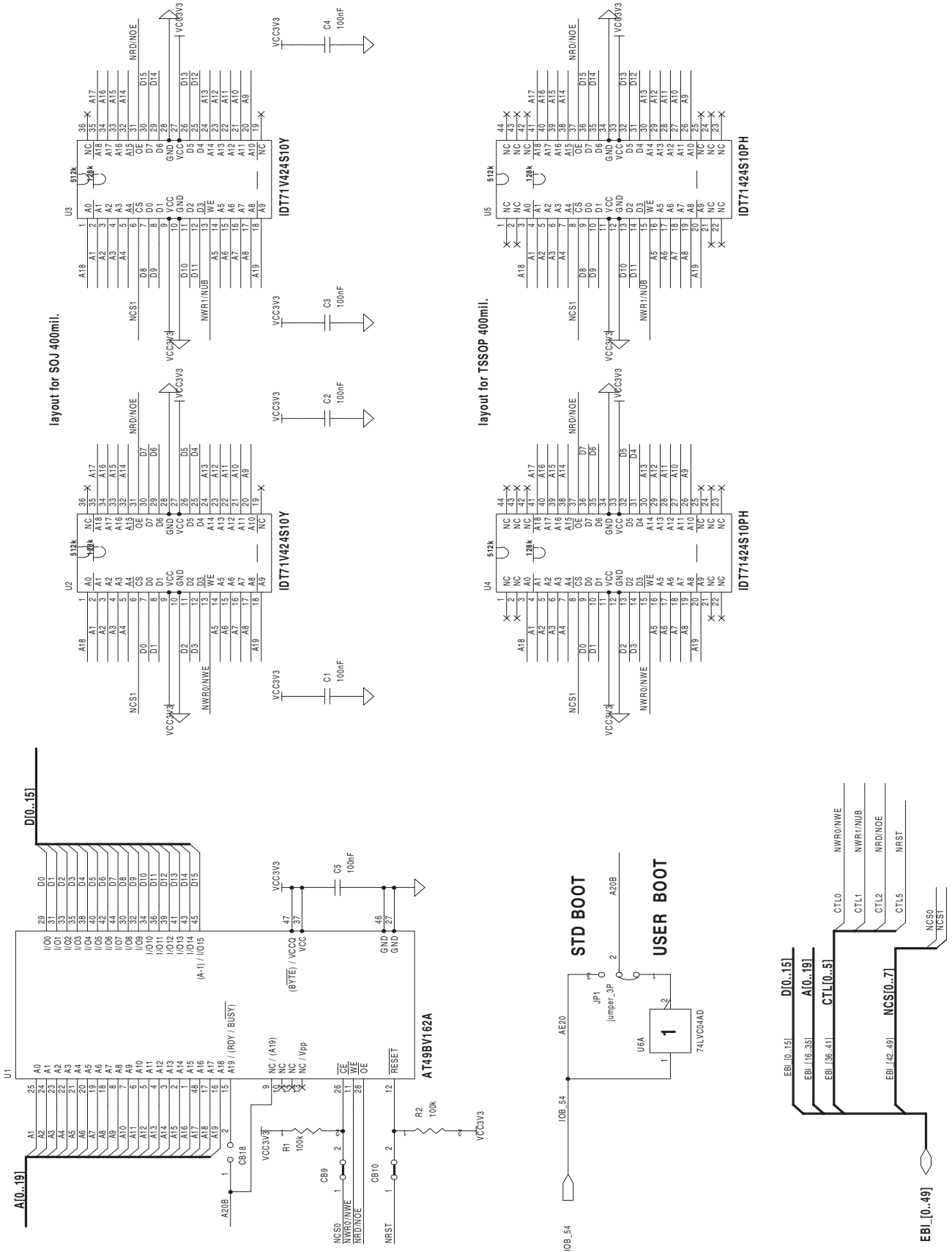


Figure 6-4. I/O and EBI Expansion Connectors

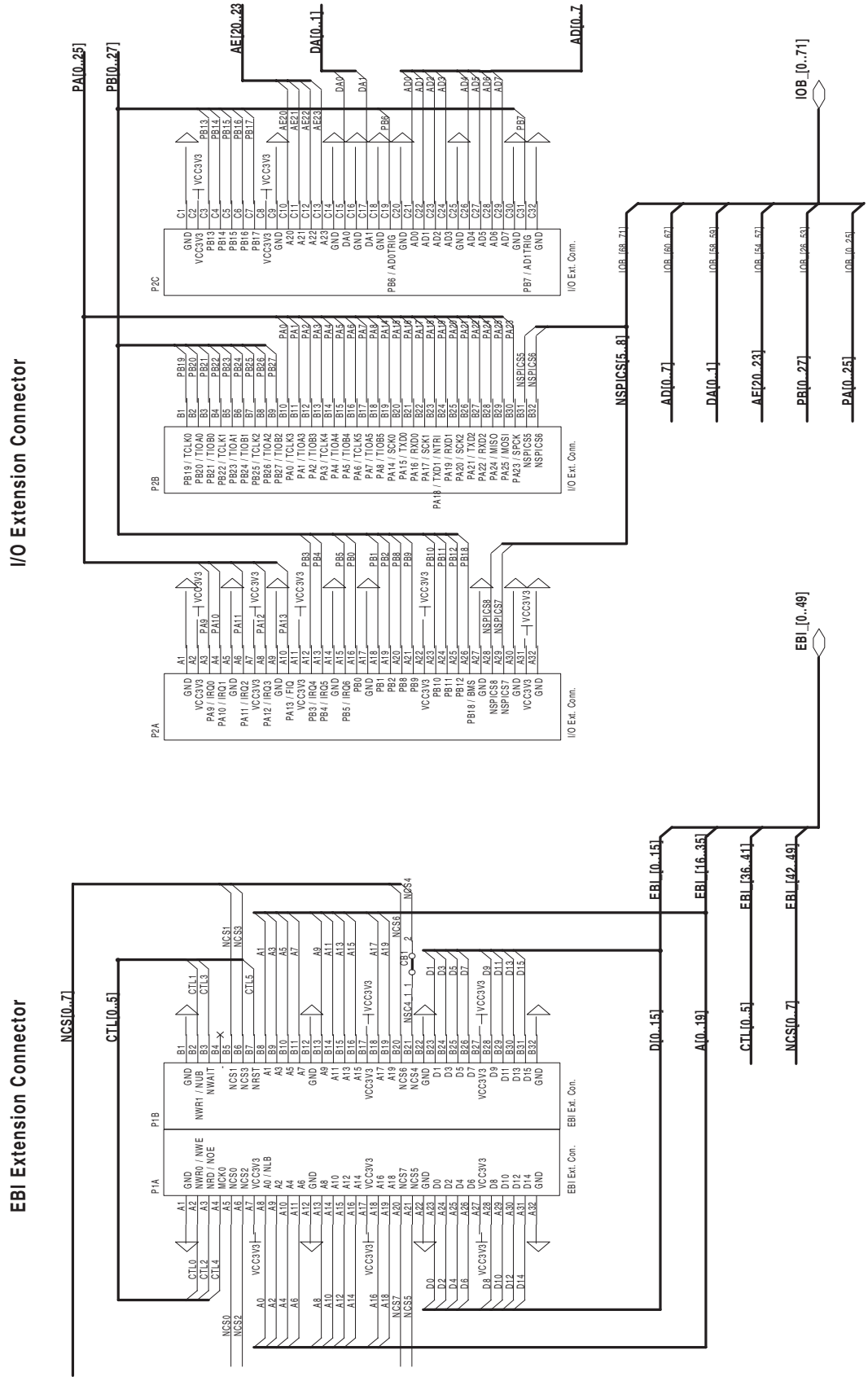


Figure 6-5. Push Buttons, LEDs and Serial Interface

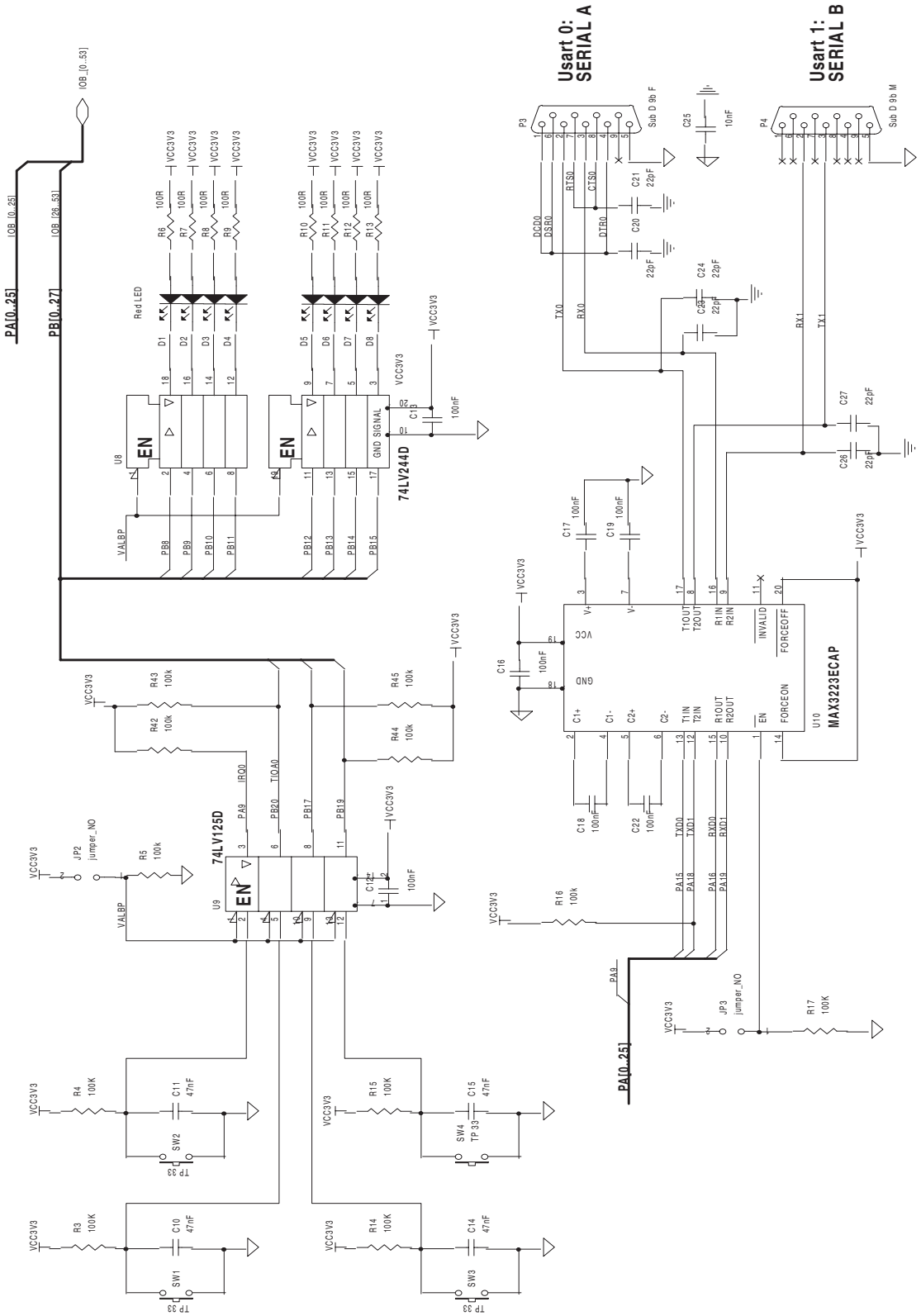


Figure 6-6. AT91M55800A

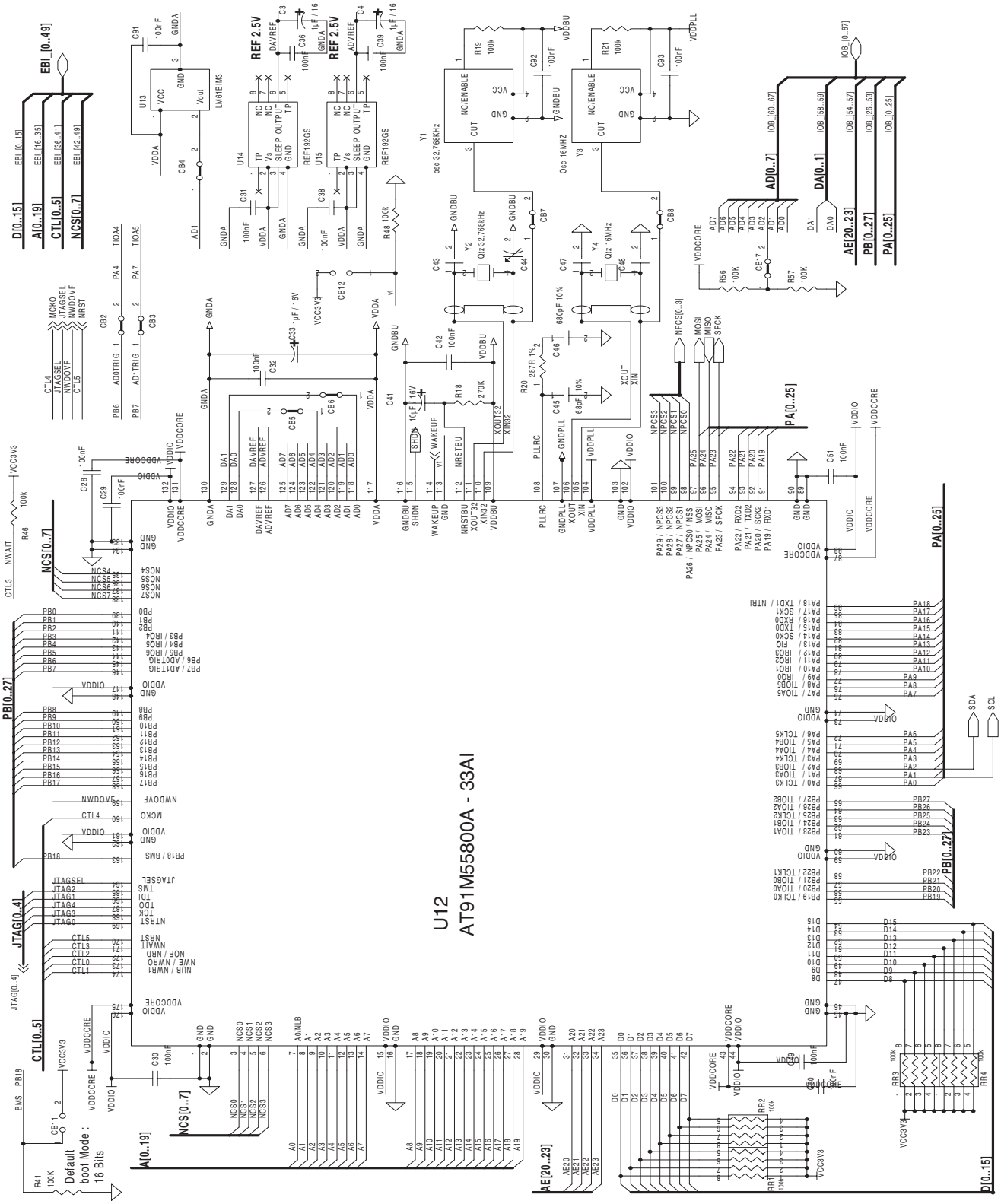


Figure 6-7. Reset and JTAG Interface

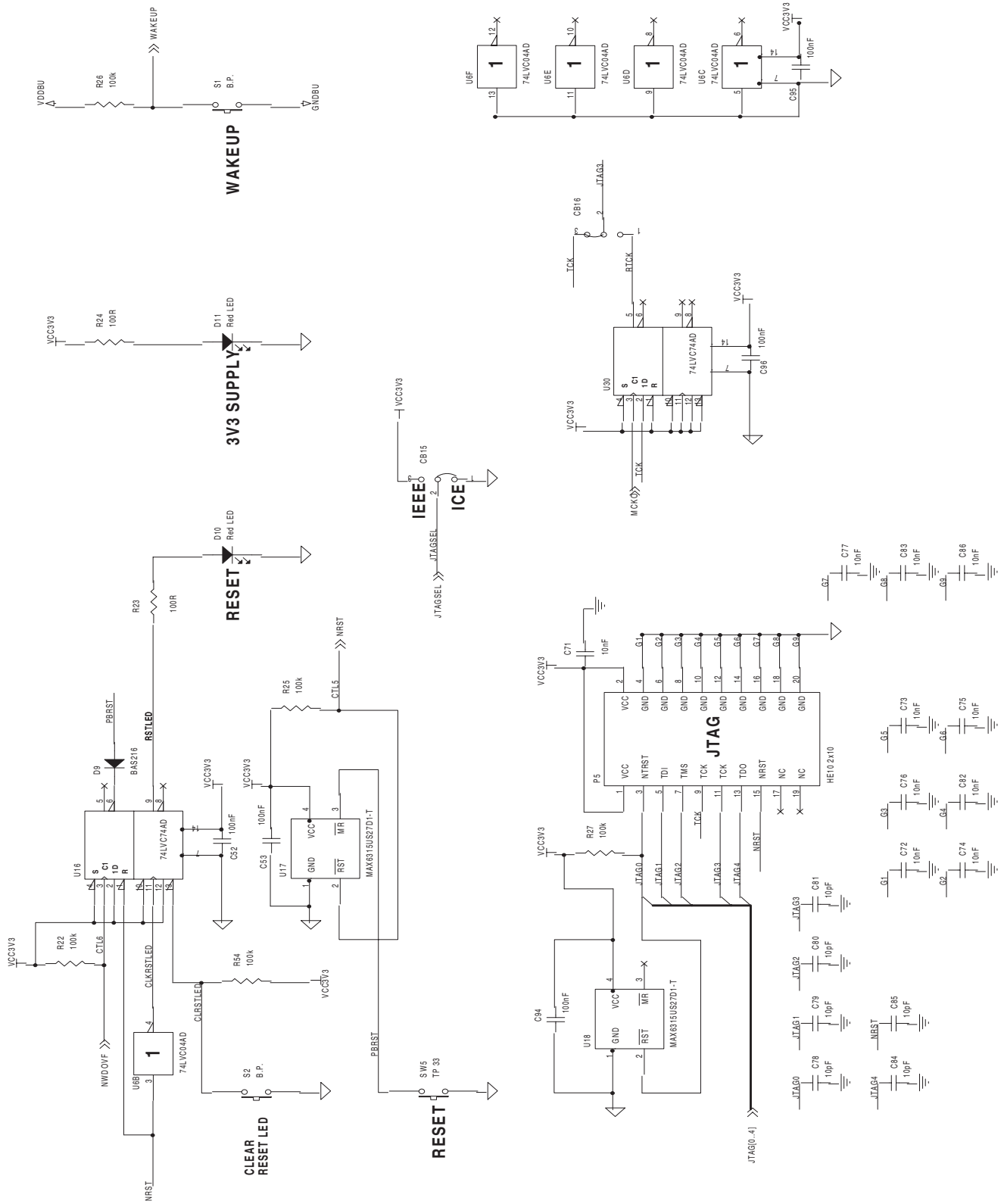


Figure 6-8. Power Supply

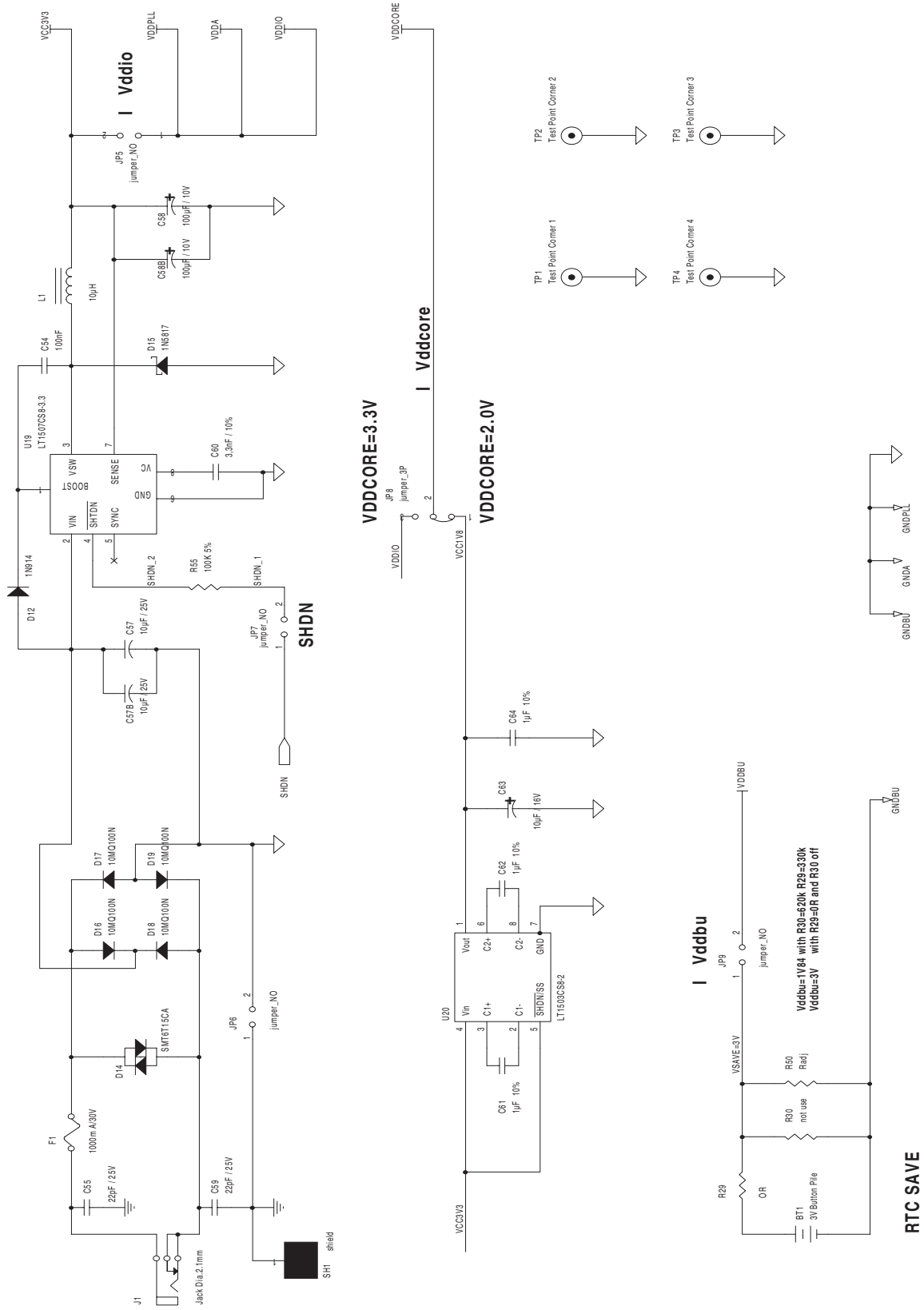
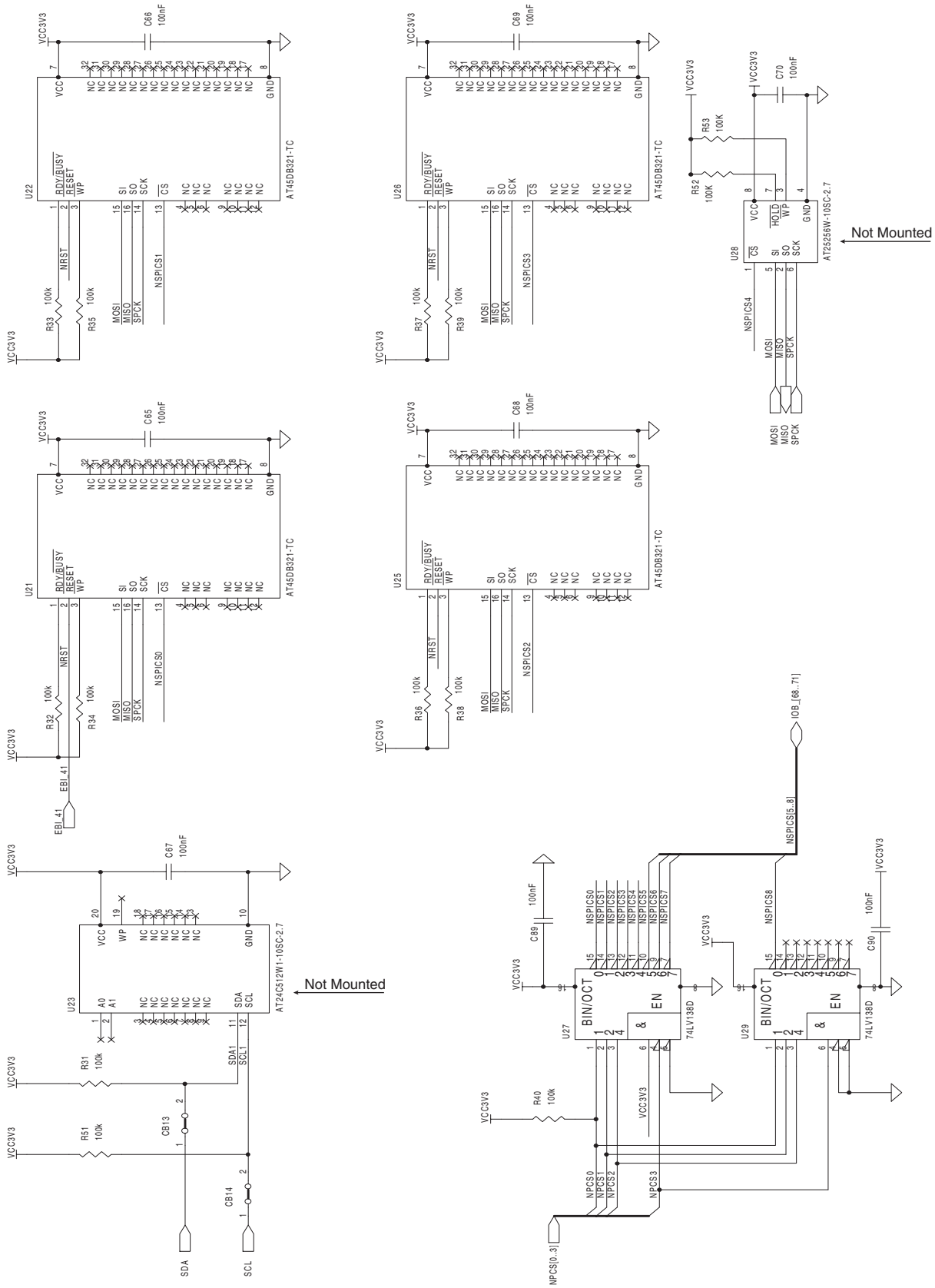


Figure 6-9. SPI and TWI Memories



Section 7

Appendix C – Bill of Material

Table 7-1. Bill of Material

Item	Qty	Reference	Part	Designation
1	1	BT1	3V Button Pile	Li/MnO2 3V 180 mAH pile UL: MH13654(N)
2	2	CB16		3 position jumper (jumper between 2-3)
3	3	CB18	CB_NO	
4	41	C1, C2, C3, C4, C5, C12, C13, C16, C17, C18, C19, C22, C28, C29, C30, C31, C32, C36, C38, C39, C42, C49, C50, C51, C52, C53, C54, C65, C66, C67, C68, C69, C70, C89, C90, C91, C94, C95, C96	100 nF	Ceramic X7R/10V
5	4	C10, C11, C14, C15	47 nF	Ceramic X7R/10V
6	6	C20, C21, C23, C24, C26, C27	22 pF	Ceramic NPO/10V
7	11	C25, C71, C72, C73, C74, C75, C76, C77, C82, C83, C86	10 nF	Ceramic X7R/16V
8	3	C33, C37, C40	1 µF/16V	Tantalum 16V/10%/TAJ
9	2	C41, C63	10 µF/16V	Tantalum 16V/10%/TAJ
10	3	C43, C47, C48	10 pF	Ceramic NPO/10V/5%
11	1	C44	4 - 25 pF	Adjustable Capacitor, serial TZBX4
12	1	C45	68 pF/10%	Ceramic X7R/10V/10%
13	1	C46	680 pF/10%	Ceramic X7R/10V/10%
14	2	C55, C59	22 pF/25V	Ceramic X7R/25V
15	1	C57	10 µF/25V	25V ESR < 0.5Ω/0.5Arms
16	1	C58	100 µF/10V	Tantalum 10V ESR < 0.5Ω

Table 7-1. Bill of Material (Continued)

Item	Qty	Reference	Part	Designation
17	1	C60	3.3 nF/10%	Ceramic X7R/25V/10%
18	3	C61, C62, C64	1 µF/10%	Ceramic X7R/10V/10%
19	6	C78, C79, C80, C81, C84, C85	10 pF	Ceramic X7R/16V
20	10	D1, D2, D3, D4, D5, D6, D7, D8, D10, D11	Red LED	Red LED H.R. 3mm/ T1/ 7mcd 60°
21	1	D9	BAS32L	Diode signal
22	1	D12	1N914	Diode signal
23	1	D14	SMT6T15CA	Transil 12.8V/600W/ VBRmini/14.3V
24	1	D15	1N5817	Schottky diode 1A/0.45V
25	4	D16,D17,D18,D19	10MQ060N	Diode rectifying 0.62V/0.77A
26	1	F1	1000 mA	Fuse rarm. 1000 mA/30V
27	3	JP1,JP8	jumper_3P	3 point jumper
28	6	JP5,JP7,JP9	jumper_NO	2 point jumper
29	1	J1	Jack Diameter 2.1mm	Jack socket 2.1mm
30	1	L1	10 µH	Self 10 µH at 1A and 500 kHz
31	1	P3	Sub D 9b F	Sub D 9b Female socket, right angle, mechanical strength, locking
32	1	P4	Sub D 9b M	Sub D 9b Male socket, right angle, mechanical strength, locking
33	1	P5	HE10 2x10	HE10 2x10 socket, low profile, right angle
34	27	R3, R4, R5, R14, R15, R16, R17, R25, R26, R27, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R51, R55	100K	Resistor 5%
35	2	R56, R57	10K	Resistor 5%
36	10	R6, R7, R8, R9, R10, R11, R12, R13, R23, R24	100R	Resistor 5%
37	1	R18	270K	Resistor 5%
38	1	R20	287R 1% E48	Resistor 1%
39	4	RR1, RR2, RR3, RR4	100K	Resistance network (4 resistors with 1 common point)
40	1	R29	0R	Shunt OR
41	16	R22, R42, R43, R44, R45, R46, R48, R52, R53, R54	100K	Resistor 5%

Table 7-1. Bill of Material (Continued)

Item	Qty	Reference	Part	Designation
42	4	SW1, SW2, SW3, SW4	TP 33	Push button with black cabochon
43	1	SW5	TP 33	Push button with red cabochon
44	2	S1, S2	Push Button	CMS Push button
45	4	TP1, TP2, TP3, TP4	Test Point Corner	CMS Test point
46	1	U1	AT49BV162A-70TI	Flash 2M bytes x 16-bits
47(1)	1	U4, U5	IDT71V124SA15PH	Static memory: 128k x 8-15 ns (double implantation)
48	1	U6	74LVC04AD	Reverser (LVC serial)
49	1	U8	74LV244D	Buffer
50	1	U9	74LV125D	Tri-state buffer
51	1	U10	MAX3223ECAP	Driver RS232 + ESD "E"
52	1	U12	AT91M55800A	Microcontroller
53	1	U13	LM61BIM3	Temperature sensor
54	2	U14, U15	REF192GS	Reference of voltage 2V5 ±0.5%
55	1	U16	74LVC74AD	D flip flop (LVC serial)
56	1	U30	74LCX74	D Flip Flop (LCX serial)
57	2	U17, U18	MAX6315US27D1-T	Circuit LVD-reset. (Threshold 2.7V; Timeout = 1 ms)
58	1	U19	LT 1507CS8-3.3	Voltage Regulator DC/DC
59	1	U20	LTC 1503CS8-2	Voltage Regulator DC/DC
60	4	U21	AT45DB321-TC	Serial DataFlash (wired according to availability)
61	1	U23	AT24C512W1-10SC-2.7	EEPROM 64K bytes
62	2	U27, U29	74LV138D	Decoder (3 to 8)
63	1	U28	AT25256W-10SC-2.7	EEPROM 32K bytes
64	1	Y2	Crystal 32768 kHz	Crystal 32768 kHz, ±20 ppm at 25° C
65	1	Y4	Crystal 16 MHz	Crystal 16 MHz, ±30ppm at 25° c
66	4	PS1, PS2, PS3, PS4	Board Support	Plastic bases H > 10mm

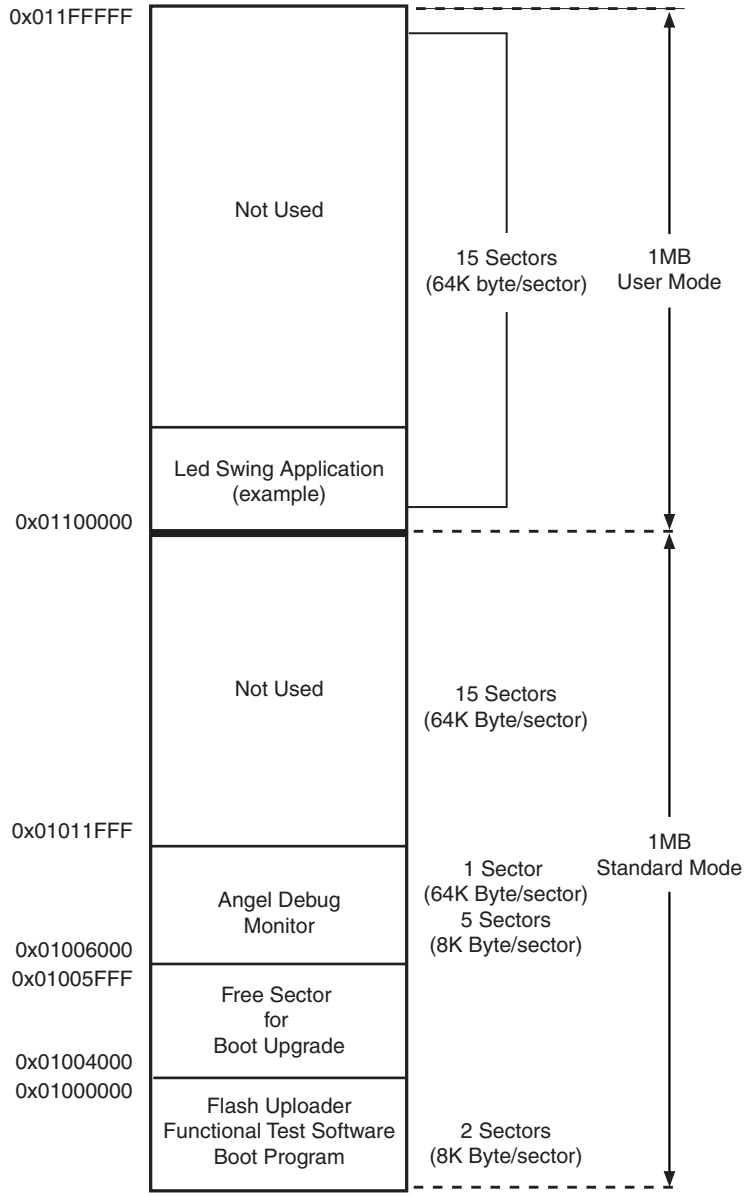
Note: 1. The EB55 is equipped with SRAM U2/U3 or U4/U5 (the difference lies in case type only). The choice is made according to availability.

Section 8

Appendix D – Flash Memory

The Figure 8-1 shows the embedded software mapping after the remap. It describes the location for the different programs in the AT49BV162A flash memory and the division into sectors.

Figure 8-1. EB55 Flash Memory Software Location



Revision History

Doc. Rev	Date	Comments	Change Request Ref.
1709A	June 2001	First Issue	
1709B	04-Aug-02	Pg. 5-2, Default positiion of CB11 changed from closed to open	
1709C	28-Apr-05	Global: Most Flash references read as AT49BV162V	CSR 05-199
		Figure 1-1, and global, reference to I2C E2PROM and SPI E2PROM removed or modified.	
		Global: Reference to SRAM downloader removed.	
		Section 3.2, SW2 button usage changed to reserved.	
		Section 3.4, 0x1004000 changed to 0x1006000.	
		Section 4.3, changes to information and note	
		Figure 6-3, AT49BV162A associated to U1	
		Table 6-9, name changed. U23 and U28 shown as “Not Mounted”.	
		Table 7-1, item 46, parts column shows AT49BV162A-70TI	
		Figure 8-1, illustration replaced	

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