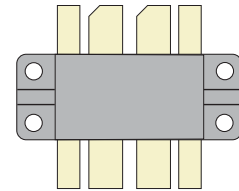
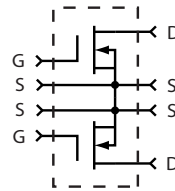




Common Source  
Push-Pull Pair


# ARF476FL



## RF POWER MOSFET N-CHANNEL PUSH - PULL PAIR

**165V 450W 150MHz**

The ARF475FL is a matched pair of RF power transistors in a common source configuration. It is designed for high voltage push-pull or parallel operation in narrow band ISM and MRI power amplifiers up to 150 MHz.

- **Specified 150 Volt, 128 MHz Characteristics:**
  - Output Power = 900 Watts Peak
  - Gain = 15dB (Class AB)
  - Efficiency = 50% min
- **High Performance Push-Pull RF Package.**
- **High Voltage Breakdown and Large SOA for Superior Ruggedness.**
- **Low Thermal Resistance.**
- **RoHS Compliant \*** 
  - \*Pb Free Terminal Finish.

### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.


Symbol	Parameter	ARF476FL	UNIT
$V_{DSS}$	Drain-Source Voltage	500	Volts
$V_{DGO}$	Drain-Gate Voltage	500	
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$ (each device)	10	Amps
$V_{GS}$	Gate-Source Voltage	$\pm 30$	Volts
$P_D$	Total Device Dissipation @ $T_C = 25^\circ\text{C}$	910	Watts
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 175	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	

### STATIC ELECTRICAL CHARACTERISTICS (each device)

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{V}, I_D = 250 \mu\text{A}$ )	500			Volts
$V_{DS(ON)}$	On State Drain Voltage <sup>①</sup> ( $I_{D(ON)} = 5\text{A}, V_{GS} = 10\text{V}$ )		2.9	4	
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = V_{DSS}, V_{GS} = 0\text{V}$ )			100	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 50\text{V}, V_{GS} = 0, T_C = 125^\circ\text{C}$ )			500	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$ )			$\pm 100$	nA
$g_{fs}$	Forward Transconductance ( $V_{DS} = 15\text{V}, I_D = 5\text{A}$ )	3	3.6		mhos
$g_{fs1}/g_{fs2}$	Forward Transconductance Match Ratio ( $V_{DS} = 15\text{V}, I_D = 5\text{A}$ )	0.9		1.1	Volts
$V_{GS(TH)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 200\text{mA}$ )	2	3.3	4	
$DV_{GS(TH)}$	Gate Threshold Voltage Match ( $V_{DS} = V_{GS}, I_D = 200\text{mA}$ )			0.2	

### THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case		0.15	0.165	$^\circ\text{C/W}$
$R_{\theta JHS}$	Junction to Sink (Use High Efficiency Thermal Grease and Planar Heat Sink Surface.)		0.30	0.33	

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$C_{iss}$	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1MHz$		780	830	pF
$C_{oss}$	Output Capacitance			125	130	
$C_{rss}$	Reverse Transfer Capacitance			7	9	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 250V$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6 W$		5.1	10	ns
$t_r$	Rise Time			4.1	8	
$t_{d(off)}$	Turn-off Delay Time			12	18	
$t_f$	Fall Time			4.0	7	

FUNCTIONAL CHARACTERISTICS (Push-Pull Configuration)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$G_{PS}$	Common Source Amplifier Power Gain	$f = 128 MHz$ $I_{dq} = 15mA$ $V_{DD} = 150V$ $P_{out} = 900W$ $PW = 3ms$ 10% duty cycle	14	16		dB
$\eta$	Drain Efficiency		50	55		%
$\Psi$	Electrical Ruggedness VSWR 5:1		No Degradation in Output Power			

① Pulse Test: Pulse width < 380  $\mu S$ , Duty Cycle < 2%.

Microsemi Reserves the right to change, without notice, the specifications and information contained herein.

Per transistor section unless otherwise specified.

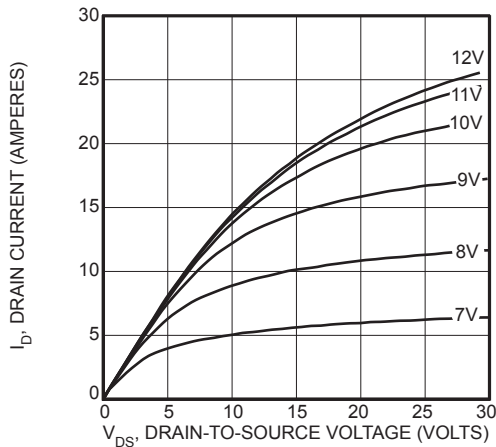


Figure 1, Typical Output Characteristics

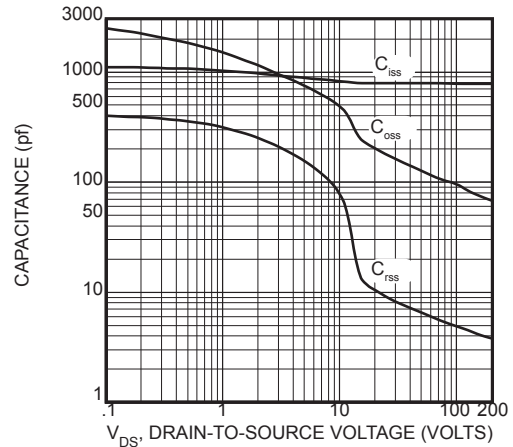


Figure 2, Typical Capacitance vs. Drain-to-Source Voltage

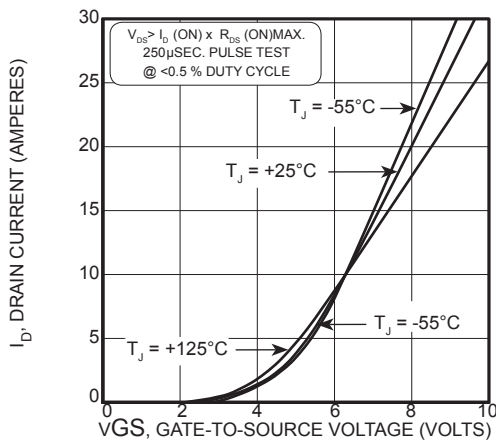


Figure 3, Typical Transfer Characteristics

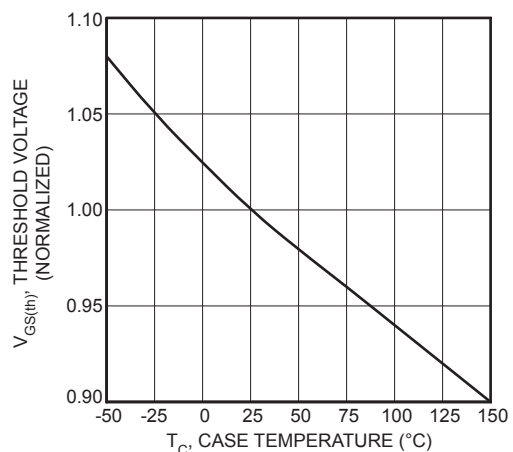


Figure 4, Typical Threshold Voltage vs Temperature

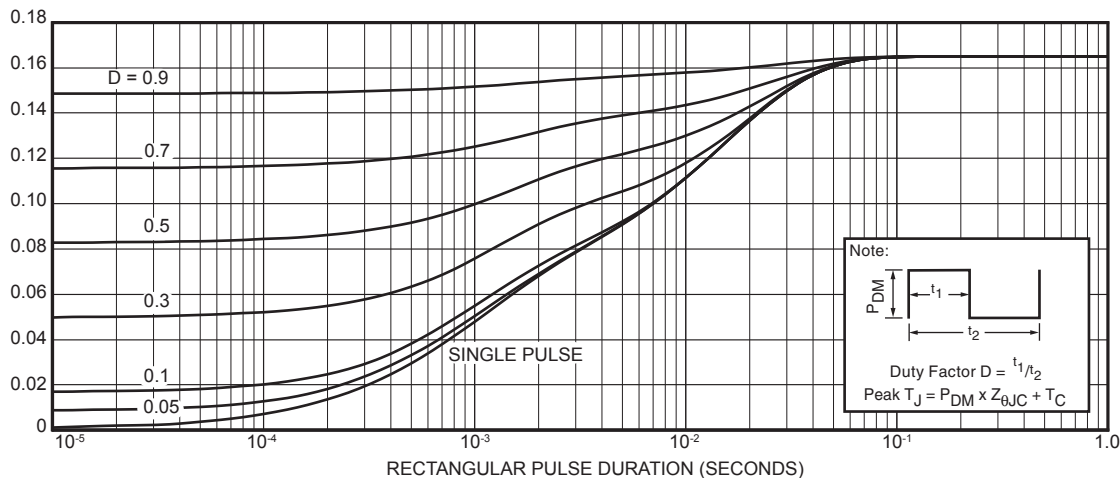
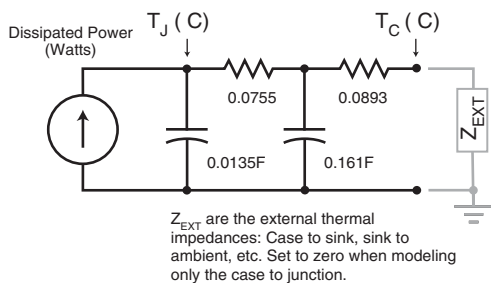


FIGURE 5a, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION



Z<sub>EXT</sub> are the external thermal impedances: Case to sink, sink to ambient, etc. Set to zero when modeling only the case to junction.

Figure 5b, TRANSIENT THERMAL IMPEDANCE MODEL

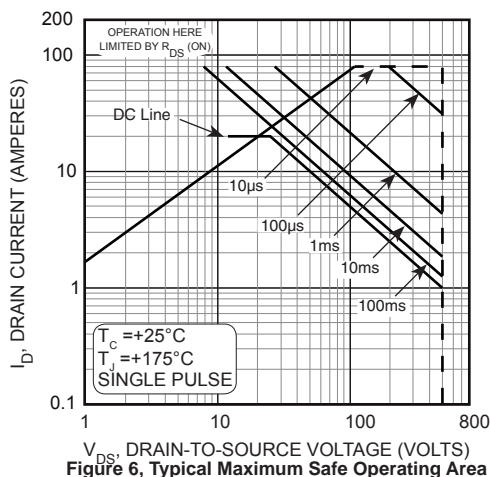


Figure 6, Typical Maximum Safe Operating Area

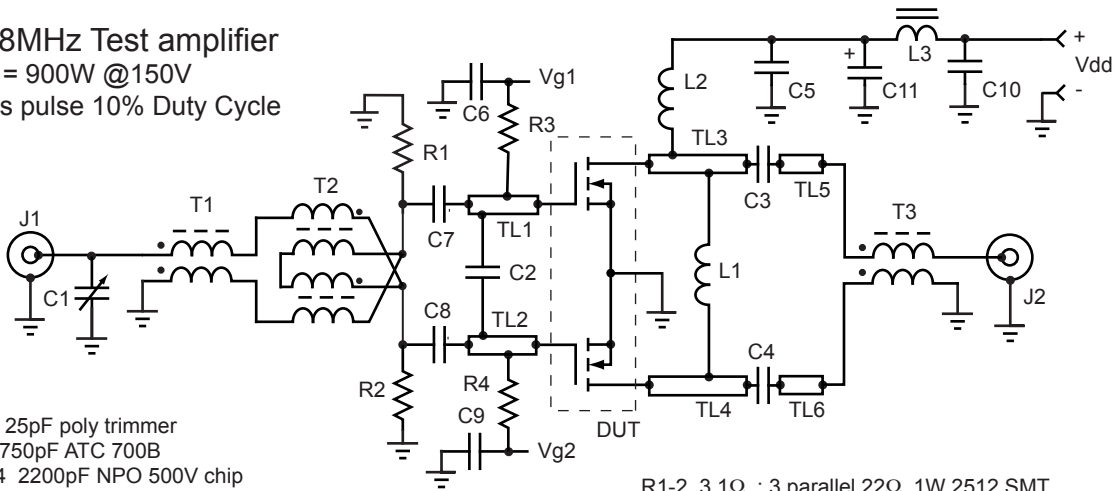
Table 1 - Typical Series Equivalent Large Signal Input - Output Impedance

Freq. (MHz)	Z <sub>in</sub> (Ω) gate to gate	Z <sub>OL</sub> (Ω) drain - drain
30	5.2 -j10	41 -j20
60	1.37 -j5.2	26 -j25
90	.53 -j2.6	16 -j23
120	.25 -j1.0	10 -j20
150	.25 +j0.2	6.7 -j17

Z<sub>in</sub> - Gate -gate shunted with 25Ω I<sub>DQ</sub> = 15mA each side  
 Z<sub>OL</sub> - Conjugate of optimum load for 600 Watts peak output at V<sub>dd</sub> = 150V  
 25% duty cycle and PW = 5ms

128MHz Test amplifier

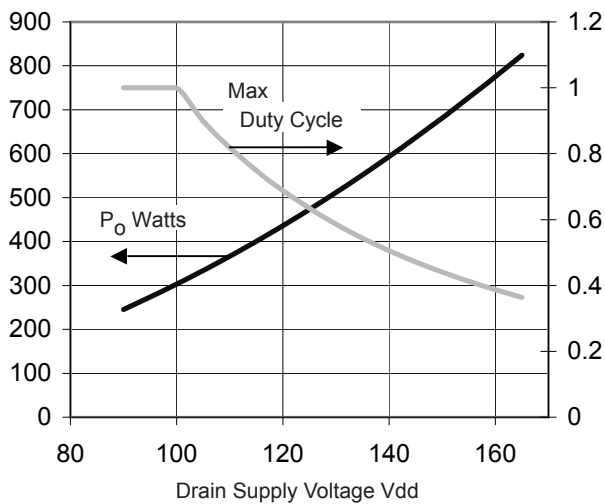
P<sub>o</sub> = 900W @150V  
 3ms pulse 10% Duty Cycle



- C1 25pF poly trimmer
- C2 750pF ATC 700B
- C3-4 2200pF NPO 500V chip
- C5-10 10nF 500V chip
- C11 1000uF 250V electrolytic
- L1 30nH 1.5t #18 enam .375" dia
- L2 680nH 12t #24 enam .312" dia
- L3 2t #20 on Fair-Rite 2643006302 bead, ~ 2uH

- R1-2 3.1Ω : 3 parallel 22Ω 1W 2512 SMT
- R3-4 2.2kΩ 1/4W axial
- T1 1:1 balun 50Ω coax on Fair-Rite 2843000102 core
- T2 4:1 25Ω coax on 2843000102 Fair-Rite balun core
- T3 1:1 coax balun RG-303 on 2861006802 Fair-Rite core
- TL1-2 Printed line L = 0.75" w = .23"
- TL3-6 Printed line L = 0.65" w = .23"  
 0.23" wide stripline on FR-4 board is ~ 30Ω Z<sub>0</sub>

Peak Output Power vs. V<sub>dd</sub> and Duty Cycle



Notes:

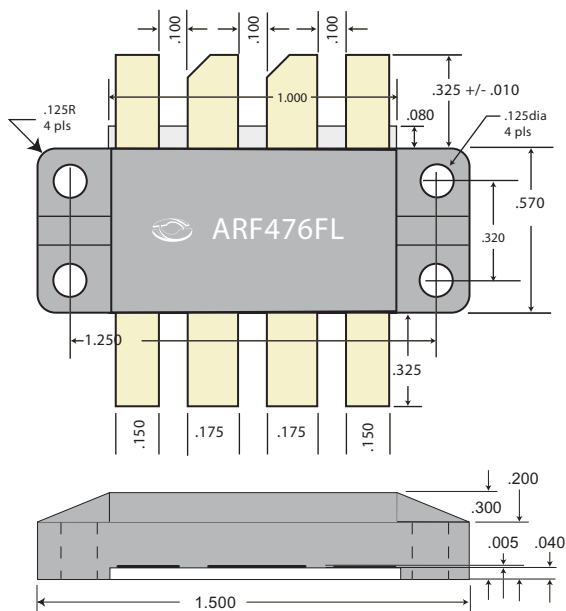
The value of L1 must be adjusted as the supply voltage is changed to maintain resonance in the output circuit. At 128MHz its value changes from approximately 40nH at 100V to 30nH at 150V.

With the 50Ω drain-to-drain load, the duty cycle above 100V must be reduced to insure power dissipation is within the limits of the device. Maximum pulse length should be 100mS or less. See transient thermal impedance, figure 5.

Thermal Considerations and Package Mounting:

The rated power dissipation is only available when the package mounting surface is at 25°C and the junction temperature is 175°C. The thermal resistance between junctions and case mounting surface is 0.16 °C/W. When installed, an additional thermal impedance of 0.15°C/W between the package base and the mounting surface is typical. Insure that the mounting surface is smooth and flat. Thermal joint compound must be used to reduce the effects of small surface irregularities. Use the minimum amount necessary to coat the surface. The heatsink should incorporate a copper heat spreader to obtain best results.

The package design clamps the ceramic base to the heatsink. A clamped joint maintains the required mounting pressure while allowing for thermal expansion of both the base and the heat sink. Four 4-40 (M3) screws provide the required mounting force. T = 6 in-lb (0.68 N-m).



HAZARDOUS MATERIAL WARNING

The white ceramic portion of the device between leads and mounting surface is beryllium oxide, BeO. Beryllium oxide dust is toxic when inhaled. Care must be taken during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste.

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