

1. General description

High voltage, high speed planar passivated NPN power switching transistor in a SOT428 (DPAK) surface mountable plastic package.

2. Features and benefits

- Fast switching
- Low thermal resistance
- Surface mountable package
- Very high voltage capability
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- High frequency electronic lighting ballasts
- Inverters
- Motor control systems

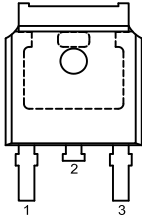
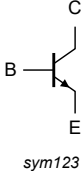
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CM}	peak collector current	Fig. 1 ; Fig. 2 ; Fig. 3	-	-	10	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ °C}$; Fig. 4	-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	-	1000	V
Static characteristics						
h_{FE}	DC current gain	$I_C = 5\text{ mA}$; $V_{CE} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 11	10	22	30	
		$I_C = 500\text{ mA}$; $V_{CE} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 11	14	25	35	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 DPAK (SOT428)	 sym123
2	C	collector ^[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUJ303AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0\text{ V}$	-	1000	V
V_{CEO}	collector-emitter voltage	$I_B = 0\text{ A}$	-	500	V
I_C	collector current	Fig. 1; Fig. 2; Fig. 3	-	5	A
I_{CM}	peak collector current		-	10	A
I_B	base current		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^{\circ}\text{C}$; Fig. 4	-	80	W
T_{stg}	storage temperature		-65	150	$^{\circ}\text{C}$
T_j	junction temperature		-	150	$^{\circ}\text{C}$

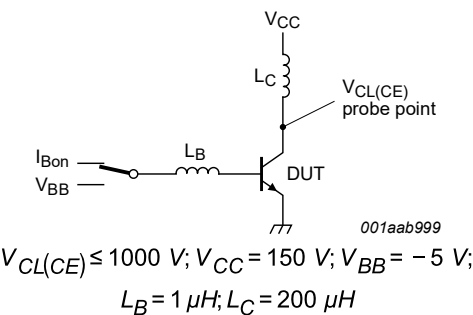


Fig. 1. Test circuit for reverse bias safe operating area

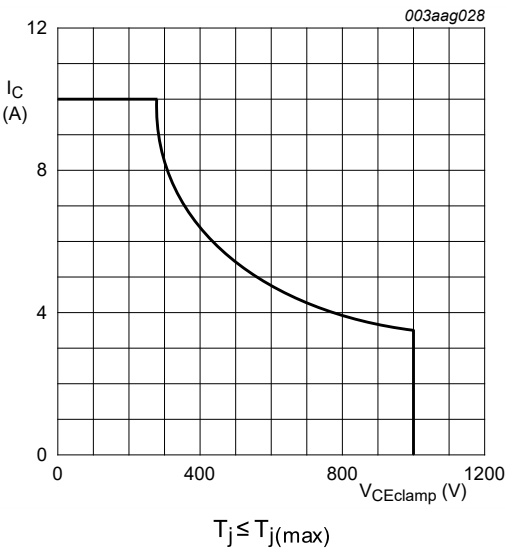
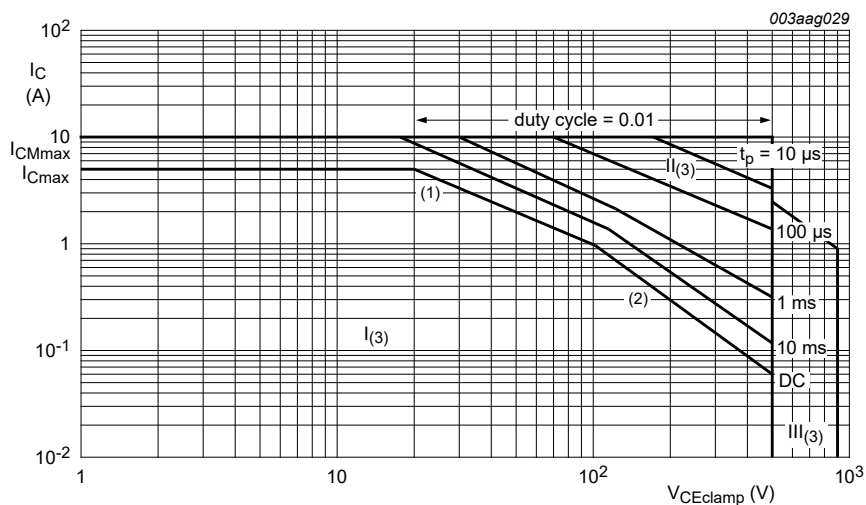
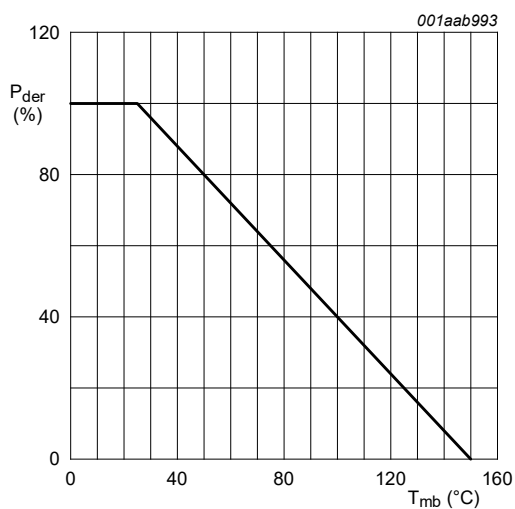


Fig. 2. Reverse bias safe operating area



- (1) P_{tot} maximum and P_{tot} peak maximum lines.
 - (2) Second breakdown limits.
 - (3) I = Region of permissible DC operation.
- II = Extension for repetitive pulse operation.
III = Extension during turn-on in single transistor converters provided that $R_{\text{BE}} \leq 100 \, \Omega$ and $t_{\text{p}} \leq 0.6 \, \mu\text{s}$.

Fig. 3. Forward bias safe operating area for $T_{mb} \leq 25^\circ\text{C}$



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig. 4. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint	-	75	-	K/W

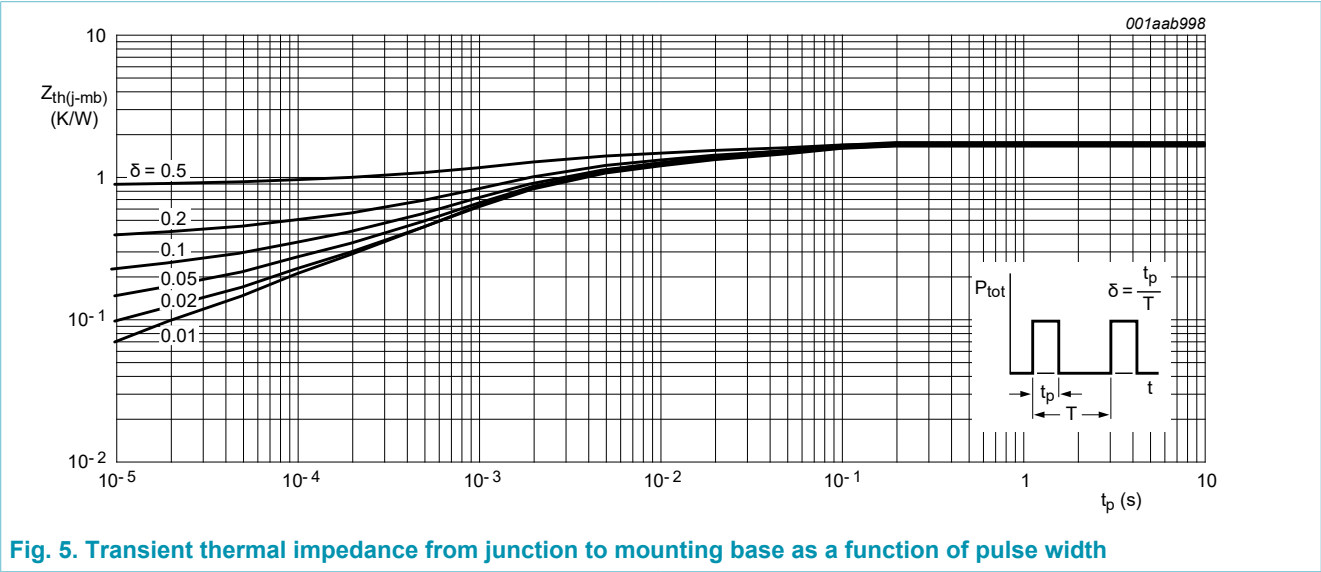


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{CES}	collector-emitter cut-off current (base shorted)	V _{BE} = 0 V; V _{CE} = 1000 V	[1]	-	-	1	mA
		V _{BE} = 0 V; V _{CE} = 1000 V; T _j = 125 °C	[1]	-	-	2	mA
I _{CBO}	collector-base cut-off current (emitter open)	V _{CB} = 1000 V; I _E = 0 A; T _{mb} = 25 °C	[1]	-	-	1	mA
I _{CEO}	collector-emitter cut-off current (base open)	V _{CE} = 500 V; I _B = 0 A; T _{mb} = 25 °C	[1]	-	-	0.1	mA
I _{EBO}	emitter-base cut-off current (collector open)	V _{EB} = 9 V; I _C = 0 A; T _{mb} = 25 °C		-	-	0.1	mA
V _{CEOsus}	collector-emitter sustaining voltage (base open)	I _B = 0 A; I _C = 100 mA; L _C = 25 mH; T _{mb} = 25 °C; Fig. 6 ; Fig. 7		500	-	-	V
V _{CEsat}	collector-emitter saturation voltage	I _C = 3 A; I _B = 0.6 A; T _{mb} = 25 °C; Fig. 8 ; Fig. 9		-	0.25	1.5	V
V _{BEsat}	base-emitter saturation voltage	I _C = 3 A; I _B = 0.6 A; T _{mb} = 25 °C; Fig. 10		-	0.97	1.3	V
h _{FE}	DC current gain	I _C = 5 mA; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		10	22	30	
		I _C = 500 mA; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		14	25	35	
h _{FESat}	DC saturation current gain	I _C = 2.5 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		10	13.5	17	
		I _C = 3 A; V _{CE} = 5 V; T _{mb} = 25 °C; Fig. 11		-	12	-	
Dynamic characteristics (switching times - resistive load)							
t _s	storage time	I _C = 2.5 A; I _{Bon} = 0.5 A; I _{Boff} = -0.5 A; R _L = 75 Ω; T _{mb} = 25 °C; Fig. 12 ; Fig. 13		-	3.4	4	μs
t _f	fall time			-	0.33	0.45	μs
Dynamic characteristics (switching times - inductive load)							
t _s	storage time	I _C = 2.5 A; I _{Bon} = 0.5 A; V _{BB} = -5 V; L _B = 1 μH; T _{mb} = 25 °C; Fig. 14 ; Fig. 15		-	1.4	1.6	μs
				-	1.7	1.9	μs
t _f	fall time	I _C = 2.5 A; I _{Bon} = 0.5 A; V _{BB} = -5 V; L _B = 1 μH; T _j = 100 °C; Fig. 14 ; Fig. 15		-	145	160	ns
				-	160	200	ns

[1] Measured with half-sine wave voltage (curve tracer).

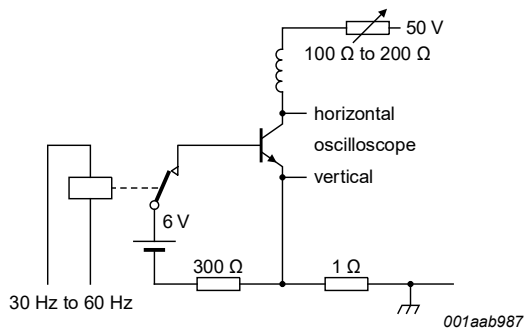


Fig. 6. Test circuit for collector-emitter sustaining voltage

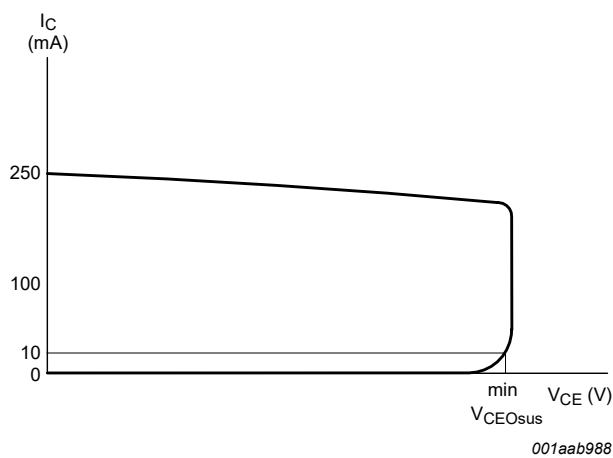


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

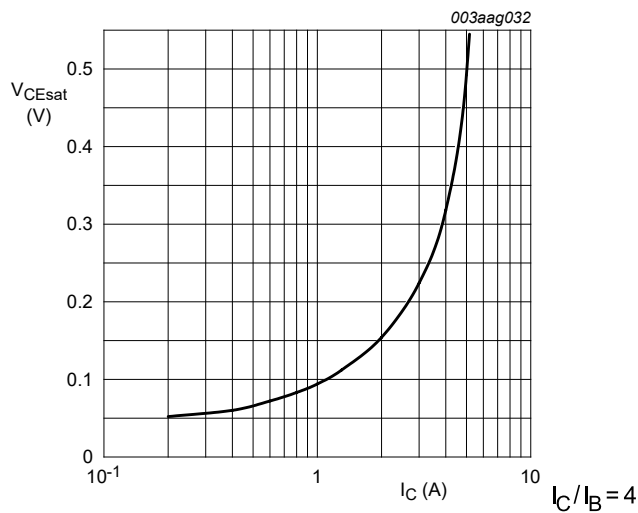


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

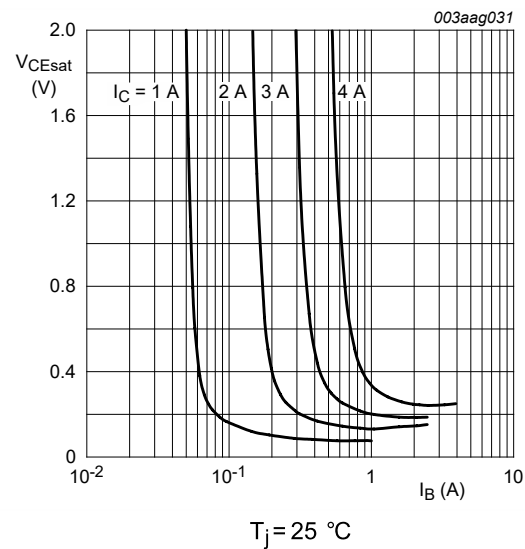


Fig. 9. Collector-emitter saturation voltage as a function of base current; typical values

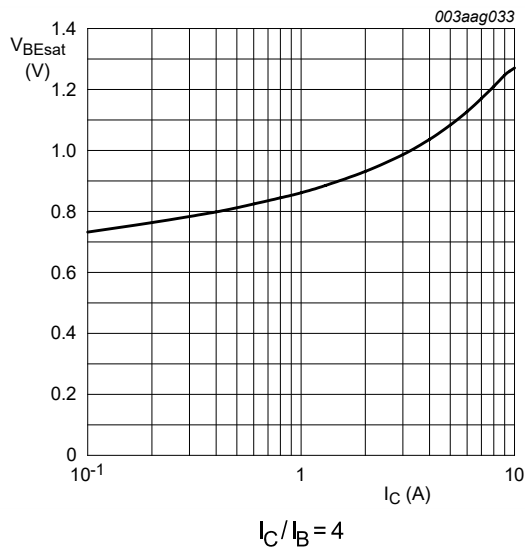


Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values

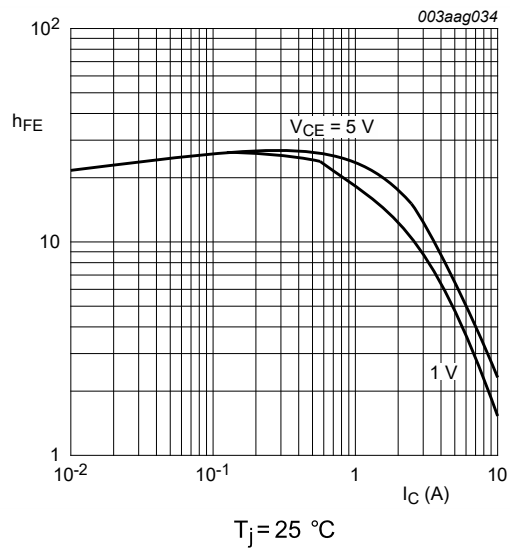
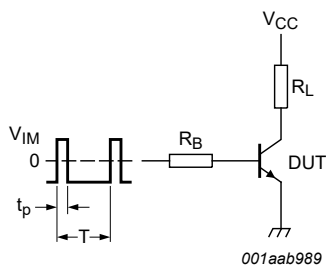


Fig. 11. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20$ μ s; $\delta = \frac{t_p}{T} = 0.01$
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 12. Test circuit for resistive load switching

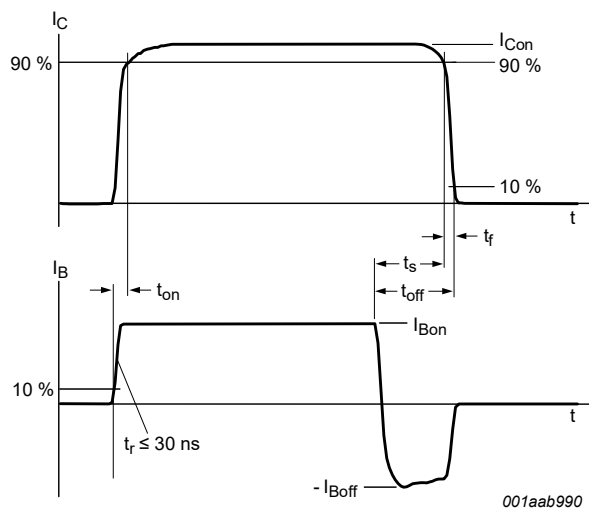


Fig. 13. Switching times waveforms for resistive load

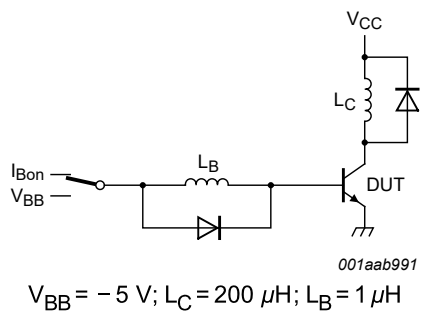


Fig. 14. Test circuit for inductive load switching

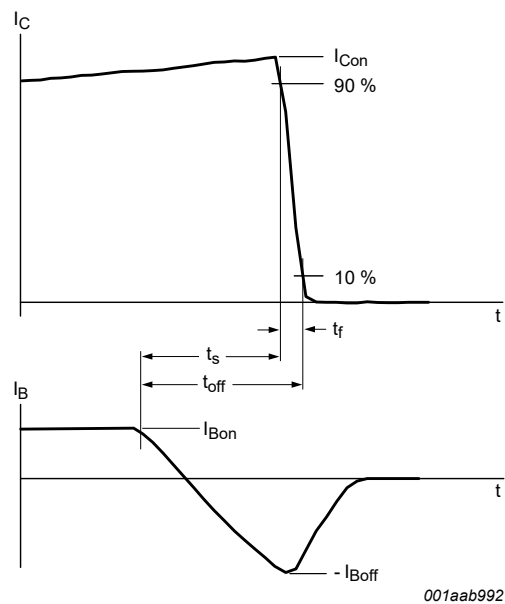
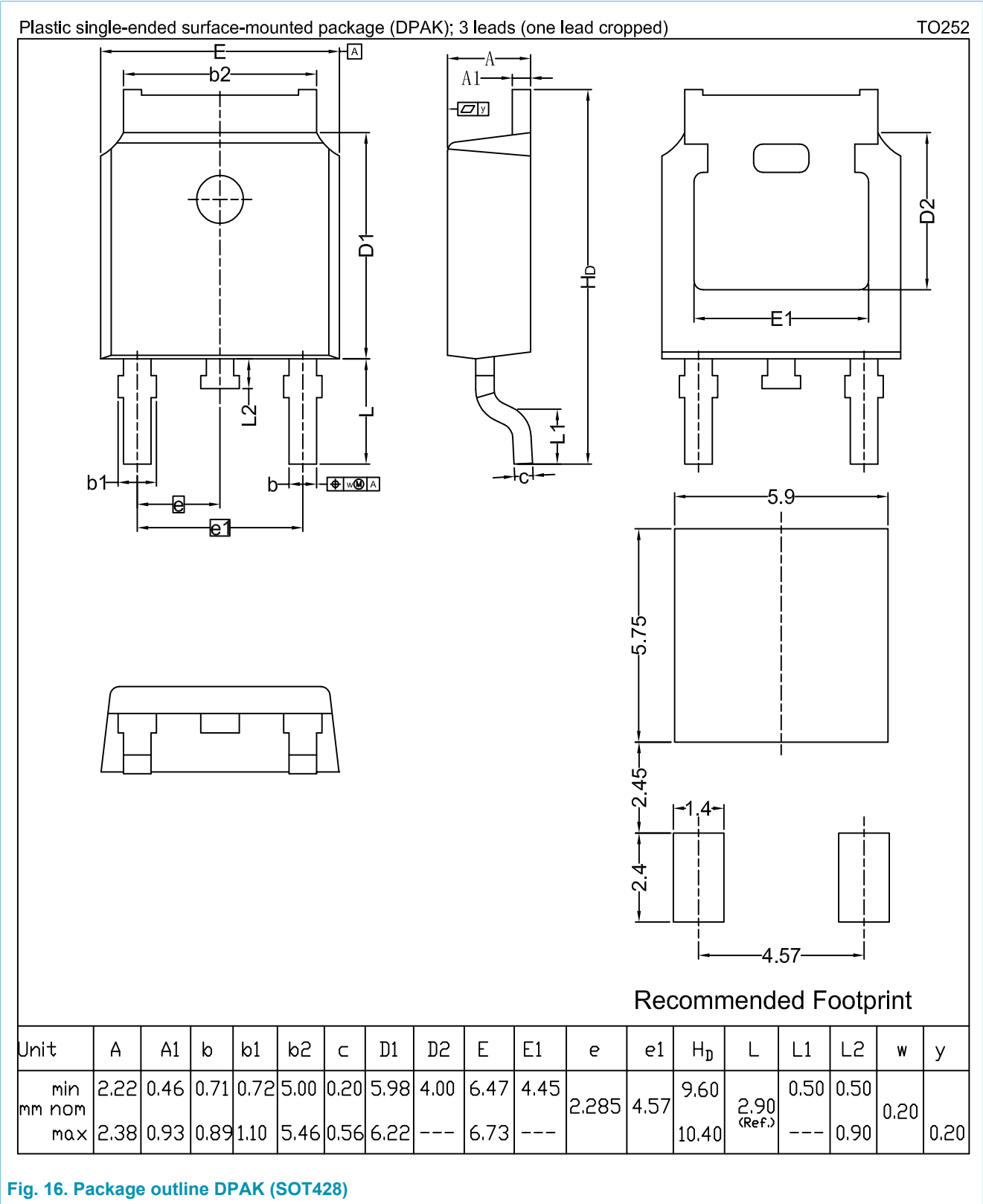


Fig. 15. Switching times waveforms for inductive load

10. Package outline



11. Legal information

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